Dr. Ambedkar Institute of Technology, Bengaluru-56

(An Autonomous Institution Affiliated to VTU, Belagavi)

Department of Electronics and Communication Engineering

Manual

LIC (Linear Integrated Circuits) Laboratory using PSPICE

Subject Code: 22ECT308A

Prepared by

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Dr. Ambedkar Institute of Technology

Bengaluru-560056

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Vision and Mission of Dr. Ambedkar Institute of Technology, Benagaluru-560056

VISION:

To create **D**ynamic, **R**esourceful, **Ad**ept and **I**nnovative **T**echnical professionals to meet global challenges.

MISSION:

- To offer state-of-the-art under graduate, post graduate and doctoral programs in the fields of Engineering, Technology and Management
- To generate new knowledge by engaging faculty and students in research, development and innovation.
- To provide strong theoretical foundation to the students, supported by extensive practical training to meet the industrial requirements.
- To instil moral and ethical values with social and professional commitment.

Vision and Mission of Electronics and Communication Engineering Department, Dr. Ambedkar Institute of Technology, Benagaluru-560056

VISION:

"To excel in education and research in Electronics and Communication Engineering and its related areas through its integrated activities"

MISSION:

- To provide students a strong foundation in Electronics and Communication Engineering.
- To provide high quality technical education in Electronics and Communication Engineering discipline and its related areas to meet the growing needs and challenges of industry and society.
- To be a contributor to the technology through the process of skill development, value based education, research and innovation.

Program Outcomes (POs)

PO1:	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2:	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3:	**Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4:	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5:	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO6:	**The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7:	**Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8:	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9:	**Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10:	**Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11:	**Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12:	**Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

PSO1:	Capability to use mathematical Techniques to model the real time problems, to optimize the implementation using mathematical techniques and to analyze the system performance.
PSO2:	Ability to Understand, Analyse and Apply the Electronic Circuits, Digital Circuits, VLSI Circuits, Antennas, Microwaves, Microcontrollers and Embedded Controllers, Communication Systems conceptsto design and implement the real time applications.
PSO3:	Ability to identify and have the social and ethical responsibilities for the betterment of Society and to become an entrepreneur.

Syllabus Copy

LIC (Linear Integrated Circuits) Lab using PSPICE	
Course Code: **21ECL3083**	CIE Marks:**50**
Teaching Hours/Week (L:T:P: S): **0:0:2:0**	SEE Marks:**50**
Credits: **1**	Exam Hours:**100**

Course objectives:

- To gain hands on experience in designing LIC applications.
- To learn simulation software used to simulate the circuits.
- To learn fundamental principles of applications of linear integrated circuits.
- To design the applications of linear integrated circuits for the given specifications.

Sl. No	Experiments using PSPICE NOTE: Every experiment has to be designed, circuit to be drawn / constructed and executed in thespecified software. Results are also to be noted and inferred.
	Note: Standard design procedure to be adopted.
1	To realize using op-amp an Inverting Amplifier and Non-Inverting Amplifier
2	To realize using op-amps i) Summing Amplifier ii)Difference amplifier
3	To realize using op-amps an Instrumentation Amplifier
4	To realize using op-amps i) Differentiator ii)Integrator
5	To realize using op-amps a Full wave Precision Rectifier
6	To realize using op-amps i) Inverting and Non-Inverting Zero Crossing Detectors ii) Positive and Negative Voltage level detectors
7	To realize using op-amp an Inverting Schmitt Trigger
8	To realize using op-amp an Astable Multivibrator
9	To design and implement using op-amps i) Butterworth I & II order Low Pass Filter ii) Butterworth I & II order High Pass Filter

10	To design and implement using op-amp a RC Phase Shift Oscillator
11	To design and implement Mono-stable Multivibrator using 555 timer
12	To design and implement 4 - bit R-2R Digital to Analog Converter

Course outcomes (Course Skill Set):

After studying this course, students will be able to;

CO1: Sketch/draw schematics of linear integrated circuit applications.

CO2: Design the applications of LIC for the given specifications.

CO3: Demonstrate the fundamentals of linear integrated circuits and their applications using PSPICE tool.

Assessment Details

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.

- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledgewill carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.
SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University
All laboratory experiments are to be included for practical examination.
(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.
General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.
The duration of SEE is 03 hours
Rubrics suggested in Annexure-II of Regulation book

Suggested Learning Resources:

- Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education, 2018.

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Introduction to PSPICE

Introduction to PSPICE

- **PSPICE** is an acronym for **P**C Version SPICE
- **SPICE** is an acronym for **S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis.
- PSPICE can be used to simulate both **Analog** circuits and **Digital** Circuits.
- PSPICE-Student Version is a **free software**, which could be used to simulate the electronic as well as electrical circuits.
- **PSPICE Student Version 9.1** is used for the simulation of Linear Integrated Circuit Applications.

Downloading and Installing PSPICE

- **Go to google search (www.google.co.in).**
- **Type PSPICE Links in search box.**
- **Click on PSPICE Links - Auburn Engineering**
- **Select Download Locally (This is the student version 9.1)**
- **A Zip file will be downloaded, Extract it by choosing your own folder and directory.**
- **You will get a message 18 files extracted successfully.**
- **Go to the folder and click on setup file(.exe file)**
- **It will guide you to install and make sure to choose SCHEMATICS as your interface, not CAPTURE (Schematics is available freely not capture mode).**

Introduction to Op-Amp

Operational Amplifiers (Op-Amps)

Introduction

The operational amplifier in short Op-Amp is a linear Integrated circuit, also called a differential amplifier. Op-Amp is a linear and active device, which performs various operations like, signal conditioning, filtering, addition, subtraction, integration, differentiation, etc...

Op-amps are voltage amplifiers designed to be used with feedback circuits, using the elements Resistors or capacitors. The feedback elements determine the operation of the op-amps.

Op-Amps have three terminals, two input terminals named inverting input terminal, Non-Inverting input terminal, and one output terminal. The op-Amp performs the amplification of the difference of the two input signals through +VCC and -VEE DC biasing power supply. Hence the name differential amplifier, shown in figure (1).

Circuit Symbol of an Op-Amp:

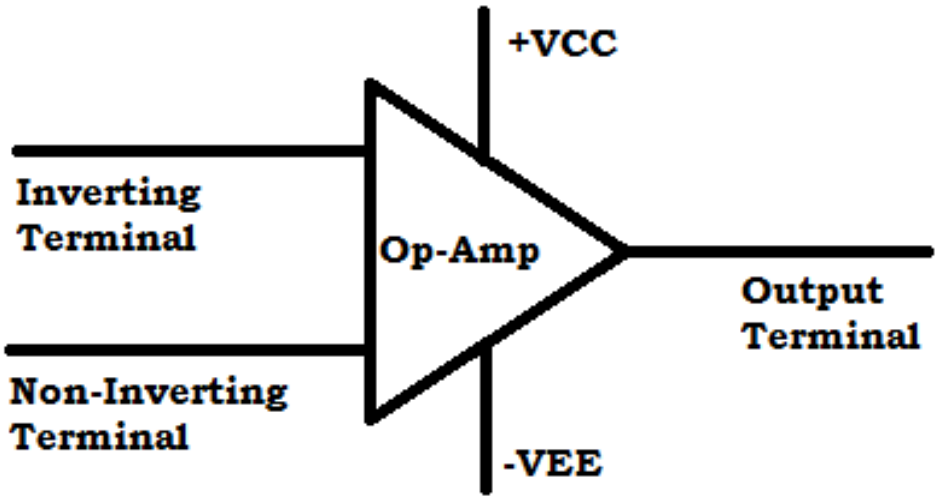

Figure 1: Circuit Symbol of an Op-Amp.

Op-amps come with an Integrated circuit(IC) package, which is an eight-pin IC, IC number is µA741.

Pin Details of µA741:

Figure (2) shows the pin diagram of IC µA741.

Pin numbers 1 and 2 are offset null terminals, used to calibrate the op-Amp. Pin 2 is inverting input terminal, pin 3 is the non-inverting terminals, pin 6 is the output terminal, pin 4 and 7 are power supply terminals -VEE and +VCC respectively, and Pin 8 is no connection(NC) reserved for future enhancement.

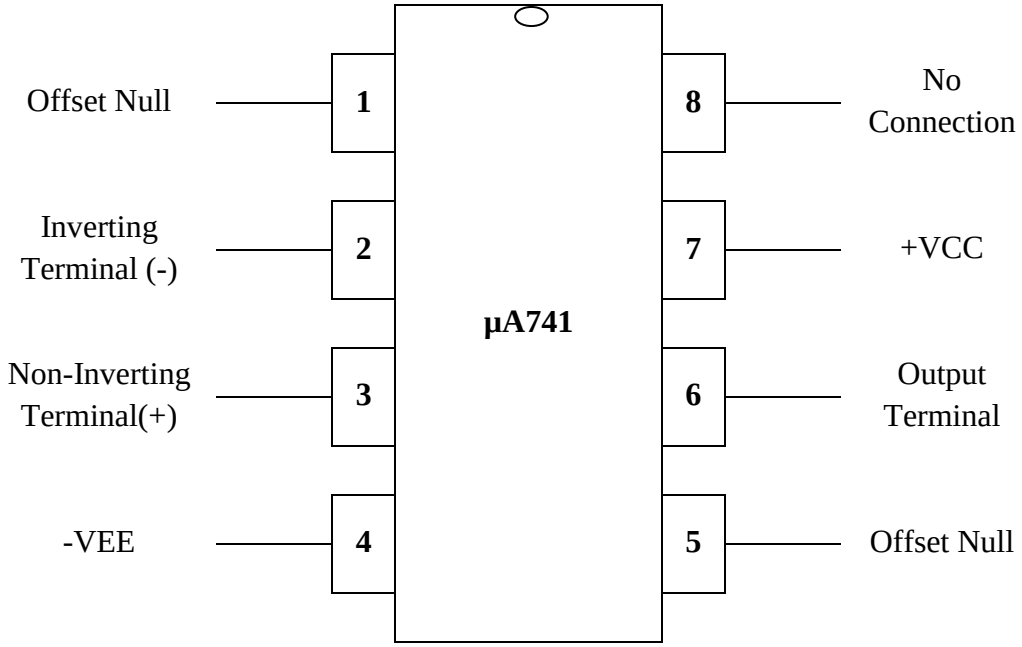

Figure 2: Pin diagram of uA741

Ideal Characteristics of Op-Amp:

i) Infinite Voltage Gain/loop gain

Voltage gain is the ratio of output voltage to the input voltage.

$$\text{i.e., } A_v = \frac{V_{out}}{V_{in}}$$

NOTE: Ideally ∞, typically $2x10^5 0$.

ii) Infinite input impedance

Input impedance is the ratio of input voltage to the input current, an Op-amp, the input current is zero., Hence, the Input impedance is infinite.

$$\text{i.e., } Z_i = \frac{V_{in}}{I_{in}}$$

NOTE: Ideally ∞, typically 1MΩ-2 MΩ.

iii) Zero output Impedance

Output impedance is the ratio of output voltage to the output current, in op-amp output current is maximum. Hence, the output impedance is zero.

$$\text{i.e., } Z_o = \frac{V_{out}}{I_{out}}$$

NOTE: Ideally 0, typically 50-75 Ω.

iv) Infinite Bandwidth

An op-amp has an infinite frequency response and can amplify the signal from DC to the highest frequencies.

NOTE: Ideally ∞, typically few GHz.

v) Infinite Common Mode Rejection Ratio (CMRR)

CMRR is the ratio of differential gain to the common-mode gain., Common-mode gain is the difference of the two input signals is zero. If Common mode voltage gain is zero, the CMRR is infinite.

$$\text{i.e., CMRR} = \frac{A_D}{A_{CM}}$$

$$A_{CM} = V_{inv} - V_{non-inv} \approx 0$$

NOTE: Ideally ∞, typically 70-90dB.

vi) Zero Slew rate

Slew rate is the rate of change of output voltage, which tells how fast the system responds to the change in the input signal.

$$\text{i.e., Slew Rate} = \frac{dV_{out}}{dt}$$

NOTE: Ideally 0, typically 0.5V/µsecs.

vi) Infinite Power supply rejection ratio(PSRR)

The ratio of change in output voltage to change in supply voltage(due to ac ripples) is called the Power supply rejection ratio.

$$\text{i.e, PSRR} = \frac{\Delta V_{out}}{\Delta V_{in}}$$

NOTE: Ideally ∞,, typically 50-100dB

vii) Input Bias Currents:

The current flowing through the base terminals of the input stage transistors circuit of an op-amp is called input bias currents, denoted as I_{B1} and I_{B2}.

NOTE: Ideally 0A, typically 80nA and maximum 500nA.

viii) Input offset current:

The magnitude of the difference between the input bias currents is called Input offset current, denoted as I_{io}.

$$\text{i.e., } I_{io} = |I_{B2} - I_{B1}|$$

NOTE: Ideally 0A, typically 20nA, and maximum 200nA.

ix) Input offset voltage:

Op-amp produces zero output voltage for zero input voltage, but practically a small dc voltage appears across the output terminal of an op-amp even if the input is zero, that voltage is called input offset voltage, denoted as V_{io}.

NOTE: Ideally 0V, typically 1mV, and maximum 5mV.

NOTE: The typical values given in the above characteristics are related to µA741.

Experiments

Experiment-01: Inverting and Non-inverting Amplifier

(i) Inverting Amplifier

AIM:

- Design an Inverting amplifier using Op-AMP with the gain of __ and simulate the circuit using PSPICE.
- Design an Inverting amplifier to get __Vp-p sinusoidal signal as output from the input of __Vp-p sinusoidal signal.

Circuit Diagram:

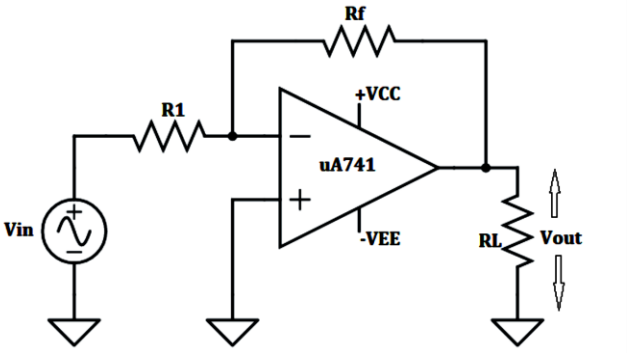

Figure 1.1: Circuit diagram of inverting amplifier

Design:

Design of inverting amplifier to amplify the sinusoidal signal of peak voltage 100mV to Sinusoidal signal of peak voltage 2V.

We know that,

$$V_o = -\left(\frac{R_f}{R_1}\right) V_{in}$$

$$R_f = 20R_1$$

Let, $\mathbf{R_1 = 1K\Omega, \therefore R_f = 20K\Omega}$

Components Required:

Table 1.1: List of components required for the simulation of inverting amplifier

Sl. No.	Part	Values/Attributes	Quantity
1	uA741	--	1
2	Resistor	1KΩ	1
3	Resistor	20KΩ	1
4	VSIN	VAMPL=100m, FREQ=1K	1
5	VDC	15V	2

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 1.1.
4. Setup the analysis
   - Analysis type: **Transient**
5. Simulate the schematic and observe the output.

PSPICE Schematic:

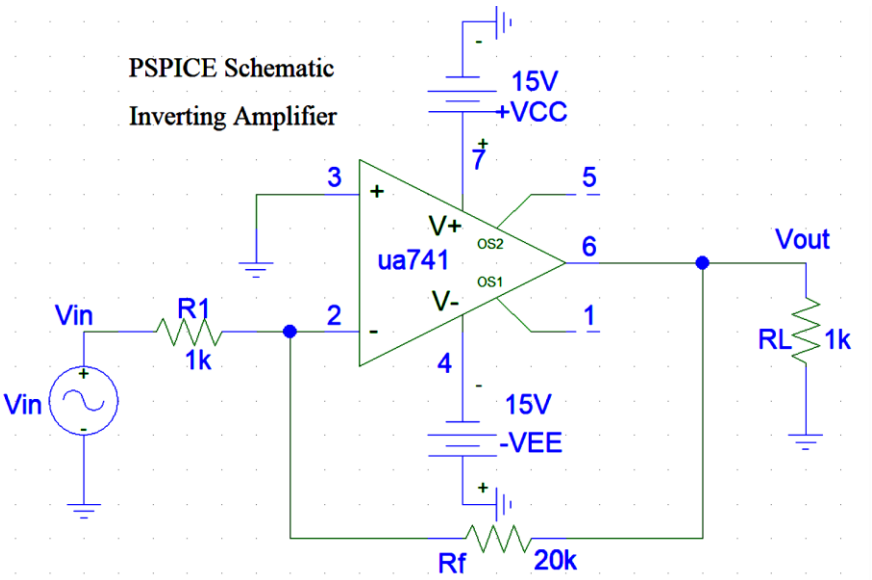

Figure 1.3: PSPICE Schematic of inverting amplifier

Simulation Result:

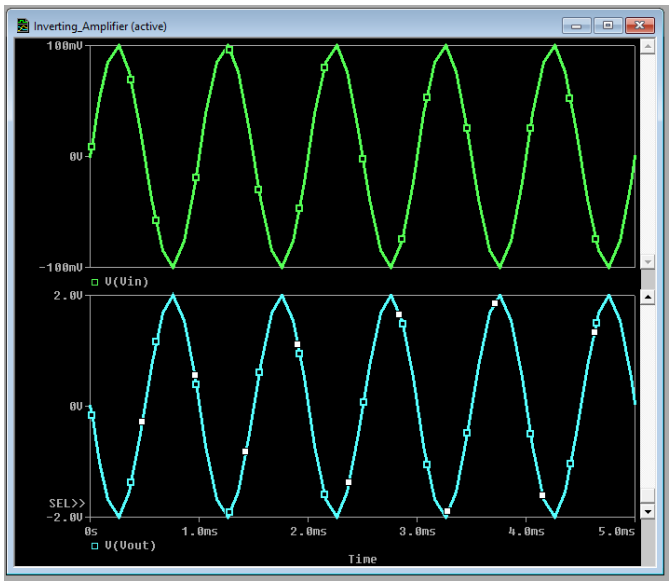

Figure 1.4: Simulation result of inverting amplifier

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(ii) Non-inverting Amplifier

AIM:

- Design a Non-inverting amplifier using Op-AMP with the gain of __ and simulate the circuit using PSPICE.
- Design a Non-inverting amplifier to get __Vp-p sinusoidal signal as output from the input of __Vp-p sinusoidal signal.

Circuit Diagram:

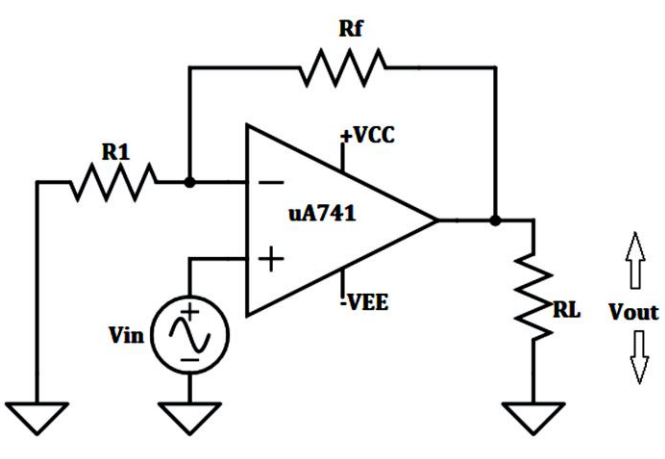

Figure 1.5: Circuit diagram of non-inverting amplifier

Design:

Design of inverting amplifier to amplify the sinusoidal signal of peak voltage 1V to sinusoidal signal of peak voltage 5V.

We know that,

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_{in}$$

$$R_f = 4R_1$$

Let, $\mathbf{R_1 = 1K\Omega, \therefore R_f = 4K\Omega}$

Components Required:

Table 1.2: List of components required for the simulation of non-inverting amplifier

Sl. No.	Part	Values/Attributes	Quantity
1	uA741	--	1
2	Resistor	1K	1
3	Resistor	4K	1
4	VSIN	VAMPL=1, FREQ=1K	1
5	VDC	15V	2

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 1.2.
4. Setup the analysis
   - Analysis type: **Transient**
5. Simulate the schematic and observe the output.

PSPICE Schematic:

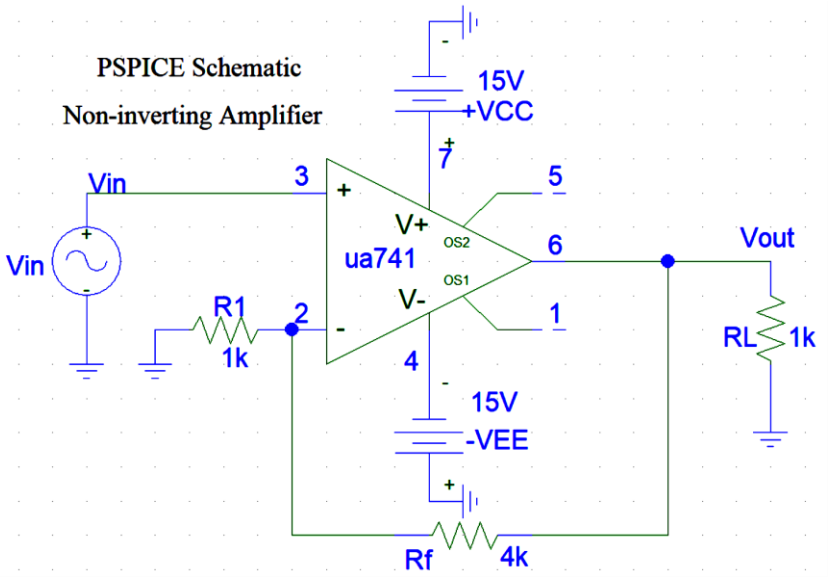

Figure 1.7: PSPICE Schematic of non-inverting amplifier

Simulation Result:

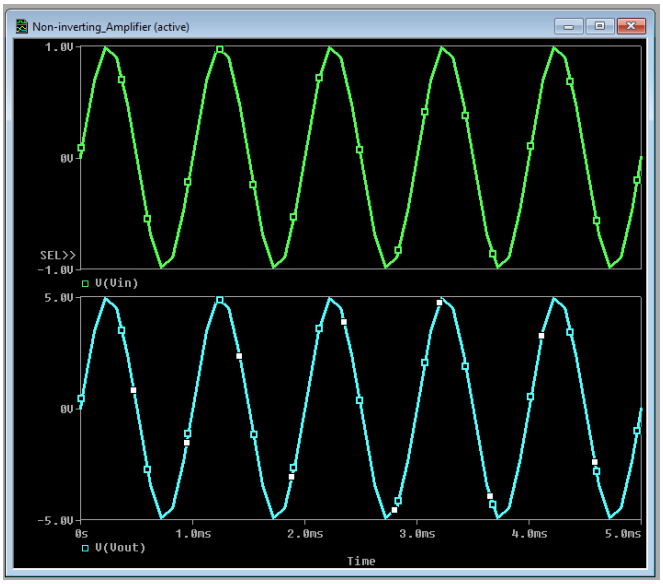

Figure 1.8: Simulation result of non-inverting amplifier

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Experiment-02: Summing and Difference Amplifiers

(i) Summing Amplifier

AIM:

- Design a Inverting summing amplifier using Op-AMP to realize $V_{out} = \pm\_V_{in1} \pm \_V_{in2} \pm \_V_{in3}$. Simulate the circuit using PSPICE by taking Vin1, Vin2 and Vin3 are sinusoidal/square/triangular signals of magnitude, __Vp-p, __Vp-p and _Vp-p respectively.

Circuit Diagram:

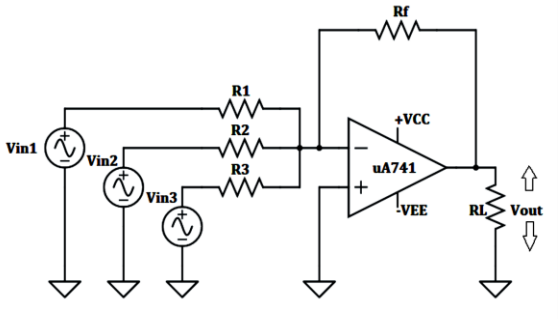

Figure 2.1: Circuit diagram of three signals inverting summing amplifier

Design:

Design of summing amplifier to combine three sinusoidal signals of peak voltage levels, -1V, 2V and 3V with unity gain.

We know that,

$$V_o = -\left[\left(\frac{R_f}{R_1}\right)V_{in1} + \left(\frac{R_f}{R_2}\right)V_{in2} + \left(\frac{R_f}{R_3}\right)V_{in3}\right]$$

For unity gain, Choose, $R_1 = R_2 = R_3 = R_f = 1K\Omega$

Hence, $V_{out} = -(-1 + 2 + 3)$

$\mathbf{V_{out} = 4V}$; Sinusoidal signal of peak voltage 4V.

Components Required:

Table 2.1: List of components required for the simulation of Summing amplifier

Sl. No.	Part	Values/Attributes	Quantity
1	uA741	--	1
2	Resistors	1K	4
3	VSIN	i. VAMPL=-1V, FREQ=1K ii. i. VAMPL=2V, FREQ=1K iii. i. VAMPL=3V, FREQ=1K	3
4	VDC	15V	2

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 2.1.
4. Setup the analysis
   - Analysis type: **Transient**
5. Simulate the schematic and observe the output.

PSPICE Schematic:

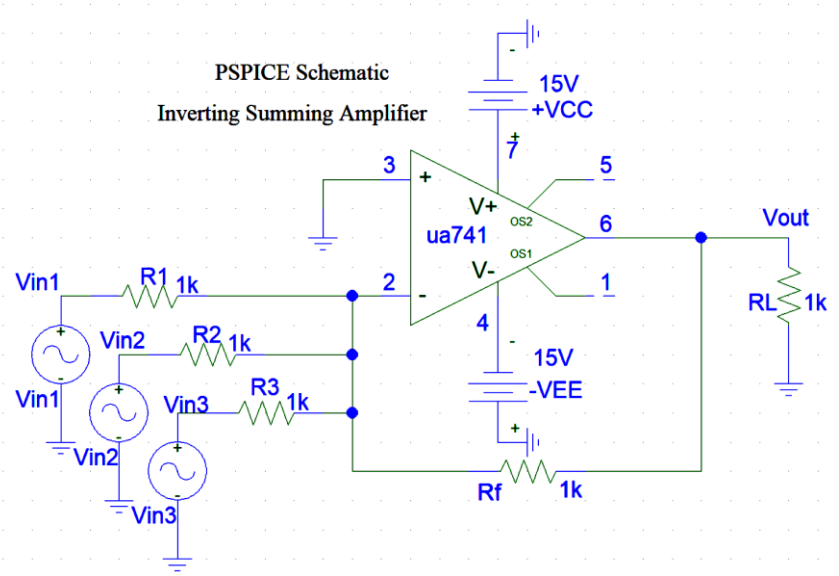

Figure 2.3: PSPICE Schematic of inverting summing amplifier

Simulation Result:

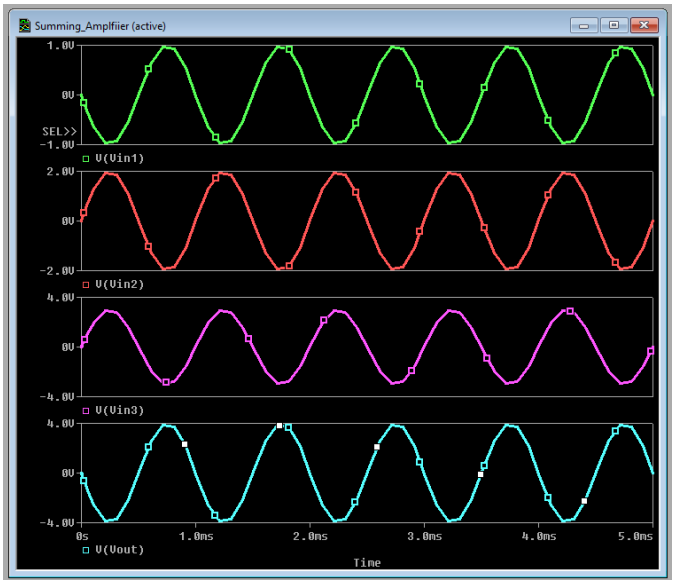

Figure 2.4: simulation result of inverting summing amplifier

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(ii) Difference Amplifier

AIM:

- Design a Difference amplifier using Op-AMP to realize $V_{out} = \_V_{in2} - \_V_{in1}$. Simulate the circuit using PSPICE by taking Vin1 and Vin2 are sinusoidal/square/triangular signals of magnitude, __Vp-p and __Vp-p respectively.

Circuit Diagram:

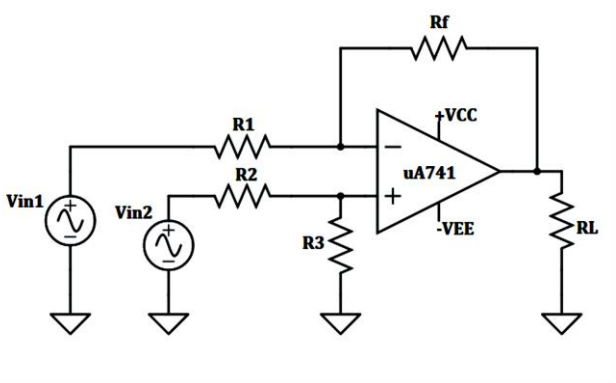

Figure 2.5: Circuit diagram of three signals Difference amplifier

Design:

Design of Difference amplifier to subtract the two sinusoidal signals of peak voltage levels, 5V and 2V, the resultant signal is a sinusoidal signal of peak voltage 3V.

We know that,

$$V_{out} = -V_{in1}\left(\frac{R_f}{R_1}\right) + V_{in2}\left(\frac{R_3}{R_2 + R_3}\right)\left(\frac{R_1 + R_f}{R_1}\right)$$

$$\text{Let, } R_1 = R_2 = R_3 = R_f = 1K$$

$$V_{out} = -V_1 + V_2$$

$$\text{Let, } V_{in1} = 2V \text{ and } V_{in2} = 5V.$$

$$\therefore \text{Resultant output is a sinusoidal signal of peak voltage 3V.}$$

Components Required:

Table 2.2: List of components required for the simulation of difference amplifier

Sl. No.	Part	Values/Attributes	Quantity
1	uA741	--	1
2	Resistor	1K	4
3	VSIN	i. VAMPL=2V, FREQ=1K ii. VAMPL=5V, FREQ=1K	2
4	VDC	15V	2

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 2.2.
4. Setup the analysis
   - Analysis type: **Transient**
5. Simulate the schematic and observe the output.

PSPICE Schematic:

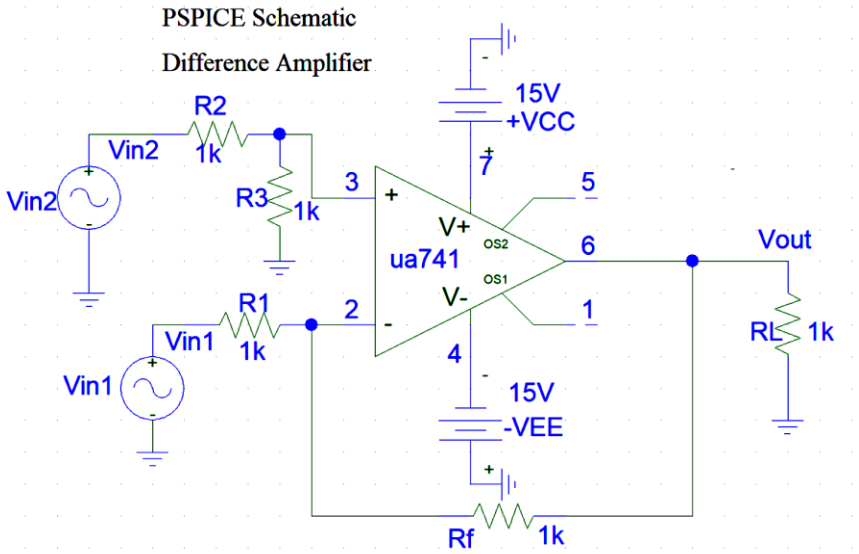

Figure 2.7: PSPICE Schematic of Difference amplifier

Simulation Result:

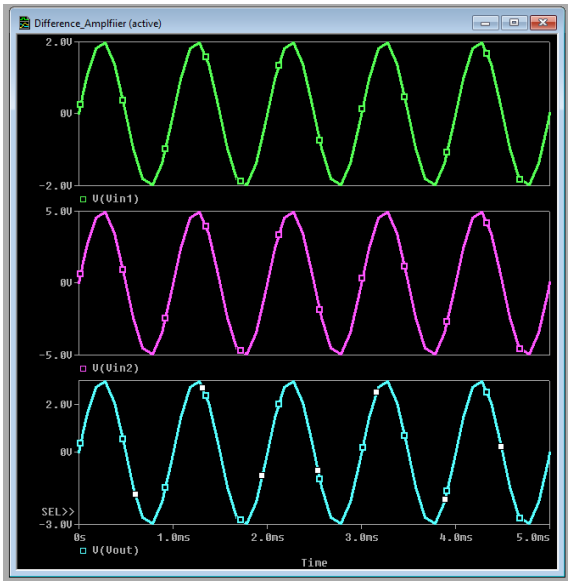

Figure 2.8: Simulation result of Difference amplifier

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Experiment No. 3: Op-Amp as an instrumentation amplifier

Instrumentation amplifier using Op-Amp

AIM:

- Design and simulate an Instrumentation Amplifier using PSPICE for the variable gain by varying only R_{gain}.

Circuit diagram:

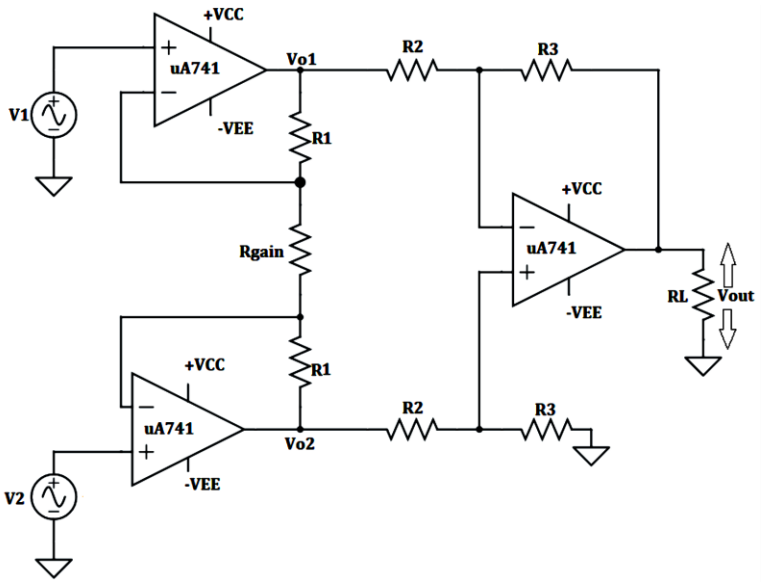

Figure 3.1: Circuit diagram of Instrumentation Amplifier

Design:

Design of op-amp based instrumentation amplifier for the variable gain.
We know that,

$$\therefore V_{out} = \left(\frac{2R_1 + R_{gain}}{R_{gain}}\right)(V_1 - V_2)\left(\frac{R_3}{R_2}\right) - - - (3.3)$$

Choose the input signals as DC sources of some arbitrary voltages

Say V1=1V, V2=0.8V.

Let $\mathbf{R_3 = 1k, R_2 = 1K \text{ and } R_1 = 1K}$

$$\therefore V_{out} = \left(1 + \frac{2K}{R_{gain}}\right)(V_1 - V_2) - - - (3.4)$$

Choose R_{gain} = variable from 100 to 500 in steps of 100.

Components required:

Table 3.1: List of parts required for PSPICE Simulation

Sl. No.	Parts	Value/Attributes	Quantity
1	uA741	--	3
2	Resistors	1KΩ	6
3	Resistor/ POT	1KΩ	1
4	VDC	15V	6
5	VDC/VSIN	Arbitrary input levels	2

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 3.1.
4. Setup the analysis
   - Analysis type: **DC Sweep**
   - Select global parameter
   - Edit the parameter name as RG
   - Choose the start value = 100, End value=500 and Increment =100.
5. Simulate the schematic and observe the characteristics RG vs Vout.
6. Compare the theoretical gain with practical.

Tabular Column:

Table 3.2: Tabular column for the conduction of Instrumentation amplifier experiment

Sl. No.	RG in Ohms	$V_1 - V_2$ in Volts	V_{out} in Volts	$\text{Gain} = \frac{Vout}{V1 - V2}$	
				Theoretical	Practical

PSPICE Schematic:

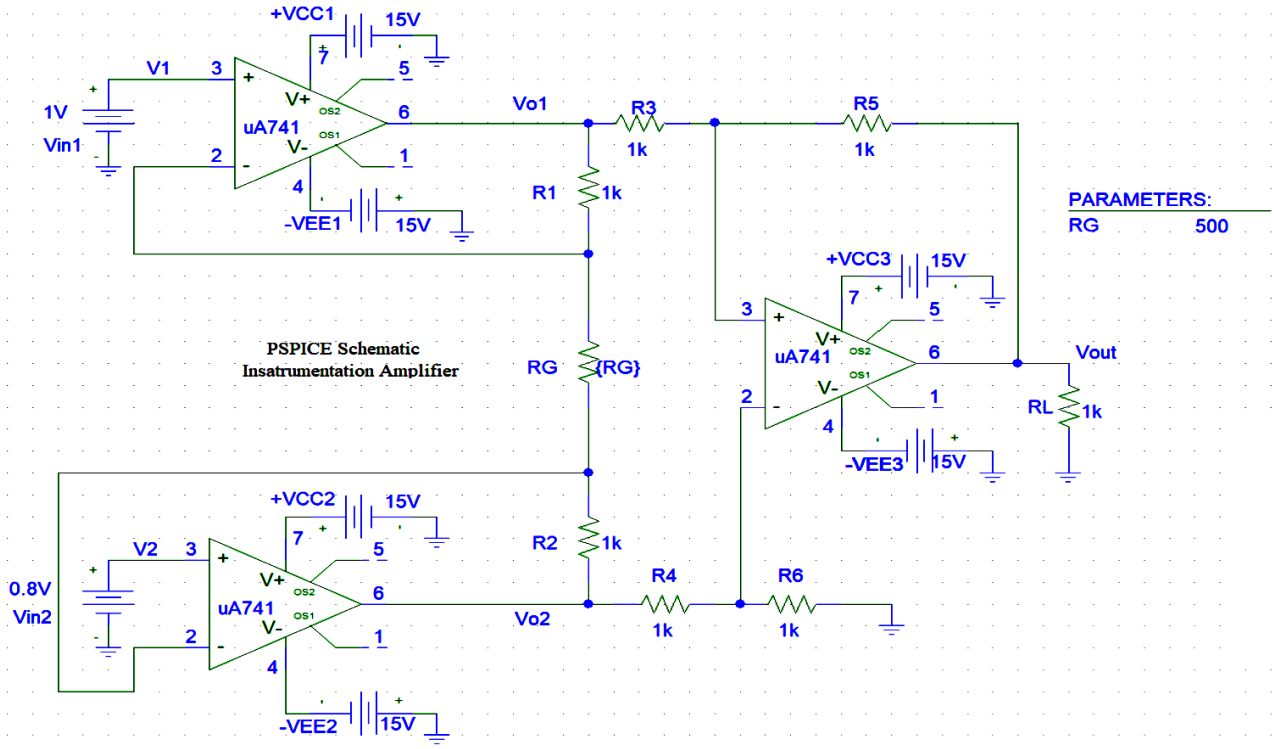

Figure 3.2: PSPICE Schematic of Instrumentation Amplifier

Simulation Result:

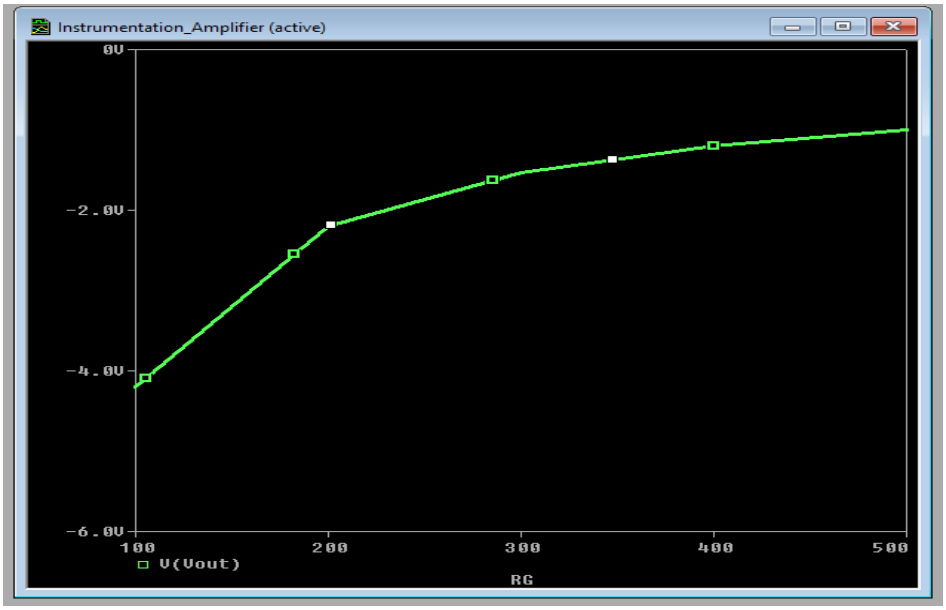

Figure 3.3: RG vs Vout Characteristics

******

Experiment-04: Op-amp Differentiator and Integrator

(i) Differentiator

- Design and simulate an Op-Amp Differentiator using PSPICE for the cut off frequencies ____Hz and ____Hz with unity gain.

Circuit Diagram:

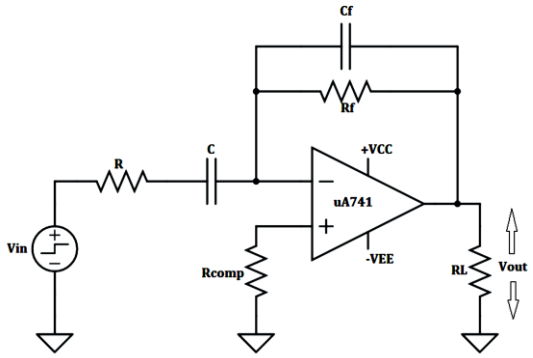

Figure 4.2: Circuit diagram of practical differentiator

Design:

Design of differentiator circuit for the cut-off frequencies 1K and 10 KHz with unity gain.

We know that,

$$f_a = \frac{1}{2\pi R_f C}$$

Let, $C = 0.01uF$

$$\therefore \mathbf{R_f \cong 16K\Omega}$$

$$f_b = \frac{1}{2\pi RC}$$

$$\therefore \mathbf{R_1 \cong 1.6K\Omega}$$

Also,

$$RC = R_f C_f$$

$$\therefore \mathbf{C_f \cong 1pF}$$

$$\mathbf{R_{Comp} = R||R_f \cong 1K\Omega}$$

Components Required:

Table 4.1: List of components required for the simulation of Summing amplifier

Sl. No.	Part	Values/Attributes	Quantity
1	uA741	--	1
2	Resistor	$1.6K\Omega$	1
3	Resistor	16K	1
4	Resistor	1K	2
5	VPULSE	V1=0, V2=5	1
6	VDC	15V	2

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 4.1.
4. Setup the analysis
   - Analysis type: **Transient**
5. Simulate the schematic and observe the output.

PSPICE Schematic:

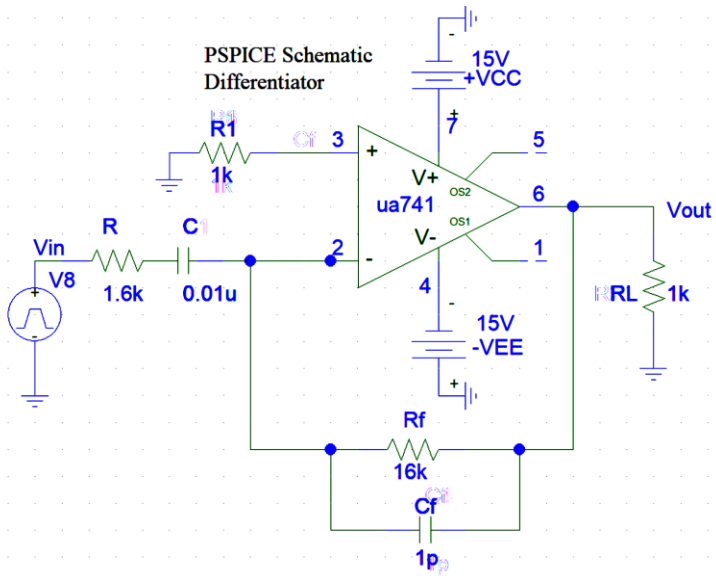

Figure 4.4: PSPICE Schematic of inverting summing amplifier

Simulation Result:

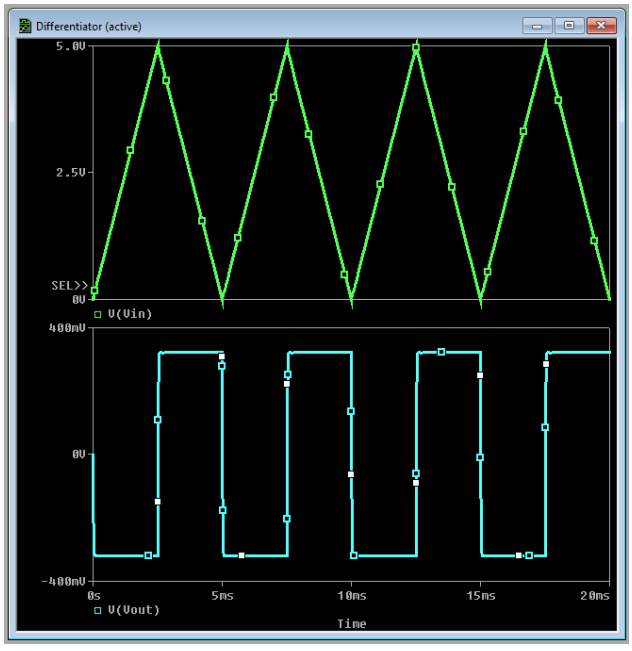

Figure 4.5: simulation result of inverting summing amplifier.

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(ii) Integrator Amplifier

AIM:

- Design and simulate an Op-Amp Integrator using PSPICE for the cut off frequencies ____Hz and ____Hz with unity gain.

Circuit Diagram:

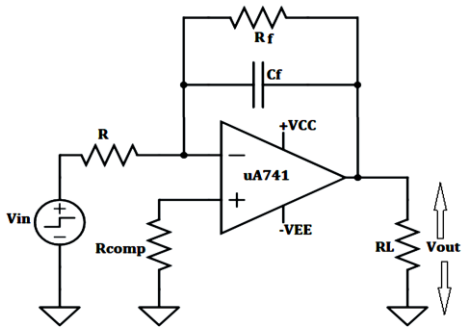

Figure 4.7: Circuit diagram of Practical Integrator

Design:

Design of Op-Amp integrator for the frequency range from 1 KHz to 10 KHz.

We know that, $f_a = \frac{1}{2\pi R_f C_f}$

Let, $C_f = 0.01uF$

$\therefore R_f \cong 16K$

Also, $f_b = \frac{1}{2\pi R C_f}$

For proper integration, $f_b = 10f_a$

$\therefore R \cong 1.6K$

$R_{Comp} = R||R_f$

$\therefore R_{Comp} \cong 1K$

Components Required:

Table 4.2: List of components required for the simulation of difference amplifier

Sl. No.	Part	Values/Attributes	Quantity
1	uA741	--	1
2	Resistor	$1.6K\Omega$	1
3	Resistor	16K	1
4	Resistor	1K	2
5	Capacitor	0.01uF	1
6	VPULSE	V1=0, V2=5	1
7	VDC	15V	2

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 4.2.
4. Setup the analysis
   - Analysis type: **Transient**
   - End time = 5m
5. Simulate the schematic and observe the output.

PSPICE Schematic:

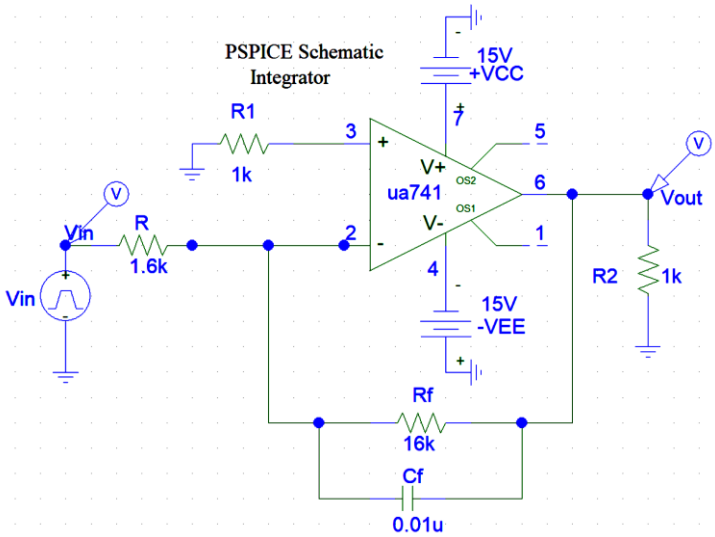

Figure 4.9: PSPICE Schematic of Difference amplifier

Simulation Result:

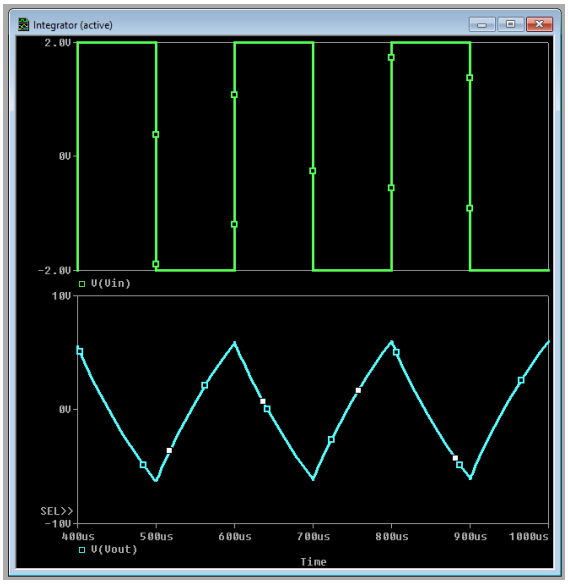

Figure 4.10: Simulation result of Difference amplifier

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Experiment No. 5: Op-Amps Precision Rectifier

Op-Amps Precision Rectifier

AIM:

- Design and simulate an Op-Amp precision rectifier using PSPICE for the gain of _____

Circuit diagram:

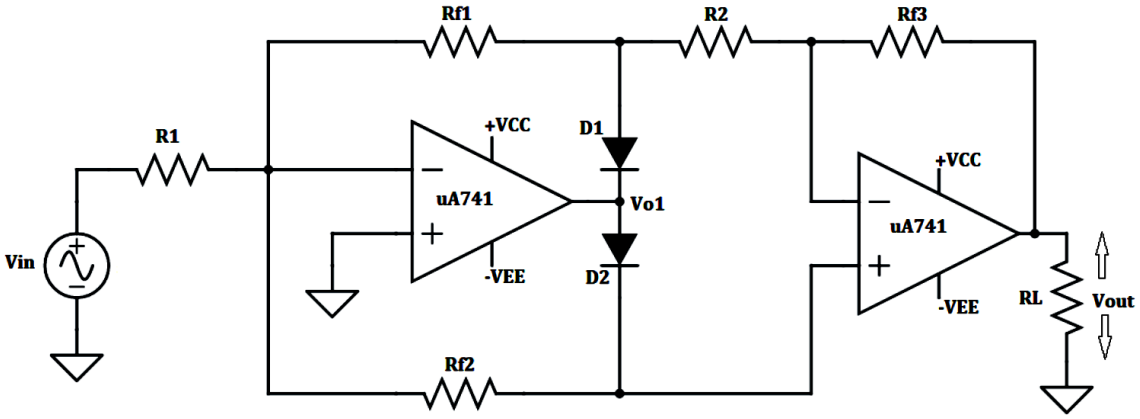

Figure 5.1: Circuit diagram of Full wave precision rectifier

Design:

During positive half cycle of input sinusoidal signal, Op-amp1 acts as an inverting amplifier and output of Op-amp 1 is negative.

$$\text{i.e., } V_{o1} = -\left(\frac{R_{f1}}{R_1}\right)V_{in} - - - (5.1)$$

Hence, diode D1 is forward biased and D2 reverse biased. Vo1 is the input to the Op-amp2 which is inverting amplifier and produces positive output.

$$\text{i.e., } V_{out} = +\left(\frac{R_{f1}}{R_1}\right)\left(\frac{R_{f3}}{R_2}\right)V_{in} - - - (5.2)$$

$$\text{if } R_{f1} = R_{f3} = R_1 = R_2 = R$$

$$V_{out} = +V_{in} - - - (5.3)$$

During Negative half cycle of input sinusoidal signal,.

$$V_{o1} = -\left(\frac{1}{R_1}\right)\left(\frac{R_{f2}(R_{f1}+R_2)}{R_{f2}+R_{f1}+R_2}\right)V_{in} \; - - - (5.4)$$

Let, $R_{f1} = R_{f2} = R_2 = R_1 = R$

$$V_{o1} = -\frac{2}{3}V_{in} - - - (5.5)$$

Hence, diode D2 is forward biased and D1 is reverse biased. Vo1 is the input to the Op-amp2 circuit, which is a non-inverting amplifier, hence output is positive.

$$\text{i.e., } V_{out} = \left(1+\frac{R_{f3}}{R_{f1}+R_2}\right)V_{o1} - - - (5.6)$$

$$V_{out} = -\left(\frac{2}{3}\right)\left(1+\frac{R_{f3}}{R_{f1}+R_2}\right)V_{in} - - - (5.7)$$

$$\text{if } R_{f_3} = R_{f1} = R_2 = R$$
$$V_{out} = -V_{in} - - - (5.8)$$

Design of Full wave precision rectifier for gain=1.
We know that, for unity gain all resistors must be of same value, hence choose

$$R_1 = R_2 = R_{f1} = R_{f2} = R_{f3} = R_L = 1K\Omega$$

Components required:

Table 5.1: List of parts required for PSPICE Simulation

Sl. No.	Parts	Value/Attributes	Quantity
1	uA741	--	2
2	Resistors	1K**Ω**	6
3	Diodes	D1N4002	2
4	VDC	15V	4
5	VSIN	VAMP=1V, FREQ=1K	1

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 5.1.
4. Setup the analysis
   - Analysis type: **Transient**
   - End time = 5m
5. Simulate the schematic and observe the output.

PSPICE Schematic:

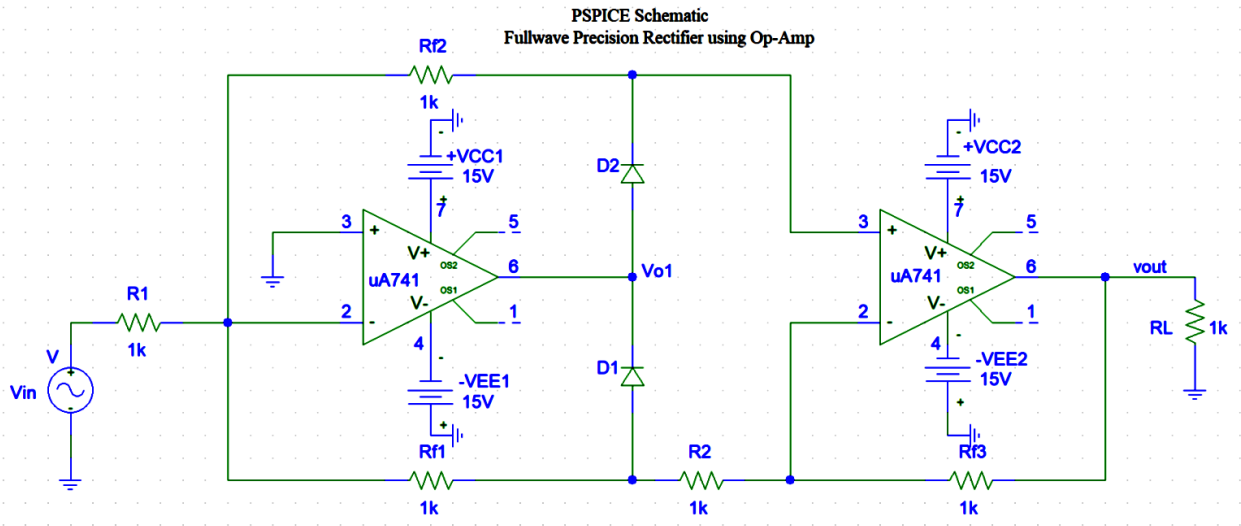

Figure 5.3: PSPICE Schematic of Full wave precision rectifier

Simulation Result:

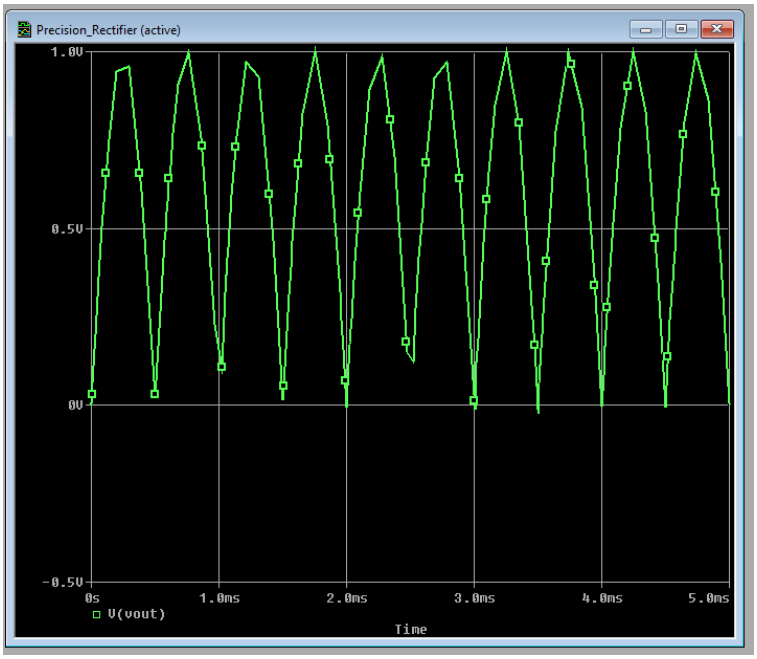

Figure 5.3: Output of full wave precision rectifier

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Experiment No. 6a: Zero Crossing Detectors

i. Non-Inverting Zero Crossing Detector

AIM:

- Design and simulate an Op-Amp non-inverting zero crossing detector.

Circuit diagram:

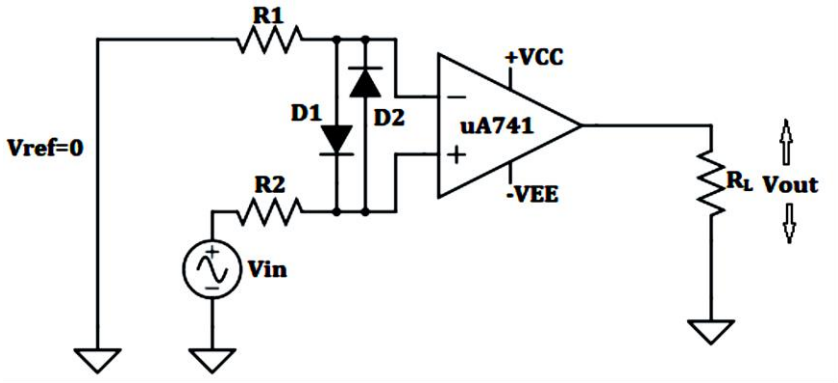

Figure 6.01: Circuit Diagram of Non-Inverting Zero Crossing Detector using Op-Amp

Design:

Choose Current limiting resistors R1 =R2=1KΩ
Choose RL=1KΩ
Apply sinusoidal signal of 1V peak as input.

Components Required:

Table 6.1: List of parts required for PSPICE Simulation

Sl. No.	Parts	Value/Attributes	Quantity
1	uA741	--	2
2	Resistors	1KΩ	3
3	Diodes	D1N4002	2
4	VDC	15V	4
5	VSIN	VAMP=1V, FREQ=1K	1

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 6.1.
4. Setup the analysis

- Analysis type: **Transient**

5. Simulate the schematic and observe the output.

PSPICE Schematic:

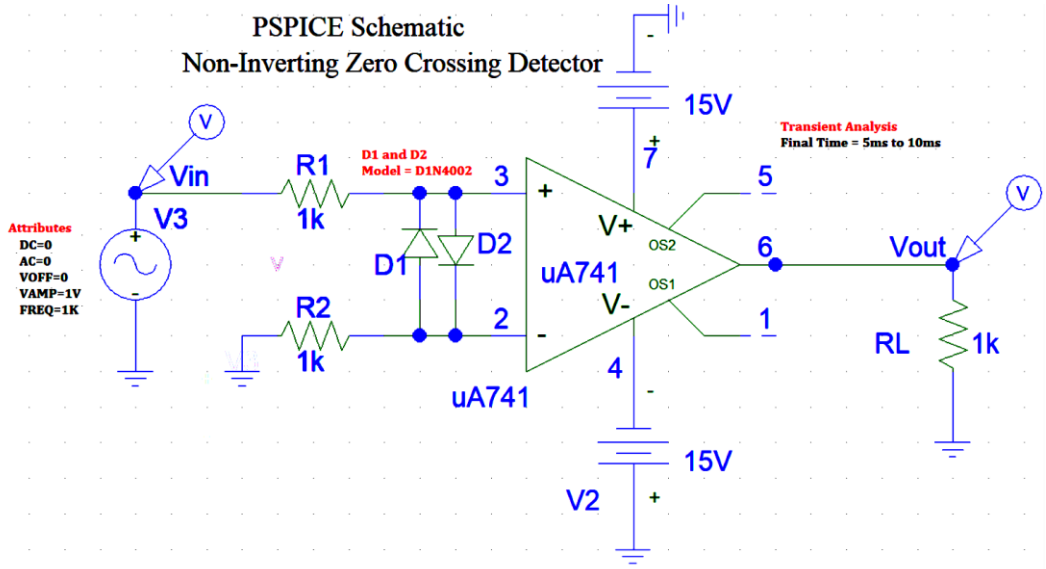

Figure 6.04: PSPICE Schematic of Non-Inverting Zero Crossing Detector

Simulation Result:

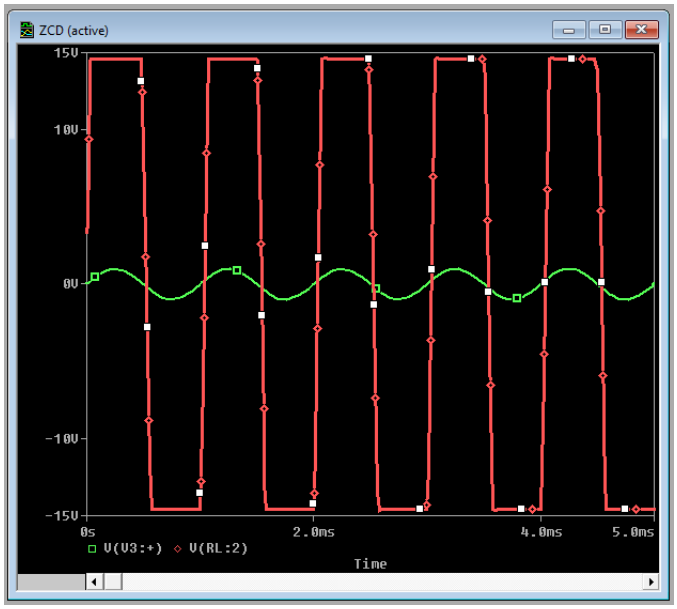

Figure 6.05: Simulation result of Non-Inverting Zero Crossing Detector

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ii. Inverting Zero Crossing Detector

AIM:

- Design and simulate an Op-Amp inverting zero crossing detector.

Circuit Diagram:

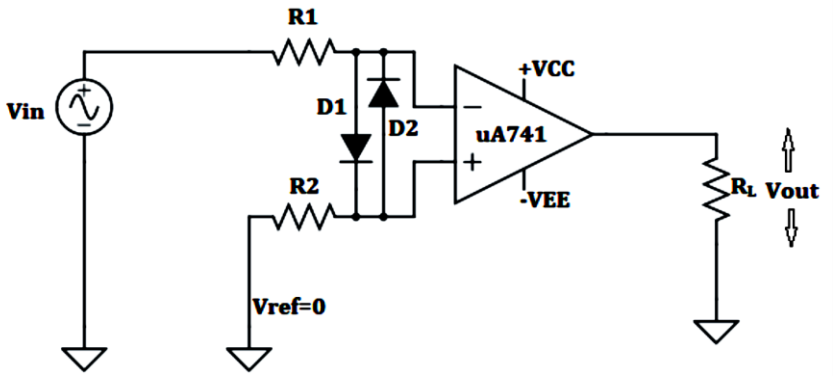

Figure 6.06: Circuit Diagram of Inverting Zero Crossing Detector

Design:

Choose Current limiting resistors R1 =R2=1KΩ
Choose RL=1KΩ
Apply sinusoidal signal of 1V peak as input.

Components Required:

Table 6.2: List of parts required for PSPICE Simulation

Sl. No.	Parts	Value/Attributes	Quantity
1	uA741	--	2
2	Resistors	1KΩ	3
3	Diodes	D1N4002	2
4	VDC	15V	4
5	VSIN	VAMP=1V, FREQ=1K	1

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 6.2.
4. Setup the analysis
   - Analysis type: **Transient**
5. Simulate the schematic and observe the output.

PSPICE Schematic

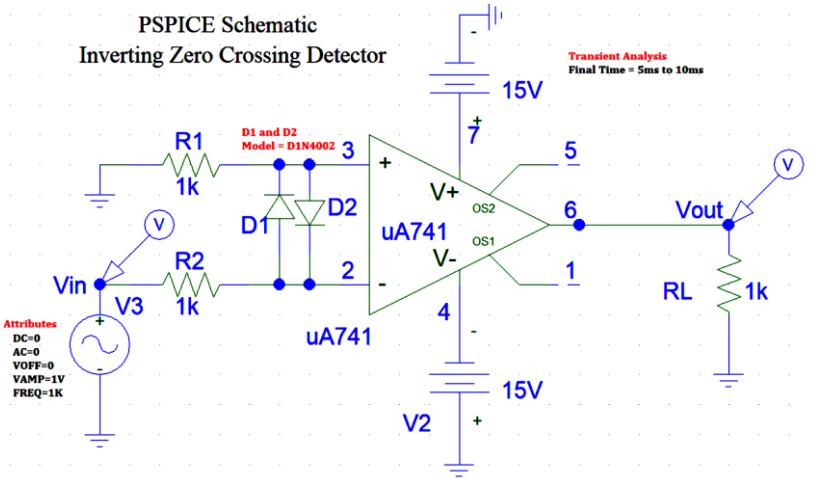

Figure 6.09: PSPICE Schematic of Inverting Zero Crossing Detector

Simulation Result:

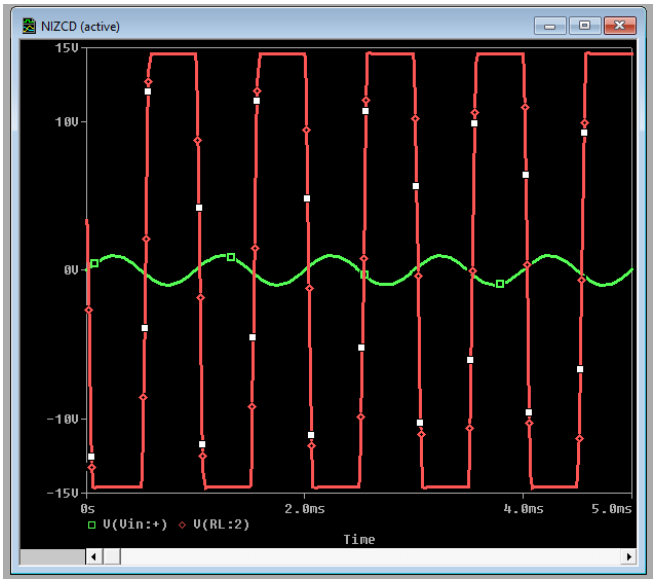

Figure 6.10: Simulation Result of Inverting Zero Crossing Detector

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Experiment No. 6b: Positive and Negative Voltage Level Detectors

i. Non-Inverting Positive Voltage level Detector

AIM:

- Design and simulate an Op-Amp non-inverting positive voltage level detector for ____volts.

Circuit diagram

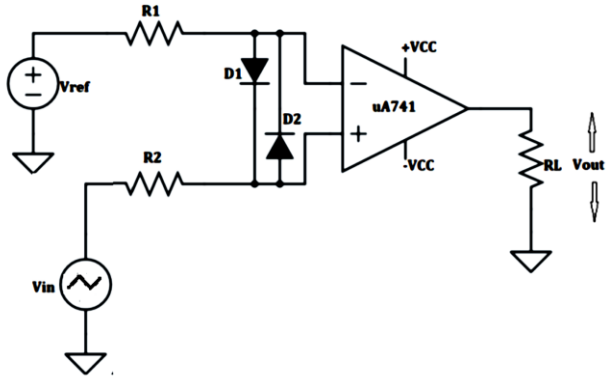

Figure 6.11: Circuit Diagram of Non-Inverting Positive Voltage Level Detector

Design:

Design of non-inverting voltage level detector for the reference voltage of +2V

During positive half cycle,

$$V_{in} > V_{ref}$$

$$V_{out} = +V_{sat} \cong +15V$$

During negative half cycle

$$V_{in} < V_{ref}$$

$$V_{out} = -V_{sat} \cong -15V$$

Choose Current limiting resistors R1 =R2=1KΩ

Choose RL=1KΩ

Apply triangular signal of 10V peak as input.

Apply Reference voltage $V_{ref} = +2V$ at inverting terminal.

Components Required:

Table 6.3: List of parts required for PSPICE Simulation

Sl. No.	Parts	Value/Attributes	Quantity
1	uA741	--	2
2	Resistors	1KΩ	3
3	Diodes	D1N4002	2
4	VDC	15V	4
5	VDC	+2V	1
6	VPULSE	V1=-10, V2=10	1

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 6.3.
4. Setup the analysis
   - Analysis type: **Transient**
   - End time = 5m
5. Simulate the schematic and observe the output.

PSPICE Schematic:

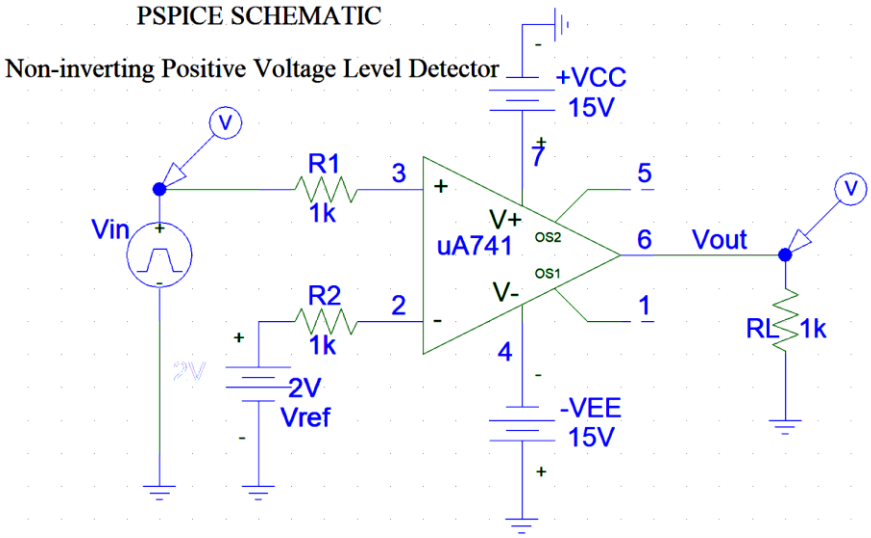

Figure 6. 14: PSPICE Schematic of Non-Inverting Positive Voltage Level Detector

Simulation result:

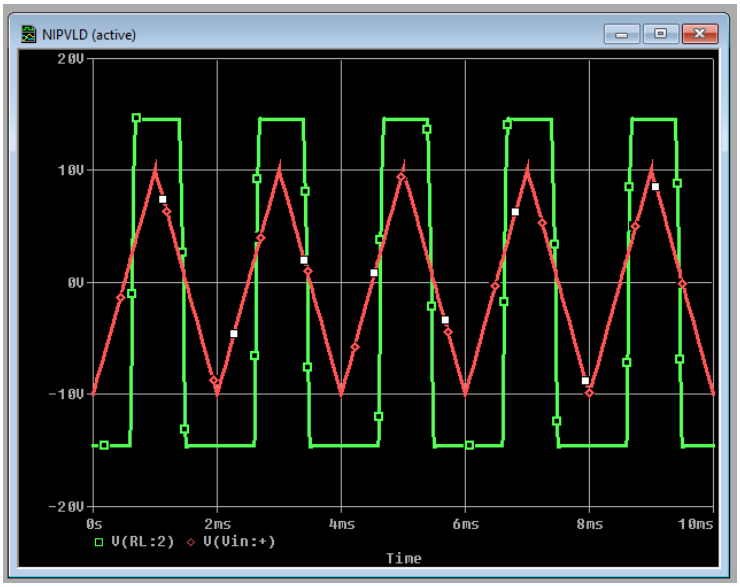

Figure 6. 15: Simulation result of Non-Inverting Positive Voltage Level Detector

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ii. Inverting Positive Voltage level Detector

AIM:

- Design and simulate an Op-Amp inverting positive voltage level detector for ____volts.

Circuit diagram

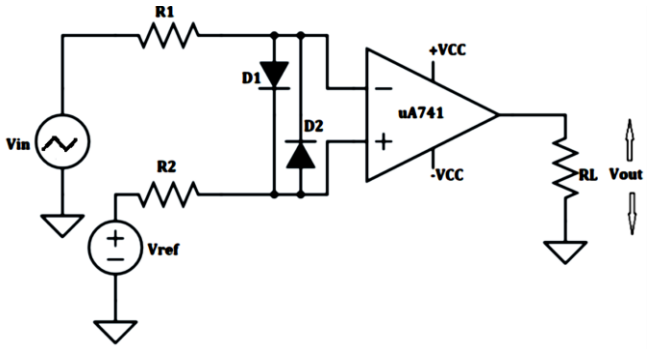

Figure 6. 16: Circuit Diagram of Inverting Positive Voltage Level Detector

Design:

Design of inverting voltage level detector for the reference voltage of +2V

During positive half cycle,

$$V_{in} > V_{ref}$$

$$V_{out} = -V_{sat} \cong -15V$$

During negative half cycle

$$V_{in} < V_{ref}$$

$$V_{out} = +V_{sat} \cong +15V$$

Choose Current limiting resistors R1 =R2=1KΩ

Choose RL=1KΩ

Apply triangular signal of 10V peak as input.

Apply Reference voltage $V_{ref} = +2V$ at the non-inverting terminal.

Components Required:

Table 6.4: List of parts required for PSPICE Simulation

Sl. No.	Parts	Value/Attributes	Quantity
1	uA741	--	2
2	Resistors	1KΩ	3
3	Diodes	D1N4002	2
4	VDC	15V	4
5	VDC	+2V	1
6	VPULSE	V1=-10, V2=10	1

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 6.4.
4. Setup the analysis
   - Analysis type: **Transient**
   - End time = 10m
5. Simulate the schematic and observe the output.

PSPICE Schematic

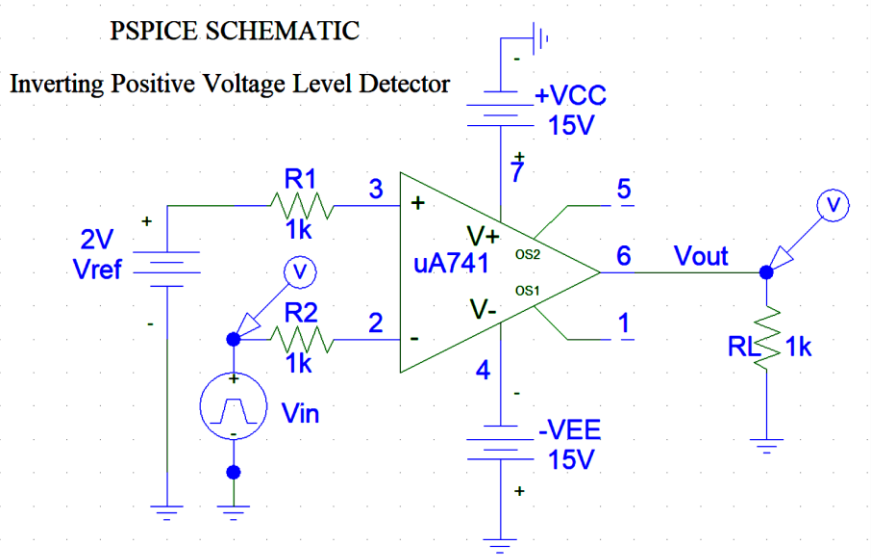

Figure 6. 19: PSPICE Schematic of Inverting Positive Voltage Level Detector

Simulation result:

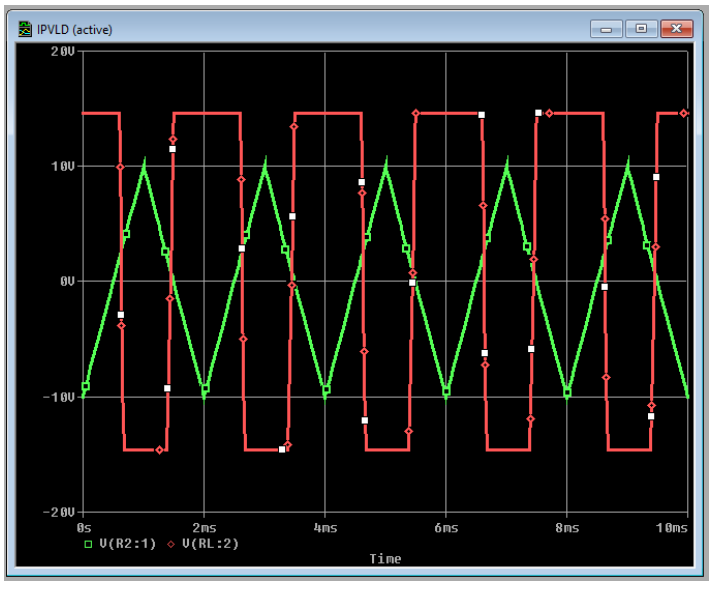

Figure 6.20: Simulation result of Inverting Positive Voltage Level Detector

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iii. Non-Inverting Negative Voltage level Detector

AIM:

- Design and simulate an Op-Amp non-inverting negative voltage level detector for ____volts.

Circuit diagram

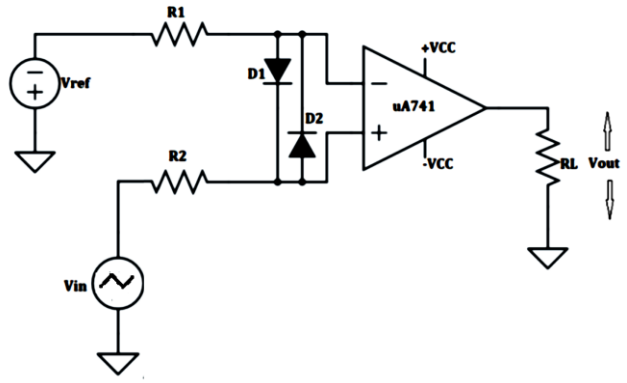

Figure 6.21: Circuit Diagram of Non-Inverting Negative Voltage Level Detector using Op-Amp

Design:

Design of non-inverting voltage level detector for the reference voltage of -2V
During positive half cycle,

$$V_{in} > V_{ref}$$

$$V_{out} = +V_{sat} \cong +15V$$

During negative half cycle

$$V_{in} < V_{ref}$$

$$V_{out} = -V_{sat} \cong -15V$$

Choose Current limiting resistors R1 =R2=1KΩ
Choose RL=1KΩ
Apply triangular signal of 10V peak as input.
Apply Reference voltage $V_{ref} = -2V$ at inverting terminal.

Components Required:

Table 6.5: List of parts required for PSPICE Simulation

Sl. No.	Parts	Value/Attributes	Quantity
1	uA741	--	2
2	Resistors	1KΩ	3
3	Diodes	D1N4002	2
4	VDC	15V	4
5	VDC	2V	1
6	VPULSE	V1=-10, V2=10	1

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 6.5.
4. Setup the analysis
   - Analysis type: **Transient**
   - End time = 10m
5. Simulate the schematic and observe the output.

PSPICE Schematic

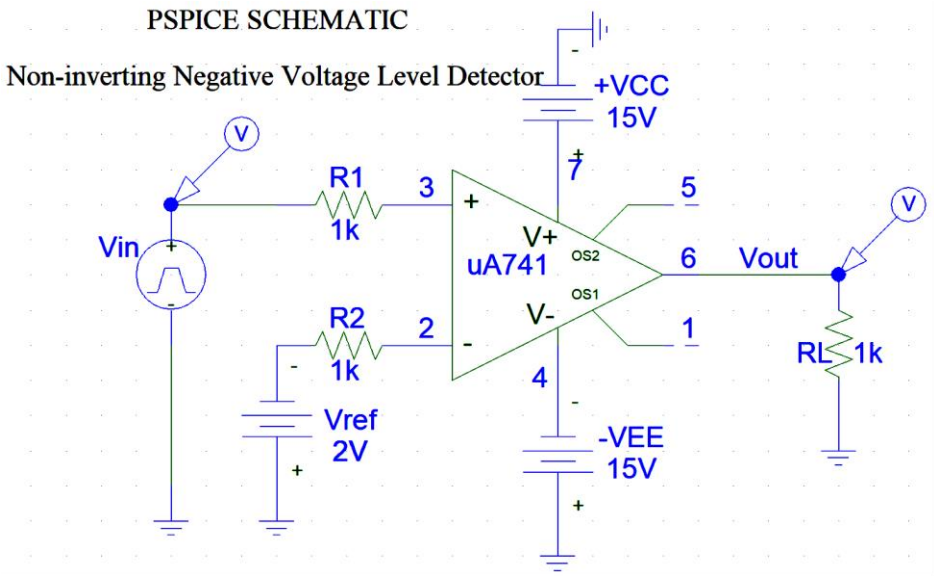

Figure 6.24: PSPICE Schematic of Non-Inverting Negative Voltage Level Detector

Simulation result:

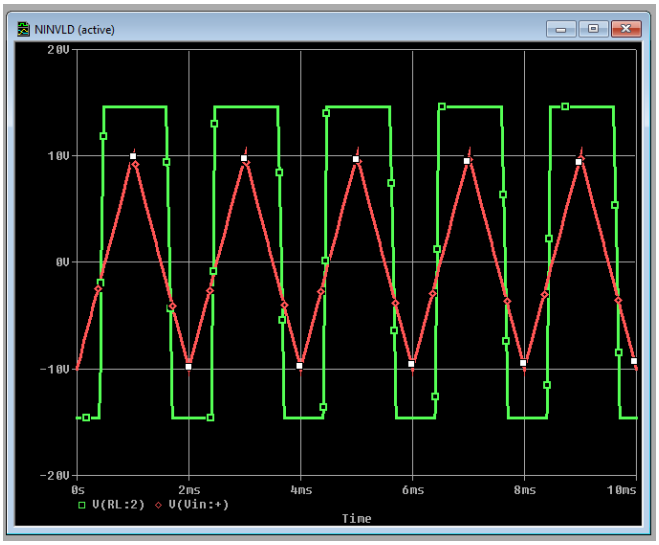

Figure 6.25: Simulation result of Non-Inverting Negative Voltage Level Detector.

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iv. Inverting Negative Voltage level Detector

AIM:

- Design and simulate an Op-Amp non-inverting negative voltage level detector for ____volts.

Circuit diagram

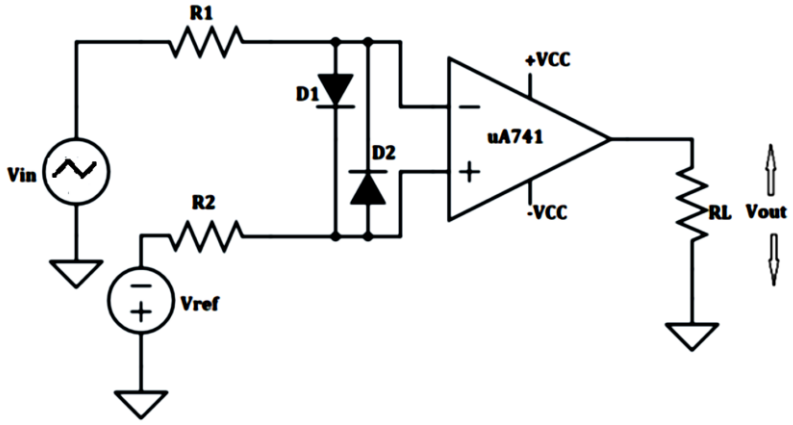

Figure 6.26: Circuit diagram of Inverting Negative Voltage Level Detector

Design:

Design of non-inverting voltage level detector for the reference voltage of -2V.
During positive half cycle,

$$V_{in} > V_{ref}$$

$$V_{out} = -V_{sat} \cong -15V$$

During negative half cycle

$$V_{in} < V_{ref}$$

$$V_{out} = +V_{sat} \cong +15V$$

Choose Current limiting resistors R1 =R2=1KΩ

Choose RL=1KΩ

Apply triangular signal of 10V peak as input.

Apply Reference voltage $V_{ref} = -2V$ at the non-inverting terminal.

Components Required:

Table 6.6: List of parts required for PSPICE Simulation

Sl. No.	Parts	Value/Attributes	Quantity
1	uA741	--	2
2	Resistors	1KΩ	3
3	Diodes	D1N4002	2
4	VDC	15V	4
5	VDC	+2V	1
6	VPULSE	V1=-10, V2=10	1

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 6.6.
4. Setup the analysis
   - Analysis type: **Transient**
   - End time = 10m
5. Simulate the schematic and observe the output.

PSPICE Schematic:

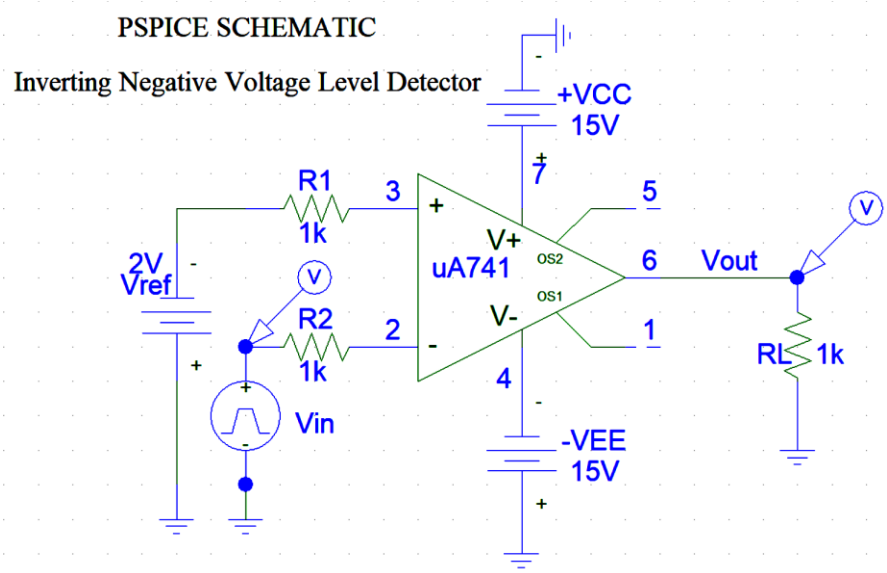

Figure 6.29: PSPICE Schematic of Inverting Negative Voltage Level Detector

Simulation result

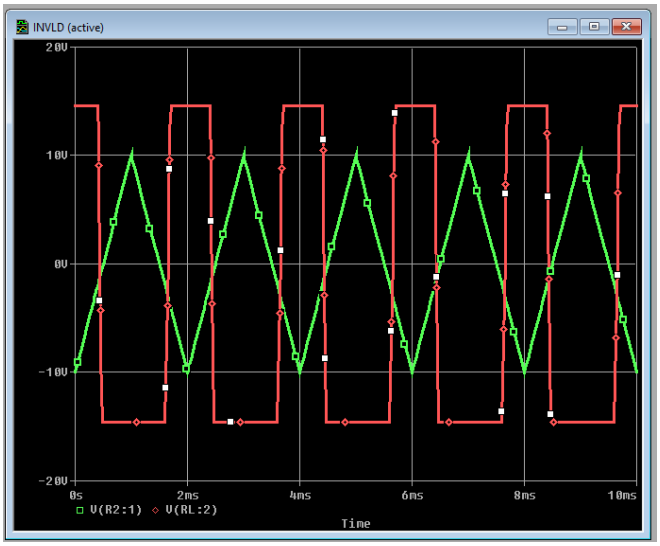

Figure 6.30: Simulation result of Inverting Negative Voltage Level Detector

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Experiment No.7: Inverting Schmitt trigger

Inverting Schmitt Trigger

AIM:

- Design and simulate an Op-Amp inverting Schmitt trigger for the UTP_____volts and LTP_____Volts.

Circuit Diagram:

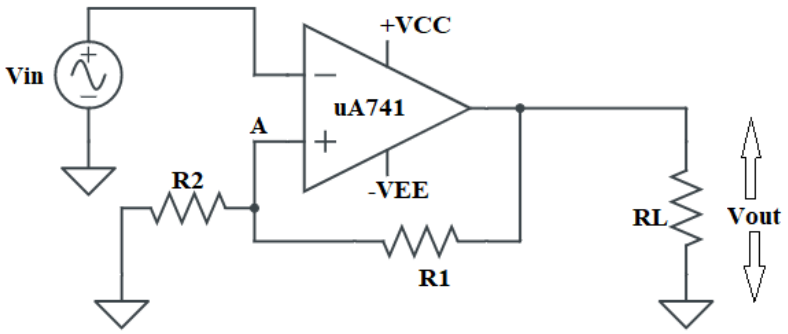


Figure 7.1: Circuit diagram of inverting Schmitt trigger

Design:

Design of Schmitt trigger for (UTV=+5V, LTV=-5V)
We know that, Ideal Saturation Voltage of Op-Amp is ±15V.

$$V_{UTV}/V_{LTV} = \frac{R_2}{R_1 + R_2} x(\pm V_{sat})$$

$$5 = \frac{R_2}{R_1 + R_2} x15$$

$$R_1 = 2R_2$$

Choose,

$$\mathbf{R_1 = 1K,}$$

$$\therefore \mathbf{R_2 = 2K}$$

Components required:

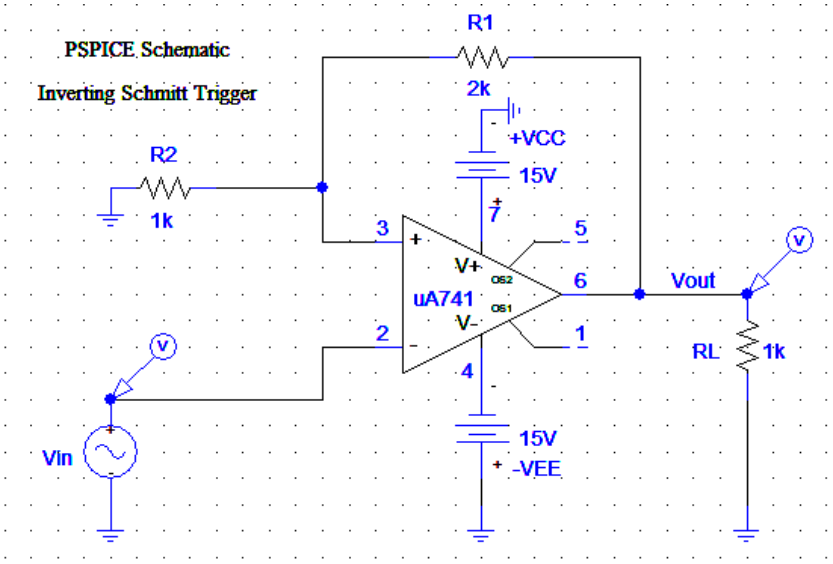
Table 7.1: Components required for the simulation of inverting Schmitt trigger

Sl. No.	Part	Values/Attributes	Quantity
1	uA741	--	1
2	Resistors	1K	2
3	Resistor	2K	1
4	VSIN	DC=0, AC-0, VAMPL=10, FREQ=1K	1
5	VDC	15V	2

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 7.1.
4. Setup the analysis
   - Analysis type: **Transient**
   - End time = 5m
5. Simulate the schematic and observe the output.

PSPICE Schematic:



Simulation Result:

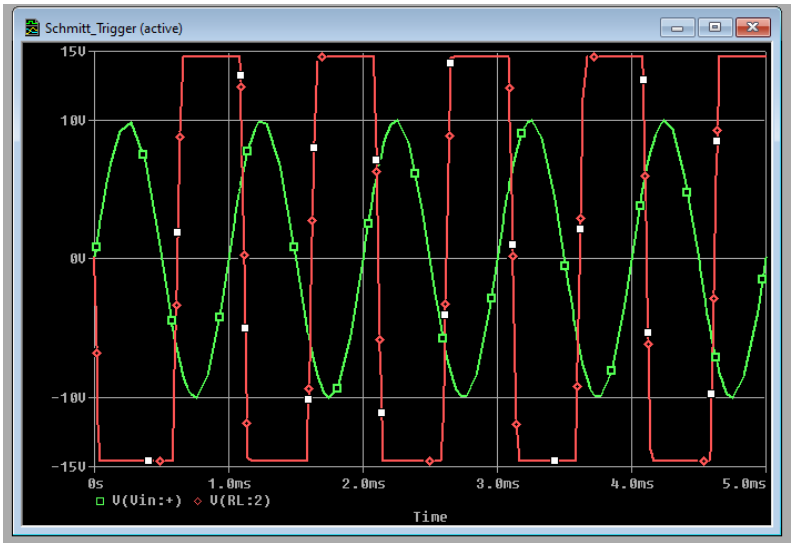


Figure 6.30: Simulation result of Inverting Schmitt trigger.

******

Experiment No. 8: Op-amp Astable Multivibrator

Astable Multivibrator

AIM:

- Design and simulate an Op-Amp astable multivibrator for the clock period of ____seconds.

Circuit diagram:

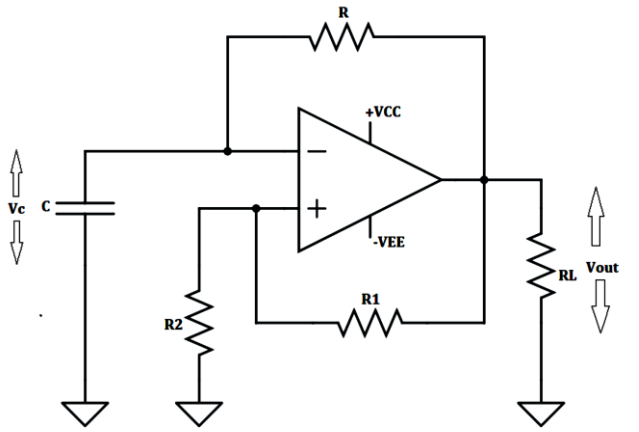


Figure 8.1: Circuit diagram of Astable Multivibrator using Op-Amp.

Design:

Design of astable multivibrator for the time period of 1ms.

We know that,

$$T = 2RC\ln\left(\frac{1+\beta}{1-\beta}\right)$$

$$1x10^{-3} = 2RC\ln\left(\frac{1+\beta}{1-\beta}\right)$$

Choose,

$$C = \mathbf{0.1uF}, \mathbf{R_1 = 10K\Omega \text{ and } R_2 = 10K\Omega}$$

$$\therefore 1x10^{-3} = 2RC\ (0.4054)$$

$$\therefore R = 12.331.98\Omega \cong \mathbf{12K\Omega}$$

Components required:

Table 8.1: Components required for the simulation of Astable Multivibrator

Sl. No.	Part	Values/Attributes	Quantity
1	uA741	--	1
2	Resistors	10K	2
3	Resistor	12K	1
4	Resistor	1K	1
5	Capacitor	0.1uF	1
6	VDC	15V	2

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 8.1.
4. Setup the analysis
   - Analysis type: **Transient**
   - End time = 5m
5. Simulate the schematic and observe the output.

PSPICE Schematic:

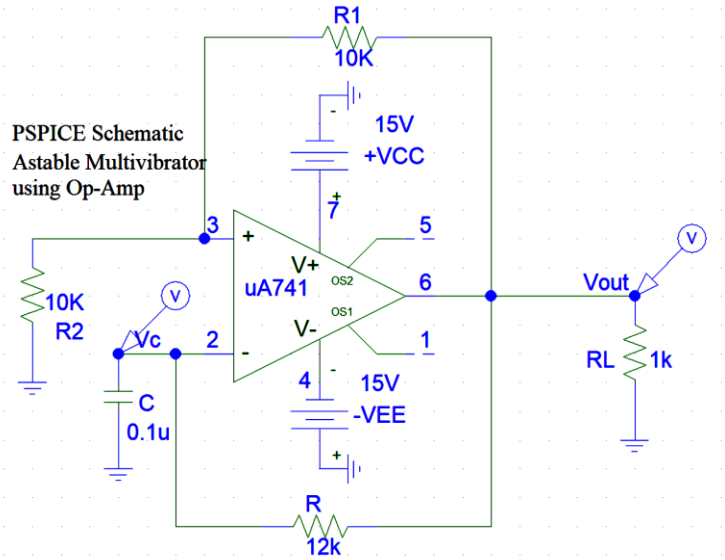


Figure 8.3: PSPICE Schematic of Astable Multivibrator using Op-Amp.

Simulation Result:

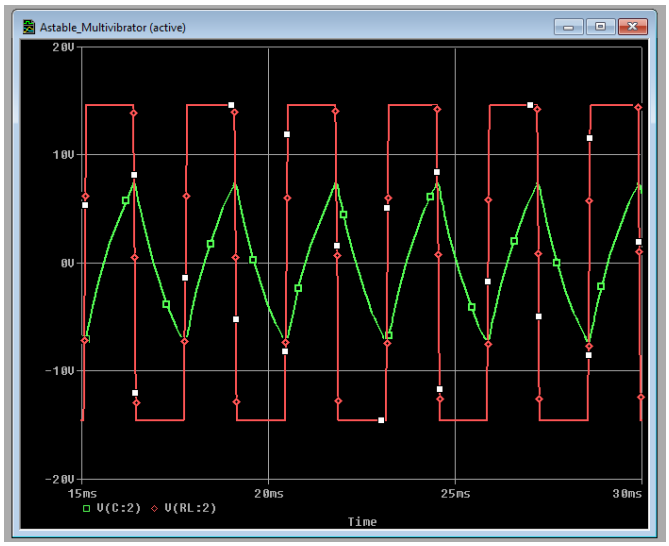


Figure 8.4: Simulation Result of Astable Multivibrator using Op-Amp.

******

Experiment No. 9: I order and II order Butterworth Low-Pass Filter

a. 1st order Butterworth low pass filter.

AIM:

- Design and simulate an Op-Amp based 1st order Butterworth low pass filter for the cut-off frequency_____Hz.

Circuit diagram:

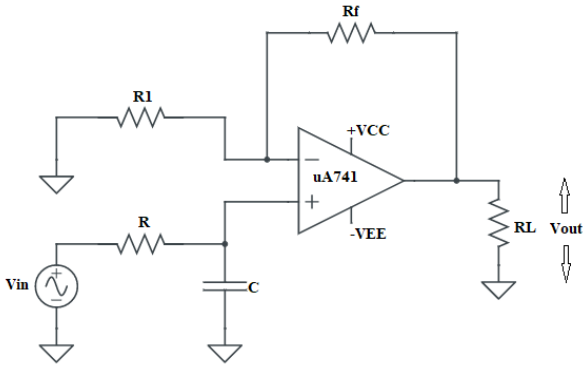


Figure 9.01: Circuit diagram of 1st order Butterworth low pass filter.

Design:

Design of 1st order Butterworth low pass filter for cut-off frequency=1KHz.

We Know that,

$$f_c = \frac{1}{2\pi RC}$$

$$1\text{KHz} = \frac{1}{2\pi RC}$$

Choose, $\mathbf{C = 0.1uF}$

$$\therefore \mathbf{R = 1.591K\Omega \cong 1.6K\Omega}$$

Design of feedback circuit for the gain of 2

We know that,

$$\mathbf{A = 1 + \frac{R_f}{R_1}}$$

Choose, $\mathbf{R_1 = 1K\Omega}$

$$\therefore \mathbf{R_f = 1K\Omega}$$

Components Required:

Table 9.1: Components required for the simulation of 1st Order Butterworth low pass filter

Sl. No.	Part	Values/Attributes	Quantity
1	uA741	--	1
2	Resistors	1K	2
3	Resistor	1.6K	1
4	VAC	ACMAG=1V	1
5	VDC	15V	2

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 9.1.
4. Setup the analysis
   - Analysis type: **AC Sweep**
5. Simulate the schematic and observe the output.

   NOTE: At the simulation window, choose the Y axis variable as $\frac{V_{out}}{V_{in}}$

PSPICE Schematic:

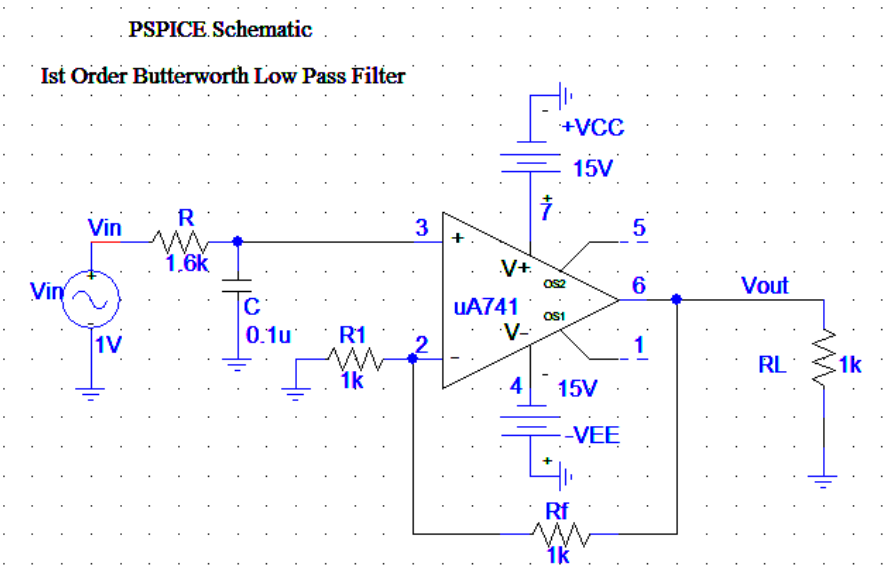


Figure 9.03: PSPICE Schematic of 1st order Butterworth low pass filter.

Simulation Result:

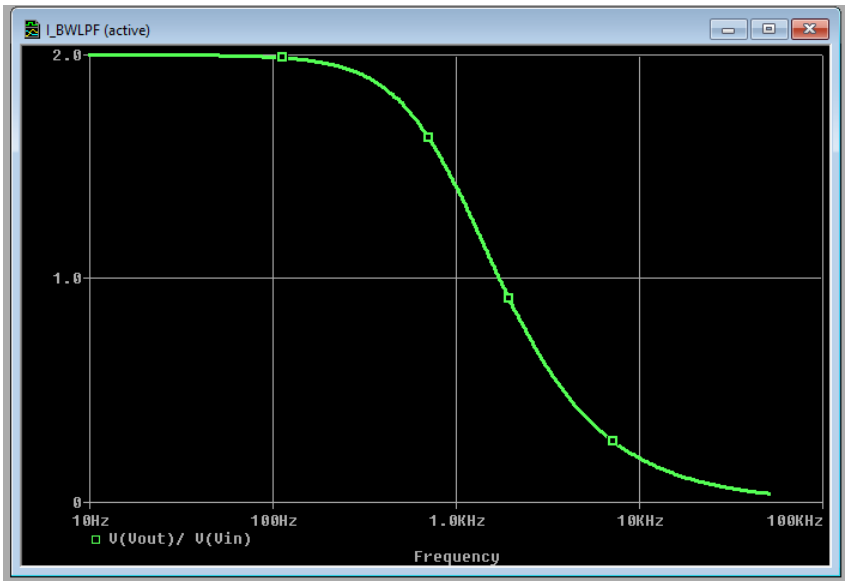


Figure 9.04: Simulation result of 1st order Butterworth low pass filter.

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b. 1st order Butterworth high pass filter

AIM:

- Design and simulate an Op-Amp based 1st order Butterworth high pass filter for the cut-off frequency_____Hz.

Circuit diagram:

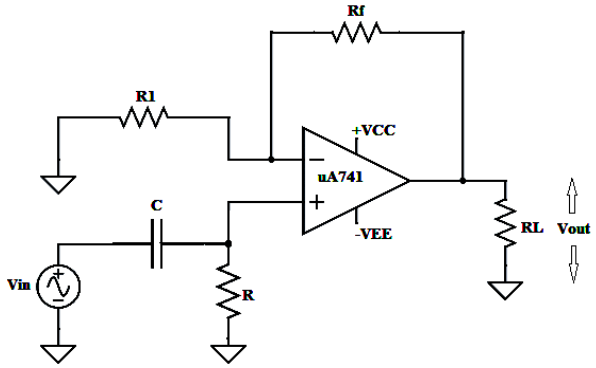

Figure 9.05: Circuit diagram of 1st order Butterworth high pass filter.

Design:

Design of 1st order Butterworth low pass filter for cut-off frequency=1KHz.

We Know that,

$$f_c = \frac{1}{2\pi RC}$$

$$1\text{KHz} = \frac{1}{2\pi RC}$$

Choose, $\mathbf{C = 0.1uF}$

$$\therefore \mathbf{R = 1.591K\Omega \cong 1.6K\Omega}$$

Design of feedback circuit for the gain of 2

We know that,

$$\mathbf{A = 1 + \frac{R_f}{R_1}}$$

Choose, $\mathbf{R_1 = 1K\Omega}$

$$\therefore \mathbf{R_f = 1K\Omega}$$

Components Required:

Table 9.2: Components required for the simulation of 1st Order Butterworth high pass filter

Sl. No.	Part	Values/Attributes	Quantity
1	uA741	--	1
2	Resistors	1K	2
3	Resistor	1.6K	1
4	VAC	ACMAG=1V	1
5	VDC	15V	2

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 9.2.
4. Setup the analysis
   - Analysis type: **AC Sweep**
5. Simulate the schematic and observe the output.

   NOTE: At the simulation window, choose the Y axis variable as $\frac{V_{out}}{V_{in}}$

PSPICE Schematic:

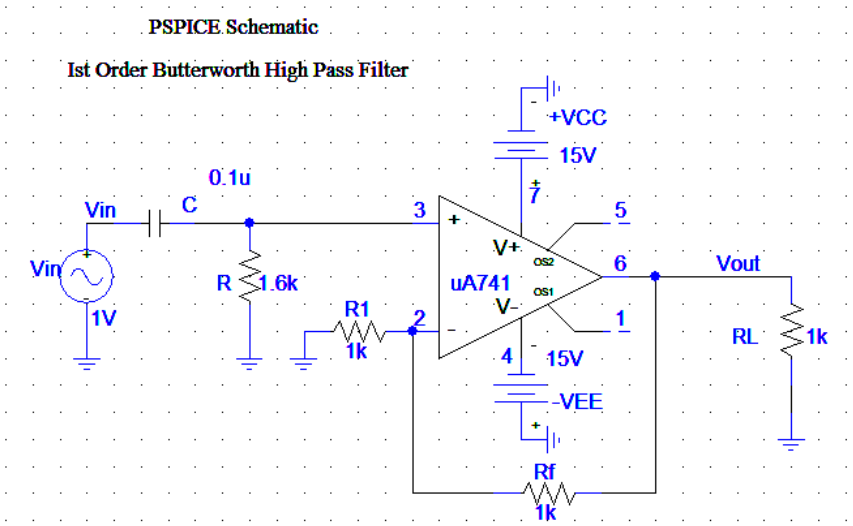

Figure 9.07: PSPICE Schematic of 1st order Butterworth high pass filter.

Simulation Result:

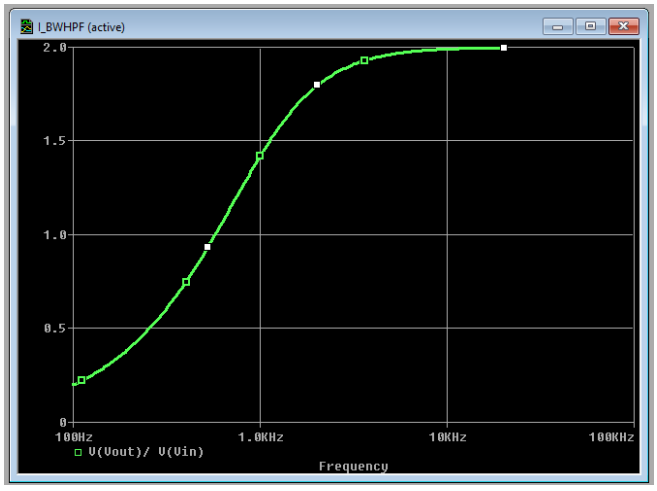

Figure 9.08: Simulation Result of 1st order Butterworth high pass filter.

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c. 2nd order Butterworth low pass filter

AIM:

- Design and simulate an Op-Amp based 2nd order Butterworth low pass filter for the cut-off frequency_____Hz.

Circuit diagram:

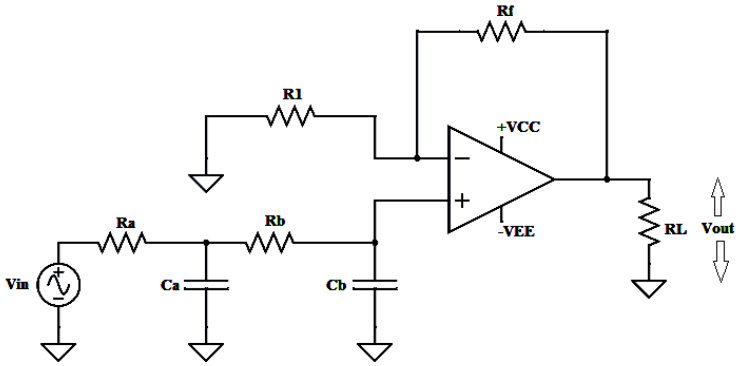

Figure 9.09: Circuit diagram of 2nd order Butterworth low pass filter.

Design:

Design of 2nd order Butterworth low pass filter for cut-off frequency=1KHz.

We Know that,

$$f_c = \frac{1}{2\pi\sqrt{R_a R_b C_a C_b}}$$

$$1\text{KHz} = \frac{1}{2\pi\sqrt{R_a R_b C_a C_b}}$$

Choose, $\mathbf{C_a = 0.1uF, C_b = 0.1uF, R_a = 1K\Omega}$

$$\therefore \mathbf{R_b = 2.533K\Omega \cong 2.6K\Omega}$$

Design of feedback circuit for the gain of 2

We know that,

$$\mathbf{A = 1 + \frac{R_f}{R_1}}$$

Choose, $\mathbf{R_1 = 1K\Omega}$

$$\therefore \mathbf{R_f = 1K\Omega}$$

Components Required:

Table 9.3: Components required for the simulation of 2nd Order Butterworth low pass filter

Sl. No.	Part	Values/Attributes	Quantity
1	uA741	--	1
2	Resistors	1K	3
3	Resistor	2.6K	1
	Capacitors	0.1uF	2
4	VAC	ACMAG=1V	1
5	VDC	15V	2

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 9.3.
4. Setup the analysis
   - Analysis type: **AC Sweep**
5. Simulate the schematic and observe the output.

   NOTE: At the simulation window, choose the Y axis variable as $\frac{V_{out}}{V_{in}}$

PSPICE Schematic:

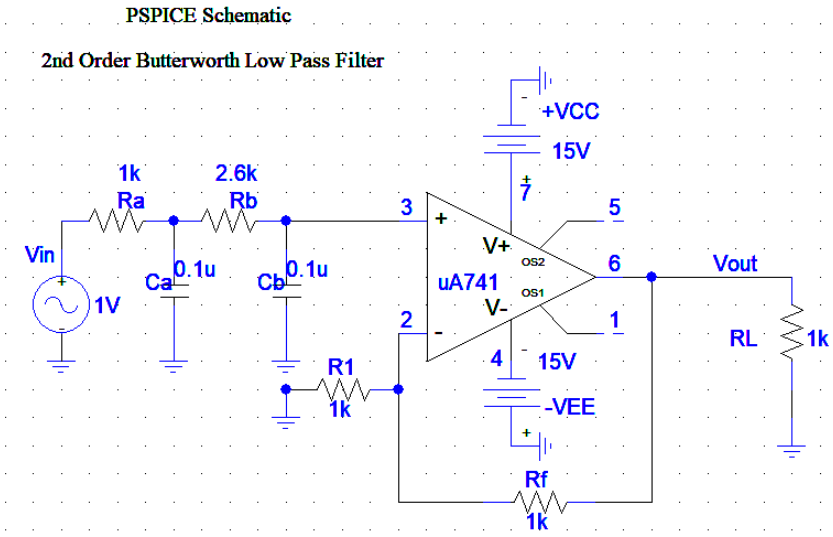

Figure 9.11: PSPICE Schematic of 2nd order Butterworth low pass filter.

Simulation Results:

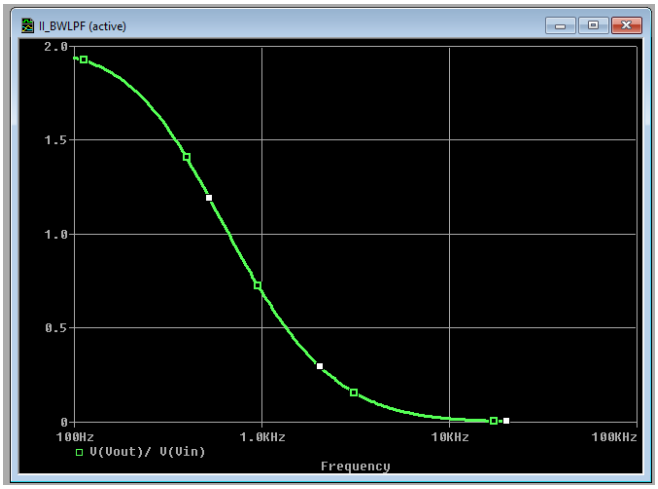

Figure 9.12: Simulation result of 2nd order Butterworth low pass filter.

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d. 2nd order Butterworth high pass filter

AIM:

- Design and simulate an Op-Amp based 2nd order Butterworth high pass filter for the cut-off frequency_____Hz.

Circuit diagram:

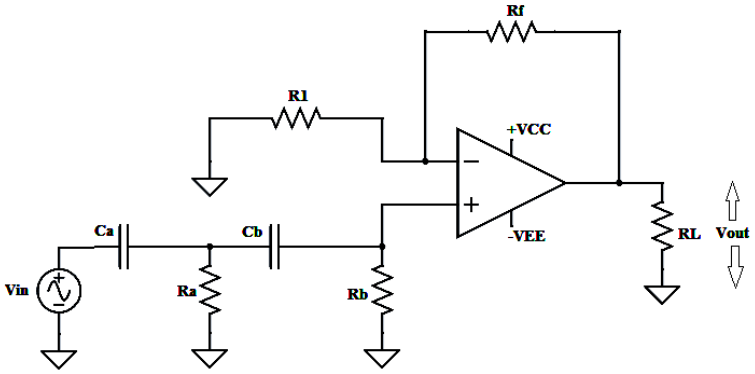

Figure 9.13: Circuit diagram of 2nd order Butterworth high pass filter.

Design:

Design of 2nd order Butterworth low pass filter for cut-off frequency=1 KHz.

We Know that,

$$f_c = \frac{1}{2\pi\sqrt{R_a R_b C_a C_b}}$$

$$1\text{KHz} = \frac{1}{2\pi\sqrt{R_a R_b C_a C_b}}$$

Choose, $\mathbf{C_a = 0.1uF, C_b = 0.1uF, R_a = 1K\Omega}$

$$\therefore \mathbf{R_b = 2.533K\Omega \cong 2.6K\Omega}$$

Design of feedback circuit for the gain of 2

We know that,

$$\mathbf{A = 1 + \frac{R_f}{R_1}}$$

Choose, $\mathbf{R_1 = 1K\Omega}$

$$\therefore \mathbf{R_f = 1K\Omega}$$

Components Required:

Table 9.4: Components required for the simulation of 2nd Order Butterworth high pass filter

Sl. No.	Part	Values/Attributes	Quantity
1	uA741	--	1
2	Resistors	1K	3
3	Resistor	2.6K	1
4	Capacitors	0.1uF	2
5	VAC	ACMAG=1V	1
6	VDC	15V	2

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 9.4.
4. Setup the analysis
   - Analysis type: **AC Sweep**
5. Simulate the schematic and observe the output.

   NOTE: At the simulation window, choose the Y axis variable as $\frac{V_{out}}{V_{in}}$

PSPICE Schematic:

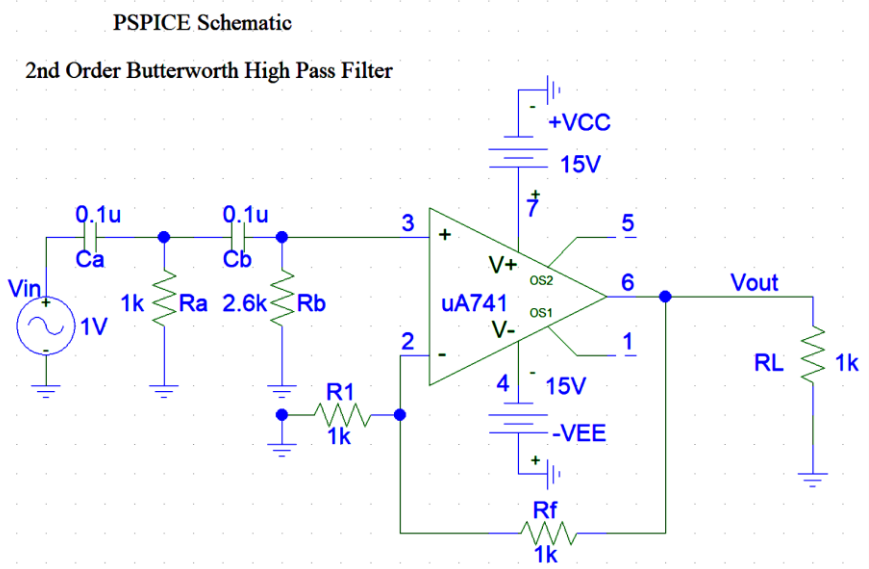

Figure 9.15: PSPICE Schematic of 2nd order Butterworth high pass filter.

Simulation Result:

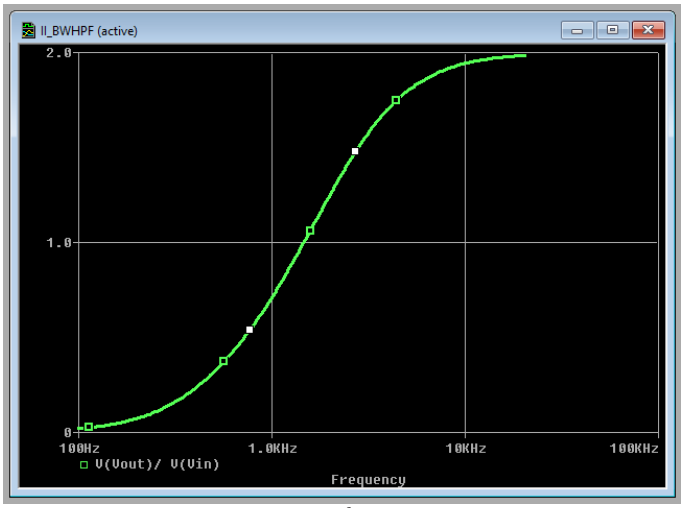

Figure 9.16: Simulation result of 2nd order Butterworth high pass filter.

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Experiment No. 10: RC Phase Shift Oscillator Using Op-Amp

RC Phase Shift Oscillator Using Op-Amp

AIM:

- Design and simulate an Op-Amp based RC phase shift oscillator for the frequency of _____Hz.

Circuit diagram:

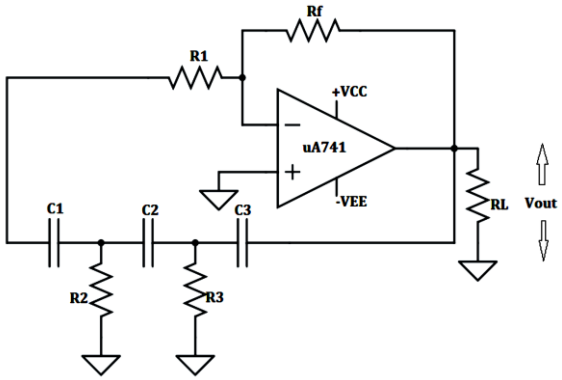

Figure 10.1: Circuit diagram of RC Phase Shift Oscillator using Op-Amp.

Design:

Design of RC feedback network for the frequency of 2KHz.

We know that,

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

$$2x10^{3} = \frac{1}{2\pi RC\sqrt{6}}$$

Choose, $\mathbf{C = 0.01uF}$

$$\therefore \mathbf{R} = 3.248K\Omega \cong \mathbf{3.3K\Omega}$$

Design for open loop gain of greater than 29

We know that,

$$A = \left|\frac{R_f}{R_1}\right|$$

Choose, $\mathbf{R_1 = R = 3.3K\Omega}$ and $A \geq 29$ say 30.

$$\therefore \mathbf{R_f} = 99K\Omega \cong \mathbf{100K\Omega}$$

Components required:

Table 10.1: List of parts required for PSPICE Simulation

Sl. No.	Parts	Value/Attributes	Quantity
1	uA741	--	1
2	Resistors	3.3K**Ω**	3
3	Resistor	99K**Ω**	1
4	VDC	15V	2
5	Capacitors	Value=0.01uF, IC=0	3

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the components required table 10.1.
4. Setup the analysis
   - Analysis type= **Transient Analysis**
5. Simulate the schematic and observe the designed values and simulation result.

PSPICE Schematic:

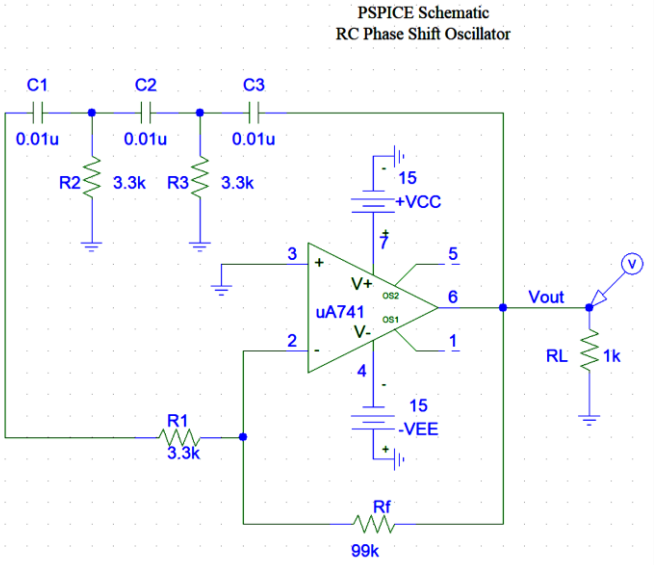

Figure 10.3: PSPICE Schematic of RC Phase Shift Oscillator using Op-Amp

Simulation Result:

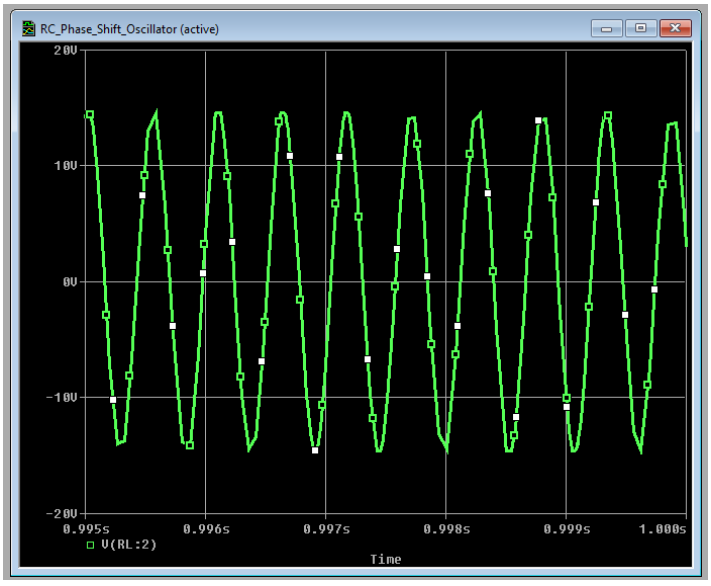

Figure 10.4: Simulation result of RC Phase Shift Oscillator using Op-Amp

******

Experiment No. 11: Monostable Multivibrator using 555 Timer

Monostable Multivibrator using 555 Timer

AIM:

- Design and simulate a monostable multivibrator using IC 555 timer for the pulse width of _____seconds.

Circuit diagram:

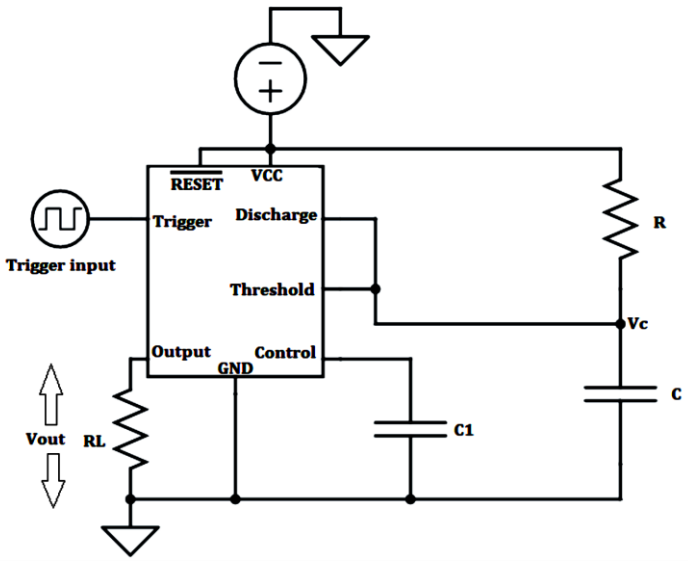

Figure 11.1: Circuit diagram of Monostable Multivibrator using 555 Timer

Design:

Design of monostable multivibrator for the period T=0.5s

We know that,

$$T \cong 1.1RC$$

Choose, $C = 10\mu F$

$$\therefore R = 45.5K\Omega$$

$$T_{trigger} < T$$

$$\therefore T_{rigger} = 0.4s, T_{on} = 0.05s$$

Choose control capacitor $C_1 = 10nF$ and Load resistor $R_L = 1K\Omega$

Components required:

Table 11.1: List of parts required for PSPICE Simulation

Sl. No.	Parts	Value/Attributes	Quantity
1	IC 555 Timer	--	1
2	Resistor	45.5KΩ	1
3	Resistor	1KΩ	1
4	VDC	5V	1
5	VPULSE	DC=0, AC=0, V1=5, V2=0 TD=0, TR=10p, TF=10p, PW=0.05, PER=0.4	4
6	Capacitor	10u	1
7	Capacitor	10n	1

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 11.1.
4. Setup the analysis
   - Analysis type= **Transient**
   - Print step=0ns(default)
   - End Time=5s
5. Simulate the schematic and observe the designed values and simulation result.

PSPICE Schematic:

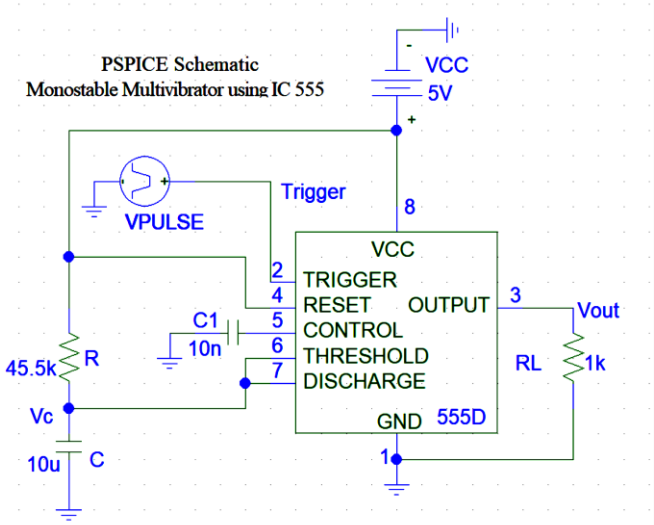

Figure 11.3: PSPICE Schematic of Monostable Multivibrator using 555 Timer

Simulation Result:

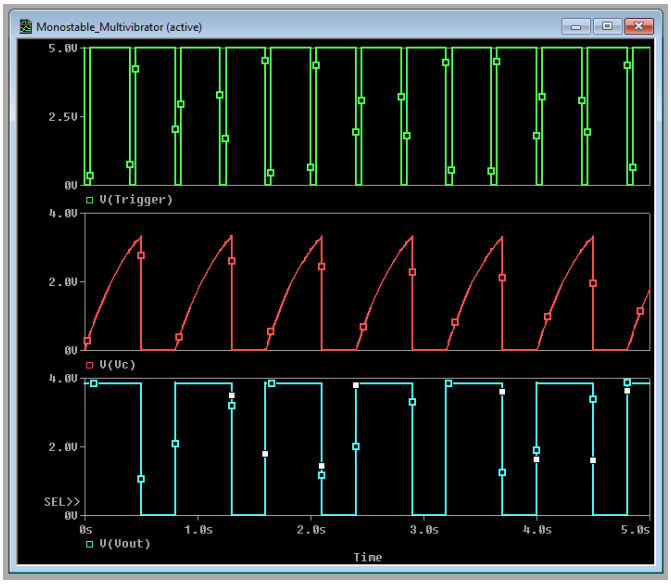

Figure 11.4: Simulation Result of Monostable Multivibrator using 555 Timer

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Experiment No. 12: R2R digital to analog converter

R2R Ladder Network DAC

AIM:

- Design and simulate an Op-Amp based four-bit R2R digital to analog converter.

Circuit diagram:

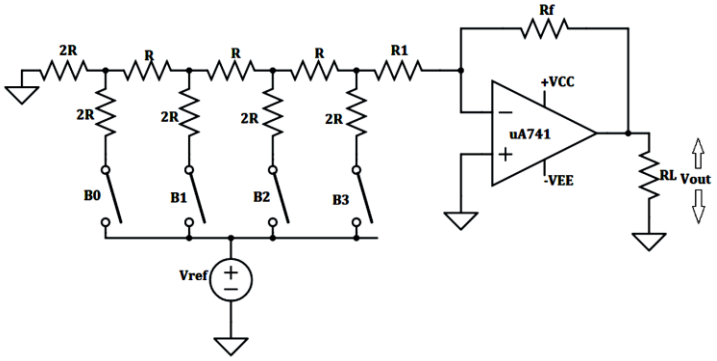

Figure 12.1: Circuit diagram of 4-bit R-2R ladder network DAC.

Design:

Design of 4-bit R-2R ladder network with the reference voltage, $V_{ref} = 5V$ and gain $A = 1$.

R-2R, ladder network, and its equivalent resistance for any combination of input is R, and if the value of R1=R, and Rf=2R1, The gain of the system becomes unity.

So, let R1=R=1K

$$\therefore R_f = 2K$$

Output equation is

$$V_{out} = -V_{ref}\left(\frac{B_3}{2^4} + \frac{B_2}{2^3} + \frac{B_1}{2^2} + \frac{B_0}{2^1}\right) - - - (12.6)$$

Expected Tabular Column:

Table 12.1: Expected results

Sl. No.	Input Bits	Output voltage		Sl. No.	Input Bits	Output voltage
1	0000	0V		9	1000	-2.49V
2	0001	-0.31V		10	1001	-2.81V
3	0010	-0.62V		11	1010	-3.12V
4	0011	-0.93V		12	1011	-3.43V
5	0100	-1.25V		13	1100	-3.74V
6	0101	-1.56V		14	1101	-4.06V
7	0110	-1.87V		15	1110	-4.37V
8	0111	-2.18V		16	1111	-4.68V

Components required:

Table 12.2: List of parts required for PSPICE Simulation

Sl. No.	Parts	Value/Attributes	Quantity
1	uA741	--	1
2	Resistors	1KΩ	4
3	Resistors	2KΩ	6
4	VDC	15V	2
5	DIGICLOCK	ONTIME=2m, 4m, 8m, 16m OFFTIME=2m, 4m, 8m, 16m	4

Procedure:

1. Place the required components on PSPICE Schematic editor window.
2. Connect the components through wires.
3. Change the attributes as per the table 12.2.
4. Setup the analysis
   - Analysis type= Transient Analysis
   - End frequency=40ms

5. Simulate the schematic and observe the designed values and simulation result.

PSPICE Schematic:

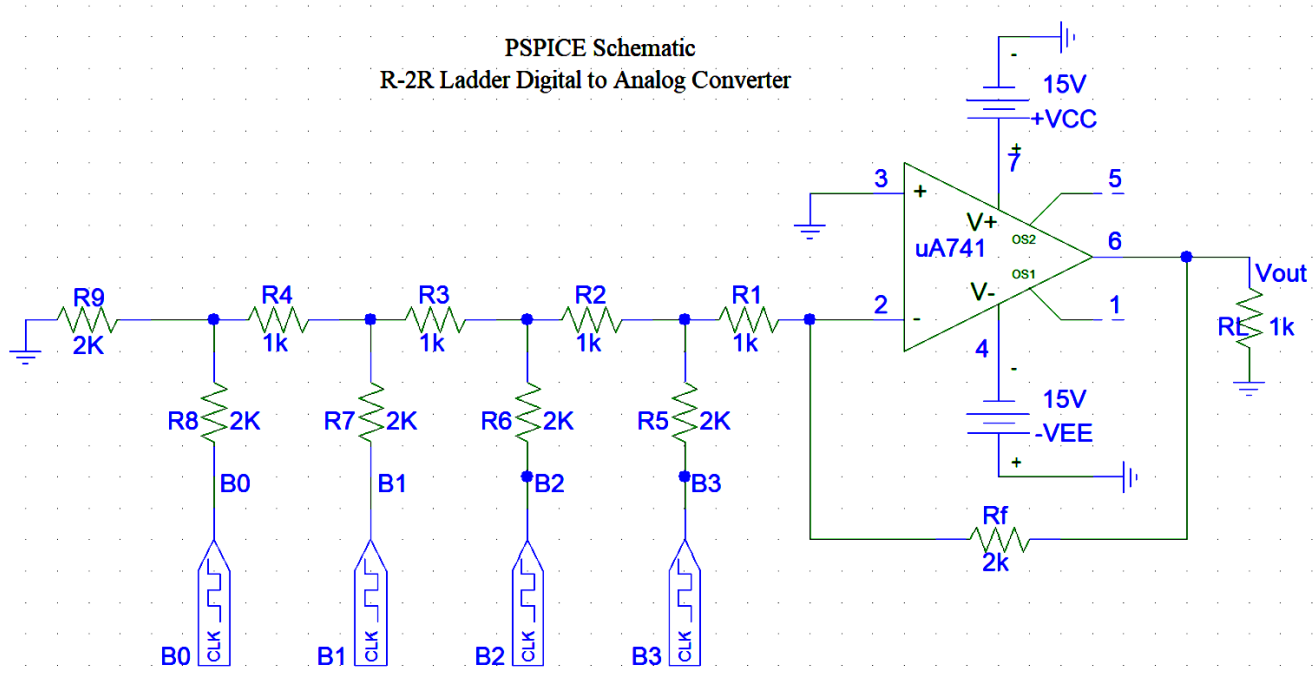

Figure 12.2: PSPICE Schematic of R-2R Ladder DAC

Simulation Results:

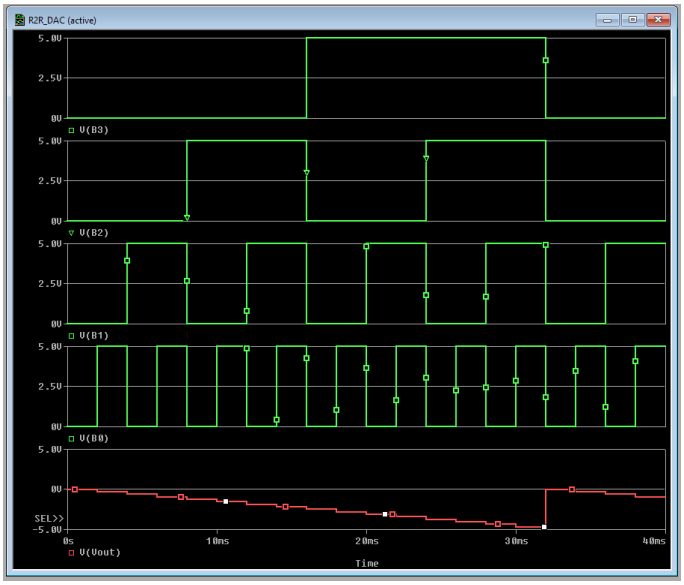

Figure 12.3: Waveforms of Input bits and output

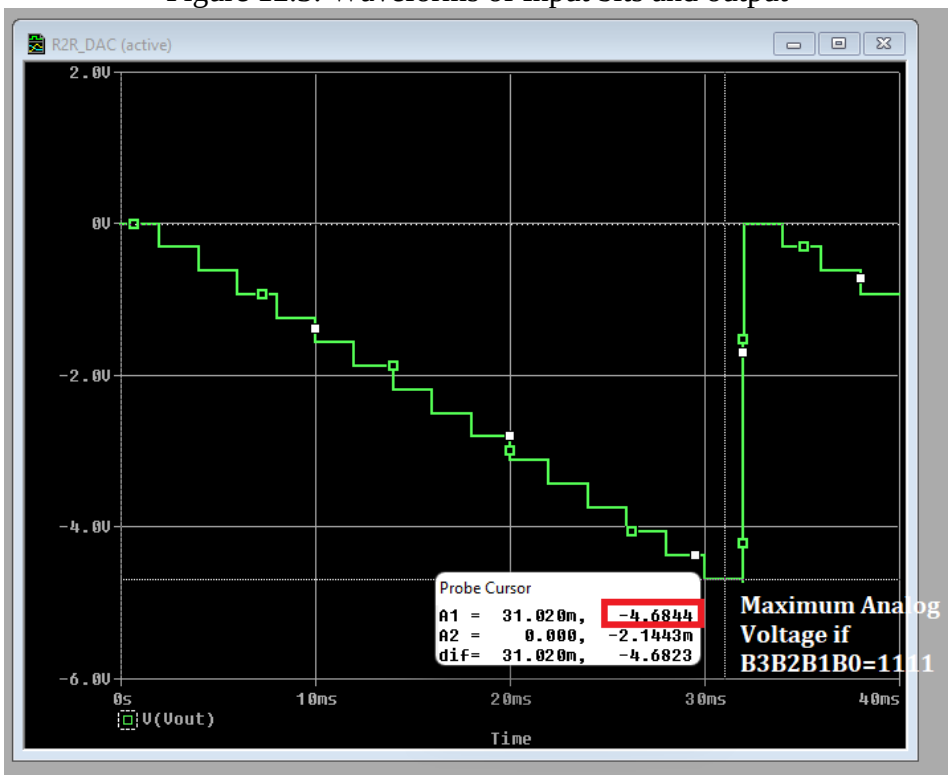

Figure 12.4: Output Waveforms without input bits.

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References

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5. https://www.allaboutcircuits.com/
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