

# Pseudo-random number generators for Monte Carlo simulations on Graphics Processing Units

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## Abstract

Basic uniform pseudo-random number generators are implemented on ATI Graphics Processing Units (GPU). The performance results of the realized generators (multiplicative linear congruential (GGL), XOR-shift (XOR128), RANECU, RANMAR, RANLUX and Mersenne Twister (MT19937)) on CPU and GPU are discussed. The obtained speed-up factor is hundreds of times in comparison with CPU. RANLUX generator is found to be the most appropriate for using on GPU in Monte Carlo simulations. The brief review of the pseudo-random number generators used in modern software packages for Monte Carlo simulations in high-energy physics is present.

*Keywords:* Monte Carlo simulations, GPGPU, pseudo-random number generators, performance

## 1 Introduction

The development of the General Purpose computing on Graphics Processing Unit (*GPGPU*) technology has opened recently a new cheap alternative to supercomputers and cluster systems for researchers. The primary role of the GPGPU technology promotion justly belongs to nVidia company which is the one of the two main GPU hardware developers. nVidia motto is “One Researcher, One Supercomputer”. It fully reflects the tendencies of the computational systems present-day market. Moreover, the systems which providing the GPGPU technology become the integral parts of the contemporary supercomputers. In particular, while assembling new supercomputer TH-1 with peak productivity 1.206 petaflops which is equipped with the ATI GPUs HD 4870X2 on every node, China became the third country to build a petaflop supercomputer (after USA and Germany) [1].

Pseudo-random numbers generation algorithms are key components in most modern packages for researches and result depends on their characteristics. The package should provide the actual investigation of the physics or the other simulated problems, but not to explore the behavior of the generator itself. Thus, while choosing generator, one should consider not only its performance productivity but also its statistical properties. Checking the key results with generator of a different class than used one is also very important [2]. “Pseudo-random” term actually means that for such values always exist an algorithm which may reproduce the whole sequence. The values, produced by some physical process, cannot be considered as random in a general sense, because even if we cannot predict the sequence of such numbers, it does not mean that there is no algorithm to produce them [3].

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The main aim of the present paper is to show the possibility to adapt for GPU the most commonly used pseudo-random number generators (*PRNG*) as the main components of the software packages for Monte Carlo (*MC*) simulations. An essential distinction of the GPU architecture from the Central Processing Unit (*CPU*) architecture causes new difficulties as well as new optimization capabilities. The question about the performances of the different PRNGs on GPU platform is arisen in this connection. The performance results and the difference between PRNGs performances on CPU and GPU will be shown in the paper.

We will restrict our investigation only to uniform PRNGs. In particular some generators were already investigated for nVidia GPUs in [4, 5]. But studied generators are not the most frequently used ones in MC simulations.

In the present paper we will not refer the question of the random-number generator testing (see for example [6] and references therein) and will content only with implementation of existing generators on GPU.

The paper is organized as follows. Section 2 contains the brief list of the software packages for MC simulations in high-energy physics with showing PRNGs which are used in the corresponding package. The details of the GPU implementation and the code listings of the realized PRNGs are described in section 3. The performance results and discussion are collected in section 4. In section 5 we draw our conclusions. Finally, appendix includes some theoretical background for the realized PRNG algorithms.

## 2 PRNGs in Monte Carlo simulations

In this section we present the list of PRNGs which are employed in nowadays MC simulations.

To choose a generator which will be used in MC simulations, it is not enough to consider only its period and algorithm output. The generator R250 was widely used due to its simplicity and long period, but it was found that this generator has the essential statistical defects which make impossible to use it in modern simulations (see [9] and reference therein). Apart from general statistical tests like *DIEHARD Battery of Tests of Randomness* and *Crush*, a generator has to pass empirical test in real conditions. That is why, while developing MC application, usually only generators with minimal statistical influence for the present MC simulations are used. For example, European Organization for Nuclear Research (*CERN*) recommends using three PRNGs: RANMAR (V113), RANECU (V114) and RANLUX (V115).

Below is the incomplete list of the software packages for MC simulations in high-energy physics and the PRNG which is used in corresponding package.

- **FermiQCD**: is an open C++ library for development of parallel Lattice Quantum Field Theory computations [32, 33]. It uses floating-point version of RANMAR generator as default PRNG.
- **UKQCD**: By indirect information UKQCD Collaboration also uses RANMAR PRNG [34] in its software.
- **MILC**: is an open code of high performance research software written in C for doing  $SU(3)$  lattice gauge theory simulations on several different (MIMD) parallel computers [35]. **MILC** uses own XOR of a 127-bit feedback shift register and a 32 bit integer congruential generator. Each node or site uses a different multiplier in the congruential generator and different initial state in the shift register. So, all nodes are generating different sequences of numbers.

$$t = (((X_{n-5} \gg 7) \text{ OR } (X_{n-6} \ll 17)) \text{ XOR } \quad (1)$$

$$\begin{aligned}
& ((X_{n-4} \gg 1) \text{ OR } (X_{n-5} \ll 23)) \text{ AND } (2^{24} - 1), \\
X_{n-6} &= X_{n-5}, \quad X_{n-5} = X_{n-4}, \quad X_{n-4} = X_{n-3}, \quad X_{n-2} = X_{n-1}, \\
X_{n-1} &= X_n, \quad X_n = t, \quad Y_n = a_j Y_{n-1} + c, \\
z_n &= (t \text{ XOR } ((Y_n \gg 8) \text{ AND } (2^{24} - 1))) / 2^{24}
\end{aligned}$$

- **CPS**: The Columbia Physics System is a large set of codes for lattice QCD simulations [36]. RAN3 is used.
- **SZIN**: is the open-source software system supports data-parallel programming constructs for lattice field theory and in particular lattice QCD [37]. RANLUX is used in **SZIN** packet.
- **ISAJet**: is a Monte Carlo event generator for  $pp$ ,  $p\bar{p}$ ,  $e^+e^-$  interactions [38, 39]. RANLUX is incorporated into **ISAJet**.
- **GEANT4**: is a toolkit for the simulation of the passage of particles through matter [40]. **GEANT4** uses the **HEPRandom** module [41] to generate pseudo-random numbers which includes 12 different random engines (RANMAR, RANECU, DRAND48, RANLUX, etc) now.
- **PYTHIA**: is a program for the generation of high-energy physics events [42, 43]. RANMAR is used in **PYTHIA** as an internal PRNG.
- **HERWIG**: is a Monte Carlo package for simulating hadron emission reactions with interfering gluons [44, 45]. RANECU is used.
- **CompHEP**: a package for evaluation of Feynman diagrams, integration over multi-particle phase space and event generation [46, 47]. DRAND48 is used in **CompHEP**.
- **MC@NLO**: is a Fortran package to implement the scheme for combining a Monte Carlo event generator with Next-to-Leading-Order calculations of rates for QCD processes [48, 49]. GGL is used.
- **SHERPA**: is a Monte Carlo event generator for the simulation of high-energy reactions of particles in lepton-lepton, lepton-photon, photon-photon and hadron-hadron collisions [50, 51]. RANMAR is used.
- **Chroma**: is a software system for lattice QCD calculations [52, 53]. In **Chroma** slightly modified linear congruential generator RANNYU is implemented – LCG( $a = 31167285, m = 2^{48}$ ).
- **GENIE**: is a neutrino event generator for experimental physics community [54, 55]. MT19937 is used.
- **ALPGEN**: is an event generator for hard multiparton processes in hadronic collisions [56, 57]. RANECU is used.

So, the most commonly used generators are RANMAR, RANLUX, RANECU and several variations of a linear congruential generator (DRAND48, RAN3, GGL, RANNYU). Also, most new packages began to include the generator MT19937 as internal PRNG. Hence, it is reasonable to implement the generators on GPU which are used in real MC simulations.

Table 1: General information about some ATI's video cards [60].

Model	Stream cores	Core (MHz)	Memory (MHz)	Bandwidth (GB/s)	Bus width (bit)	Tflops (peak)
HD 4850	800	625	993*	64	256	1.0
HD 4870	800	750	900	115.2	256	1.2
HD 4870X2	$2 \times 800$	$2 \times 750$	900	$2 \times 115.2$	$2 \times 256$	2.4
HD 5850	1440	725	1000	128	256	2.1
HD 5870	1600	850	1200	153.6	256	2.7
HD 5970	$2 \times 1600$	$2 \times 725$	1000	$2 \times 128$	$2 \times 256$	4.6

### 3 GPU implementation

In this section we give the base ideas for PRNG implementation on GPU and describe the source codes of the following PRNGs realizations on ATI GPUs: GGL, XOR128, RANECU, RANMAR, RANLUX and MT19937.

We use ATI Stream SDK [61] for the realization of the PRNGs on ATI GPU as software environment. ATI CAL allows using ATI GPU hardware in the most effective way [58]. That is why all PRNGs realizations presented below are made on ATI Intermediate Language (*IL*) [59], and not on higher level, for example OpenCL or Brook+.

Three different ATI video cards are used to check the algorithm efficiency – ATI Radeon HD 5850, HD 4870 and HD 4850. The essential for GPGPU-applications parameters about some ATI's video cards are presented in Table 1. All cards are equipped with the GDDR5 memory except HD 4850 which contains GDDR3 memory (this fact was marked with the asterisk). GDDR5 memory possesses a quadruple effective data transfer rate relative to its physical clock rate, instead of double as with GDDR3 memory. It is necessary to note that HD 4870X2 and HD 5970 are two-core cards. For our purposes at program level they are equivalent to two devices installed in the system.

#### 3.1 General implementation scheme

To design the GPU-applications it must be accounted the following main features of hardware architecture:

- each general-purpose register and memory cell has the four 32-bit components that are designated as *.x*, *.y*, *.z* and *.w*;
- floating point operations are more productive on GPU than integer operations (in compare with CPUs);
- double precision floating point operations are the slowest on GPU;
- ATI GPU can perform up to five operations on each VLIW processor simultaneously.

Computing programs working for GPU are known as kernels. All kernels are run by the host program. Each kernel must perform a complete operation, because of ATI Stream SDK does not support the execution of a kernel from another kernel (except OpenCL applications).

We offer to use PRNGs directly in MC procedures as the separate subroutines. Undoubtedly such scheme allows the possibility to keep generated random numbers

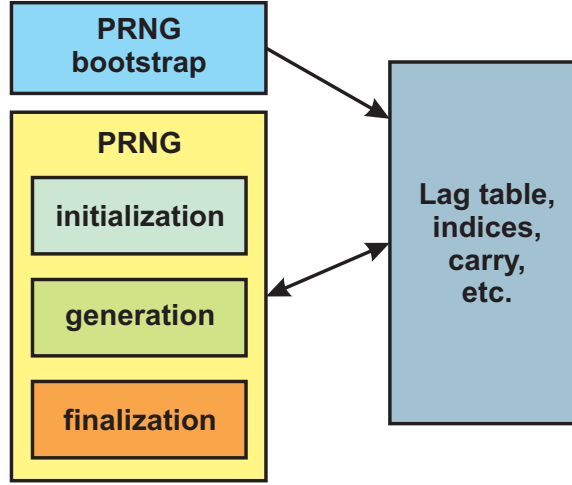


Figure 1: PRNG structure scheme

in GPU-memory, for example, for further usage by other procedures, as it is usually made in CPU-simulations. However, it seems to be more effective to “virtualize” produced by PRNG pseudo-random numbers as it allows to eliminate unnecessary additional read-write operations to the GPU-memory for the random numbers as well as to decrease the GPU-memory consumption of the application.

In order to accelerate GPU-applications work, we recommend to keep all data needed for kernel operations directly in GPU-memory, because memory operations are a bottleneck of GPU.

For MC simulations on GPU it is convenient to produce four random numbers through one PRNG pass which is closely related to GPU memory architecture. Under such conditions one can use GPU performance in the most efficient way. As a rule more than one random number are used in MC simulations for updating (for example, one for update proposition and one for probability). So, it seems to be natural to generate the corresponding number of the pseudo-random numbers for further purposes.

The common structure scheme of PRNGs is shown in Figure 1. All implemented PRNGs are divided into 3 phases:

- *initialization*: loading and preparing the previous state of PRNG and all preparing operations for PRNG;
- *random number generation*: actually all PRNG operations which generate pseudo-random numbers;
- *finalization*: storing the final state of PRNG for the next run.

It allows to make the best use of PRNG, as it is needed a few more random numbers. For example, at multihit updating method the several pseudo-random numbers are required per one pass of the updating procedure. The initialization subroutine of the PRNG is called on the start of the updating procedure. During the work the updating procedure may call the PRNG generation subroutine many times. And finally, at the end it must call the finalization subroutine of the PRNG.

All PRNG lag tables are stored directly in GPU-memory and it avoids needless transfer the data between CPU and GPU memory. Each instance of the PRNG uses its own lag table to parallelize the process. The universal method of the paralleling is used in all realized PRNGs – using the independent sequences. To be exact, every

```

il_cs_2_0
...
call 10
...
call 11
// random number in r200
...
call 12
...
endmain

func 10 // PRNG initialization
dcl_literal 1200, 0, 0, 0, %PM_r%, %PM_m, FP%
dcl_literal 1201, %PMSEED_MASK%, %PM_a%, %PM_m%, %PM_q%
and r201.x, vaTid.x, 1201.x
mov r203, g[r201.x+%iIPMSEED_START%]
ret_dyn
endfunc

func 11 // PRNG generation
udiv r202, r203, 1201.www
umod r204, r203, 1201.www
umul r205, r202, 1200.zzzz
imad r206, r204, 1201.yyyy, r205
ilt r207, 1200.xxxx, r206
cmov_logical r208, r207, 1200.xxxx, 1201.zzzz
iadd r203, r206, r208
utof r200, r203
div r200, r200, 1200.www
ret_dyn
endfunc

func 12 // PRNG finalization
mov g[r201.x+%iIPMSEED_START%], r203
ret_dyn
endfunc
end

```

Figure 2: Source code of GGL PRNG

running instance of PRNG obtains its own index  $J = 0, 1, \dots, J_{max}$ . The lowest bits of  $J$  serve to identify the lag table for PRNG. Another possible scheme which may be used is the selection of the lag table through the modulo operation.

We use a little bigger number of actual PRNG instances than the number of the stream cores in particular GPU to avoid possible collisions among threads. For example, top one-unit ATI GPU card HD 5870 has 1600 stream cores (see Table 1), while 13 lowest bits were used to identify the lag table for PRNG. It corresponds to the 8192 parallel instances of the PRNG.

Almost all generators require the initialization procedure to bootstrap the lag table (three of presented here generators, RANMAR, RANLUX and MT19937). This procedure is realized directly on the GPU unit, not with the help of the CPU with further transfer the lag table into GPU-memory. We do not show lag table initialization procedure here to save the space in the article.

For convenience and performance purposes all the kernels have been precompiled to replace all constants %VariableName% with the corresponding values. It allows to avoid the constant buffer using and put the runtime constant parameters directly in assembler code. Under %VariableName% the value of the respecting variable will be implied in source codes below. Sometimes before the VariableName it will stay the prefix i (like %iVariableName%) which will show the decimal format instead of the default hexadecimal format. Decimal format is needed to specify the relative offsets in global memory operations.

Note that each of the presented generators can be easily modified for the generation of the pseudo-random numbers with double precision. All presented generators are either 24-bit, or 32-bit, while for number representation with double precision 64 bits are required. Thus, for correct generation pseudo-random numbers with double precision one should use several numbers with single precision, but not only covert a number with the single precision into the double precision number by the regular conversion command (it considerably decreases the quantity of possible realization).

### 3.2 GGL

GGL is one of the simplest and computational “light” portable PRNG which could be implemented on GPU. GGL has been studied by Langdon on nVidia Tesla T10P with CUDA SDK [5]. The obtained peak performance of the PRNG is about  $2 \times 10^9$  pseudo-random numbers per second. It is obvious that while period  $P_{GGL} \leq 2147483646$  and its run in 1024-threads and output  $10^9$  pseudo-random numbers per second the GGL period could be exhausted in about 0.002 second. So, GGL are realized here just to check the performance of the pseudo-random number production on ATI GPUs on a very simple generator which requires to store only one seed value per PRNG instance.

Park and Miller have published the four Pascal implementations of the GGL [12], for integer and real arithmetic (one direct scheme and one avoiding the overflow). For implementation we chose the “*Integer version 2*” of the GGL [12]. The ATI IL source code of GGL PRNG is presented in Figure 2. There are three subroutines 10, 11 and 12 after the main module. Subroutines 10 and 12 are called only once and perform the initialization and the finalization of the PRNG, correspondingly. Subroutine 11 produces four-component pseudo-random numbers in register R200 per one pass. This program scheme fully corresponds to the basic scheme, described in subsection 3.1, and hereinafter will be used for the rest of generators presented in this work.

The used variables are:

$$\begin{aligned} \text{PM\_m} &= 2147483647, & \text{PM\_m\_FP} &= 2147483647.0, \\ -\text{PM\_r} &= -2836, & \text{PM\_a} &= 16807, \\ \text{PM\_q} &= 127773, \end{aligned}$$

PMSEED\_MASK specifies the PRNG instance and iPMSEED\_START is the offset of the lag table in the global buffer which is prepared by the host program.

The parallelization scheme with separate sequences is implemented here – every GPU thread produces four separate pseudo-random sequences (by every slot of general purpose register R200). So, the whole number of the pseudo-random sequences is the quadruple number of the threads to be run. The threads must be initialized carefully to reach the maximal period length of the PRNG and avoid the sequences overlapping.

Generator requires to keep only one seed-value per thread for work which is equal to choosing only one four-component cell per thread in global memory which is read and kept only once per PRNG cycle. Thus, for 4096-thread run (or 16384 subthreads) the size of the lag table will be 64kB. Initial seeds are filled with the host program and transferred to GPU memory before the first run of the GGL. Seed values must be exactly chosen to reach the maximal period of PRNG. But in our case the performance of the generator is the main aim, so all the seeds are selected randomly, because the generator exhausted whole the period for very short time and it is not so important when and where the overlapping of the sequences will began.

The other LCGs could be easily realized on the given example of the PRNG by substituting the corresponding LCG parameters. GGL generator possesses very good performance, as it will be shown in the next section. Nevertheless, in spite of the PRNG performance, it would not be used for practical purposes due to very short period.

### 3.3 XOR128

Next PRNG implemented on ATI GPU is XOR128, a very fast generator with much better statistical properties and considerably longer period than GGL. The distinctive feature of this PRNG is the usage of the four-component 32-bit values to produce the sequence which exactly corresponds to bit-capacity of GPU memory.

The ATI IL source code of XOR128 is shown in Figure 3. The following variables are used

$$\begin{aligned} \text{XR\_L1} &= 11, & \text{XR\_R1} &= 19, \\ \text{XR\_R2} &= 8, & \text{XR\_m} &= 4294967295.0, \end{aligned}$$

XRSEED\_MASK specifies the PRNG instance, iXRMSEED\_START is the offset of the lag table in global buffer which is prepared by host program.



```

il_cs_2_0
...
call 10
...
call 11
// random number in r200
...
call 12
...
endmain

func 10 // XOR128 initialization
dcl_literal 1200, %XRSEED_MASK%, %XR_L1%, %XR_R1%, %XR_R2%
dcl_literal 1201, %XR_m%, 0, 0, 0
and r204.x, vaTid.x, 1200.x
mov r201.g[r204.x+%iXRSEED_START%]
ret_dyn
endfunc

func 11 // XOR128 generation
ishl r202,r201,1200.yyyy
ixor r202,r202,r201
ushr r203,r202,1200.www
ixor r203,r202,r203
ushr r201.x,r201.w,1200.z
ixor r201.x,r201.x,r201.w
ixor r201.x,r201.x,r203.x
ushr r201.y,r201.x,1200.z
ixor r201.y,r201.y,r201.x
ixor r201.y,r201.y,r203.y
ushr r201.z,r201.y,1200.z
ixor r201.z,r201.z,r201.y
ixor r201.z,r201.z,r203.z
ushr r201.w,r201.z,1200.z
ixor r201.w,r201.w,r201.z
ixor r201.w,r201.w,r203.w
utof r200,r201
div r200,r200,1201.xxxx
ret_dyn
endfunc

func 12 // XOR128 finalization
mov g[r204.x+%iXRSEED_START%],r201
ret_dyn
endfunc
end

```

Figure 3: Source code of XOR128 PRNG

The number of sequences produced by XOR128 corresponds to the number of threads. One thread generates four successive pseudo-random numbers from one sequence in every components of the general purpose register R200. Marsaglia’s algorithm [25] is slightly modified to parallelize sequence production into four sub-threads – four items of the lag table are composed in one four-component memory cell and are produced in one pass. Unfortunately, it is impossible to avoid recursion without making the algorithm more complicated. Therefore among the four-component operations in the source code there are single-slot operations which are partially parallelized further by the IL compiler.

Except the final integer-to-float conversion operations in the algorithm, there are only bit shift and exclusive-OR operations which are “computationally light” GPU operations in compare with integer operations. Along with few memory operations (one read and one written operations per run), it also increases the performance of PRNG on GPU.

The XOR128 generator has a period large enough to be used on GPU. For 2048-threads run and average performance about  $10^{10}$  samples per second it could be exhausted in about  $10^{17}$  years only. And only strong criticism of L’Ecuyer [26] does not to allow use XOR128 as standard PRNG on GPU.

Generator requires keeping four 32-bit integers per thread. In the present realization PRNG produces four sequential pseudo-random numbers per thread which allows reserving only one 4-component cell per thread in global memory. This 4-component seed is read and written only once per PRNG cycle. The size of the XOR128 lag table is the same to GGL, i.e. for 4096-thread run it takes the 64kB of the GPU memory.

### 3.4 RANECU

Another high-performed PRNG realized on ATI GPU is RANECU. This generator is recommended by CERN and used in some software packages, listed in the previous section. Relatively long period and quite good statistical properties make RANECU reasonably attractive generator for small tasks.

The scheme like in the case of GGL generator is implemented here: each thread produces the four independent sequences which are composed into the four components of the general purpose register R200. For RANECU run in 1024-threads and output  $5 \times 10^9$  pseudo-random numbers per second the RANECU period could be exhausted in about 31 hours. Despite this fact the generator is still acceptable for



```

il_cs_2_0
...
call 10
...
call 11
// random number in r200
...

call 12
...
endmain

func 10 // RanEcu initialization
dcl_literal l200, %RESEED_MASK%, %RESEEDP11%,
             %-RESEEDP11%, %-RESEEDP12%
dcl_literal l201, %RESEEDP13%, 0, %REICONS%, %RESEEDP21%
dcl_literal l202, %-RESEEDP21%, %-RESEEDP22%,
             %RESEEDP23%, %REICONS2%
dcl_literal l203, 1, %REICONS3%, %RETWOM31%, 0
and r201.x, vaTid.x, l200.x
mov r202.g[r201.x+%iIRESEED_START%]
mov r203.g[r201.x+%iIRESEED_START2%]
ret_dyn
endfunc

func 11 // RanEcu generation
udiv r204, r202, l200.yyyy
imad r205, r204, l200.zzzz, r202
imul r206, r204, l200.wwww
imad r205, r205, l201.xxxx, r206
ilt r207, r205, l201.yyyy
cmov_logical r207, r207, l201.zzzz, l201.yyyy
iadd r202, r205, r207
udiv r204, r203, l201.wwww
imad r205, r204, l202.xxxx, r203
imul r206, r204, l202.yyyy
imad r205, r205, l202.zzzz, r206
ilt r207, r205, l201.yyyy
cmov_logical r207, r207, l202.wwww, l201.yyyy
iadd r203, r205, r207
inegate r204, r203
iadd r205, r202, r204
ilt r207, r205, l203.xxxx
cmov_logical r207, r207, l203.yyyy, l201.yyyy
iadd r200, r205, r207
utof r200, r200
mul r200, r200, l203.zzzz
ret_dyn
endfunc

func 12 // RanEcu finalization
mov g[r201.x+%iIRESEED_START%], r202
mov g[r201.x+%iIRESEED_START2%], r203
ret_dyn
endfunc
end

```

Figure 4: Source code of RANECU PRNG

wide range of MC simulation tasks.

The ATI IL source code of the RANECU PRNG is presented in Figure 4. The following variables are used

RESEEDP11 = 53668,	-RESEEDP11 = -53668,
-RESEEDP12 = -12211,	RESEEDP13 = 40014,
RESEEDP21 = 52774,	-RESEEDP21 = -52774,
-RESEEDP22 = -3791,	RESEEDP23 = 40692,
REICONS = 2147483563,	REICONS2 = 2147483399,
REICONS3 = 2147483562,	RETWOM31 = 1.0/2147483648.0,

iIRESEED\_START and iIRESEED\_START2 are the offsets of two tables of seeds in global buffer, RESEED\_MASK specifies the PRNG instance. In fact, the RANECU lag table is divided into two tables for convenience here. These tables are prepared by the host program.

The generator requires keeping two integer seed-values per thread which are grouped into two lag subtables. So for 4096-thread run the size of the lag table is 128kB.

The generator kernel is made on integer arithmetic base which slightly brings down the generator performance while using GPUs. However, simplicity of the algorithm and small amount of the lag table elements completely compensate this “drawback”. On the base of the present code, one can easily construct another MRG by substitution of the corresponding parameters.

### 3.5 RANMAR

The next generator realized on ATI GPU is the 24-bit Marsaglia PRNG RANMAR. It was previously implemented on ATI GPU in [58] for Ising model and  $SU(2)$  gluodynamics simulations.

In contrast to previously presented PRNGs, RANMAR has a larger lag table which contains 97 elements. All these lag table items must be prepared before the first working pass of the generator. Of course, the lag table may be directly initialized by the user, but it is not convenient in practice. So, the RANMAR lag table is initialized by stand-alone procedure RMARIN, proposed by James [23]. In

```

il_cs_2_0
...
call 10
...
call 11
// random number in r200
...
call 12
...
endmain

func 10 // RanMar initialization
dcl_literal 1200, %RMSEED_MASK%, %RMSEED_START%, -1, 0
dcl_literal 1201, 0.0, 1.0, 0.0, 0.0
dcl_literal 1202, %RM_CD%, %RM_CM%, 0, 0
dcl_literal 1203, %RMSEED_ALL%, %RMSEED_ALL%,
                %RMSEED_97%, %RMSEED_97-1%
iand r201.x, vaTid.x, 1200.x
umad r202.xy, r201.xx, 1203.xy, 1200.yy
iadd r203.xy, r202.xy, 1203.zw
mov r204.xy, g[r203.x].xy
mov r205, g[r203.x+1]
iadd r206.xy, r202.xy, r204.xy
ret_dyn
endfunc

func 11 // RanMar generation
sub r207, g[r206.x], g[r206.y]
lt r208, r207, 1201.xxxx
cmov_logical r210, r208, 1201.yyyy, 1201.xxxx
add r207, r207, r210
mov g[r206.x], r207
iadd r206.xy, r206.xy, 1200.zz
ilt r211.xy, r206.xy, r202.xy
cmov r206.xy, r211.xy, r203.yy
sub r205, r205, 1202.xxxx
lt r212, r205, 1201.xxxx
cmov_logical r209, r212, 1202.yyyy, 1200.wwww
add r205, r205, r209
sub r207, r207, r205
lt r209, r207, 1201.xxxx
cmov_logical r209, r209, 1201.yyyy, 1200.wwww
add r207, r207, r209
mov r200, r207
ret_dyn
endfunc

func 12 // RanMar finalization
iadd g[r203.x].xy, r206.xy, r202.xy_neg(xy)
mov g[r203.x+1], r205
ret_dyn
endfunc
end

```

Figure 5: Source code of RANMAR PRNG

this procedure, the whole lag table is initialized on the base of only two given 5-digit integers, each set of which causes an independent sequence of the sufficient length for an entire calculation. The seed variables can have values between 0 and 31328 for the first variable and 0 and 30081 for the second variable, respectively. RANMAR can create, therefore, 900 million independent subsequences for different initial seeds with each subsequence having a length of about  $10^{30}$  pseudo-random numbers. This approach considerably reduces the number of the possible generator states. Still it brings an important element of the generator features – easy division of sequences produced by generator among PRNG instances without overlapping. Possible sequences quantity (900 millions) at existing or developing hardware is considered to be sufficient even in medium-term perspective.

The generator consists of two parts:

- kernel which produces the seed numbers on initial seed values; in fact this kernel is a replica of the RMARIN subroutine of the James’ version [23];
- subroutines which directly produce the random numbers.

First part is executing only for initialization.

The floating-point version of the RANMAR generator is realized here which produces the pseudo-random directly in the interval  $[0; 1)$ . So, it is not needed to use slowest integer-to-floating point converting operation.

Apart from 97 elements in the lag table each RANMAR instance must store previous value of arithmetic sequence and two indices which are connected to each other. As in the case of GGL PRNG, every GPU thread produces four independent sequences in the presented implementation of RANMAR. Obviously at such approach, it is necessary to keep only one pair of indices for all four subthreads, because these subthreads are executed out synchronously. So, it requires 2.5 memory cells be read and written for one PRNG pass. The size of RANMAR lag table for 4096-thread run is about 6MB. Initially lag table is prepared by stand-alone procedure RMARIN which is not shown here.

The ATI IL source code of RANMAR PRNG is presented in Figure 5. The following variables are used

$$\begin{aligned}
 \text{RM\_CD} &= 7654321.0/16777216.0, & \text{RM\_CM} &= 16777213.0/16777216.0, \\
 \text{RMSEED\_97} &= 97, & \text{RMSEED\_97} - 1 &= 96, \\
 \text{RMSEED\_ALL} &= 99,
 \end{aligned}$$

RMSEED\_START is the offset of the lag table in global buffer, RMSEED\_MASK specifies the PRNG instance.

### 3.6 RANLUX

Nowadays RANLUX PRNG is one of the standard high-performed generators for Monte-Carlo simulations. The statistical properties of the generator are well-known. From the realization point of view, distinctive feature of the generator is the necessity to discard out groups of generated pseudo-random numbers after one generation cycle. Omitted values quantity is determined by the “luxury” parameter. While implementation of the algorithm on the central processing unit such discarding is “virtual”, because lag table fits in processor cache very well, as a rule. Still this algorithm phase is very resource-intensive on GPU, because global buffer is not a generally cached object. Thus it is obvious, that the PRNG performance is strongly depend on this phase of algorithm realization.

To implement the RANLUX generator, we use three quite different approaches. First of all, the direct translation of algorithm is performed. In this scheme all the seed values are updated directly in GPU global memory. Every thread in point of fact generates simultaneously the four independent sequences of the pseudo-random numbers. Luxury is performed for all four subthreads at the same time. This approach makes the algorithm considerably simpler, but does not allow getting the best performance.

Next evident approach is to use the indexed temporary array for luxury operation. It allows to make process execution much faster: at luxury level=3 3.5 times faster and 5 times faster at luxury level=4, keeping the complexity of the algorithm meanwhile.

Third approach which really allows to make algorithm faster and in practice minimize the dependence of the execution time on luxury level, is the “planar” scheme. The geometry of the lag table is taken into account as much as possible in this scheme. For RANLUX it consists of the 24 elements which naturally could be grouped into six 4-component 32-bit registers. The new difficulty to vectorize the RANLUX algorithm is arisen due to the necessity of the recursive calculation of the carry bit  $c_n$  which depends on the preceding states of the generator. Therefore, some serial operations are appeared in planar RANLUX code as well as in presented here XOR128 implementation. Planar RANLUX procedure produces four pseudo-random numbers from one sequence for one pass of the generator.

Base algorithm RANLUX requires discarding 24, 73, 199 and 365 values after one RANLUX cycle for luxury level 1, 2, 3 and 4, respectively. However to perform luxury in the planar implementation of the RANLUX, it is convenient to discard some larger number than ones, proposed by Lüscher [30]. Strictly speaking, it is convenient to discard the number of the values which are multiply by 24. In CPU implementation such approach seems to be redundant (see [30]), but on GPU it shows better performance. Thus, in planar scheme the following numbers are discarded: 24, 96, 216 and 384 (for luxury levels 1, 2, 3 and 4, respectively).

The ATI IL source code of planar RANLUX PRNG is presented in Figure 6. The following variables are used

$$\begin{aligned} \text{RLSEED\_ALL\_4} &= 7, & \text{RLTWOM24} &= 2^{-24}, \\ \text{RLSEED\_24\_4} &= 24/4 = 6, & \text{RLSEED\_24\_4} - 1 &= 5, \end{aligned}$$

RLSEED\_START is the offset of the lag table in global buffer, RLNSKIP is the number of generated values to be discarded (is defined by the luxury level), RLSEED\_MASK specifies the PRNG instance.

Due to relatively large lag table, RANLUX as well as RANMAR generator requires the stand-alone initializing procedure. This procedure is running only once and does

```

il_cs_2_0
...
call 10
...
call 11
// random number in r200
...

call 12
...
endmain

func 10 // RanLux initialization
dcl_literal l200, %RLSEED_MASK%, %RLSEED_ALL_4%,
               %RLSEED_START%, -24
dcl_literal l201, %RLNSKIP%, %RLTWOM24%, %RLSEED_24_4%,
               %RLSEED_24_4-1%
dcl_literal l202, 19, 5, 20, 2
dcl_literal l203, 3, 1, -1, -4
dcl_literal l204, 0.0, 1.0, 0, 0
and r201.x,vaTid.x,l200.x
umadd r201.x,r201.x,l200.y,l200.z
iadd r202.xy,r201.xx,l201.zw
fence_memory
mov r203,g[r202.x]
ushr r204.xyz,r203.xyz,l202.ww0
iadd r205.xyz,r201.xx0,r204.xyz
mov r206,g[r205.y]
ret_dyn
endfunc

func 11 // RanLux generation
if_logicalz r205.z
mov r207.x,l201.x
if_logicalnz r207.x
mov r208,g[r201.x ]
mov r209,g[r201.x+1]
mov r210,r206
mov r211,g[r201.x+3]
mov r212,g[r201.x+4]
mov r213,g[r201.x+5]
whileloop
ilt r207._y,l204.z,r207.x
break_logicalz r207.y
mov r214,r213
mov r215,r209
call 13
mov r213.xyzw,r216.wzyx
mov r214,r212
mov r215,r208
call 13
mov r212.xyzw,r216.wzyx
mov r214,r211
mov r215,r213
call 13
mov r211.xyzw,r216.wzyx
mov r214,r210
mov r215,r212
call 13
mov r210.xyzw,r216.wzyx
mov r214,r209
mov r215,r211
call 13
mov r209.xyzw,r216.wzyx
mov r214,r208
mov r215,r210
call 13
mov r208.xyzw,r216.wzyx
iadd r207.x,r207.x,l200.w
endloop
mov r206,r210
mov r214,r213
mov r215,r209
call 13

mov r213.xyzw,r216.wzyx
mov r200,r216
mov r203.xyz,l202.xyz
ushr r204.xyz,r203.xyz,l202.ww0
iadd r205.xyz,r201.xx0,r204.xyz
mov g[r201.x ],r208
mov g[r201.x+1],r209
mov g[r201.x+2],r210
mov g[r201.x+3],r211
mov g[r201.x+4],r212
mov g[r201.x+5],r213
else
mov r214,g[r205.x]
iadd r217.xyz,r205.xyz,l203.zzw
ige r218.xy,r217.xy,r201.xx
cmov_logical r217.xy,r218.xy,r217.xy,r202.yy
mov r215,g[r217.y]
call 13
mov g[r205.x].xyzw,r216.wzyx
mov r205,r217
endif
else
mov r214,g[r205.x]
iadd r217.xyz,r205.xyz,l203.zzw
ige r218.xy,r217.xy,r201.xx
cmov_logical r217.xy,r218.xy,r217.xy,r202.yy
mov r215,g[r217.y]
call 13
mov g[r205.x].xyzw,r216.wzyx
mov r205,r217
endif
mov r200,r216
ret_dyn
endfunc

func 12 // RanLux finalization
fence_memory
iadd r203.xyz,r205.xyz,r201.xx0_neg(xy)
ishl r203.xyz,r203.xyz,l202.ww0
iadd r203.xy,r203.xy,l203.xy
mov g[r201.x+6],r203
ret_dyn
endfunc

func 13 // RanLux update
sub r216.xy,r206.yx,r214.wz
sub r216.x,r216.x,r203.w
lt r219.x,r216.x,l204.x
cmov_logical r220.x,r219.x,l204.y,l204.x
add r216.x,r216.x,r220.x
cmov_logical r203.__w,r219.x,l201.y,l204.x
sub r216._y,r216.y,r203.w
lt r219.x,r216.y,l204.x
cmov_logical r220.x,r219.x,l204.y,l204.x
add r216._y,r216.y,r220.x
cmov_logical r203.__w,r219.x,l201.y,l204.x
sub r221.xy,r215.wz,r214.yx
sub r221.x,r221.x,r203.w
lt r219.x,r221.x,l204.x
cmov_logical r220.x,r219.x,l204.y,l204.x
add r221.x,r221.x,r220.x
cmov_logical r203.__w,r219.x,l201.y,l204.x
sub r221._y,r221.y,r203.w
lt r219.x,r221.y,l204.x
cmov_logical r220.x,r219.x,l204.y,l204.x
add r221._y,r221.y,r220.x
cmov_logical r203.__w,r219.x,l201.y,l204.x
mov r216.__z,r221.x
mov r216.__w,r221.y
mov r206,r215
ret_dyn
endfunc
end

```

Figure 6: Source code of RANLUX PRNG

not take much resources, so its listing is not presented here. Also, it may be realized in the host program with further copying the result to the GPU global buffer.

Generator RANLUX, as well as RANMAR PRNG, possesses the important feature in the context of the GPU realization – the generator kernel is build on floating-point arithmetic. Each instance of the planar version of the RANLUX requires storing seven 4-component cells only (three indices which are connected to each other, 24 items of lag table and carry bit). So for 4096-thread run the size of the lag table is 448kB (or 1664kB for the case of the global buffer and temporary indexed array RANLUX versions).

### 3.7 Mersenne Twister

The last PRNG which is implemented in this work is MT19937, one of the Mersenne Twister generators family. This generator seems to be very attractive nowadays due to its extremely long period and relatively easy algorithm.

Mersenne Twister is incorporated in nVidia SDK as sample. The realized in nVidia SDK version of the Mersenne Twister contains 19 element lag table and period about  $2^{607}$ . It is easy to implement the MT19937 generator on the basis of this example by substituting the relevant parameters.

In the presented realization of MT19937 we use the same scheme as in the planar implementation of RANLUX. Whole 624-element lag table is located into 156 four-component cells. So, for the one pass of the PRNG it is easy to obtain four sequential pseudo-random numbers. But unfortunately, it is impossible to store whole lag table in the general-purpose registers to perform the lag table updating procedure, because the total number of the general-purpose registers allocated for one thread is 128. Thus, all operations with the lag table are realized with the slow direct access to the global buffer, what greatly reduces the total performance of the generator. Nevertheless, the using of the four-component elements somewhat compensates this disadvantage.

The ATI IL source code of MT19937 PRNG is presented in Figure 7. The following variables are used

```

MTSEED_624_4 = 156,    MTSEED_ALL = 157,
MTSEEDP2 = 9D2C568016, MTSEEDP3 = EFC6000016,
MTSEEDP4 = 0.5,        MTSEEDP5 = 4294967296.0,
MT_UPPER_MASK = 8000000016, MT_LOWER_MASK = 7FFFFFFF16,
MT_MATRIX_A = 9908B0DF16,
```

MTSEED\_START is the offset of the lag table in global buffer, MTSEED\_MASK specifies the PRNG instance.

The lag table of the MT19937 is the biggest one among the lag tables of the presented generators. For 4096-thread run its size is about 10MB. MT19937 also requires the initialization procedure which prepares the lag table for the first run.

## 4 Performance results and discussion

For all PRNGs implemented here we use the MS Visual Studio 2008 Express edition (C++ compiler) [63]. Original codes are presented in corresponding literature (see Section A) and in several cases they are translated into C++.

The CPU implementation of the PRNGs is constructed on the following common scheme: each PRNG is implemented as subroutine which produces only one pseudo-random number per call. Then the main program sums up all produced values and checks the elapsed time. The  $10^8$  pseudo-random numbers are used for this

```

il_cs_2_0
...
call 10
...
call 11
// random number in r200
...

call 12
...
endmain

func 10 // MT19937 initialization
dcl_literal 1200, %MTSEED_MASK%, 1, %MTSEED_624_4%, 0
dcl_literal 1201, %MTSEED_ALL%, %MTSEED_START%, 155, 56
dcl_literal 1202, 11, 7, 15, 18
dcl_literal 1203, %MTSEEDP2%, %MTSEEDP3%, %MTSEEDP4%,
                    %MTSEEDP5%
dcl_literal 1204, 0, 1, 99, 100
dcl_literal 1205, 56, 57, -1, 0
dcl_literal 1206, 0, 155, 98, 99
dcl_literal 1207, 0, %MT_UPPER_MASK%, %MT_LOWER_MASK%,
                    %MT_MATRIX_A%
and r201.x, vaTid.x, 1200.x
umad r201.xy, r201.xx, 1201.xx, 1201.yy
mov r202.x, g[r201.x+%MTSEED_624_4%].x
ret_dyn
endfunc

func 11 // MT19937 generation
ult r202.y, r202.x, 1200.z
call_logicalz r202.y, 13
call 14
ret_dyn
endfunc

func 12 // MT19937 finalization
iadd g[r201.x+%MTSEED_624_4%].x, r202.x, 1200.y
ret_dyn
endfunc

func 13 // MT19937 update seeds
fence_memory
iadd r203, r201.xxxx, 1204
iadd r204.xy, r201.xx, 1201.zw
mov r206, g[r203.x]
mov r208, g[r203.z]
whileloop
mov r205, r206
mov r206, g[r203.y]
mov r207, r208
mov r208, g[r203.w]
mov r210.xyz, r207.yzw
mov r210.__w, r208.x
iand r211, r205, 1207.yyyy
iand r212.xyz, r205.yzw, 1207.zzz
iand r212.__w, r206.x, 1207.z
ior r213, r211, r212
iand r214, r213, 1200.yyyy
ushr r209, r213, 1200.yyyy
cmov_logical r214, r214, 1207.www, 1200.www
ixor r209, r210, r209
ixor r209, r209, r214
mov g[r203.x], r209
iadd r203, r203, 1200.yyyy
uge r211.y, r203.x, r204.y
break_logicalnz r211.y
endloop

fence_memory
iadd r203, r201.xxxx, 1205
whileloop
mov r205, r206
mov r206, g[r203.y]
mov r207, r208
mov r208, g[r203.w]
mov r210.xyz, r207.yzw
mov r210.__w, g[r203.w].x
iand r211, r205, 1207.yyyy
iand r212.xyz, r205.yzw, 1207.zzz
iand r212.__w, r206.x, 1207.z
ior r213, r211, r212
iand r214, r213, 1200.yyyy
ushr r209, r213, 1200.yyyy
cmov_logical r214, r214, 1207.www, 1200.www
ixor r209, r210, r209
ixor r209, r209, r214
mov g[r203.y], r209
mov r202.x, 1200.w
ret_dyn
endfunc

func 14 // MT19937 generate rnd()
iadd r201.y, r201.x, r202.x
fence_memory
mov r200, g[r201.y]
ushr r215, r200, 1202.xxxx
ixor r200, r200, r215
ishl r215, r200, 1202.yyyy
iand r215, r215, 1203.xxxx
ixor r200, r200, r215
ishl r215, r200, 1202.zzzz
iand r215, r215, 1203.yyyy
ixor r200, r200, r215
ushr r215, r200, 1202.www
ixor r200, r200, r215
utof r200, r200
add r200, r200, 1203.zzzz
div r200, r200, 1203.www
ret_dyn
endfunc
end

```

Figure 7: Source code of MT19937 PRNG

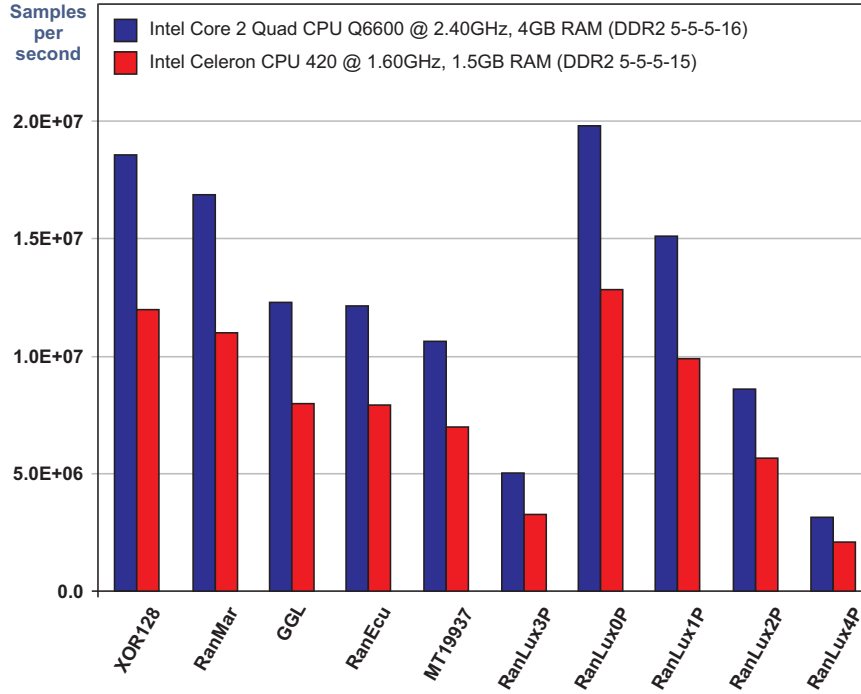


Figure 8: Performance results for some PRNGs on two PCs

procedure. Elapsed time is averaged over several single thread executions and the mean CPU performance is found. For the reference PCs we use two machines:

- Intel Core 2 Quad CPU Q6600 @ 2.40GHz (L1 cache 4×32KB, L2 cache 2×4MB), 4GB RAM DDR2 400MHz Dual Symmetric (5-5-5-16) Command rate 2T;
- Intel Celeron CPU 420 @ 1.60GHz (L1 cache 32KB, L2 cache 512KB), 1.5GB RAM DDR2 333MHz Dual (5-5-5-15) Command rate 1T,

which correspond to the middle-level and entry-level computers, respectively.

The CPU performance results are presented in Figure 8 and Table 2. It could be seen that the differences among the performances of the generators are about 5-6 times. XOR128 and RANMAR show the best performance results. Under CPU performance here and after we mean the performance of the one-thread instance of the algorithm. Of course, one-thread run does not provide maximal system utilization, however it allows comparing the potential performances of the systems. To show impartial assessment we can just multiply CPU performance by the quantity of the threads, supported up by peculiar processor, because it is always possible to run several PRNG instances to produce different independent pseudo-random sequences.

All the PRNGs implementations on GPU are carried out in ATI Intermediate Language [59] (ATI Catalyst 10.1 display driver is used [62]). The host environment is also realized in MS Visual Studio 2008 C++ [63]. All used here GPUs are the main GPU devices installed in the system (i.e. they also provide visualization for the operational system) which lowers down the maximal performance of the system, but reflects more precisely the usual configuration of the GPU computational system. To obtain the performance of each PRNG, we run them up to 1000 times each to produce  $4 \times 10^7$  pseudo-random samples on every pass. Each produced pseudo-random number is stored in global buffer. Elapsed time is averaged over several



Table 2: The performance results of the presented here PRNG implementations on different ATI GPUs (here **CPU** is Intel Core 2 Quad CPU Q6600 at 2.40GHz and **CPU<sub>2</sub>** is Intel Celeron CPU 420 at 1.60GHz)

PRNG	$\times 10^9$ per second			$\times 10^7$ per second		Speed-up factor
	5850	4870	4850	CPU	CPU <sub>2</sub>	
GGL	8.37	5.05	4.21	1.23	0.80	681
XOR128	8.45	6.29	4.52	1.86	1.20	455
RANECU	4.98	3.32	2.66	1.21	0.79	411
RANLUX3P	1.08	1.02	0.63	0.50	0.33	216
RANLUX4P	1.02	0.86	0.58	0.32	0.21	322
MT19937	0.50	0.62	0.36	1.07	0.69	47
RANMAR	0.18	0.23	0.14	1.69	1.10	11

executions. The time spending to copy the initial input seeds to GPU memory and final mapping the GPU memory into host memory is not taken into account.

The performance results are collected in Figure 9 and Table 2. The first column of the Table 2 contains the name of the implemented generator. The number pseudo-random numbers which could be produced by corresponding PRNG per one second on corresponding GPU are show in the columns 2-4. Here HD5850, HD4870 and HD4850 are the ATI Radeon video cards. The next two columns contain the same information obtained on two mentioned CPUs. The last column shows the speed-up factor of the using the ATI Radeon HD5850 in compare with the using of the Intel Core 2 Quad CPU Q6600 at 2.40GHz.

Memory access is a bottleneck of the GPU-applications. It is confirmed once again by different PRNG performance results on different ATI GPU hardware. The PRNGs with the greater number of the memory operations demonstrate the worst performance results.

In the present realizations GGL and XOR128 generators require to keep only one 4-component seed-value per thread. This directly influences their work – both generators showed the best productivity. Despite the generator XOR128 in the present code has sequential part which slightly lowers the speed of the generator operation its performance turned out to be the highest. It may be explained by the fact that only bit operations are used in the arithmetic kernel of the XOR128 generator which along with floating-point operations are the fastest implemented on ATI hardware. Generator GGL is realized on the base of the integer scheme of Park and Miller [12] which slightly brings down its output in compare with XOR128, in spite of less quantity of the intermediate operations.

The RANECU generator already requires keeping two seed-values for its operation. Along with using integer arithmetical operations in RANECU kernel it somewhat lowers its performance in compare with GGL and XOR128 generators. The algorithm simplicity, the performance up to  $5 \times 10^9$  samples per second and the considerably better statistical properties allow extensively using RANECU generator on GPU. In order to increase the RANECU period it is reasonable to employ the MRG based on the combinations not two but three MLCGs. However this extension requires the additional study of the new generator statistical properties. It may be a subject of the further research in this field.

The RANLUX generator shows considerably high performance on GPU. To a significant degree it may be explained by fortunate matching of GPU architecture and the generator parameters. It is managed to minimize generator dependence

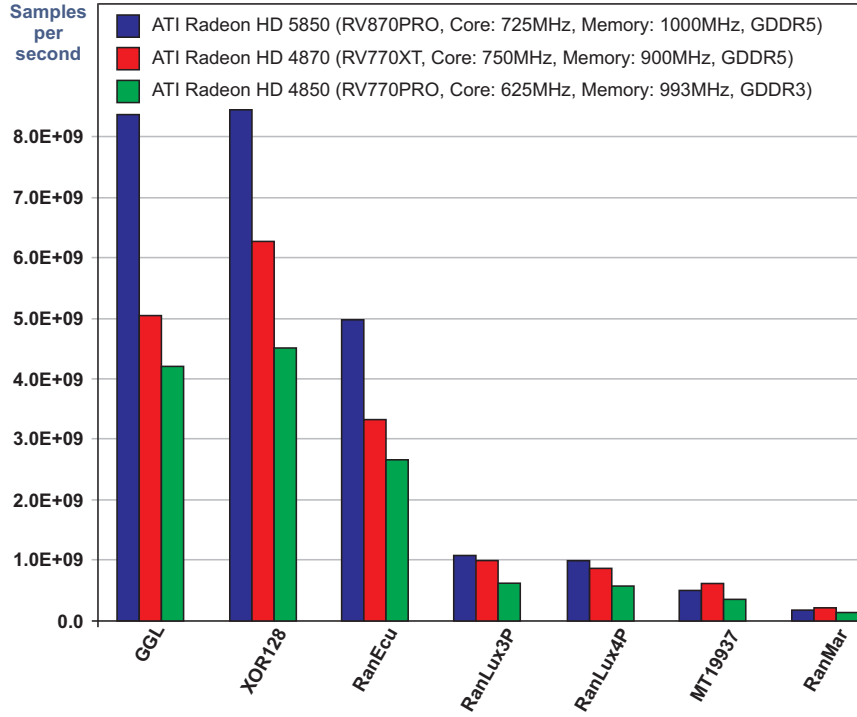


Figure 9: Performance results for some PRNGs on different GPUs

on decorrelating luxury procedure by the actual organization of the virtual cache. Thereby it is possible to use maximal luxury level with the minimal performance penalty in practical applications. In the opposition to CPU realization where the difference between the performances at luxury level=0 and luxury level=4 reaches 6 and more times, on GPU this parameter is only 10-23% (for different hardware).

It is obviously that performance advantage also depends on the way of algorithm realization. In order to demonstrate this fact, we showed in Table 3 the performance values of different realization of the same algorithm for RANLUX generator for a number of GPUs. RANLUX implementation through the global buffer is the slowest one. In fact the present realization of algorithm entirely reproduces the dependence of the GPU realization on luxury level. Acceleration in compare with CPU is achieved only because of such GPU parameters as number of stream cores and engine clock rate. An unexpected result was the fact that realization of for global buffer realization of RANLUX HD4870 GPU shows better performance than HD5850. It is closely related to the fact that memory data access in the kernel is organized not in the best way and a lot of time is spent to synchronize memory access operations. Obtaining better performance is possible by lowering the instructions density which refer to the global buffer.

Second RANLUX realization, through the indexed temporary array, is a bit faster than the first one. But the same situation with HD4870 and HD5850 GPUs performances can be observed here as well. The present realization has sense only for luxury levels 2-4, when time share, which is spent on indexed temporary array preparation, is compensated by luxury operation saving time itself. The main strong feature of this implementation is the complete correspondence to the classic algorithm, published in [31].

The last presented implementation of RANLUX (which is called planar here) possesses the best performance due to maximal reduction of memory access opera-

Table 3: Performance results of the different implementations of RANLUX generator on some ATI GPUs (ATI Radeon HD5850, HD4870, HD4850),  $\times 10^8$  pseudo random numbers per second

luxury level	Planar			Temporary array			Global buffer		
	5850	4870	4850	5850	4870	4850	5850	4870	4850
0	11,35	10,64	6,54	4,07	5,56	3,35	5,02	6,92	4,32
1	11,00	10,14	6,19	4,05	5,39	3,33	3,50	4,66	2,71
2	11,01	10,17	6,20	4,02	5,00	3,23	2,18	2,61	1,55
3	10,85	10,17	6,27	3,85	4,18	2,83	1,11	1,20	0,72
4	10,24	8,62	5,77	3,51	3,44	2,42	0,68	0,71	0,43

tions quantity. General advantage of performance on GPU in compare with CPU is up to 322 times (highest luxury level = 4). The modified algorithm is used here (see section 3.6) at which a bit higher quantity of pseudo-random numbers after one PRNG cycle are discarded away for decorrelation of lag table elements, than it is set up in the classic algorithm.

In the first two RANLUX realizations of the algorithm, it requires to read four memory cells (not accounting for the luxury procedure operations) and write three cells (two lag table items, carry bit and indices) to obtain one pseudo-random number (updated lag table item, new carry bit and new indices). In planar scheme the carry bit occupies one of the four-component cells with the indices, so it needs less quantity of reading and writing operations (four read and two writes).

The performance of the shown code of the MT19937 generator is turned out to be rather low. The main factor is the size of the lag table, the update of which is required after each PRNG cycle. Planar scheme applied here allows increasing the generator performance roughly in four times in compare with the direct four-threads realization, but the quantity of the memory access operations remains rather high which does not allow to achieve acceptable results. It is possible to reduce the lag table size by choosing another generator from the Mersenne Twister family. But from one hand, MT19937 generator parameters allow to realize the planar scheme (proved to be a good here), and from another hand there is a task to build the analogue of the actually used generators on GPU while algorithms realization. Although to generate one pseudo-random number it is needed only two read operations and one write only, the lag table update procedure drastically decelerates the generator.

The worst performance is shown by RANMAR generator which differs by the large enough lag table and high memory access operation density (four reads and three writes).

All presented generators realizations allow to produce at slight changes pseudo-random numbers with double precision either by using the pairs of the generated numbers or directly through the double precision conversion. The last method is not fully correct, because it considerable lowers the quantity of the possible realization of the obtained double precision number.

Paying attention to the XOR128 performance one can asserts that L'Ecuyer generator Seven-XORShift [26] is seemed to be very promising for realization on GPU due to the similarity to the XOR128 structure except for the eight-element lag table.

The periods of the XOR128, RANLUX, RANMAR and MT19937 generators are considered to be unachievable in medium-term perspective even for GPU clusters. Meanwhile the period of the GGL generator can be exhausted in a split second even on one relatively old GPU. So, it is necessary to pay special attention to the

generator applicability borders while developing applications on GPU.

Undoubtedly the presented algorithms realization on the platform independent level such as OpenCL will be very important, but it goes beyond the present work frame and is a task for future research. The obtained results of the generators performances make it interesting to use the GPU for the investigation of the generators statistical properties.

## 5 Conclusions

In the present paper the most popular uniform pseudo-number generators which are used in Monte Carlo simulations in high-energy physics are realized on GPU. The list of the modern software packages with the indication of the generators used is represented. A theoretical background for pseudo-random number generation is described. The source codes of the implemented generators (multiplicative linear congruential (GGL), XOR-shift (XOR128), RANECU, RANMAR, RANLUX and Mersenne Twister (MT19937)) are shown<sup>1</sup>.

The comparative analysis of the PRNG performances on CPU and ATI GPU is presented. The obtained speed-up factor is hundreds of times higher as compare to CPU. Performance analysis of the mentioned generators with taking into account their statistical properties allows to conclude that the most appropriate generator for Monte Carlo simulations on GPU is planar RANLUX with luxury level 4. Offered planar scheme makes it possible to increase significantly the performance of the most generators by the reducing memory access operations.

Offered PRNG program model (generator division into separate subroutines) also allows to obtain additional considerable gain of performance at the multiple calls of the PRNG generating subprogram. This is achieved by means of a substantial reduction in the number of the memory access operations per PRNG cycle.

In the present paper the generator performances in different realizations are analyzed by way of RANLUX PRNG example. It is shown once again that the memory access operations are the bottleneck of GPUs. It is possible to conclude that for GPU implementations of PRNGs it is better to choose algorithms with the minimal lag table size (which to be advisable multiply by 4) perhaps in spite of some complication of algorithms.

Potential of GPU implementation in Monte Carlo simulations is not fully realized nowadays. This is despite of large amount of works dedicated to this problem. GPU sector development dynamics makes it possible to predicate that this trend is one of the most promising nowadays.

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<sup>1</sup> When the present paper was prepared for publication, a new version of ATI Stream SDK v.2.01 has been released which includes the Park-Miller generator with Bays-Durham shuffle and the Mersenne Twister generator

## A Basic classes of PRNGs

In this section we briefly provide the theoretical background for the main classes of the pseudo-random number generators. There are numerous books and reviews about the subject, so the details could be found in the references.

While pseudo-random numbers generation, there are only two internal sources of the randomness which could be used in the algorithm. They are the sequence itself (previous values in a sequence precisely) and the starting parameters (PRNG parameters and seed values). Actually, the algorithms of the PRNGs are distinguished by the way of the using these sources. So, particular PRNG is a certain function  $f$  which produces the next value  $X_n$ ,

$$X_n^{\text{PRNG}} = f(X_{n-1}, X_{n-2}, \dots, X_{n-r}). \quad (2)$$

Here and below we will use upper index PRNG to identify the sequence produced by particular generator PRNG. The maximum period of the generator is the length of the cyclic sequences produced by PRNG and is limited by the number of the states that can be represented by PRNG.

First simple PRNGs uses only one previous value  $X_{n-1}$  ( $r = 1$ ) for generation, but in such scheme the PRNG period is limited by the bit capacity of the machine. If one uses the longer tables of the sequence of the previous values, from one hand it makes the generator period longer and its statistics properties better, as well as allows to simplify transformation function  $f$  for getting better output of the generator. From the other hand, longer tables require more complicated generator initialization and reduce its portability (the strict control of the architecture is needed, for example, the size of the cache memory), and it is obviously necessary to have much more memory to store such tables. A good generator is always a golden middle between algorithm complexity, the statistical properties of the generator and the size of the seed table.

According to the basic requirement for PRNG – repeatability, any starting state of the generator may cause only one specified sequence. The initialization of the seed table is often made by simpler generator which has lower requirements. Most of all linear congruential generators or their combination is used for initialization. So, it allows to set starting generator states by the limited set of the input seed values (often 1-2 numbers). But Marsaglia [3] drew our attention to the fact that the quantity of the starting states decreases drastically. For example, Mersenne Twister generator MT19937 uses 624-element seed table (which may contain about  $(2^{32})^{624} \simeq 10^{6011}$  different values) whenever 32-bit number is usually used for its initialization, for which only  $(2^{32}) \simeq 4 \times 10^9$  possible values are given. Certainly, algorithm contains the possibility of the vector initialization. Nevertheless, only one seed is used to simplify the initialization.

The period of PRNG nearly always depends on its parameters and seed values. Thus, we always show only the upper bound for the value of the generator period.

### A.1 Linear congruential generators

Linear congruential generators (*LCG*) is one of the oldest and most popular class of the PRNGs, which is widely used in computations in particular due to the encyclopedic work of Knuth [11]. It is based on so-called linear congruential integer recursion,

$$X_n^{\text{LCG}} = (aX_{n-1} + c) \bmod m, \quad (3)$$

where increment  $c$  and modulus  $m$  are desired to be positive coprime integers ( $c < m$ ) to provide a maximum period, multiplier  $a$  is an integer in the range  $[2; (m-1)]$ .

If increment  $c = 0$  the LCG is often called the multiplicative linear congruential generator (*MLCG*),

$$X_n^{\text{MLCG}} = aX_{n-1} \bmod m. \quad (4)$$

The maximum period of LCG  $P_{\text{LCG}}$  strongly depends on LCG parameters and

$$P_{\text{LCG}} \leq (m - 1). \quad (5)$$

Demonstrative situation with poor choice of LCG parameters happened with infamous generator **RANDU** -  $\text{MLCG}(a = 2^{16} + 3, m = 2^{31})$ ,

$$X_n^{\text{RANDU}} = 65539X_{n-1} \bmod 2147483648, \quad (6)$$

which suffers from three-point correlations among the sequential elements:

$$X_n^{\text{RANDU}} = 6X_{n-1} - 9X_{n-2}. \quad (7)$$

Another well-known LCG is the standard 48-bit generator **DRAND48**, which is a  $\text{LCG}(a = 25214903917, c = 11, m = 2^{48})$

$$X_n^{\text{DRAND48}} = (25214903917X_{n-1} + 11) \bmod 2^{48}. \quad (8)$$

Park and Miller propose [12] a portable minimal standard Lehmer generator<sup>2</sup> [13] known as prime modulus multiplicative linear congruential generator (**PMMLCG**). Sometimes it is also denoted by the acronyms **RAN0**, **CONG**, **SURAND** or **GGL**. Park and Miller choose the Mersenne prime number  $2^{31} - 1$  as the modulus  $m$ , multiplier  $a = 7^5$  and increment  $c = 0$ ,

$$X_n^{\text{GGL}} = 16807X_{n-1} \bmod 2147483647. \quad (9)$$

The total period of the GGL is relatively short,  $P_{\text{GGL}} = (2^{31} - 1) - 1 = 2147483646$ .

One of the main well-known problems of the LCG is that every LCG produces  $n$ -tuples of uniform variates which lie in at most parallel hyperplanes [14, 15]. The other defects of the LCG are:

- the dependence of the generator period on initial seed;
- the influence of the chosen modulus on statistical properties of the pseudo-random sequence;
- lowest bits are not random.

And finally, the minimal integer value produced by MLCG is 1, not 0.

## A.2 Feedback shift register generators

In 1965 Tausworthe [18] introduced a new generator based on bit sequence

$$X_n^{\text{LFSR}} = \left( \sum_{i=1}^r a_i X_{n-i} \right) \bmod 2, \quad (10)$$

where  $a_i = \{0, 1\}$ ,  $X_i = \{0, 1\}$ ,  $r \leq n$ , is called linear feedback shift register algorithm (*LFSR*).

The period of the LFSR is the smallest positive integer  $P$  for which

$$(X_{r-1}, \dots, X_0) = (X_{P+r-1}, \dots, X_P). \quad (11)$$

---

<sup>2</sup>The original parameters of Lehmer generator are  $a = 23$ ,  $m = 10^8 + 1$

The next state could be obtained with the following transformation

$$\begin{pmatrix} X_n \\ X_{n-1} \\ \vdots \\ X_{n-r+1} \end{pmatrix} = \begin{pmatrix} a_1 & \cdots & a_{r-1} & a_r \\ 1 & \cdots & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots \\ 0 & \cdots & 1 & 0 \end{pmatrix} \begin{pmatrix} X_{n-1} \\ X_{n-2} \\ \vdots \\ X_{n-r} \end{pmatrix} \quad (12)$$

or equivalently for initial state it is

$$\begin{pmatrix} X_n \\ X_{n-1} \\ \vdots \\ X_{n-r+1} \end{pmatrix} = \begin{pmatrix} a_1 & \cdots & a_{r-1} & a_r \\ 1 & \cdots & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots \\ 0 & \cdots & 1 & 0 \end{pmatrix}^{n-r+1} \begin{pmatrix} X_{r-1} \\ X_{r-2} \\ \vdots \\ X_0 \end{pmatrix}. \quad (13)$$

The characteristic polynomial of  $r \times r$  transformation matrix  $A$

$$A = \begin{pmatrix} a_1 & \cdots & a_{r-1} & a_r \\ 1 & \cdots & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots \\ 0 & \cdots & 1 & 0 \end{pmatrix} \quad (14)$$

is

$$a(x) = \det(A - xI) = x^r - \sum_{i=1}^r a_i x^{r-i}, \quad a_r = 1, \quad (15)$$

where  $I$  is an identity matrix.

According to the theory of the finite fields [19] the maximal period  $P_{\text{FSRG}} = 2^r - 1$  is achieved if and only if the characteristic polynomial  $a(x)$  is an irreducible polynomial over Galois field  $GF(2)$ . In other words, if and only if the smallest positive integer  $p$ :  $(x^p \bmod a(x)) \bmod 2 = 1$  is  $p = 2^r - 1$  [7].

For computational efficiency, most of the  $a_i$  in (10) should be zero. In  $GF(2)$  there is only one irreducible binomial,  $x + 1$ , which would yield an unacceptable period [8]. Consequently, the trinomials are usually used to express the recurrence sequence (10),

$$X_n = (X_{n-r} + X_{n-s}) \bmod 2, \quad s < r < n. \quad (16)$$

Addition modulo 2 for one-bit variables is ordinary binary exclusive-or operation XOR, so (16) may be rewritten as

$$X_n = X_{n-r} \text{ XOR } X_{n-s}. \quad (17)$$

LFSR recursion (10) produces pseudo-random bit sequence. To obtain  $k$ -bit pseudo-random integers  $Y_n$  from such recursion, one can group up  $k$  sequential bits,

$$Y_n = \sum_{j=1}^k 2^{k-j} X_{n+j-1}. \quad (18)$$

Such method is called the digital multistep method of Tausworthe [20].

Another method proposed by Lewis and Payne [21] is the generalized feedback shift register (*GFSR*). In GFSR scheme bits in the positions  $j$  of the pseudo-random integer are filled with the copy of initial one-bit recursion (17) which has a period  $2^r - 1$  with some nonnegative offsets  $d_j$ ,

$$Y_n = \sum_{j=1}^k 2^{k-j} X_{n+d_j}. \quad (19)$$



Clearly, LFSR is the particular case of GFSR.

For example of GFSR it could be mentioned the R250 generator [22]. It is another infamous PRNG which causes the severe problems in the Monte-Carlo simulations of the two-dimensional Ising model using the single-cluster Wolff update algorithm (see [9] and references therein). For R250 the GFSR parameters are  $r = 250$  and  $s = 103$ ,

$$X_n^{\text{R250}} = X_{n-250} \text{ XOR } X_{n-103}. \quad (20)$$

The R250 period is  $P_{\text{R250}} = 2^{250} - 1 \approx 1.81 \times 10^{75}$ .

### A.3 Lagged Fibonacci generators

Lagged Fibonacci generators (*LFG*) is another class of the PRNGs. It is based on the well-known Fibonacci recurrence sequence

$$X_n = X_{n-1} + X_{n-2}. \quad (21)$$

Because the simple Fibonacci generator is not very good [23] one always uses the generalized relation (21) with respect to any given binary arithmetic operation  $\odot$  and prehistory

$$X_n^{\text{LFG}} = (X_{n-r} \odot X_{n-s}) \bmod m, \quad (22)$$

where  $r$  and  $s$  are called “lags”,  $r \leq n$  and  $1 < s < r$ .

The LFG period  $P_{\text{LFG}}$  for different operations  $\odot$  is

$$P_{\text{LFG}} \leq \begin{cases} (2^r - 1)m/2 & \text{for } + \text{ or } - \\ (2^r - 1)m/8 & \text{for } \times \\ (2^r - 1) & \text{for XOR} \end{cases}. \quad (23)$$

The main attractive features of the LFGs are long period, potential absence of conversion integer into float operations and simple recursive scheme which not requires the heavy mathematical operations. However, for generation LFGs it is needed to store  $r$  previous pseudo-random values.

There are numerous possible pairs of the LFG lags [11]. The larger lags lead to the decreasing of the correlations between the numbers in the sequence. But even for relatively short lag table  $r \gtrsim 20$  it passes many statistical tests.

RAN3 generator [11] could be mentioned as an example of the LFG. It was proposed by Mitchell and Moore (unpublished), with lags  $r = 55$  and  $s = 24$ ,  $m = 10^9$  and operation subtraction,

$$X_n^{\text{RAN3}} = (X_{n-55} - X_{n-24}) \bmod 10^9. \quad (24)$$

The RAN3 period is  $P_{\text{RAN3}} = (2^{55} - 1)10^9/2 \approx 1.8 \times 10^{25}$ .

### A.4 Combined generators

Combined generators are a special class of the PRNGs, which contains the features of the different PRNG classes. There are two main motivations to use combined generators:

- the period increasing of the generator,
- the improving of the generator statistical properties.

#### A.4.1 Multiple recursive generators

The obvious extensions of the LCG is the multiple recursive generator (*MRG*) [16, 17] which is determined as the combination of the MLCGs

$$X_n^{\text{MRG}} = (a_1 X_{n-1} + a_2 X_{n-2} + \dots + a_k X_{n-k} + c) \bmod m. \quad (25)$$

When  $k > 1$ , MRG is usually called MRG of the  $k$  order. The maximal period of the MRG is  $P_{\text{MRG}} \leq m^k - 1$ . In fact LFG is the special case of the MRG (for multipliers  $a_i = 1$  and  $c = 0$ ).

By decomposition of the modulus of the MLCG into two terms  $m = aq + r$  and eqn.(4) may be written as following [16]

$$\begin{aligned} X_n &= aX_{n-1} \bmod m = (a(X_{n-1} \bmod q) - \lfloor X_{n-1}/q \rfloor r) \bmod m, \\ X_n &= X_n + m \text{ for } X_n < 0, \end{aligned} \quad (26)$$

where  $\lfloor a/b \rfloor$  denotes the integer part of the  $(a/b)$  and

$$q = \lfloor m/a \rfloor, \quad r = m \bmod a. \quad (27)$$

To provide the uniform distribution the combinations of  $l$  generators (26) may be combined as [16]

$$\begin{aligned} X_n &= \left( \sum_{j=1}^l (-1)^{j-1} X_{j,n} \right) \bmod (m_1 - 1), \\ X_n &= X_n + (m_1 - 1) \text{ for } X_n \leq 0. \end{aligned} \quad (28)$$

Here the new index  $j$  in  $X_{j,n}$  means the  $n$ -th value (26) of  $j$ -th generator.

One of the possible MRGs is the RANECU generator [16]. It is the combination of two MLCGs ( $l = 2$ ) with  $a_1 = 40014$ ,  $m_1 = 2147483563$  and  $a_2 = 40692$ ,  $m_2 = 2147483399$ . The RANECU period is  $P_{\text{RANECU}} = (m_1 - 1)(m_2 - 1)/2 \approx 2.30584 \times 10^{18}$ . MRGs have good statistics and pass most the tests.

#### A.4.2 XORShift

XORShift PRNG, proposed by Marsaglia [25], is another member of the GFSR generators class. Let  $X_0$  be a some initial  $k$ -bit row-state of XORShift and  $T$  is  $k \times k$  nonsingular binary matrix which sets linear transformation. The  $n$ -th PRNG state may be derived through the following equation

$$X_n^{\text{XORShift}} = X_0 T^n. \quad (29)$$

To ensure the performance requirements Marsaglia proposed the special form of matrix  $T$ ,

$$T = (I + L^a)(I + R^b)(I + L^c), \quad (30)$$

where matrices  $L$  and  $R$  are  $k \times k$  binary matrices which effect shift of one to the left and right, correspondingly. So, if  $X_m$  is a  $k$ -bit state then  $L^a$  causes the new state  $L^a X_m \equiv (X_m \ll a)$  as well as  $(I + L^a)$  – the state  $(I + L^a)X_m \equiv X_m \text{ XOR } (X_m \ll a)$ . In [25] Marsaglia lists all possible full-period triplets  $(a, b, c)$  for 32-bit (648 combinations) and 64-bit (2200 combinations) XORShift PRNG.

The maximal period of XORShift is

$$P_{\text{XORShift}} \leq 2^k - 1. \quad (31)$$

In spite of XORShift PRNG passes the *DIEHARD Battery of Tests of Randomness* [25] L'Ecuyer appoints that it “spectacular failed” the *SmallCrush* and *Crush* tests [26]. L'Ecuyer does not recommend to use this class of the generators, but proposes the own version of the XORShift implementation – **Seven-XORShift**.

Marsaglia gives an example of the XORShift generator for 128-bit vector with four 32-bit components – XOR128 PRNG [25],

$$(X_{n-3}, X_{n-2}, X_{n-1}, X_n)^{\text{XOR128}} = (X_{n-4}, X_{n-3}, X_{n-2}, X_{n-1}) \cdot \begin{pmatrix} 0 & 0 & 0 & (I + L^{11})(I + R^8) \\ I & 0 & 0 & 0 \\ 0 & I & 0 & 0 \\ 0 & 0 & I & (I + R^{19}) \end{pmatrix}, \quad (32)$$

or in the terms of the 32-bit components

$$\begin{aligned} t &= (X_{n-4} \text{ XOR } (X_{n-4} \ll 11)), \\ X_{n-3} &= X_{n-2}, \quad X_{n-2} = X_{n-1}, \quad X_{n-1} = X_n, \\ X_n &= (X_{n-1} \text{ XOR } (X_{n-1} \gg 19)) \text{ XOR } (t \text{ XOR } (t \gg 8)). \end{aligned} \quad (33)$$

The XOR128 period is  $P_{\text{XOR128}} \leq 2^{128} - 1$ .

#### A.4.3 Mersenne twister

One of the most “fashionable” modern PRNGs is the Twisted GFSR generator (*TGFSR*) or Mersenne twister generator [27, 28]. TGFSR is the modernization of the GFSR and its algorithm is based on the following recurrence for  $w$ -bit vectors  $X_n$

$$X_{n+r}^{\text{TGFSR}} = X_{n+s} \text{ XOR } (X_n^{\text{upper}} \text{ OR } X_{n+1}^{\text{lower}}) A, \quad (34)$$

where superscript indices “upper” and “lower” denote the  $w - u$  highest and  $u$  lowest bits of a corresponding binary vector  $X_i$ , respectively,

$$\begin{aligned} X_i^{\text{upper}} &= X_i \text{ AND } (2^w - 2^u), \\ X_i^{\text{lower}} &= X_i \text{ AND } (2^u - 1), \end{aligned} \quad (35)$$

and matrix  $A$  is a “twisting” binary  $w \times w$  matrix, which form is chosen by performance reason

$$A = \begin{pmatrix} 0 & 1 & 0 & & 0 \\ 0 & 0 & 1 & & 0 \\ & & & \ddots & \\ 0 & 0 & 0 & & 1 \\ a_{w-1} & a_{w-2} & a_{w-3} & \cdots & a_0 \end{pmatrix}. \quad (36)$$

So, only one  $w$ -bit vector  $a = (a_{w-1}, a_{w-2}, \dots, a_0)$  defines the product  $X_i A$ ,

$$X_i A = \begin{cases} (X_i \gg 1) & \text{if } (X_i \text{ AND } 1) = 0 \\ (X_i \gg 1) \text{ XOR } a & \text{if } (X_i \text{ AND } 1) = 1 \end{cases}. \quad (37)$$

For improving the statistical properties of the sequence so-called tempering procedure is applied for the output sequence  $X_n$ . This procedure is defined with the

$$\begin{aligned} t &= X_n \text{ XOR } (X_n \gg m), \\ t &= t \text{ XOR } ((t \ll d) \text{ AND } b), \\ t &= t \text{ XOR } ((t \ll e) \text{ AND } c), \\ Y_n^{\text{TGFSR}} &= t \text{ XOR } (t \gg l). \end{aligned} \quad (38)$$

By appropriate choosing of  $r$ ,  $u$  parameters and binary vector  $a$ , it might reach the maximal period of the TGFSR,

$$P_{\text{TGFSR}} \leq (2^{rw-u} - 1). \quad (39)$$

The most famous implementation of the TGFSR PRNG is MT19937 [28]. The TGFSR parameters of the MT19937 are the following:

$$\begin{aligned} w = 32, \quad r = 624, \quad s = 397, \quad u = 31, \\ a = 9908B0DF_{16} = 10011001000010001011000011011111_2 \end{aligned} \quad (40)$$

and tempering parameters are

$$\begin{aligned} m = 11, \quad l = 18, \\ d = 7, \quad b = 9D2C5680_{16}, \\ e = 15, \quad c = EFC60000_{16}. \end{aligned} \quad (41)$$

The maximal period of the MT19937 is

$$P_{\text{MT19937}} \leq 2^{624 \times 32 - 31} - 1 = 2^{19937} - 1 \approx 4.3 \times 10^{6001}. \quad (42)$$

#### A.4.4 RANMAR

RANMAR [23, 24] is a combination of two generators, 24-bit lagged Fibonacci generator  $LFG(97, 33, -)$   $Y_n$  with  $m = 2^{24} = 16777216$  and simple arithmetic sequence  $C_n$  for the prime modulus  $M = 2^{24} - 3 = 16777213$ ,

$$X_n^{\text{RANMAR}} = (Y_n - C_n) \bmod m. \quad (43)$$

Or equivalently the producing recurrence is,

$$\begin{aligned} X_n^{\text{RANMAR}} &= Y_n - C_n, \\ X_n &= X_n + m \quad \text{for } X_n < 0. \end{aligned} \quad (44)$$

Here  $Y_n$  and  $C_n$  are

$$\begin{aligned} Y_n &= (Y_{n-97} - Y_{n-33}) \bmod m, \\ C_n &= (C_{n-1} - D) \bmod M, \end{aligned} \quad (45)$$

where  $D = 7654321$ .

The  $LFG(97, 33, -)$  period is  $P_{LFG(97, 33, -)} \leq (2^{97} - 1)2^{24}/2 \simeq 2^{120}$  (see eqn.(23)) and the period of the arithmetic sequence  $C_n$  is  $P_{LCG(1, 2^{24})} \leq (2^{24} - 1)$  (see eqn.(5)). Therefore, the total period of the RANMAR is

$$P_{\text{RANMAR}} \lesssim 2^{144} \simeq 2.23 \times 10^{43}. \quad (46)$$

#### A.4.5 Add-With-Carry and Subtract-With-Borrow generators

In 1991 Marsaglia and Zaman introduced a new class of PRNGs: add-with-carry (AWC) and subtract-with-borrow (SWB) [29], which are small modifications of the LFG with respect to supplementing an extra carry or borrow bit. Due to the branching it became the first class of nonlinear PRNGs [8]. The AWC generator is described by the sequence

$$\begin{aligned} X_n^{\text{AWC}} &= (X_{n-r} + X_{n-s} + c_{n-1}) \bmod m, \\ c_n &= \begin{cases} 1 & \text{if } (X_{n-r} + X_{n-s} + c_{n-1}) \geq m \\ 0 & \text{if } (X_{n-r} + X_{n-s} + c_{n-1}) < m \end{cases}. \end{aligned} \quad (47)$$

In addition to  $r$  seed values  $(X_1, \dots, X_r)$  generator must be initialized with the carry bit  $c_r$ . The maximal period of the AWC generator is

$$P_{\text{AWC}} \leq m^r + m^s - 2. \quad (48)$$

In the SWB case the subsequent values of the sequence are obtained by

$$\begin{aligned} X_n^{\text{SWB}} &= (X_{n-r} - X_{n-s} - c_{n-1}) \bmod m, \\ c_n &= \begin{cases} 1 & \text{if } (X_{n-r} - X_{n-s} - c_{n-1}) < 0 \\ 0 & \text{if } (X_{n-r} - X_{n-s} - c_{n-1}) \geq 0 \end{cases}. \end{aligned} \quad (49)$$

L'Ecuyer noted [10] that SWB has a second variant, in which indices  $r$  and  $s$  in (49) are swapped. The maximal period of the SWB generator is

$$P_{\text{SWB}} \leq m^r - m^s - 2. \quad (50)$$

The well-known example of the SWB is RCARRY [23] which underlies the RANLUX PRNG. The RCARRY parameters in (49) are  $m = 2^{24}$ ,  $r = 24$  and  $s = 10$ ,

$$\begin{aligned} X_n^{\text{RCARRY}} &= (X_{n-24} - X_{n-10} - c_{n-1}) \bmod 2^{24}, \\ c_n &= \begin{cases} 1 & \text{if } (X_{n-24} - X_{n-10} - c_{n-1}) < 0 \\ 0 & \text{if } (X_{n-24} - X_{n-10} - c_{n-1}) \geq 0 \end{cases}. \end{aligned} \quad (51)$$

The RCARRY period is about [29]

$$P_{\text{RCARRY}} \leq ((2^{24})^{24} - (2^{24})^{10} - 2) / 48 \simeq 1/3 \times 2^{572} \simeq 5.15 \times 10^{171}. \quad (52)$$

It is less than the maximal period of the SWB (50) because modulus  $m = 2^{24}$  is not a prime number.

#### A.4.6 RANLUX

Despite all advantages (extremely long period, portability and good productivity) AWC and SWB generators suffer from some statistical defects (a bad lattice structure), showed by Lüscher [30]. To eliminate these lacks James [31] implements the Lüscher's [30] idea to modify the SWB generator RCARRY. In the new generator which was called RANLUX (for LUXury RANdom numbers [31]) after producing  $r = 24$  pseudo-random values the  $p - r$  following sequential values are discarded. It might be used any values of  $p$ , but there are five generally accepted levels of the luxury every of which has its own value  $p$  [30, 31],

- **level 0** ( $p = 24$ ): complete equivalent to original RCARRY generator, there are no discarding values
- **level 1** ( $p = 48$ ): throws out 24 values after one generation cycle; considerable improvement in quality over RCARRY, passes the gap test, but still fails spectral test
- **level 2** ( $p = 97$ ): passes all known tests, but theoretically still defective
- **level 3** ( $p = 223$ ): default level, any theoretically possible correlations have a very small chance of being observed
- **level 4** ( $p = 389$ ): highest possible luxury, all 24 bits of the mantissa are chaotic.

Lüscher recommends [30] to use a default value  $p = 223$  and notes that employment of values  $p > 389$  is pointless.

## References

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