SpaceTeamSat1
Preliminary Design Document
Communication and On-board Computer Hardware

17.05.2023

Version 1.0

Revision History

Revision	Date	Author(s)	Description
0.1	21.01.2023	Raphael Behrle	Preliminary version
0.2	03.04.2023	Patrick Kappl	Reworked LaTeX code and title page. Improved citations.
1.0	17.05.2023	David Wagner	PDR findings implementation in the discussion.

Review History

The Preliminary Design Review (PDR) consists of two parts: First, this document itself and second, a review meeting in which the topics are discussed in person. In the following table the invited reviewers are listed. Additionally, it is stated if feedback to the document was received (DOC) as well as if the person participated in the PDR meeting (PDR).

Time and place of PDR: 24.01.2023 17:00 in person at the TU Wien Space Team HQ

Contribution	**Reviewer**	**Email**	**Justification**
Electronics, **PDR**	Andreas Sinn	andreas.sinn @spaceteam.at	Pegasus/DISCO One
Electronics, Testing, **PDR**	Bernhard Seifert	seifert@fotec.at	Pegasus
Electronics, Testing	Dominik Kohl	dominik.kohl @schiebel.net	Pegasus/former TUST president
Satellite systems, RF, **PDR**	Lars Mehnen	lars.mehnen @technikum-wien.at	SSETI Express/RF specialist
Standards, Documentation	Martina Meisnar	martina.meisnar @esa.int	ESA Mat. and Process Eng./FYS
Electronics, Mission design	Martin Langer	martin.langer @ororatech.com	CTO Ororatech/MOVE (TU Munich)

Authors

Contribution	Name	Email
Microcontroller, Memories	Simon Klaus	simon.klaus@spaceteam.at
RF Communication	Jakob Riepler	jakob.riepler@spaceteam.at
Voltage Regulation, PCB design	Peter Kremsner	peter.kremsner@spaceteam.at
Requirements	David Wagner	david.wagner@spaceteam.at
General	Raphael Behrle	raphael.behrle@spaceteam.at

Contents

Glossary

BWM Burn wire mechanism used to release and unfold the antenna system of SpaceTeamSat1. 8, 16

CDR Critical Design Review; A technical review, where the defined requirements are opposed with the design on hand. Moreover, the design shall be challenged in terms of its use case. 1, 4

COBC Communication and on-board computer; Microcontroller that is responsible for the CubeSat management tasks and the RF communication. 1–10, 14–24

CSBI CubeSat Bus Interface; The bus which is used on SpaceTeamSat1 for the communication and power distribution between the subsystems. 2–4, 10–13, 22

CubeSat A satellite, that adheres to the CubeSat design specification. SpaceTeamSat1 is a 1U-standard CubeSat. vi, vii, 1, 2, 6–10, 14, 21–23

EDU Educational Unit; The payload aboard of SpaceTeamSat1. The main component is a Raspberry Pi CM3+. 1, 6–8, 10, 15, 16

EPS Electric Power System; The subsystem of a CubeSat, that provides and conditions electric energy. 1, 3, 4, 7–10, 15, 16, 22, 23

Flash Memory, which is capable to perform 100k read/write cycles. However, tends to be less resistant against radiation.
At the moment it is designated to store students code as well as results on the flash. 1, 8, 20, 21

FlatSat A printed circuit board (PCB), which holds all subsystem PCBs and allows easy access, development and debugging in a more structured way than it would be in the stacked CubeSat-integrated configuration. 1

FRAM Ferroelectric random access memory; Memory, which is dedicated for sensitive data, i.e. COBC SW. Additionally, FRAMs come with high read/write cycles of approx. 1000 trillion and are more resistant to radiation than other memory technologies.
At the moment it is not defined, which data exactly get stored on the FRAM. 1, 8, 20

FSK Frequency shift keying; used in the scope of RF communication. 21

FW Embedded software instructions to tell an electronic device how to operate. 8

FYS Fly Your Satellite!; An ESA program, that sponsors CubeSat missions with academic goals and guides selected teams in the development of CubeSats. 2

GFSK Gaussian frequency shift keying; used in the scope of RF communication. 21

GS Ground station which uplinks data to the CubeSat. 6, 9, 21

GSE The HW and SW on the ground which is connected via the Umbilical Cord Interface to the CubeSat. 24

HW All mechanical as well as electronic and electrical components of the CubeSat. 1, 3

IC Integrated circuit. 2, 8, 18, 22

LED Light emitting diode. 17

LNA Low noise amplifier; used in the scope of RF communication. 21, 22

OOK On-off keying. For example, morse code is also a very slow form of OOK. 21

OS Operating system; software environment which is responsible for some dedicated tasks, e.g. priority assignment, etc. . 1

PA Power amplifier; used in the scope of RF communication. 21, 22

PCB Printed Circuit Board; Board that mounts electronics and the electrical connectors. 6, 10, 22

PDD Preliminary Design Document; The corresponding document published in consequence of the PDR. 15

PDR Preliminary Design Review; A technical review, where the preliminary requirements are evaluated and locked in. Furthermore, design choices, that have been made until this point shall be challenged. 1, 8, 14, 17

RF Radio frequency. 1, 2, 6, 9, 10, 18, 21–23

RTC Real time clock. 17

RX Receive; used in the scope of RF communication. 9, 16, 21, 22

SPI Serial Peripheral Interface. 2, 10, 15–17, 20

STS1 SpaceTeamSat1; The name of the first CubeSat mission of the TU Wien Space Team and the corresponding satellite. vii, 1

SW Programs running on the microcontroller. Here, it needs to be differentiated between SW on the COBC and on the EDU (Raspberry Pi). 1, 3, 8, 14–17

TID Total ionizing dose. 14

TUST TU Wien Space Team; The team behind SpaceTeamSat1 (STS1). 1

TX Transmit; used in the scope of RF communication. 9, 16, 21, 22

UART A universal asynchronous receiver-transmitter is a computer hardware device for asynchronous serial communication in which the data format and transmission speeds are configurable. 24

UCI Umbilical Cord Interface; External connector at the CubeSat, that is specified by the CubeSat specification. 10, 15, 16

UHF Ultra high frequency. The frequency range around 430 MHz. 21, 22

USART Universal synchronous asynchronous receiver transceiver. 10, 15, 16

VBUS Voltage bus from the EPS to all subsystems. 10, 18

1 Introduction

This document serves as the Preliminary Design Review (PDR) of the Communication and on-board computer (COBC) subsystem of the STS1 CubeSat developed and built by the TU Wien Space Team (TUST). As this document is created at an early project phase, requirements and design may be subject to change, until they are reviewed and locked in at a future PDR or even Critical Design Review (CDR).
At moment (14.01.2023) the COBC is running on a configuration, which allows to use the microcontroller as well as memories for the Software (SW) development. The actual status is V2. Note that the only difference between V1 and V2 is the Radio frequency (RF) communication path, as V1 used a RF module, whereas the actual used RF circuit uses a RF IC and a RF amplifier stage. The circuit is more or less copy from another CubeSat mission (Oresat-1). Details about the actual RF implementation is discussed in section 3.4. The existing COBC prototype is integrated in a running demo project on the FlatSat. The COBC V2 holds the microcontroller (STM32F411RE) with an external watchdog timer, a Ferroelectric random access memory (FRAM) and a Flash memory, the RF circuit as well as a linear voltage regulator for these devices.
Unfortunately, the RF path could not be verified in the scope of this document as we are facing an issue with a SW bug in Rodos (used Operating system (OS) on the COBC), which is solved from a Hardware (HW) point of view. In this respect, further details again can be found in section 3.4.

In the following document design decisions on the COBC architecture as well as design parameters are discussed. Moreover, further plans on the development of the COBC are considered and presented. Note that this document merely discusses the HW design of the COBC and does not include any details regarding SW, as it would exceed the scope of this document resp. review. In this respect, additional documents dedicated to the COBC software will be prepared. The document is structured as follows. In the section 1.1 a more specific description of the COBC is given and some basic characteristics are discussed. Additionally, section 1.2 lists all relevant documents, which relate directly to the COBC platform. The requirements that lay the foundation of this subsystem are described in section 1.3. Chapter 2 discusses the high-level architecture and sketches the purpose of the components of the COBC. Building on that, chapter 3 goes into the detailed structure of the COBC parts. The suggested behaviour of the COBC is discussed in chapter 4. It needs to be considered, that merely the electrical behaviour is discussed and no insights are given on the software behavior. Finally, in chapter 5 the existing results and major conclusions are elaborated. Moreover, an outlook regarding the next steps is documented.

1.1 The Communication and On-Board Computer

The COBC is the functional master of the CubeSat architecture and is responsible for all actions executed on the CubeSat. The main tasks are handling in-coming RF commands, organising data stored on the CubeSat, as well as initiating the execution of software on the Educational Unit (EDU) module. Finally, the COBC is responsible for any data to be downlinked, i.e. beacons, obtained results of the EDU and requested commands. The main components are a STM32 microcontroller, an external watchdog timer, memories (at the moment Flash and FRAM), the RF circuit - consisting of a RF chip and an output stage, a voltage regulation circuit to cope with inconsistencies in voltage provision through the Electric Power System (EPS), whereas a linear voltage regulator ($V_{out} = 3.3\,\mathrm{V}$) is used for

the microcontroller, the memories and the watchdog timer, and a DC/DC converter providing 5 V for the RF stage. Importantly, the CubeSat Bus Interface (CSBI) is used for communication with the other subsystems and is the solely connection to power the COBC.

1.2 Related Documents

This section is separated in two parts: The first table gives documents which build the base of the CubeSat architecture established so far. Additionally, an attached list gives an overview of the used Integrated circuit (IC)s and a website link to their datasheets for easy access.

Short Sign	Document Name	Purpose
STS1PDD[1]	CubeSat SpaceTeamSat1: Preliminary Design Document: System Architecture	Mission definition and design of the CubeSat system architecture
STS1DATA[2]	CubeSat SpaceTeamSat1: Dataflow Game	Design of the dataflow from the ground station to the CubeSat and within the CubeSat
STS1EPSPDD[3]	Cubesat SpaceTeamSat1: Preliminary Design Electric Power System	Design of the architecture, functionality and usage of the EPS
FYSD[4]	Fly Your Satellite! Design Specification Version 3.0	Describes requirements of CubeSats that participate in the FYS program. (18.06.2022)
CDS[5]	CubeSat Design Specification Rev.14	Specifies the CubeSats standard. (18.06.2022)

In the following all relevant documents on a component level, i.e. datasheets, as well as relevant design guidelines, which are referred and used throughout this document and the design process are listed.

1. **Microcontroller STM32F411RE**:
   ARM-Cortex-M4 100 MHz microcontroller, 512 kB Flash, 128 kB SRAM, 49 GPIOs, 3 USARTs, 5 SPIs/I2Cs.
   Link to datasheet: STM32F411RE datasheet
2. **External Watchdog STWD100NPWY3F**:
   Self-contained device to prevent system failures by triggering a restart.
   Link to datasheet: Watchdog datasheet
3. **FRAM CY15B108QN**:
   8 Mbit ferroelectric random access memory, 40 MHz, Serial peripheral interface (SPI) interface
   Link to datasheet: FRAM datasheet
4. **Flash W25Q01JV**:
   1 Gbit flash memory, SPI interface
   Link to datasheet: Flash datasheet
5. **RF chip Si4463**:
   Fully integrated sub-GHz RF transceiver with support for FSK and GFSK with a data-rate of up to 1 Mbps.
   Link to datasheet: RF IC datasheet
6. **Voltage regulation MP28167GQ and MCP1725-3302EMC**:

a) **MP28167GQ**: Synchronous, 4-switch integrated buck-boost converter.
Link to datasheet: Buck-boost converter datasheet

b) **MCP1725-3302EMC**: Low-dropout linear regulator
Link to datasheet: Linear regulator datasheet

1.3 Requirements

In the following section some basic requirements are described for the COBC. In comparison to, e.g. the EPS subsystem, the requirements for the COBC HW are described in short key facts, as the main and crucial requirements are SW defined. Note that the same documentation procedure as in [3] is used.

The following subsystem requirement is deduced from STS1 System Architecture Requirement 1.3.[1] Each subsystem of STS1 shall be powered, via the CSBI, by a voltage level between 5 V and 8.4 V:

1.3.COBC.1 The COBC shall be operational at a voltage between 5 V and 8.4 V.

Note: The COBC is powered solely via the CSBI.

Fulfilled: In Section 2.1.1

The following subsystem requirement is deduced from STS1 System Architecture Requirement 1.4.[1] The power generating subsystem of STS1 shall provide a voltage level with a ripple lower than 100 mV:

1.4.COBC.1 The COBC shall be operational with a voltage ripple of at less than 100 mV.

Note: The COBC is powered solely via the CSBI.

Fulfilled: In Section 3.1.3

The following subsystem requirement is deduced from STS1 System Architecture Requirement 3.1.[1] The CubeSat shall automatically send out a beacon at least once every 30 s:

3.1.COBC.1 The COBC shall be connected to an antenna.

Fulfilled: In Section 3.4.2

The following subsystem requirement is deduced from STS1 System Architecture Requirement 5.1.[1] The CubeSat shall have two bus connectors, which ensure communication between all subsystems:

5.1.COBC.1 All communication the COBC needs to other subsystems shall be done via the CSBI.

Fulfilled: In Section 2.2

The following subsystem requirements are deduced from STS1 System Architecture Requirement 5.2.[1] The CubeSat shall have a reusable satellite framework:

5.2.COBC.1 The COBC shall be operable up to a TID of 100 krad.

Fulfilled: In Chapter 3

5.2.COBC.2 The COBC shall be designed to withstand, as a minimum, an operational temperature range of -5°C to +50°C.

Note: Operational temperature refers to the temperature the surrounding structure of STS1 has, e.g. PCB above and below the COBC.

Fulfilled: In Chapter 3

5.2.COBC.3 STS1 shall have a reusable satellite framework. This means that the hardware of the COBC shall work independently from the science payload.

Fulfilled: In Chapter 2

5.2.COBC.4 The components mounted on the COBC shall have a maximum height of 6.35 mm and shall only be placed on the TOP-Layer of the PCB.

Fulfilled: In V3 of the COBC: Will be considered in the CDR

The following subsystem requirement is deduced from STS1 System Architecture Requirement 5.3.[1] The CubeSat shall have the science payload PCB(s) (here: EDU module) at the top (first PCB(s)) or at the bottom (last PCB(s)) of the electronic stack:

5.3.COBC.1 The COBC should be located at the bottom of the electronic stack.

Note: This is favourable as the antenna is placed on the Z- side of STS1 and the connection form the antenna to the COBC can be done easily if this is fulfilled.

Fulfilled: In Section 3.4.3

The following subsystem requirement is deduced from STS1 System Architecture Requirement 5.5.[1] The CubeSat shall have an antenna release mechanism. The mechanism shall be controlled via the master and powered via the EPS.

5.5.COBC.1 The COBC shall have dedicated connection to the CSBI for the triggering of the burn wire mechanism of the antenna.

Fulfilled: In Section 3.4.2

The following subsystem requirement is deduced from STS1 System Architecture Requirement 7.2.[1] The CubeSat shall have a central processing unit (here: COBC) which is able to activate and deactivate the science payload (here: EDU):

7.2.COBC.1 There shall be a feature to activate and deactivate the EDU.

Fulfilled: In Chapter 2

The following subsystem requirement is deduced from STS1 System Architecture Requirement 8.6.[1] The CubeSat shall be able to download the entire generated data of one student code at least once every 48 h:

8.6.COBC.1 The communication module of STS1 shall be able to send a file with the size of 1 MByte within 48 h.

Note: We expect to have a downlink data rate with 9600 baud. Furthermore, we expect to have an average communication window of 30 minutes a day. This means an average maximum downlink of just over 4 MB. With protocol losses and a safety factor of 2 we arrive at approximately 1 MByte.

Fulfilled: In Section 3.4

The following subsystem requirements are deduced from STS1 System Architecture Requirement 11.1.[1] The CubeSat shall comply with the mechanical FYS Requirements [6] where it makes sense:

11.1.COBC.1 The COBC shall be designed to withstand, as a minimum, a non-operational temperature range of -15°C to +60°C.

Fulfilled: In the introduction of Chapter 3

11.1.COBC.2 The COBC shall withstand a relative humidity level in the range of 25-75%.

Fulfilled: In the introduction of Chapter 3

2 Overview

This chapter gives an overview of the proposed architecture, in order to give a preliminary understanding of the COBC components. Figure 2.1 shows images of the COBC architecture for a better overview of the main components.

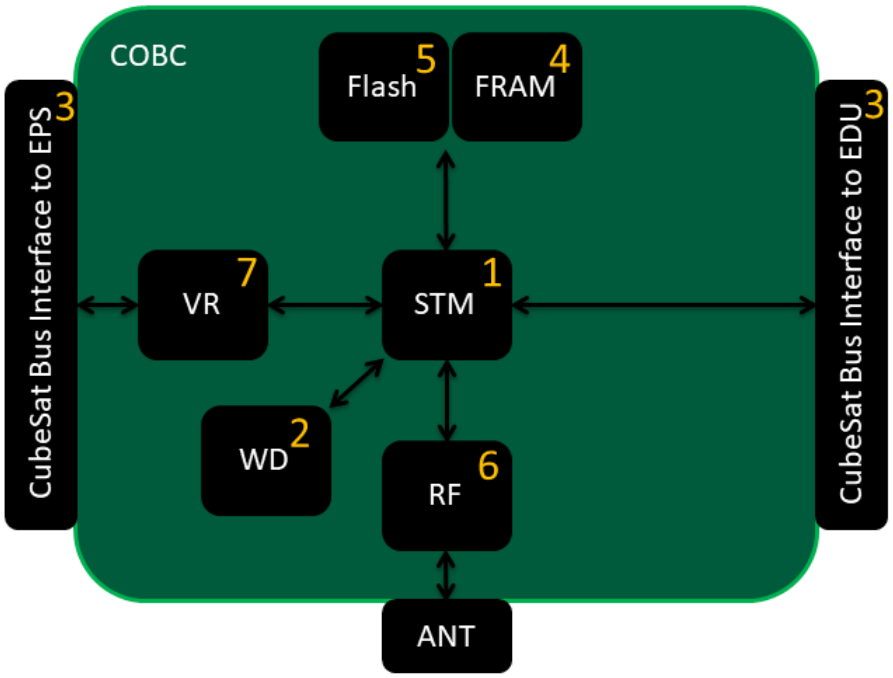
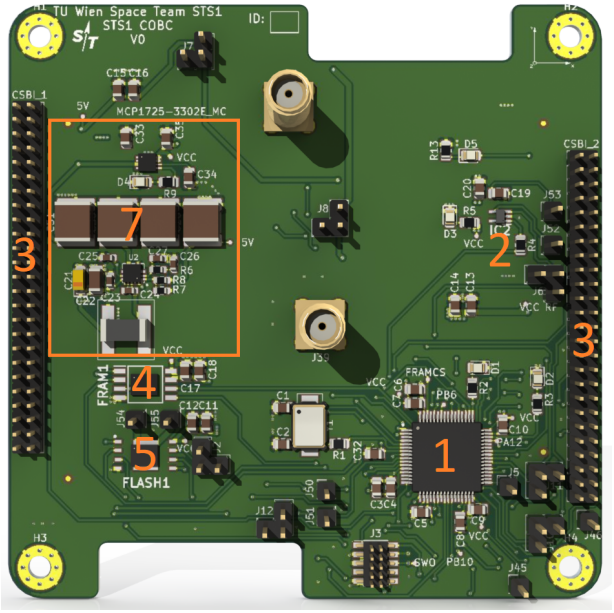


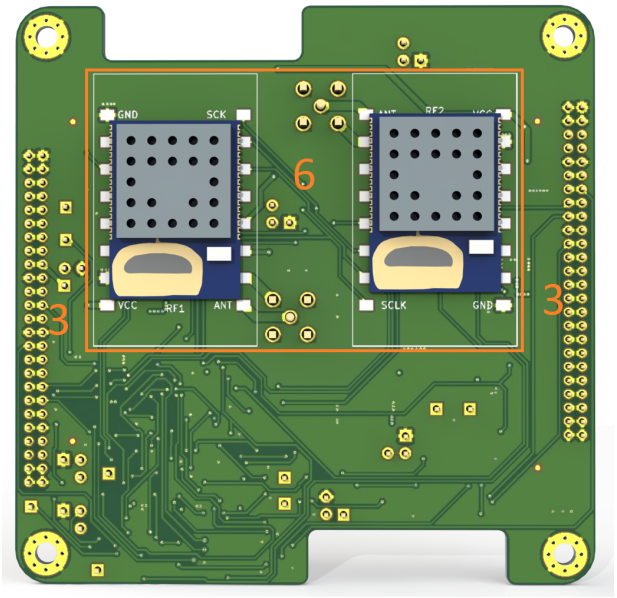
Figure 2.1: Block schematic of the COBC.
1. STM-Microcontroller, 2. WD-External watchdog, 3. EPS-Electrical Power System, EDU-Educational Unit, 4. FRAM-External memory, 5.Flash-External memory, 6. RF-RF circuit, 7. VR-Voltage regulation, ANT-Antenna.

In the following 3D render models of the COBC Printed Circuit Board (PCB)s are shown and shortly introduced. As V1 and V2 are considered in the scope of this work, both models are shown respectively compared.

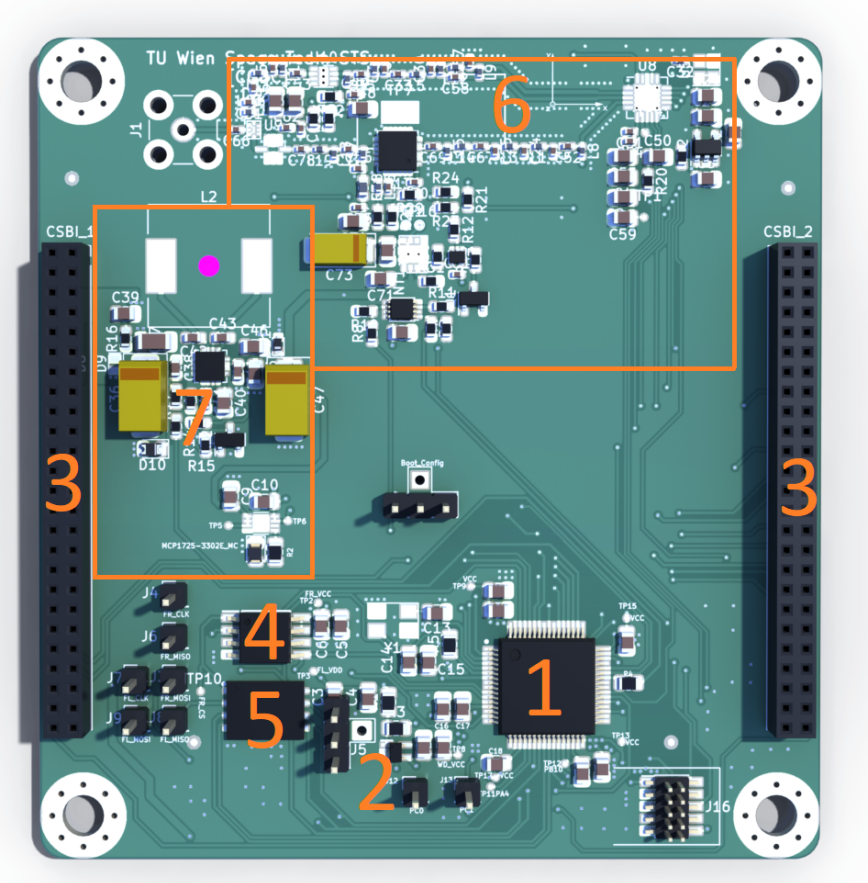
As already depicted in Figure 2.1, the COBC combines two crucial subsystems common in CubeSats into a single subsystem. Here, the ”C” in ”COBC” stands for ”Communication module” and the ”OBC” for ”On-Board Computer”. The decision to combine these two subsystems was made to reduce the amount of PCBs, as there is no need to specify two separate boards in the scope of the mission. Moreover, our objectives do not require two dedicated systems aboard the CubeSat and moreover minimizes complexity, which is an important aspect of this mission. The COBC is responsible for all actions happening on the CubeSat. This includes processing and evaluating all incoming and outgoing data as well as controlling the communication, which physically consists of RF communication from and to the Ground station (GS) and the communication with the EDU subsystem. Moreover, the COBC is actually setting the EDU in operation mode, managing the memory access and storage on the COBC, as well as creating beacons and transmitting them. The COBC acts as the master on the



(a) TOP view of the COBC V1



(b) BOT view of the COBC V1



(c) TOP view of the COBC V2

Figure 2.2: Relating to the block schematic, the components of the COBC are indicated.

CubeSat. This means that the COBC is not depending on the functionality of the EDU and continues its work regardless even if the EDU works, does not work, or actively tries to interrupt the COBC. The COBC is fully powered by the EPS which means, that the COBC only works if the EPS is functional.

(see [7]). Maintaining safe operation of the CubeSat, the COBC is always the first subsystem which will be powered as soon as power is provided by the EPS. The other subsystem – the EDU – can only be activated by the COBC. Also, the Burn wire mechanism (BWM) is initiated by the COBC although the electrical circuit is placed on, and powered by the EPS. It is also possible to carry out Firmware (FW) updates, which are possible via two separate and dedicated FW memory areas. Moreover, other memory units will be used for storing Python programs dedicated for the EDU subsystem as well as obtained result files generated by the EDU.

2.1 Architecture

As mentioned in the introduction of this chapter, the architecture is designed to be minimal complex and thus reliable. Therefore, no redundancy is implemented. Note that the reliability of the subsystem is increased by intensive testing rather than increasing complexity. The COBC subsystem architecture was evaluated within the Dataflow Game.[2] Hence, it was also determined that the communication module can be combined with the on-board computer, as no dedicated communication module is necessary for the expected data rates and communication capabilities. More details regarding this aspect is stated in section 3.4.

2.1.1 Design

As already mentioned before, the COBC design is designed to have a relatively trivial non-redundant design to reduce complexity and risk of malfunction, as the COBC is the core of the CubeSat itself. Therefore, when applicable and accessible components were chosen, which were already used in past space missions. However, due to the semiconductor crisis this aspect could not be fully met, as it was and still is difficult to get the desired components.

A general overview of all components and their dedicated purpose is elaborated in the following list, which matches the numbering of fig. 2.1 and fig. 2.2:

1. **Microcontroller**: As microcontroller a STM32F411RE is used and acts as heart and brain of the CubeSat. It handles all telemetry and housekeeping tasks required to keep the CubeSat operational. Moreover, the microcontroller itself is responsible for the memory management. From a payload point of view, the microcontroller handles all data to and from the EDU subsystem. Moreover, the microcontroller is responsible to trigger the BWM.
2. **Watchdog**: The external watchdog IC (STWD100PYW83F) is capable to enable an external reset in case an unexpected error occurs at the microcontroller unit. This is a crucial component to not immediately lose the whole mission after a small error. At the moment, it is not defined in which time intervals the external watchdog timer shall trigger a reset between two hours and two days (tbd).
3. **CubeSat Bus Interface**: Interface to the CubeSat bus, which consists of data and power lines. A detailed description is given in section 2.2.
4. **FRAM**: Ferro-electric random access memory. Through its higher radiation resistance it will be used to store more important files like the FW. Furthermore, the telemetry and persistent state data shall be stored at the FRAM as well, as these need to be overwritten often. Details regarding the explicit data will be discussed in the COBC SW PDR.
5. **Flash**: The Flash is less radiation resistant than the FRAM which is the reason why it will be mainly used to store volatile data. These are mostly related to EDU relevant data. More information about the EDU will be available at a later point in the EDU preliminary design.

6. **RF module/circuit**: The RF4463F30 module was considered in the COBC V1. However, due to limited output power and unknown thermal behaviour, we decided to use just the RF chip that is used inside the module and pair it with schematic parts of the OreSat[8] and SatNogs-COMMS[9] RF hardware design in V2.
   It is responsible to transmit (TX) and receive (RX) all communication between the CubeSat and the GS. All received data packets are forwarded directly to the microcontroller for further processing. The most frequent operation will be downlinking beacons every 30 s which will contain various information such as housekeeping data or telemetry data. Note that the beacon transmission is triggered by the STM.

7. **Voltage regulation**: The voltage regulation circuit ensures that all COBC components are powered. The EPS delivers 5 V–8.4 V which will be transformed into stable 5 V by the first part of the circuit. These 5 V are necessary to run the RF circuit. The second part of the circuit will transform these 5 V to 3.3 V needed by everything else.

Pin Header X- V1

			Pin Function	Used in Subsystem
1		2	GND	
3		4	GND	
5		6	VBUS	EPS, COBC, EDU
7		8	VBUS	EPS, COBC, EDU
9		10	GND	
11		12	SPARE_1	
13		14	EDU_HEARTBEAT	COBC, EDU
15		16	UART_COBC_EDU_TX	COBC, EDU
17		18	UART_COBC_EDU_RX	COBC, EDU
19		20	GND	
21		22	EDU_EN	COBC, EDU
23		24	EDU_UPDATE	COBC, EDU
25		26	GND	
27		28	EDU_SPI_CLK	EPS, EDU
29		30	EDU_SPI_MOSI	EPS, EDU
31		32	EDU_SPI_MISO	EPS, EDU
33		34	EDU_SPI_CS1	EPS, EDU
35		36	EDU_SPI_CS2	EPS, EDU
37		38	EDU_SPI_CS3	EPS, EDU
39		40	GND	
41		42	SPARE_2	
43		44	SPARE_3	
45		46	SPARE_4	
47		48	GND	
49		50	GND	

Table 2.1: The definition of Version 1 of the CSBI header in X- direction.

2.2 Interfaces

The COBC has an interface to the CSBI, which provides power from the EPS via VBUS. Other relevant pins for the COBC are connections to enable or disable the EDU, the Universal synchronous asynchronous receiver transceiver (USART) between COBC and EDU and the SPI between the COBC and the EPS as well as to the memories and the RF chip. According to the distributed system approach, the EPS does not guarantee a fixed voltage level on the power bus. Therefore, an additional voltage regulator to power its individual components is required. Furthermore, the COBC (and EPS) connect to the Umbilical Cord Interface (UCI) for accessibility (via USART) to the microcontroller on the COBC as well as charging the batteries. The CSBI connectors are placed on both sides of the COBC and are the only way to communicate with other subsystems. Table 2.1 and table 2.2 show the pin assignment of the CSBI which is used in the V1 of the CubeSat. Table 2.3 and table 2.4 show the pin assignment of the updated versions of the CSBI. Unfortunately there was an update after the initial version of the V2 of the CSBI, leading to the fact that the EDU_BOOT pin was moved from X+ CSBI to X- CSBI SPARE_4. Furthermore, SPARE_2 and SPARE_3 will be used for the communication from EDU to the potential dosimeter PCB from Seibersdorf. These shall be corrected in the V3 of the CubeSat.

Pin Header X+ V1

			Pin Function	Used in Subsystem
1		2	GND	
3		4	GND	
5		6	EPS_BAT_FAULT	
7		8	SPARE_6	
9		10	SPARE_7	
11		12	SPARE_8	
13		14	UCI_COBC_UART_TX	EPS, COBC
15		16	UCI_COBC_UART_RX	EPS, COBC
17		18	UCI_COBC_3V3	EPS, COBC
19		20	GND	
21		22	EPS_BAT_GOOD	
23		24	EPS_ANT_DEPLOY	EPS, COBC
25		26	EPS_CHARGING	EPS, COBC
27		28	GND	EPS, COBC
29		30	COBC_SPI_CLK	EPS,COBC
31		32	COBC_SPI_MOSI	EPS, COBC
33		34	COBC_SPI_MISO	EPS, COBC
35		36	COBC_SPI_CS1	EPS, COBC
37		38	COBC_SPI_CS2	EPS, COBC
39		40	COBC_SPI_CS3	EPS, COBC
41		42	GND	
43		44	VBUS	
45		46	VBUS	
47		48	GND	
49		50	GND	

Table 2.2: The definition of the CSBI header in X+ direction.

Pin Header X- V2

			Pin Function	Used in Subsystem
1		2	GND	
3		4	GND	
5		6	VBUS	EPS, COBC, EDU
7		8	VBUS	EPS, COBC, EDU
9		10	GND	
11		12	EDU_SPI_CS3	EPS, EDU
13		14	EDU_SPI_CS2	EPS, EDU
15		16	EDU_SPI_CS1	EPS, EDU
17		18	EDU_SPI_MISO	EPS, EDU
19		20	EDU_SPI_MOSI	EPS, EDU
21		22	EDU_SPI_CLK	EPS, EDU
23		24	GND	
25		26	SPARE_1	
27		28	SPARE_2	
29		30	SPARE_3	
31		32	SPARE_4	
33		34	GND	
35		36	EDU_HEARTBEAT	COBC, EDU
37		38	EDU_UPDATE	COBC, EDU
39		40	EDU_EN	COBC, EDU
41		42	GND	
43		44	UART_COBC_EDU_RX	COBC, EDU
45		46	UART_COBC_EDU_TX	COBC, EDU
47		48	GND	
49		50	GND	

Table 2.3: The definition of Version 2 of the CSBI header in X- direction.

Pin Header X+ V2

			Pin Function	Used in Subsystem
1		2	GND	
3		4	GND	
5		6	UCI_COBC_UART_TX	EPS, COBC
7		8	UCI_COBC_UART_RX	EPS, COBC
9		10	GND	
11		12	SPARE_5	
13		14	EPS_BAT_FAULT	
15		16	EDU_BOOT	COBC, EDU
17		18	GND	
19		20	UCI_COBC_3V3	
21		22	EPS_BAT_GOOD	EPS, COBC
23		24	EPS_ANT_DEPLOY	EPS, COBC
25		26	EPS_CHARGING	EPS, COBC
27		28	GND	
29		30	COBC_SPI_CLK	EPS,COBC
31		32	COBC_SPI_MOSI	EPS, COBC
33		34	COBC_SPI_MISO	EPS, COBC
35		36	COBC_SPI_CS1	EPS, COBC
37		38	COBC_SPI_CS2	EPS, COBC
39		40	COBC_SPI_CS3	EPS, COBC
41		42	GND	
43		44	VBUS	
45		46	VBUS	
47		48	GND	
49		50	GND	

Table 2.4: The definition of Version 2 of the CSBI header in X+ direction.

3 Components

Chapter 2 laid out the high level architecture of the CubeSat. This chapter focuses on the technological details and discusses the detailed description of the COBC components as well as their justification. As all components receive a certain amount of radiation, they shall be resistant to at least a Total ionizing dose (TID) of 100 krad. This will ensure the function of the CubeSat over at least one year. At the moment it is planned to perform radiation tests in cooperation with Seibersdorf.
Concerning the requirements stated in section 1.3 it can be stated that all components and circuits are operational with a voltage ripple of 100 mV, can be operated in the specified temperature range of −5 °C to 50 °C. Moreover, the specified non-operational environment parameters (temperature and rel. humidity) are fulfilled. All values were cross-checked with the corresponding datasheets of the used components.

3.1 Microcontroller

The microcontroller was chosen according operability with a suitable operating system (here: Rodos) and flight heritage, which is fulfilled by the selected microcontroller. Details regarding this aspects are discussed in the following sections. Moreover, the available interfaces played an important role of selection. In the following the most important aspects which lead to the decision as well as implications are discussed.

3.1.1 Overview

As brain of the COBC, the STM32F411RE is used. It is responsible for everything that happens on the CubeSat and is the logical master of the whole system. The STM32F411RE was already operated with Rodos and hence comes with a SW port. Further details regarding this aspect will be considered in the COBC SW PDR.
The basic specification are listed below and were extracted from the corresponding datasheet [10]:

1. **CPU**: 32-bit Cortex-M4
2. **Voltage**: 1.7 V–3.6 V
3. **Current**: Maximum V_{DD}-driven current = 160 mA
   Maximum current into V_{DD} = 100 mA
4. **Frequency**: Maximum of 100 MHz
5. **Power consumption**: 33 mW at 100 MHz and 3.3 V
6. **Internal memory**: 512 Kbyte Flash, 128 Kbyte SRAM
7. **Operating temperature range**: −40 °C to 125 °C

In the following "STM" will be used as a substitute of "STM32F411RE". The STM communicates fully through SPI and USART to its peripheral components. This includes a SPI connection to the flash, the FRAM, the EPS and the RF circuit. USART is used to communicate with the EDU and the UCI. On the COBC no I^2C is used as it is not reliable enough in this delicate application. Regarding SPI the following details can be stated:
SPI1 is used to communicate with the flash memory
SPI2 is used to communicate with the FRAM memory
SPI3 is used to communicate with the EPS
SPI4 is used to communicate with both RF-Modules. Unfortunately, due to a Rodos SW bug SPI4 cannot be used and would only be functional by an additional SW implementation, which would require additional testing and verification of the new components. Therefore, it was decided to not use SPI4 and change the SPI assignments physically to SPI3 together with the EPS sensor data. This will be implemented in the upcoming version V3.

The STM runs on a voltage domain of 3.3 V which will be provided by the COBC voltage regulation, discussed in section 3.2.

3.1.2 STM32F4 vs. STM32F3

At the start of the mission both STM32F4 and STM32F3 families were considered as microcontroller units. After evaluating both types it was concluded that the STM32F4 fits better for our application. A comparison between both is listed below:

Feature	STM32F411	STM32F303
SPI	5 with up to 50 Mbit/s	4 with up to 18 Mbit/s
USART	3; full DMA controller	2; one DMA controller
Frequency	100 MHz	72 MHz
Voltage range	1.7 V–3.6 V	2.0 V–3.6 V
Timers	11	14
CAN Interface	No	Yes

Although the STM32F4 has some flaws in comparison to the STM32F3, these issues will not really affect the mission as e.g. 14 timers or a CAN interface are not required. Another important aspect is the available Rodos port for the STM32F4 and its flight heritage. Unluckily, first troubles appeared when the component were ordered. There was literally no available stock of STMs available. This problem was solved with ordering NUCLEO development boards and desoldering the STM from such boards. This is possible as only a small amount of STMs were required. Luckily these NUCLEO boards contained STMs in the perfect footprint (LQFP-64) which made it easy to solder them onto the COBC. Lately we got sponsored by ST and therefore received free samples of the STM32F4.

3.1.3 COBC Inter-communication

This chapter only specifies the definition of the interfaces to resp. from the STM. For detailed settings and details, a separate COBC SW Preliminary Design Document (PDD) will be published.

Memories

The communication between the STM and the memories is happening via two separate SPI lines. Specifically, SPI1 is used to communicate with the Flash while SPI2 is used to communicate with the FRAM. Both memories chip select (CS) lines are connected to the SPI2 CS (see section 3.3).

RF modules/RF chip

V1 of the COBC uses two different RF modules for evaluation purposes. Both modules are connected via SPI4 while the CS is handled via two GPIO pins (A8 and C9). This is done as it is not intended to send with both modules active at the same time (see section 3.4).
In V2 a RF circuit was used, which was already implemented and flown successfully on OreSat.[8] As SPI4 is still used, but comes with the already mentioned Rodos SW bug, a full evaluation couldn't be done yet. In a mid-version (V2.5) the SPI interfaces are physically fixed for proper evaluation of the RF circuit.

EDU

For communicating with the EDU an EDU enable, an EDU update and a EDU heartbeat pin alongside an USART are available. The EDU enable pin is B0 the EDU update pin is B1 and the EDU heartbeat pin is C5. For file transfer USART1 is used. The EDU enable pin will enable/disable the EDU. The EDU update pin will inform the COBC that the EDU wants to communicate.

EPS

The COBC communicates via SPI3 with the EPS. The COBC acts as the master component. This connection is solely for communicating sensor values from the EPS to the COBC. Furthermore, there are three EPS status pins. These are the EPS Battery good pin, which indicates that the battery has enough power to function the EDU, the EPS antenna deployment pin, which will trigger the BWM and the EPS charging pin which indicates if the EPS is charging.

UCI

The UCI is used to program (and charge the batteries), when the CubeSat is assembled and in its stowed configuration. Therefore, three pins are used to connect to the UCI. These are TX and RX from USART2 and the UCI COBC 3V3 pin which can be used as an external power supply through the UCI.

Programming

Programming of the STM is done using an STLINK-V3. That programmer is plugged in via an 2x5 JTAG connector aboard the COBC. The SWD protocol is used to communicate with the STM. Programming it effectively only needs two pins to enable communication. These pins are the SWDClock pin and the SWDIO pin. Furthermore there are connections to the STM reset pin, VCC and GND.

Lessons learned

V1 of the COBC used Light emitting diode (LED)s on important data lines which caused inconsistencies during programming of the STM. These LEDs already got removed and will not be a problem in V2. However, indication LEDs for debugging will be implemented, i.e. indicating voltage levels as well as debugging LEDs There is also a problem with SPI4 as it was tested if it is possible to short MOSI and MISO lines of the SPI. However during that test, the high voltage dropped from the usual 3.3 V down to 2 V. This error only occurs on SPI4 an not on all the other SPIs. Finally, it was proven to be Rodos SW bug, which will be "fixed" by physically not using SPI4.

3.1.4 Real Time Clock

There are two options to compensate the STM's internal Real time clock (RTC) temperature deviation. Although it was decided to not use them they will be explained below.[11]

Analog approach On the input and the output of the oscillator are capacitor banks. The overall load capacitance seen by the crystal needs to be adjusted by the software, leading to a change in the oscillator frequency.

Digital approach The compensation is not made on an oscillator level but rather at time-keeping logic/function level. A few cycles need to be added or removed from the clock signal. The RTC is built with a register to configure the number of clock cycles to add/remove from the feeding clock signal.

As mentioned before, no dedicated adjustment of the RTC will be implemented and will solely be tackled by the COBC SW. Note that this issue will be discussed in the COBC SW PDR.

3.1.5 Watchdog

To be able to external reset the STM we will use a watchdog timer, which is suggested by ST. This is crucial to our mission as it prevents system failures which can occur after some hardware or software errors. At the moment we did not decide on the refresh time as we are unsure about the timing. Therefore, the suggested watchdog timer (see section 1.1) is not mounted as it prevented proper operation of the COBC due to too short refresh times, as it will be elaborated below.

Overview At the moment, the watchdog timer STWD100NPWY3F is considered. Basic specifications are listed below:

1. **Timeout periods**: 3.4 ms, 6.3 ms, 102 ms and 1.6 s.
2. **Voltage**: 2.7 V–5.5 V
3. **Current**: typ. 13 µA
4. **Operating temperature range**: −40 °C to 125 °C

Pins and application The watchdog IC has 5 pins. These are the watchdog Output pin (WDO), the enable pin (EN), the watchdog input pin (WDI), VCC and GND.
The basic functionality is that the WDI pin needs to be reset regularly. If a reset during the timeout period is missed, a system alert is generated and the WDO is asserted.
The EN pin allows to enable/disable the watchdog timer IC. If it is left floating it is as well enabled.
The watchdogs WDO pin is connected to the STM reset pin. It is not directly connected as the datasheet item 2 requires an 4.7 kΩ between the WDO and the STMs reset pin.

3.2 Voltage Regulation

A DC/DC converter is used to supply current from the battery bus to the systems on the COBC. The converter needs to generate a stable 5 V supply mainly for the high power RF amplifier of the radio module. Note that, the battery bus voltage can drop to or slightly below 5 V including voltage losses in the wires a buck/boost architecture is chosen. Importantly, a following linear voltage regulator (see 1.2 and 2.1.1) sets constant 3.3 V for all other IC used on the COBC subsystem.

Schematic and function

The chosen IC is the MP28167GQ by Monolithic Power Systems which delivers up to 3 A at 5 V, which should be enough to provide power to every subsystem on the COBC.
The design implements a under voltage lockout which is set to about 3.99V and a startup voltage of about 4.4V, this ensures that the input voltage is in an usable range for the converter to deliver 15W output power, however the EPS is considered to shutdown the systems on such a low bus voltage anyways. A over current protection is also present which is set to 3.56A (if needed a lower current limit can be set by changing the value of the resistor R5), this limits the bus and output current in case of a short circuit or other over current fault and ensures that other components would still work if such a condition is present so that the other systems would be able to handle the fault. To handle spurious over voltage situations, such as electrostatic discharges, a TVS diode is placed in the 5V rail as well as in the input rail of the dcdc converter, to protect the converter itself and also the electronic on the 5V rail. An optional snubber at the input voltage formed with a 1uF MLCC and a 100 milliohms resistor was also added to the design to suppress supply voltage ringing. This snubber is not populated in the current design, but could be populated if needed.
Q1 is currently used to disable the dcdc when the battery is near empty. This signal is intended to be driven by the EPS. Setting the $\overline{EN}$ input to high results in current consumption of $3\mu A$ for the dcdc and disables the power for the 5V rail. A mosfet was chosen for Q1 to reduce the static current consumption when the dcdc is disabled, however this can be substituted by a transistor if this is needed for radiation hardening. If the $\overline{EN}$ line is driven by a push pull source that would never float the R11 could also be omitted, since the only function of this resistor is to define the low level for the gate when the $\overline{EN}$ line is left floating. The main function for D2 is to provide an over voltage protection for the mosfet gate, however the chosen diode is a simple Z-Diode, so if a better ESD protection is needed, for example when the $\overline{EN}$ is left floating, or if this line could be susceptible to ESD then an additional TVS diode should be placed before R1.

Linear regulation

As the buck boost converter converts the VBUS voltage to 5 V, a second regulation down to 3.3 V is still needed to power the remaining components. For this regulation a linear regulator (LDO), specifically the MCP1725-3302E_MC, is used.

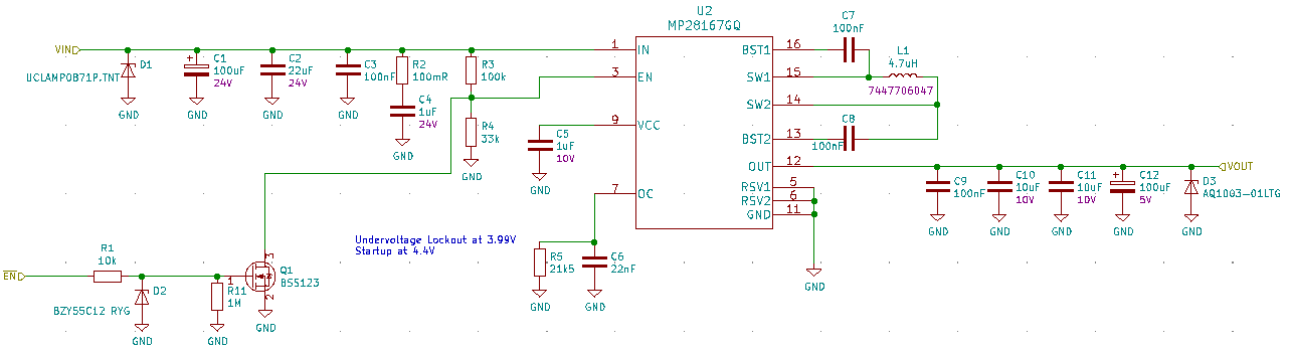


Figure 3.1: Schematic of the dcdc converter

Function description The MCP1725 is a 500 mA Low Dropout linear regulator. The MCP1725 comes in a fixed 3.3 V version and is non-adjustable. The MCP1725 is stable using ceramic output capacitors that inherently provide lower output noise and reduce the size and cost of the entire regulator solution. Only 1 µF of output capacitance is needed to stabilize the LDO. Using CMOS construction, the quiescent current consumed by the MCP1725 is typically less than 120 µA over the entire input voltage range. When shut down, the quiescent current is reduced to less than 0.1 µA. The scaled-down output voltage is internally monitored and a power good (PWRGD) output is provided when the output is within 92% of regulation (typical). An external capacitor can be used on the CDELAY pin to adjust the delay from 200 µs to 300 ms. The COBC doesnt use a capacitor at the CDELAY pin. This means that the delay is 200 µs.

Pinout The following list mentions all relevant pins and describes them briefly.

1. **Shutdown control input (SHDN)**: The SHDN input is used to turn the LDO output voltage on and off. When the SHDN input is at a high level, the LDO output voltage is enabled. When the SHDN input is pulled to a low level, the LDO output voltage is disabled. When the SHDN input is pulled low, the PWRGD output also goes low and the LDO enters a low quiescent current shutdown state where the typical quiescent current is 0.1 µA.
2. **Power good output (PWRGD)**: The PWRGD output is an open drain output used to indicate when the LDO output voltage is within 92% of its nominal regulation value. The PWRGD output is delayed by 200 µs, as no capacitance is used.
3. **Power Good Delay Set-Point Input (Cdelay**: The Cdelay input sets the power-up delay time for the PWRGD output. By connecting an external capacitor from the Cdelay pin to ground, the typical delay times for the PWRGD output can be adjusted from 200 µs (no capacitance) to 300 ms (0.1 µF capacitor).
4. **Sense**: The sense pin provides output voltage feedback to the MCP1725. The sense pin typically improves load regulation by allowing the device to compensate for voltage drops.

3.3 Memories

3.3.1 Overview

In version 1 of the COBC two separate memories are used (one FRAM and one FLASH memory). Although the final flight version will only carry one memory, two are used for evaluation purposes now. Basic specifications are listed in section 3.3.2, section 3.3.3 and in the datasheets ([12], [13]). Both

memories run on a voltage domain of 3.3 V. This was chosen as we only use 5 V or 3.3 V on the COBC section 3.2. Both memories operate as a slave device.

3.3.2 FRAM

The properties of the FRAM are listed below:

1. **Storage**: 8 Mb
2. **Frequency**: up to 40 MHz
3. **Endurance**: 1000 trillion read/write cycles
4. **Write protection**: Hardware and Software write protection
5. **Temperatur range**: 0 °C - 70 °C (commercial) and −40 °C - 85 °C (industrial)
6. **Supply voltage**: 1.8 V - 3.6 V
7. **Power consumption**: 4.62 mW at 3.3 V and 20 MHz

Pins and Communication The FRAM communicates via SPI, this means it has one active low chip select (CS) pin, one Serial Clock (SCK), one serial input pin (SI) and one serial output pin (SO). Next to these SPI specific pins it also has an active low write protect pin (WP) and power supply pins (VDD and VSS). It communicates solely with the STM section 3.1 through SPI2.

Architecture Internal the FRAM consist of 1024000 memory blocks of 8 bits each. The memory access time is essentially zero besides the time needed for the SPI. This means that the memory is written at the speed of the SPI bus.

3.3.3 Flash

The properties of the Flash are listed below:

1. **Storage**: 1 Gb
2. **Frequency**: 133 MHz
3. **Endurance**: minimum of 100k write/erase cycles
4. **Write protection**: Hardware and Software write protect
5. **Temperature range**: −40 °C - 85 °C
6. **Supply voltage**: 2.7 V - 3.6 V
7. **Power consumption**: 231 mW at 3.3 V and 70 mA during data read.

Pins and communication The Flash uses SPI to communicate with the STM section 3.1 and acts as the slave device. For the SPI connection it uses a chip select pin (CS), a data output pin (DO), a data input pin (DI) and a clock pin (CLK). Furthermore a active low hold pin exists, which (if on low) sets the DO pin to high impedance and ignores the CLK and the DI pin. There is also a write protect pin (WP), which can be used to protect the status register form being written. Through this register it is possible to either protect a section of 4 kB or the whole memory array.

Architecture The Flash is a two 512M-bit stack die that supports linear addressing for the full 1G-bit memory address range. The memory array is organized as 524.288 programmable pages of 256 bytes each. 256 bytes can be programmed at a time.

3.4 RF Communication

For communication with the GS the COBC has an Ultra high frequency (UHF) transceiver and a turnstile antenna mounted on the Z- face of the CubeSat together with a matching network.

3.4.1 UHF Transceiver

Transceiver IC

The transceiver is based on a Si4463 all-in-one frequency shift keying (FSK)/gaussian frequency shift keying (GFSK)/on-off keying (OOK) transceiver IC that does preamble detection, synchronization and demodulation in the RX path and preamble- and sync-word generation and modulation in the TX path for us. This specific IC was chosen because there are ready-built modules that enabled quick testing while already being proven to work in CubeSat missions before (the Lucky-7 CubeSat mission used this chip in their design and it is working without problems since July of 2019 and still in orbit now in April 2022).

RX Low Noise Amplifier

To further increase the RX sensitivity of the transceiver, it is paired with a 20dB low noise amplifier (LNA). This design was already used by the communication module designed by the Librespace foundation and is also known to work flawlessly (based around the TQP3M9036 fully integrated LNA IC). As another European CubeSat student team told us, we have to expect a lot of noise from radar systems in the UHF band while over Europe so we'll probably add a method to bypass the LNA in case it is clipping. This would allow us to still reach the CubeSat by increasing transmit power on the ground station in case of enough noise to drive the LNA into clipping. In case the LNA bypass is necessary, a logarithmic detector will be added in between the input band pass filter and LNA so the COBC microcontroller can decide wether to enable or to bypass the LNA based on the input signal level.

TX High Power Amplifier

To get more output power than the 100mW provided by the Si4463, a Power amplifier (PA) based on the TQP7M9106 monolithic 2W RF amplifier chip will be used. The Oresat0 uses the "smaller brother" TQP7M9105 with only 1W of output power. To give us the possibility of a higher downlink data rate we opted for the 2W version instead.

Filters and RX/TX Switching

On the input side, a discrete 3rd order band pass filter is used to reduce the chance of clipping the LNA with noise, while on the output side an integrated (LFCG-490+) low pass filter is used to reduce the harmonics of the PA. These filter architectures were chosen as they are proven to work well with similar RF systems in other CubeSat missions and both filters are simple and small. For RX/TX switching, an integrated low-loss, solid-state RF switch (QPC1022) is used as it also is known to work in space (in Oresat0) and does everything we require in a small package. The same switch will probably be used for the LNA bypass.

3.4.2 Antenna

The antenna is mounted to the Z- faceplate of the CubeSat which simultaneously serves as the PCB for the matching network. This allows for a mechanically rigid solution while still saving space compared to a separate PCB in the CubeSat stack up for antenna matching. The antenna will be deployed through the EPS, which will heat up some resistors which then burn through the wire. The whole mechanism is kicked off by the COBC via the "EPS_ANT_DEPLOY" Pin on the CSBI section 2.2. The COBC PCB is located just above the antenna PCB.

3.4.3 Antenna Design

The antenna is a simple turnstile type UHF antenna. Mechanically it is made from spring steel to allow easy automatic deployement. The length of the antenna elements will be around $\frac{\lambda}{4}$ (and the necessary shortening factor for steel). If the mechanical design (specifically the antenna deployement) allows for it, $\frac{\lambda}{2}$ element length will also be simulated and tested to see if it is advantageous (because it would provide more gain) or not (because it will make the antenna pattern less isotropic). As some sources suggested coating the antenna with either copper or silver to improve their electrical characteristics, this is also something we'd like to test if there is enough time during testing. Antennas made from spring steel without coating are working well (see Oresat0 or Lucky-7) so it certainly isn't a requirement but some commercial antennas seem to be coated (as pictures look more silvery or coppery than would be expected from spring steel) so it's something we'd like to explore.

Antenna Matching

Antenna matching is using a simple phase shift matching network based on mini-circuits QBA-07+ 90° hybrid coupler IC. This design has been proven to work in Oresat0, which is why the matching network will be built to be as close as possible to their design. The antenna matching network will be on the side panel PCB that mounts the antenna to the CubeSat.

4 Behaviour

The COBC shall continuously operate as long as enough power is provided by the EPS. It is the main master on the CubeSat and manages all memory access operations as well as enables or disables the payload. The STM is responsible to handle all dataflow happening on the CubeSat. At moment (17.05.2023) the RF circuit is under investigation and will be discussed in the upcoming reviews, i.e. communication review and CDR of the COBC HW. Importantly, also the memory assignment of FRAM and Flash will be discussed in up-coming reviews, i.e. COBC HW as well as COBC SW reviews.

As the COBC HW merely consists of single blocks and any logic involved is implemented within the COBC SW no further behaviour details will be given here.

5 Discussion

During the PDR several major points were addressed by the reviewers:

1. **External Watchdog**: The external watchdog can and shall be used to protect against Universal asynchronous receiver-transmitter (UART) latchups. UART is vulnerable to latchups where the only way to solve them is a power cycle of the complete system. The external watchdog shall be used to power cycle the whole COBC system, meaning that it also shall be used to power cycle the external memories. The trigger time of the external watchdog shall be set higher than 24 h, to have the possibility to communicate with the CubeSat.
2. **External memory**: MRAM is more radiation tolerant than FRAM. The size of the memory shall be chosen according to the size of the data we can transmit, for example, if we can transmit 1 MiB of data every day we have no use case for a 1000 MiB FRAM.
3. **Latchup protection version**: Latchup protection shall be implemented on at least one version prior to the flight HW.
4. **Ground Support Equipment**: The Ground support equipment (GSE) shall be able to evaluate the SW on the COBC. This means that the GSE shall be able to evaluate the integrity and functionality of the COBC SW.
5. **Real-time**: It is hard to maintain real-time on a CubeSat. Do not have system critical operations linked to specific real-times.
6. **Test driven development**: It is mentioned that when we design HW we should first and foremost think about how we can test that HW. This is also true when it comes to possible error states of the microcontroller, it must be possible to test those error states. Here close cooperation with the COBC SW development is needed.
7. **RF interfaces**: It is mentioned that the used RF interfaces by STS1 shall be compliant with the used amateur radio band.

Finally, the following requirement issues were discussed:

- The subsystem requirements resulting from STS1 System Architecture Requirement 11.1.[1] will be removed.
- The requirements shall include a verification methodology. This can be something like ”verified by design” or ”verified by testing”

The next document that will describe the COBC will be the COBC CDR. This document will have all the points discussed with the reviewers implemented.

Bibliography

[1] Raphael Böckle et al. *SpaceTeamSat1 Preliminary Design Document: System Architecture*. Version 4.2. Apr. 2023. DOI: 10.5281/zenodo.7791608. URL: https://doi.org/10.5281/zenodo.7791608.

[2] Raphael Behrle et al. *SpaceTeamSat1 Dataflow Game Document*. Version 1.1. Apr. 2023. DOI: 10.5281/zenodo.7791595. URL: https://doi.org/10.5281/zenodo.7791595.

[3] David Freismuth and David Wagner. *SpaceTeamSat1 Preliminary Design Document: Electric Power System*. Version 0.2. Apr. 2023. DOI: 10.5281/zenodo.7791655. URL: https://doi.org/10.5281/zenodo.7791655.

[4] *Fly Your Satellite! Design SpecificationVersion 3.0*.

[5] *CubeSat Design Specification Rev. 12*. Tech. rep. Cal Poly - San Luis Obispo, 2009.

[6] *ESA: Fly Your Satellite! programme*. URL: https://www.esa.int/Education/CubeSats_-_Fly_Your_Satellite/Fly_Your_Satellite!_programme (visited on 24/09/2020).

[7] David Freismuth. *SpaceTeamSat1 Preliminary Requirements Document: Electric Power System*. Version 1.2. Apr. 2023. DOI: 10.5281/zenodo.7791676. URL: https://doi.org/10.5281/zenodo.7791676.

[8] *OreSat communication board*. URL: https://github.com/oresat/oresat-c3 (visited on 16/01/2023).

[9] *SatNogs COMMS board by Libre Space Foundation*. URL: https://gitlab.com/librespacefoundation/satnogs-comms/satnogs-comms-hardware (visited on 16/01/2023).

[10] *STM32F411xC STM32F411xE*. Datasheet. Rev. 7. STMicroelectronics. 2017. URL: https://www.st.com/resource/en/datasheet/stm32f411re.pdf (visited on 13/05/2022).

[11] STMicroelectronics. *Using the hardware real-time clock (RTC) and the tamper management unit (TAMP) with STM32 microcontrollers*. Ed. by STMicroelectronics. Application Note. 2021. URL: https://www.st.com/resource/en/application_note/an4759-using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-microcontrollers-stmicroelectronics.pdf (visited on 15/05/2022).

[12] Infineon Technologies AG. *8Mb EXCELON™ LP Ferroelectric RAM*. Ed. by Infineon Technologies AG. Datasheet. 1st Feb. 2022. URL: https://www.infineon.com/dgdl/Infineon-CY15B108QN_CY15V108QN_Excelon(TM)_LP_8-Mbit_(1024K_X_8)_Serial_(SPI)_F-RAM-DataSheet-v10_00-EN.pdf?fileId=8ac78c8c7d0d8da4017d0ee7134b6ff4 (visited on 21/05/2022).

[13] Winbond Electronics Corporation. *3V 1G-BIT (DUAL DIE) SERIAL FLASH MEMORY WITH DUAL/QUAD SPI*. Ed. by Winbond Electronics Corporation. Datasheet. URL: https://www.mouser.at/datasheet/2/949/W25Q01JV_SPI_RevB_11132019-1760416.pdf (visited on 21/05/2022).