

HFSS 3D Layout - IHP Technology Layer Stackup Definition

EM Simulation Setup Reference

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1 Material Properties

1.1 Conductor Materials

Material Name	Conductivity (S/m)	Permit.	Color
Activ	3.57141e5	1	00ff00
Metal1	2.164e7	1	39bfff
Metal2	2.319e7	1	ccccd9
Metal3	2.319e7	1	d80000
Metal4	2.319e7	1	93e837
Metal5	2.319e7	1	dcd146
TopMetal1	2.78e7	1	ffe6bf
TopMetal2	3.03e7	1	ff8000
TopVia2	3.143e6	1	ff8000
TopVia1	2.191e6	1	ffe6bf
Via4	1.66e6	1	deac5e
Via3	1.66e6	1	9ba940
Via2	1.66e6	1	ff3736
Via1	1.66e6	1	ccccff
Cont	2.39e6	1	00ffff
LOWLOSS	1e10	1	ff0000

1.2 Dielectric Materials

Material	Permit.	Loss Tan.	Cond.	Color
Passive	6.6	0.0	0	a0a0f0
SiO2	4.1	0.0	0	fffcad
AIR	1.0	0.0	0	d0d0d0
MIM_equiv	16.87	0.0	0	ff0000

1.3 Semiconductor Materials

Material	Permit.	Loss Tan.	Cond. (S/m)	Color
Substrate	11.9	0	2.0	01e0ff
EPI	11.9	0	5.0	294fff

2 Complete Layer Stackup (Bottom to Top)

Important Setup Parameters:

- **Substrate Offset:** 283.75 μm
- **Length Unit:** Micrometers (μm)
- **Layer Type:** Use “signal” for all conductor/via layers, “dielectric” for dielectric layers

#	Layer Name	Type	Zmin	Zmax	Thick.	Material	L#
SUBSTRATE REGION							
1	Substrate	dielectric	-283.75	-3.75	280.00	Substrate	-
2	SUBGND	signal	-283.75	-283.75	0.00	LOWLOSS	210
3	EPI	dielectric	-3.75	0.00	3.75	EPI	-
ACTIVE & INTERCONNECT REGION							
4	Activ	signal	0.00	0.40	0.40	Activ (3.57e5)	1
5	Passive fill	dielectric	0.40	1.04	0.64	Passive	-
6	Cont	signal	0.40	1.04	0.64	Cont (2.39e6)	6
METAL1 LAYER							
7	SiO2 fill	dielectric	1.04	1.46	0.42	SiO2	-
8	Metal1	signal	1.04	1.46	0.42	Metal1 (2.164e7)	8
9	SiO2 fill	dielectric	1.46	2.00	0.54	SiO2	-
10	Via1	signal	1.46	2.00	0.54	Via1 (1.66e6)	19
METAL2 LAYER							
11	SiO2 fill	dielectric	2.00	2.49	0.49	SiO2	-
12	Metal2	signal	2.00	2.49	0.49	Metal2 (2.319e7)	10
13	SiO2 fill	dielectric	2.49	3.03	0.54	SiO2	-
14	Via2	signal	2.49	3.03	0.54	Via2 (1.66e6)	29
METAL3 LAYER							
15	SiO2 fill	dielectric	3.03	3.52	0.49	SiO2	-
16	Metal3	signal	3.03	3.52	0.49	Metal3 (2.319e7)	30
17	SiO2 fill	dielectric	3.52	4.06	0.54	SiO2	-
18	Via3	signal	3.52	4.06	0.54	Via3 (1.66e6)	49
METAL4 LAYER							
19	SiO2 fill	dielectric	4.06	4.55	0.49	SiO2	-

#	Layer Name	Type	Zmin	Zmax	Thick.	Material	L#
20	Metal4	signal	4.06	4.55	0.49	Metal4 (2.319e7)	50
21	SiO2 fill	dielectric	4.55	5.09	0.54	SiO2	-
22	Via4	signal	4.55	5.09	0.54	Via4 (1.66e6)	66
METAL5 & MIM LAYERS							
23	SiO2 fill	dielectric	5.09	5.58	0.49	SiO2	-
24	Metal5	signal	5.09	5.58	0.49	Metal5 (2.319e7)	67
25	MIM_DK	dielectric	5.58	5.68	0.10	MIM_equiv	136
26	MIM	signal	5.68	5.78	0.10	Metal5 (2.319e7)	137
27	SiO2 fill	dielectric	5.58	6.43	0.85	SiO2	-
28	TopVia1	signal	5.58	6.43	0.85	TopVia1 (2.191e6)	125
TOPMETAL1 LAYER							
29	SiO2 fill	dielectric	6.43	8.43	2.00	SiO2	-
30	TopMetal1	signal	6.43	8.43	2.00	TopMetal1 (2.78e7)	126
31	SiO2 fill	dielectric	8.43	11.23	2.80	SiO2	-
32	TopVia2	signal	8.43	11.23	2.80	TopVia2 (3.143e6)	133
TOPMETAL2 LAYER (TOP)							
33	SiO2 fill	dielectric	11.23	14.23	3.00	SiO2	-
34	TopMetal2	signal	11.23	14.23	3.00	TopMetal2 (3.03e7)	134
35	AIR	dielectric	14.23	314.23	300.00	AIR	-

Table 4: Complete unified stackup with conductors and dielectric fillers (all dimensions in μm)

3 Manual Entry Steps in HFSS 3D Layout

3.1 Material Properties Quick Reference

- **Conductors:** Activ (3.57e5), Metal1 (2.164e7), Metal2-5 (2.319e7), TopMetal1 (2.78e7), TopMetal2 (3.03e7), Cont (2.39e6), Via1-4 (1.66e6), TopVia1 (2.191e6), TopVia2 (3.143e6), LOWLOSS (1e10)
- **Dielectrics:** SiO2 ($\epsilon_r=4.1$), Passive ($\epsilon_r=6.6$), AIR ($\epsilon_r=1.0$), MIM_equiv ($\epsilon_r=16.87$)
- **Semiconductors:** Substrate ($\epsilon_r=11.9$, $\sigma=2.0$), EPI ($\epsilon_r=11.9$, $\sigma=5.0$)

3.2 Stackup Entry Procedure

1. Create all materials first using the tables above
2. In Layer Stackup Manager, set Substrate Offset = 283.75 μm
3. Enter layers from bottom to top following the unified stackup table
4. For conductor layers: Enter Name, Type=signal, Zmin, Zmax, Material, Layer#
5. For dielectric fill: Enter Name, Type=dielectric, Zmin, Zmax, Material (no Layer# needed)
6. **Note:** Dielectric fills represent the insulating material between and around conductors