Laboratory Report

Course: Coen 316

Lab Section: DL-X

Experiment No: 1

Date Performed: 2023 – 09 – 21

Report Due Date: 2023 – 10 – 05

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I certify that this submission is my original work and meets the Faculty's Expectations of Originality

Signature:

Date: 2023 – 10 – 05

Objectives

The objective of this laboratory experiment is to design a 32-bit Arithmetic Logic Unit (ALU) using VHDL (VHSIC Hardware Description Language). The ALU is a fundamental component of the CPU, and its purpose is to perform various arithmetic and logical operations on two 32-bit input operands (denoted as x and y). The ALU will be capable of executing addition, subtraction, AND, OR, XOR, and NOR operations based on control inputs provided by func, logic_func, and add_sub. Specifically, func determines the type of operation to be performed (load upper immediate, set less than zero, arithmetic, or logic), logic_func specifies the logical operation (AND, OR, XOR, NOR), and add_sub selects between addition and subtraction.

The ALU will be implemented as a VHDL component, utilizing the given entity specification, which defines the input and output ports, as well as the control signals necessary for the ALU operations. In addition, overflow and zero results are displayed as outputs.

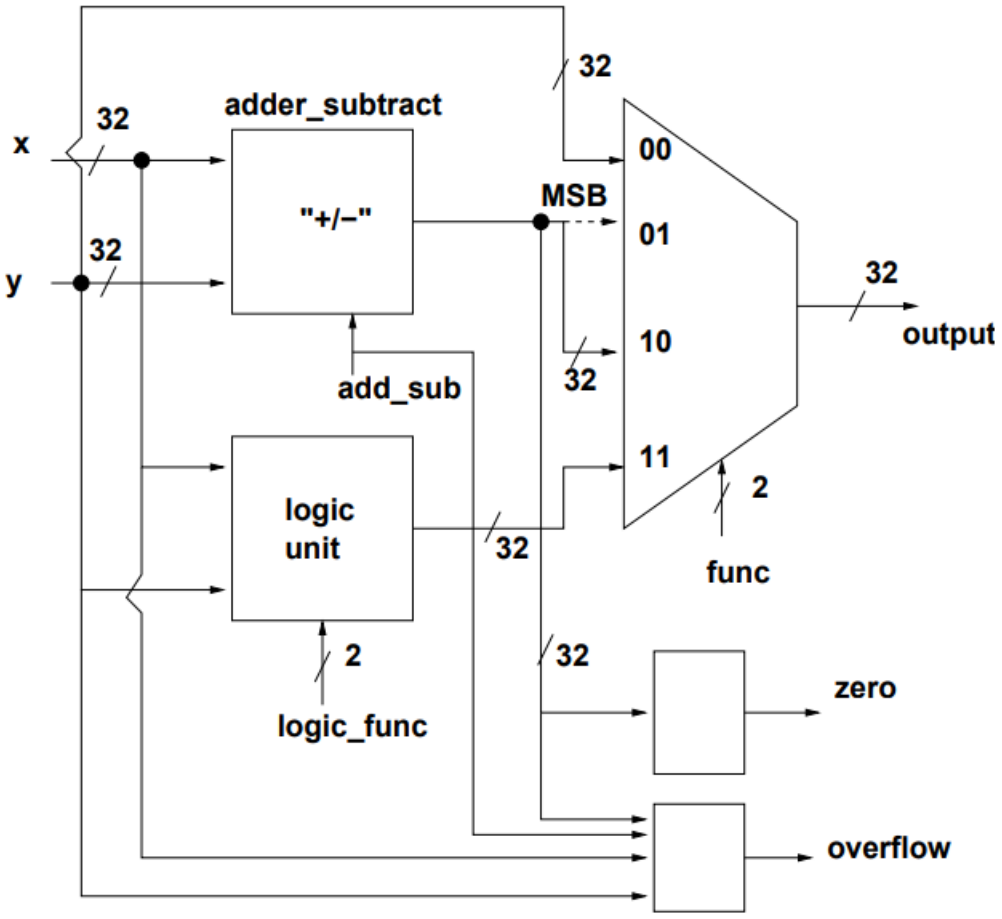

Figure 1: ALU block diagram

Once the simulations are done using the 32-bit source code, it is necessary to do a “board version” as the board only supports 4 bits.

Results

In this part I’ll be showing the results of the conducted lab with screenshots at every step.

32-bit source code:

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_signed.all;

entity alu is
port(x, y : in std_logic_vector(31 downto 0); -- two input
 add_sub : in std_logic;
 logic_func : in std_logic_vector(1 downto 0);
 func : in std_logic_vector(1 downto 0);
 output_out : out std_logic_vector(31 downto 0);
 overflow : out std_logic;
 zero : out std_logic);
end alu ;

architecture ALU_arch of alu is


signal out_add, out_func : std_logic_vector(31 downto 0);

begin

--x(3 downto 0) <= x_in(3) & x_in(2) & x_in(1) & x_in(0);
--y(3 downto 0) <= y_in(3) & y_in(2) & y_in(1) & y_in(0);
--x(31 downto 4) <= (others => '0');
--y(31 downto 4) <= (others => '0');

--add-sub
-------------------------------------------------------------
add_overflow_process:process(add_sub,x,y) --inputs

begin

if (add_sub = '0') then --addition -> (x+y)
out_add <= x+y;
 --if (x(31) = y(31) AND out_add(31) /= y(31)) then -- overflow check (MSB)
 -- overflow <= '1';
 --else
 -- overflow <= '0';
 --end if;


elsif (add_sub = '1') then --substraction
out_add <= x-y;
 --if (x(31) /= y(31) AND out_add(31) /= x(31)) then -- overflow check
 -- overflow <= '1';
 --else
 -- overflow <= '0';
 --end if;

end if;
end process;

--if (x(31) = y(31) & out_add(31) /= y(31)) then -- overflow check (MSB)
--  overflow <= '1';
-- else
```

```
--  overflow <= '0';
-- end if;

--if (x(31) /= y(31) & out_add(31) /= x(31)) then -- overflow check
--  overflow <= '1';
-- else
--  overflow <= '0';
-- end if;

-----------------------------------------------------logic_func
logic_func_process:process(logic_func,x,y)

begin

if (logic_func = "00") then
out_func <= x AND y;

elsif (logic_func = "01") then
out_func <= x OR y;

elsif (logic_func = "10") then
out_func <= x XOR y;

elsif (logic_func = "11") then
out_func <= x NOR y;

end if;

---ERROR
--out_func <= x AND y when (logic_func = "00") else
--     x OR y  when (logic_func = "01") else
--     x XOR y when (logic_func = "10") else
--     x NOR y;

-- can do select

end process;
-----------------------------------------------------

zero_process:process(out_add)

begin

if (out_add = "00000000000000000000000000000000") then
zero <= '1';

else
zero <= '0';

end if;
end process;

-----------------------------------------------------
overflow_process:process(add_sub,x,y,out_add)
```

```
begin

if (add_sub = '0') then --from k-map

 overflow <= (not x(31) AND not y(31) and out_add(31)) or (x(31) AND y(31) and not out_add(31));


else

 overflow <= (x(31) AND not y(31) and not out_add(31)) or (not x(31) AND y(31) AND out_add(31));


end if;
end process;

-------------------------------------------------------

multiplexer_process:process(out_add,y,out_func,func)

begin

--case func is

-- when "00" =>
--  output_out <= y;

-- when "01" =>
--  output_out <= out_add(31) & "00000000000000000000000000000000";

-- when "10" =>
--  output_out <= out_add;

-- when "11" =>
--  output_out <= out_func;

--end case;

 if (func = "00")then
  output_out <= y;
 elsif (func = "01")then
  output_out <= out_add(31) & "00000000000000000000000000000000";
 elsif (func = "10")then
  output_out <= out_add;
 else
  output_out <= out_func;

end if;


end process;

end ALU_arch;
```

Figure 2: ALU.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_signed.all;

entity alu is
port(x_in, y_in : in std_logic_vector(3 downto 0); -- two input
 add_sub : in std_logic;
 logic_func : in std_logic_vector(1 downto 0);
 func : in std_logic_vector(1 downto 0);
 output_out : out std_logic_vector(3 downto 0);
 overflow : out std_logic;
 zero : out std_logic);
end alu ;

architecture ALU_arch of alu is


signal x,y,out_add, out_func, out_signal : std_logic_vector(31 downto 0);

begin

x(3 downto 0) <= x_in(3) & x_in(2) & x_in(1) & x_in(0);
y(3 downto 0) <= y_in(3) & y_in(2) & y_in(1) & y_in(0);
x(31 downto 4) <= (others => '0');
y(31 downto 4) <= (others => '0');
output_out(3 downto 0) <= out_signal(3 downto 0); -- taking last 4 bits of 32 bits

--add-sub
------------------------------------------------------------------
add_overflow_process:process(add_sub,x,y) --inputs

begin

if (add_sub = '0') then --addition -> (x+y)
out_add <= x+y;
 --if (x(31) = y(31) AND out_add(31) /= y(31)) then -- overflow check (MSB)
 -- overflow <= '1';
 --else
 -- overflow <= '0';
 --end if;


elsif (add_sub = '1') then --substraction
out_add <= x-y;
 --if (x(31) /= y(31) AND out_add(31) /= x(31)) then -- overflow check
 -- overflow <= '1';
 --else
 -- overflow <= '0';
 --end if;

end if;
end process;

--if (x(31) = y(31) & out_add(31) /= y(31)) then -- overflow check (MSB)
--  overflow <= '1';
```

```
-- else
--  overflow <= '0';
-- end if;

--if (x(31) /= y(31) & out_add(31) /= x(31)) then -- overflow check
--  overflow <= '1';
-- else
--  overflow <= '0';
-- end if;

------------------------------------------------------------logic_func
logic_func_process:process(logic_func,x,y)

begin

if (logic_func = "00") then
out_func <= x AND y;

elsif (logic_func = "01") then
out_func <= x OR y;

elsif (logic_func = "10") then
out_func <= x XOR y;

elsif (logic_func = "11") then
out_func <= x NOR y;

end if;

---ERROR
--out_func <= x AND y when (logic_func = "00") else
--     x OR y  when (logic_func = "01") else
--     x XOR y when (logic_func = "10") else
--     x NOR y;

-- can do select

end process;
------------------------------------------------------------

zero_process:process(out_add)

begin

if (out_add = "00000000000000000000000000000000") then
zero <= '1';

else
zero <= '0';

end if;
end process;

-----------------------------------------------------
overflow_process:process(add_sub,x,y,out_add)
```

```
begin

If (add_sub = '0') then --from k-map

 overflow <= (not x(31) AND not y(31) and out_add(31)) or (x(31) AND y(31) and not out_add(31));


else

 overflow <= (x(31) AND not y(31) and not out_add(31)) or (not x(31) AND y(31) AND out_add(31));


end if;
end process;

-------------------------------------------------------

multiplexer_process:process(out_add,y,out_func,func)

begin

--case func is

-- when "00" =>
--  output_out <= y;

-- when "01" =>
--  output_out <= out_add(31) & "00000000000000000000000000000000";

-- when "10" =>
--  output_out <= out_add;

-- when "11" =>
--  output_out <= out_func;

--end case;

 if (func = "00")then
  out_signal <= y;
 elsif (func = "01")then
  out_signal <= out_add(31) & "00000000000000000000000000000000";
 elsif (func = "10")then
  out_signal <= out_add;
 else
  out_signal <= out_func;

end if;


end process;


end ALU_arch;
```

Figure 3: Board wrapper (4-bit version)

```
set_property -dict { PACKAGE_PIN J15   IOSTANDARD LVCMOS33 } [get_ports { x_in[3] }]; #IO_L24N_T3_RS0_15 Sch=sw[0]

set_property -dict { PACKAGE_PIN L16   IOSTANDARD LVCMOS33 } [get_ports { x_in[2] }]; #IO_L3N_T0_DQS_EMCCLK_14 Sch=sw[1]

set_property -dict { PACKAGE_PIN M13   IOSTANDARD LVCMOS33 } [get_ports { x_in[1] }]; #IO_L6N_T0_D08_VREF_14 Sch=sw[2]

set_property -dict { PACKAGE_PIN R15   IOSTANDARD LVCMOS33 } [get_ports { x_in[0] }]; #IO_L13N_T2_MRCC_14 Sch=sw[3]

set_property -dict { PACKAGE_PIN R17   IOSTANDARD LVCMOS33 } [get_ports { y_in[3] }]; #IO_L12N_T1_MRCC_14 Sch=sw[4]

set_property -dict { PACKAGE_PIN T18   IOSTANDARD LVCMOS33 } [get_ports { y_in[2] }]; #IO_L7N_T1_D10_14 Sch=sw[5]

set_property -dict { PACKAGE_PIN U18   IOSTANDARD LVCMOS33 } [get_ports { y_in[1] }]; #IO_L17N_T2_A13_D29_14 Sch=sw[6]

set_property -dict { PACKAGE_PIN R13   IOSTANDARD LVCMOS33 } [get_ports { y_in[0] }]; #IO_L5N_T0_D07_14 Sch=sw[7]

set_property -dict { PACKAGE_PIN T8    IOSTANDARD LVCMOS18 } [get_ports { add_sub }]; #IO_L24N_T3_34 Sch=sw[8]

set_property -dict { PACKAGE_PIN U8   IOSTANDARD LVCMOS18 } [get_ports { logic_func[1] }]; #IO_25_34 Sch=sw[9]

set_property -dict { PACKAGE_PIN R16  IOSTANDARD LVCMOS33 } [get_ports { logic_func[0] }]; #IO_L15P_T2_DQS_RDWR_B_14 Sch=sw[10]

set_property -dict { PACKAGE_PIN T13   IOSTANDARD LVCMOS33 } [get_ports { func[1] }]; #IO_L23P_T3_A03_D19_14 Sch=sw[11]

set_property -dict { PACKAGE_PIN H6   IOSTANDARD LVCMOS33 } [get_ports { func[0] }]; #IO_L24P_T3_35 Sch=sw[12]

#output LED in order

set_property -dict { PACKAGE_PIN H17   IOSTANDARD LVCMOS33 } [get_ports { output_out[3] }]; #IO_L18P_T2_A24_15 Sch=led[0]

set_property -dict { PACKAGE_PIN K15   IOSTANDARD LVCMOS33 } [get_ports { output_out[2] }]; #IO_L24P_T3_RS1_15 Sch=led[1]
```

```
set_property -dict { PACKAGE_PIN J13   IOSTANDARD LVCMOS33 } [get_ports { output_out[1] }];
#IO_L17N_T2_A25_15 Sch=led[2]

set_property -dict { PACKAGE_PIN N14   IOSTANDARD LVCMOS33 } [get_ports { output_out[0]
}]; #IO_L8P_T1_D11_14 Sch=led[3]

set_property -dict { PACKAGE_PIN R18   IOSTANDARD LVCMOS33 } [get_ports { overflow }];
#IO_L7P_T1_D09_14 Sch=led[4]

set_property -dict { PACKAGE_PIN V17   IOSTANDARD LVCMOS33 } [get_ports { zero }];
#IO_L18N_T2_A11_D27_14 Sch=led[5]
```

Figure 3: Contraints file .xdc for converter FPGA implementation

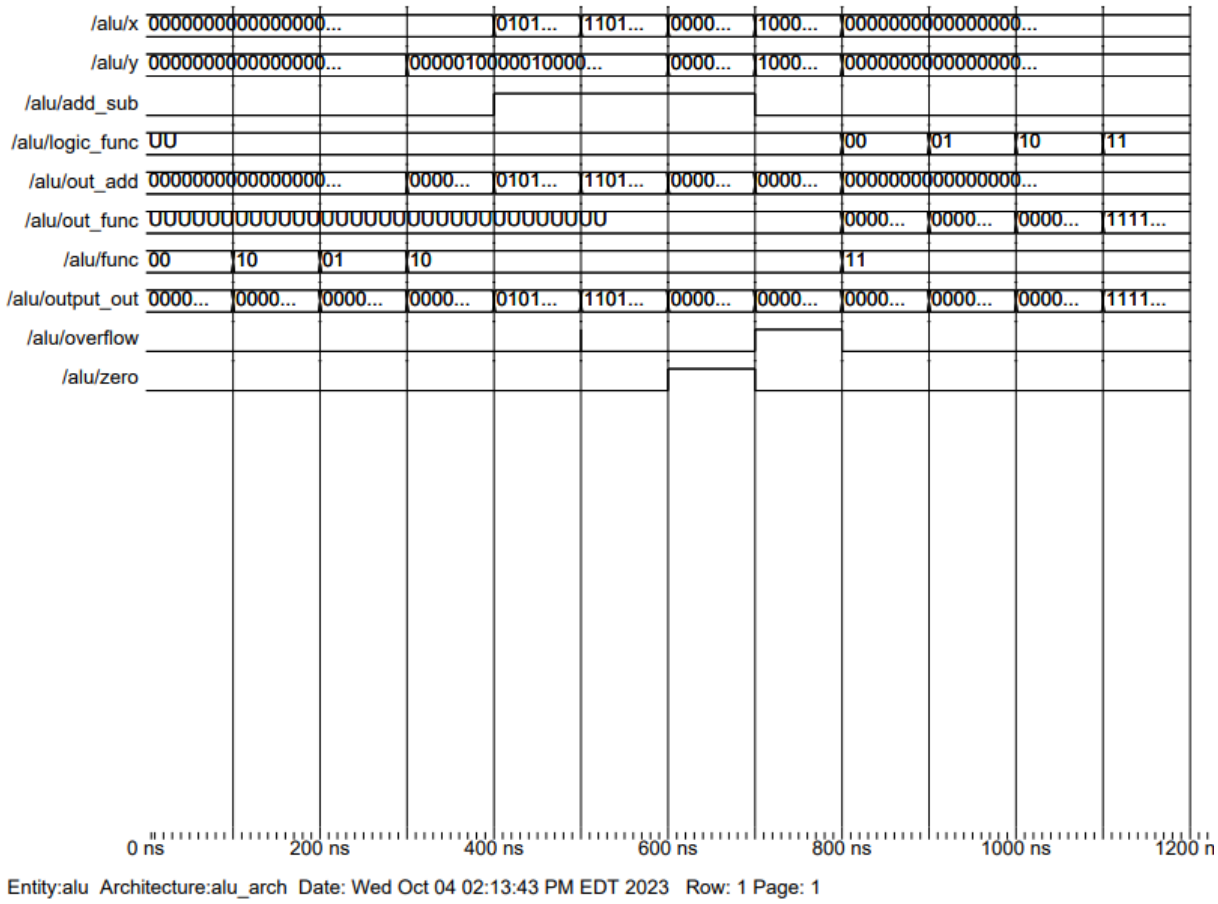

Figure 4: modelsim waveform

add wave x

add wave y

add wave add_sub

add wave logic_func

add wave out_ad

add wave out_func

add wave func

add wave output_out

add wave overflow

add wave zero

force x 00000000000000000000000000001101

force y 00000000000000000000000000001001

force add_sub 0

force func 00

run 100

force func 10

run 100

force func 01

run 100

force x 00000000000000000000000000001101

force y 00000100000100000010001000100001

force add_sub 0

force func 10

run 100

force x 01011111101111011111110111111110

force y 00000100000100000010001000100001

force add_sub 1

force func 10

run 100

force x 11011111101111011111110111111110

force y 00000100000100000010001000100001

force add_sub 1

force func 10

run 100

force x 00000000000000000000000000001101

force y 00000000000000000000000000001101

force add_sub 1

force func 10

run 100

force x 10000001000000000000000000001101

force y 10000000000000010000000000001101

force add_sub 0

force func 10

run 100

force x 00000000000000000000000000001101

force y 00000000000000000000000000001001

force logic_func 00

force func 11

run 100

force x 00000000000000000000000000001101

force y 00000000000000000000000000001001

force logic_func 01

force func 11

run 100

force x 00000000000000000000000000001101

force y 00000000000000000000000000001001

force logic_func 10

force func 11

run 100

force x 00000000000000000000000000001101

force y 00000000000000000000000000001001

force logic_func 11

force func 11

run 100

Figure 5: DO file

Vivado logs can be found in the appendix section.

Discussion

Concerning the overflow detection, it is important to mention that I used the truth table for the addition and subtraction and then minimized it using a k-map and fund the resulting equation.

I performed 12 cycles for my modelsim using the above DO file.

1st cycle: func is set to 00 to make sure that the multiplexer output is the y value

2nd cycle: the multiplexer outputs the result of the addition of x and y

3rd cycle: using same values, we output the most significant bit of the addition of x and y

4th cycle: check another addition for a different y value and output the result

5th cycle: check the subtraction and output the result

6th cycle: check the subtraction and output the result

7th cycle: check the zero-output using subtraction of same numbers

8th cycle: check the overflow using the addition of large numbers

9th cycle: check the AND

10th cycle: check the OR

11th cycle: check the XOR

12th cycle: check the NOR

Conclusion

To conclude, we successfully created a 32-bit Arithmetic Logic Unit (ALU) using VHDL. By carefully configuring control inputs like func, logic_func, and add_sub, we enabled the ALU to handle a range of operations, from basic addition and subtraction to complex logical functions such as AND, OR, XOR and NOR.

This practical exercise immersed us in VHDL intricacies and allowed us to deepen our grasp of digital logic and computer architecture fundamentals. Overcoming challenges related to two's complement arithmetic and overflow detection enhanced our problem-solving skills in digital design.

Appendix

Vivado Synthesis

```
*** Running vivado
    with args -log alu.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -
source alu.tcl


****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source alu.tcl -notrace
Command: synth_design -top alu -part xc7a100tcsg324-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 16157
---------------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak =
1401.582 ; gain = 85.801 ; free physical = 10582 ; free virtual = 22314
---------------------------------------------------------------------------------
INFO: [Synth 8-638] synthesizing module 'alu'
[/nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/ALU_board.vhd:15]
WARNING: [Synth 8-3936] Found unconnected internal register 'out_signal_reg' and it is
trimmed from '32' to '4' bits.
[/nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/ALU_board.vhd:26]
INFO: [Synth 8-256] done synthesizing module 'alu' (1#1)
[/nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/ALU_board.vhd:15]
---------------------------------------------------------------------------------
Finished RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:03 . Memory (MB): peak
= 1446.223 ; gain = 130.441 ; free physical = 10579 ; free virtual = 22312
---------------------------------------------------------------------------------

Report Check Netlist:
+------+-----------------+-------+---------+-------+------------------+
|      |Item             |Errors |Warnings |Status |Description       |
+------+-----------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+-----------------+-------+---------+-------+------------------+
```

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1446.223 ; gain = 130.441 ; free physical = 10579 ; free virtual = 22312

Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1446.223 ; gain = 130.441 ; free physical = 10579 ; free virtual = 22312

INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [/nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/vivado/lab1_316/lab1_316.srcs/constrs_1/imports/DO/lab1_constraints.xdc]
Finished Parsing XDC File [/nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/vivado/lab1_316/lab1_316.srcs/constrs_1/imports/DO/lab1_constraints.xdc]
INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [/nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/vivado/lab1_316/lab1_316.srcs/constrs_1/imports/DO/lab1_constraints.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/alu_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in [.Xil/alu_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 1810.492 ; gain = 0.000 ; free physical = 10296 ; free virtual = 22029

Finished Constraint Validation : Time (s): cpu = 00:00:07 ; elapsed = 00:00:19 . Memory (MB): peak = 1810.492 ; gain = 494.711 ; free physical = 10386 ; free virtual = 22119

Start Loading Part and Timing Information

Loading part: xc7a100tcsg324-1

Finished Loading Part and Timing Information : Time (s): cpu = 00:00:07 ; elapsed = 00:00:19 .

```
Memory (MB): peak = 1810.492 ; gain = 494.711 ; free physical = 10386 ; free virtual = 22119
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Applying 'set_property' XDC Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:07 ; elapsed =
00:00:19 . Memory (MB): peak = 1810.492 ; gain = 494.711 ; free physical = 10388 ; free virtual
= 22121
---------------------------------------------------------------------------------
INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent
sharing consider applying a KEEP on the output of the operator
[/nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/ALU_board.vhd:34]
WARNING: [Synth 8-3936] Found unconnected internal register 'out_func_reg' and it is trimmed
from '32' to '4' bits. [/nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/ALU_board.vhd:72]
WARNING: [Synth 8-327] inferring latch for variable 'out_func_reg'
[/nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/ALU_board.vhd:72]
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:07 ; elapsed = 00:00:19 . Memory
(MB): peak = 1810.492 ; gain = 494.711 ; free physical = 10379 ; free virtual = 22113
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Adders :
  3 Input     32 Bit       Adders := 1
+---XORs :
  2 Input      4 Bit         XORs := 1
+---Muxes :
  2 Input     32 Bit         Muxes := 1
  4 Input      4 Bit         Muxes := 2
  2 Input      1 Bit         Muxes := 1
  4 Input      1 Bit         Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
Hierarchical RTL Component report
```

```
Module alu
Detailed RTL Component Info :
+---Adders :
  3 Input     32 Bit       Adders := 1
+---XORs :
  2 Input      4 Bit         XORs := 1
+---Muxes :
  2 Input     32 Bit        Muxes := 1
  4 Input      4 Bit        Muxes := 2
  2 Input      1 Bit        Muxes := 1
  4 Input      1 Bit        Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 240 (col length:80)
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Cross Boundary and Area Optimization
---------------------------------------------------------------------------------
Warning: Parallel synthesis criteria is not met
WARNING: [Synth 8-3332] Sequential element (out_func_reg[3]) is unused and will be removed
from module alu.
WARNING: [Synth 8-3332] Sequential element (out_func_reg[2]) is unused and will be removed
from module alu.
WARNING: [Synth 8-3332] Sequential element (out_func_reg[1]) is unused and will be removed
from module alu.
WARNING: [Synth 8-3332] Sequential element (out_func_reg[0]) is unused and will be removed
from module alu.
---------------------------------------------------------------------------------
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:08 ; elapsed = 00:00:20
. Memory (MB): peak = 1810.492 ; gain = 494.711 ; free physical = 10367 ; free virtual = 22102
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Applying XDC Timing Constraints
```


Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:11 ; elapsed = 00:00:25 . Memory (MB): peak = 1810.492 ; gain = 494.711 ; free physical = 10246 ; free virtual = 21981

Start Timing Optimization

Finished Timing Optimization : Time (s): cpu = 00:00:11 ; elapsed = 00:00:25 . Memory (MB): peak = 1810.492 ; gain = 494.711 ; free physical = 10246 ; free virtual = 21981

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+

Start Technology Mapping

Finished Technology Mapping : Time (s): cpu = 00:00:11 ; elapsed = 00:00:25 . Memory (MB): peak = 1810.492 ; gain = 494.711 ; free physical = 10246 ; free virtual = 21980

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+

Start IO Insertion

Start Flattening Before IO Insertion

Finished Flattening Before IO Insertion

Start Final Netlist Cleanup

Finished Final Netlist Cleanup

Finished IO Insertion : Time (s): cpu = 00:00:11 ; elapsed = 00:00:26 . Memory (MB): peak = 1810.492 ; gain = 494.711 ; free physical = 10246 ; free virtual = 21980

Report Check Netlist:
+------+-----------------+-------+---------+-------+-----------------+
| |Item |Errors |Warnings |Status |Description |
+------+-----------------+-------+---------+-------+-----------------+
|1 |multi_driven_nets | 0| 0|Passed |Multi driven nets |
+------+-----------------+-------+---------+-------+-----------------+

Start Renaming Generated Instances

Finished Renaming Generated Instances : Time (s): cpu = 00:00:11 ; elapsed = 00:00:26 . Memory (MB): peak = 1810.492 ; gain = 494.711 ; free physical = 10246 ; free virtual = 21980

Report RTL Partitions:
+-+-------------+-----------+----------+
| |RTL Partition |Replication |Instances |
+-+-------------+-----------+----------+
+-+-------------+-----------+----------+

Start Rebuilding User Hierarchy

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:11 ; elapsed = 00:00:26 . Memory (MB): peak = 1810.492 ; gain = 494.711 ; free physical = 10246 ; free virtual = 21980

Start Renaming Generated Ports

Finished Renaming Generated Ports : Time (s): cpu = 00:00:11 ; elapsed = 00:00:26 . Memory (MB): peak = 1810.492 ; gain = 494.711 ; free physical = 10246 ; free virtual = 21980

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:11 ; elapsed = 00:00:26 . Memory (MB): peak = 1810.492 ; gain = 494.711 ; free physical = 10246 ; free virtual = 21980

Start Renaming Generated Nets

```
---------------------------------------------------------------------------------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:11 ; elapsed = 00:00:26 . Memory
(MB): peak = 1810.492 ; gain = 494.711 ; free physical = 10246 ; free virtual = 21980
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+------+------+
|      |Cell  |Count |
+------+------+------+
|1     |LUT4  |     2|
|2     |LUT5  |     7|
|3     |LUT6  |     4|
|4     |MUXF7 |     2|
|5     |IBUF  |    13|
|6     |OBUF  |     6|
+------+------+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    34|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:11 ; elapsed = 00:00:26 . Memory
(MB): peak = 1810.492 ; gain = 494.711 ; free physical = 10245 ; free virtual = 21980
---------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 6 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:07 ; elapsed = 00:00:12 . Memory (MB):
peak = 1810.492 ; gain = 130.441 ; free physical = 10298 ; free virtual = 22033
Synthesis Optimization Complete : Time (s): cpu = 00:00:11 ; elapsed = 00:00:26 . Memory
(MB): peak = 1810.492 ; gain = 494.711 ; free physical = 10308 ; free virtual = 22043
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 15 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
```

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis
15 Infos, 7 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:13 ; elapsed = 00:00:26 . Memory (MB): peak = 1823.492 ; gain = 520.363 ; free physical = 10295 ; free virtual = 22030
WARNING: [Constraints 18-5210] No constraint will be written out.
INFO: [Common 17-1381] The checkpoint '/nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/vivado/lab1_316/lab1_316.runs/synth_1/alu.dcp' has been generated.
INFO: [runtcl-4] Executing : report_utilization -file alu_utilization_synth.rpt -pb alu_utiliz

Vivado Implementation

*** Running vivado
    with args -log alu.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source alu.tcl -notrace

****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source alu.tcl -notrace
Command: link_design -top alu -part xc7a100tcsg324-1
Design is defaulting to srcset: sources_1
Design is defaulting to constrset: constrs_1
INFO: [Netlist 29-17] Analyzing 15 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-479] Netlist was created with Vivado 2018.2
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [/nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/vivado/lab1_316/lab1_316.srcs/constrs_1/imports/DO/lab1_constraints.xdc]
Finished Parsing XDC File [/nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/vivado/lab1_316/lab1_316.srcs/constrs_1/imports/DO/lab1_constraints.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

7 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
link_design completed successfully
link_design: Time (s): cpu = 00:00:05 ; elapsed = 00:00:14 . Memory (MB): peak = 1652.375 ; gain = 344.242 ; free physical = 10413 ; free virtual = 22147
Command: opt_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command opt_design

Starting DRC Task
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Project 1-461] DRC finished with 0 Errors
INFO: [Project 1-462] Please refer to the DRC report (report_drc) for more information.

Time (s): cpu = 00:00:00.76 ; elapsed = 00:00:01 . Memory (MB): peak = 1727.402 ; gain = 75.027 ; free physical = 10406 ; free virtual = 22140

Starting Cache Timing Information Task
INFO: [Timing 38-35] Done setting XDC timing constraints.
Ending Cache Timing Information Task | Checksum: fb769a3d

Time (s): cpu = 00:00:07 ; elapsed = 00:00:17 . Memory (MB): peak = 2186.902 ; gain = 459.500 ; free physical = 9985 ; free virtual = 21718

Starting Logic Optimization Task

Phase 1 Retarget
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Opt 31-49] Retargeted 0 cell(s).
Phase 1 Retarget | Checksum: fb769a3d

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2186.902 ; gain = 0.000 ; free physical = 10008 ; free virtual = 21741
INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Phase 2 Constant propagation | Checksum: fb769a3d

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2186.902 ; gain = 0.000 ; free physical = 10008 ; free virtual = 21741
INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep
Phase 3 Sweep | Checksum: fb769a3d

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2186.902 ; gain = 0.000 ; free physical = 10008 ; free virtual = 21741
INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization
Phase 4 BUFG optimization | Checksum: fb769a3d

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2186.902 ; gain = 0.000 ; free physical = 10008 ; free virtual = 21741
INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization
Phase 5 Shift Register Optimization | Checksum: fb769a3d

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2186.902 ; gain = 0.000 ; free physical = 10008 ; free virtual = 21741
INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist
Phase 6 Post Processing Netlist | Checksum: fb769a3d

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2186.902 ; gain = 0.000 ; free physical = 10008 ; free virtual = 21741
INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2186.902 ; gain = 0.000 ; free physical = 10008 ; free virtual = 21741
Ending Logic Optimization Task | Checksum: fb769a3d

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2186.902 ; gain = 0.000 ; free physical = 10008 ; free virtual = 21741

Starting Power Optimization Task
INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
Ending Power Optimization Task | Checksum: fb769a3d

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2186.902 ; gain = 0.000 ; free physical = 10008 ; free virtual = 21741

Starting Final Cleanup Task
Ending Final Cleanup Task | Checksum: fb769a3d

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2186.902 ; gain = 0.000 ; free physical = 10008 ; free virtual = 21741

INFO: [Common 17-83] Releasing license: Implementation
23 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
opt_design completed successfully
opt_design: Time (s): cpu = 00:00:08 ; elapsed = 00:00:18 . Memory (MB): peak = 2186.902 ; gain = 534.527 ; free physical = 10008 ; free virtual = 21741
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2218.918 ; gain = 0.004 ; free physical = 10006 ; free virtual = 21740
INFO: [Common 17-1381] The checkpoint '/nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/vivado/lab1_316/lab1_316.runs/impl_1/alu_opt.dcp' has been generated.
INFO: [runtcl-4] Executing : report_drc -file alu_drc_opted.rpt -pb alu_drc_opted.pb -rpx alu_drc_opted.rpx
Command: report_drc -file alu_drc_opted.rpt -pb alu_drc_opted.pb -rpx alu_drc_opted.rpx
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/vivado/lab1_316/lab1_316.runs/impl_1/alu_drc_opted.rpt.
report_drc completed successfully
Command: place_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
Running DRC as a precondition to command place_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Starting Placer Task
INFO: [Place 30-611] Multithreading enabled for place_design using a maximum of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2306.961 ; gain = 0.000 ; free physical = 9963 ; free virtual = 21696
Phase 1.1 Placer Initialization Netlist Sorting | Checksum: f71bbf5b

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2306.961 ; gain = 0.000 ; free physical = 9963 ; free virtual = 21696
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2306.961 ; gain = 0.000 ; free physical = 9963 ; free virtual = 21696

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device
INFO: [Timing 38-35] Done setting XDC timing constraints.
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: f71bbf5b

Time (s): cpu = 00:00:00.51 ; elapsed = 00:00:00.28 . Memory (MB): peak = 2306.961 ; gain = 0.000 ; free physical = 9958 ; free virtual = 21691

Phase 1.3 Build Placer Netlist Model
Phase 1.3 Build Placer Netlist Model | Checksum: 1058ddc15

Time (s): cpu = 00:00:00.56 ; elapsed = 00:00:00.30 . Memory (MB): peak = 2306.961 ; gain = 0.000 ; free physical = 9959 ; free virtual = 21693

Phase 1.4 Constrain Clocks/Macros
Phase 1.4 Constrain Clocks/Macros | Checksum: 1058ddc15

Time (s): cpu = 00:00:00.56 ; elapsed = 00:00:00.30 . Memory (MB): peak = 2306.961 ; gain = 0.000 ; free physical = 9959 ; free virtual = 21693
Phase 1 Placer Initialization | Checksum: 1058ddc15

Time (s): cpu = 00:00:00.56 ; elapsed = 00:00:00.30 . Memory (MB): peak = 2306.961 ; gain = 0.000 ; free physical = 9959 ; free virtual = 21693

Phase 2 Global Placement

Phase 2.1 Floorplanning
Phase 2.1 Floorplanning | Checksum: 1058ddc15

Time (s): cpu = 00:00:00.59 ; elapsed = 00:00:00.31 . Memory (MB): peak = 2306.961 ; gain = 0.000 ; free physical = 9958 ; free virtual = 21692
WARNING: [Place 46-29] place_design is not in timing mode. Skip physical synthesis in placer
Phase 2 Global Placement | Checksum: 1a09460a1

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.42 . Memory (MB): peak = 2367.980 ; gain = 61.020 ; free physical = 9940 ; free virtual = 21673

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros
Phase 3.1 Commit Multi Column Macros | Checksum: 1a09460a1

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.42 . Memory (MB): peak = 2367.980 ; gain = 61.020 ; free physical = 9940 ; free virtual = 21673

Phase 3.2 Commit Most Macros & LUTRAMs
Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 16ebe7b96

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.43 . Memory (MB): peak = 2367.980 ; gain = 61.020 ; free physical = 9940 ; free virtual = 21674

Phase 3.3 Area Swap Optimization
Phase 3.3 Area Swap Optimization | Checksum: 1118bec59

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.44 . Memory (MB): peak = 2367.980 ; gain = 61.020 ; free physical = 9940 ; free virtual = 21673

Phase 3.4 Pipeline Register Optimization
Phase 3.4 Pipeline Register Optimization | Checksum: 1118bec59

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.44 . Memory (MB): peak = 2367.980 ; gain = 61.020 ; free physical = 9940 ; free virtual = 21673

Phase 3.5 Small Shape Detail Placement
Phase 3.5 Small Shape Detail Placement | Checksum: 99e2ef58

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.51 . Memory (MB): peak = 2367.980 ; gain = 61.020 ; free physical = 9936 ; free virtual = 21670

Phase 3.6 Re-assign LUT pins
Phase 3.6 Re-assign LUT pins | Checksum: 99e2ef58

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.51 . Memory (MB): peak = 2367.980 ; gain = 61.020 ; free physical = 9936 ; free virtual = 21670

Phase 3.7 Pipeline Register Optimization
Phase 3.7 Pipeline Register Optimization | Checksum: 99e2ef58

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.51 . Memory (MB): peak = 2367.980 ; gain = 61.020 ; free physical = 9936 ; free virtual = 21670
Phase 3 Detail Placement | Checksum: 99e2ef58

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.51 . Memory (MB): peak = 2367.980 ; gain = 61.020 ; free physical = 9936 ; free virtual = 21670

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization
Phase 4.1 Post Commit Optimization | Checksum: 99e2ef58

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.52 . Memory (MB): peak = 2367.980 ; gain = 61.020 ; free physical = 9936 ; free virtual = 21670

Phase 4.2 Post Placement Cleanup
Phase 4.2 Post Placement Cleanup | Checksum: 99e2ef58

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.52 . Memory (MB): peak = 2367.980 ; gain = 61.020 ; free physical = 9938 ; free virtual = 21672

Phase 4.3 Placer Reporting
Phase 4.3 Placer Reporting | Checksum: 99e2ef58

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.52 . Memory (MB): peak = 2367.980 ; gain = 61.020 ; free physical = 9938 ; free virtual = 21672

Phase 4.4 Final Placement Cleanup
Phase 4.4 Final Placement Cleanup | Checksum: 99e2ef58

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.52 . Memory (MB): peak = 2367.980 ; gain = 61.020 ; free physical = 9938 ; free virtual = 21672
Phase 4 Post Placement Optimization and Clean-Up | Checksum: 99e2ef58

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.52 . Memory (MB): peak = 2367.980 ; gain = 61.020 ; free physical = 9938 ; free virtual = 21672
Ending Placer Task | Checksum: 4ced512d

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.52 . Memory (MB): peak = 2367.980 ; gain = 61.020 ; free physical = 9955 ; free virtual = 21689
INFO: [Common 17-83] Releasing license: Implementation
41 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
place_design completed successfully
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.11 . Memory (MB): peak = 2367.980 ; gain = 0.000 ; free physical = 9951 ; free virtual = 21686
INFO: [Common 17-1381] The checkpoint '/nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/vivado/lab1_316/lab1_316.runs/impl_1/alu_placed.dcp' has been generated.
INFO: [runtcl-4] Executing : report_io -file alu_io_placed.rpt
report_io: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.09 . Memory (MB): peak = 2367.980 ; gain = 0.000 ; free physical = 9948 ; free virtual = 21682
INFO: [runtcl-4] Executing : report_utilization -file alu_utilization_placed.rpt -pb alu_utilization_placed.pb

report_utilization: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.06 . Memory (MB): peak = 2367.980 ; gain = 0.000 ; free physical = 9957 ; free virtual = 21690
INFO: [runtcl-4] Executing : report_control_sets -verbose -file alu_control_sets_placed.rpt
report_control_sets: Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.08 . Memory (MB): peak = 2367.980 ; gain = 0.000 ; free physical = 9956 ; free virtual = 21689
Command: route_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command route_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Starting Routing Task
INFO: [Route 35-254] Multithreading enabled for route_design using a maximum of 8 CPUs
Checksum: PlaceDB: 62660c4 ConstDB: 0 ShapeSum: 46c6f069 RouteDB: 0

Phase 1 Build RT Design
Phase 1 Build RT Design | Checksum: 1b5e6cd96

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2397.977 ; gain = 29.996 ; free physical = 9819 ; free virtual = 21553
Post Restoration Checksum: NetGraph: e212023c NumContArr: d3d4cb5a Constraints: 0 Timing: 0

Phase 2 Router Initialization
INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints
Phase 2.1 Fix Topology Constraints | Checksum: 1b5e6cd96

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2403.965 ; gain = 35.984 ; free physical = 9788 ; free virtual = 21522

Phase 2.2 Pre Route Cleanup
Phase 2.2 Pre Route Cleanup | Checksum: 1b5e6cd96

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2403.965 ; gain = 35.984 ; free physical = 9788 ; free virtual = 21522
 Number of Nodes with overlaps = 0
Phase 2 Router Initialization | Checksum: 11612bac2

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2411.230 ; gain = 43.250 ; free physical = 9784 ; free virtual = 21518

Phase 3 Initial Routing
Phase 3 Initial Routing | Checksum: 7d723a35

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2411.230 ; gain = 43.250 ; free physical = 9782 ; free virtual = 21516

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0
 Number of Nodes with overlaps = 1
 Number of Nodes with overlaps = 0
Phase 4.1 Global Iteration 0 | Checksum: 17a0636a6

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2411.230 ; gain = 43.250 ; free physical = 9782 ; free virtual = 21516
Phase 4 Rip-up And Reroute | Checksum: 17a0636a6

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2411.230 ; gain = 43.250 ; free physical = 9782 ; free virtual = 21516

Phase 5 Delay and Skew Optimization
Phase 5 Delay and Skew Optimization | Checksum: 17a0636a6

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2411.230 ; gain = 43.250 ; free physical = 9782 ; free virtual = 21516

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter
Phase 6.1 Hold Fix Iter | Checksum: 17a0636a6

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2411.230 ; gain = 43.250 ; free physical = 9782 ; free virtual = 21516
Phase 6 Post Hold Fix | Checksum: 17a0636a6

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2411.230 ; gain = 43.250 ; free physical = 9782 ; free virtual = 21516

Phase 7 Route finalize

Router Utilization Summary
  Global Vertical Routing Utilization   = 0.0146668 %
  Global Horizontal Routing Utilization = 0.0130009 %
  Routable Net Status*
  *Does not include unroutable nets such as driverless and loadless.
  Run report_route_status for detailed report.
  Number of Failed Nets   = 0

```
  Number of Unrouted Nets             = 0
  Number of Partially Routed Nets     = 0
  Number of Node Overlaps             = 0

Congestion Report
North Dir 1x1 Area, Max Cong = 16.2162%, No Congested Regions.
South Dir 1x1 Area, Max Cong = 16.2162%, No Congested Regions.
East Dir 1x1 Area, Max Cong = 4.41176%, No Congested Regions.
West Dir 1x1 Area, Max Cong = 5.88235%, No Congested Regions.

------------------------------
Reporting congestion hotspots
------------------------------
Direction: North
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: South
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: East
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: West
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: 17a0636a6

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2411.230 ; gain = 43.250
; free physical = 9782 ; free virtual = 21515

Phase 8 Verifying routed nets

 Verification completed successfully
Phase 8 Verifying routed nets | Checksum: 17a0636a6

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2414.230 ; gain = 46.250
; free physical = 9781 ; free virtual = 21515

Phase 9 Depositing Routes
Phase 9 Depositing Routes | Checksum: ee710e41

Time (s): cpu = 00:00:14 ; elapsed = 00:00:10 . Memory (MB): peak = 2414.230 ; gain = 46.250
```

; free physical = 9781 ; free virtual = 21515
INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:14 ; elapsed = 00:00:10 . Memory (MB): peak = 2414.230 ; gain = 46.250 ; free physical = 9816 ; free virtual = 21549

Routing Is Done.
INFO: [Common 17-83] Releasing license: Implementation
54 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
route_design completed successfully
route_design: Time (s): cpu = 00:00:15 ; elapsed = 00:00:12 . Memory (MB): peak = 2414.234 ; gain = 46.254 ; free physical = 9816 ; free virtual = 21549
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2414.234 ; gain = 0.000 ; free physical = 9810 ; free virtual = 21545
INFO: [Common 17-1381] The checkpoint '/nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/vivado/lab1_316/lab1_316.runs/impl_1/alu_routed.dcp' has been generated.
INFO: [runtcl-4] Executing : report_drc -file alu_drc_routed.rpt -pb alu_drc_routed.pb -rpx alu_drc_routed.rpx
Command: report_drc -file alu_drc_routed.rpt -pb alu_drc_routed.pb -rpx alu_drc_routed.rpx
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/vivado/lab1_316/lab1_316.runs/impl_1/alu_drc_routed.rpt.
report_drc completed successfully
INFO: [runtcl-4] Executing : report_methodology -file alu_methodology_drc_routed.rpt -pb alu_methodology_drc_routed.pb -rpx alu_methodology_drc_routed.rpx
Command: report_methodology -file alu_methodology_drc_routed.rpt -pb alu_methodology_drc_routed.pb -rpx alu_methodology_drc_routed.rpx
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [DRC 23-133] Running Methodology with 8 threads
INFO: [Coretcl 2-1520] The results of Report Methodology are in file /nfs/home/n/n_louvet/Coen316/lab1/Modelsim/Code/vivado/lab1_316/lab1_316.runs/impl_1/alu_methodology_drc_routed.rpt.
report_methodology completed successfully
INFO: [runtcl-4] Executing : report_power -file alu_power_routed.rpt -pb alu_power_summary_routed.pb -rpx alu_power_routed.rpx
Command: report_power -file alu_power_routed.rpt -pb alu_power_summary_routed.pb -rpx alu_power_routed.rpx
WARNING: [Power 33-232] No user defined clocks were found in the design!
Resolution: Please specify clocks using create_clock/create_generated_clock for sequential

elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate
INFO: [Timing 38-35] Done setting XDC timing constraints.
Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation
66 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.
report_power completed successfully
INFO: [runtcl-4] Executing : report_route_status -file alu_route_status.rpt -pb alu_route_status.pb
INFO: [runtcl-4] Executing : report_timing_summary -max_paths 10 -file alu_timing_summary_routed.rpt -pb alu_timing_summary_routed.pb -rpx alu_timing_summary_routed.rpx -warn_on_violation
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max, Timing Stage: Requireds.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs
WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.
INFO: [runtcl-4] Executing : report_incremental_reuse -file alu_incremental_reuse_routed.rpt
INFO: [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
INFO: [runtcl-4] Executing : report_clock_utilization -file alu_clock_utilization_routed.rpt
INFO: [runtcl-4] Executing : report_bus_skew -warn_on_violation -file alu_bus_skew_routed.rpt -pb alu_bus_skew_routed.pb -rpx alu_bus_skew_routed.rpx
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max, Timing Stage: Requireds.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs
INFO: [Common 17-206] Exiting Vivado at Tue Oct 3 17:50:03 2023...

*** Running vivado
    with args -log alu.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source alu.tcl -notrace

****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source alu.tcl -notrace
Command: open_checkpoint alu_routed.dcp

Starting open_checkpoint Task

Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.07 . Memory (MB): peak = 1277.113 ; gain = 0.000 ; free physical = 10707 ; free virtual = 22441
INFO: [Netlist 29-17] Analyzing 15 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-479] Netlist was created with Vivado 2018.2
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Timing 38-478] Restoring timing data from binary archive.
INFO: [Timing 38-479] Binary timing data restore complete.
INFO: [Project 1-856] Restoring constraints from binary archive.
INFO: [Project 1-853] Binary constraint restore complete.
Reading XDEF placement.
Reading placer database...
Reading XDEF routing.
Read XDEF File: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.12 . Memory (MB): peak = 2085.062 ; gain = 0.004 ; free physical = 9993 ; free virtual = 21727
Restored from archive | CPU: 0.110000 secs | Memory: 0.960503 MB |
Finished XDEF File Restore: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.12 . Memory (MB): peak = 2085.062 ; gain = 0.004 ; free physical = 9993 ; free virtual = 21727
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
open_checkpoint: Time (s): cpu = 00:00:12 ; elapsed = 00:00:33 . Memory (MB): peak = 2085.062 ; gain = 807.953 ; free physical = 9993 ; free virtual = 21727
Command: write_bitstream -force alu.bit
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command write_bitstream
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG_VOLTAGE voltage property is set in the current_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

```
 set_property CFGBVS value1 [current_design]
 #where value1 is either VCCO or GND

 set_property CONFIG_VOLTAGE value2 [current_design]
 #where value2 is the voltage provided to configuration bank 0
```

Refer to the device configuration user guide for more information.
INFO: [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings
INFO: [Vivado 12-3200] Please refer to the DRC report (report_drc) for more information.

```
INFO: [Designutils 20-2272] Running write_bitstream with 8 threads.
Loading data files...
Loading site data...
Loading route data...
Processing options...
Creating bitmap...
Creating bitstream...
Writing bitstream ./alu.bit...
INFO: [Vivado 12-1842] Bitgen Completed Successfully.
INFO: [Common 17-83] Releasing license: Implementation
21 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
write_bitstream completed successfully
write_bitstream: Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 2556.902
; gain = 471.840 ; free physical = 9929 ; free virtual = 21667
INFO: [Common 17-206] Exiting Vivado at Tue Oct  3 17:51:16 2023...
```