

Sheet: Sheet5F148FF8

1A

File: fpga-private-logic.sch

Sheet: sheet5F29CA30

2A

File: fpga-user-logic.sch

Sheet: Sheet5E8B0B5C

1B

File: fpga-private-power.sch

Sheet: sheet5F29CA2E

2B

File: fpga-user-power.sch

Sheet: sheet5F455DB7

3

File: mcu-master.sch

Sheet: sheet60915335

4

File: mcu-user.sch

Sheet: sheet5F56111F

5

File: analog.sch

Sheet: sheet5F5E2911

6

File: conn-user.sch

Sheet: sheet5F5A0C07

7

File: power.sch

Sheet: sheet5FE34FAC

8

File: conn-user2.sch

X1
logo

Sheet: sheet5F594D44

9

File: stlink.sch

FID1 Fiducial FID2 Fiducial FID3 Fiducial FID4 Fiducial FID5 Fiducial FID6 Fiducial FID7 Fiducial FID8 Fiducial
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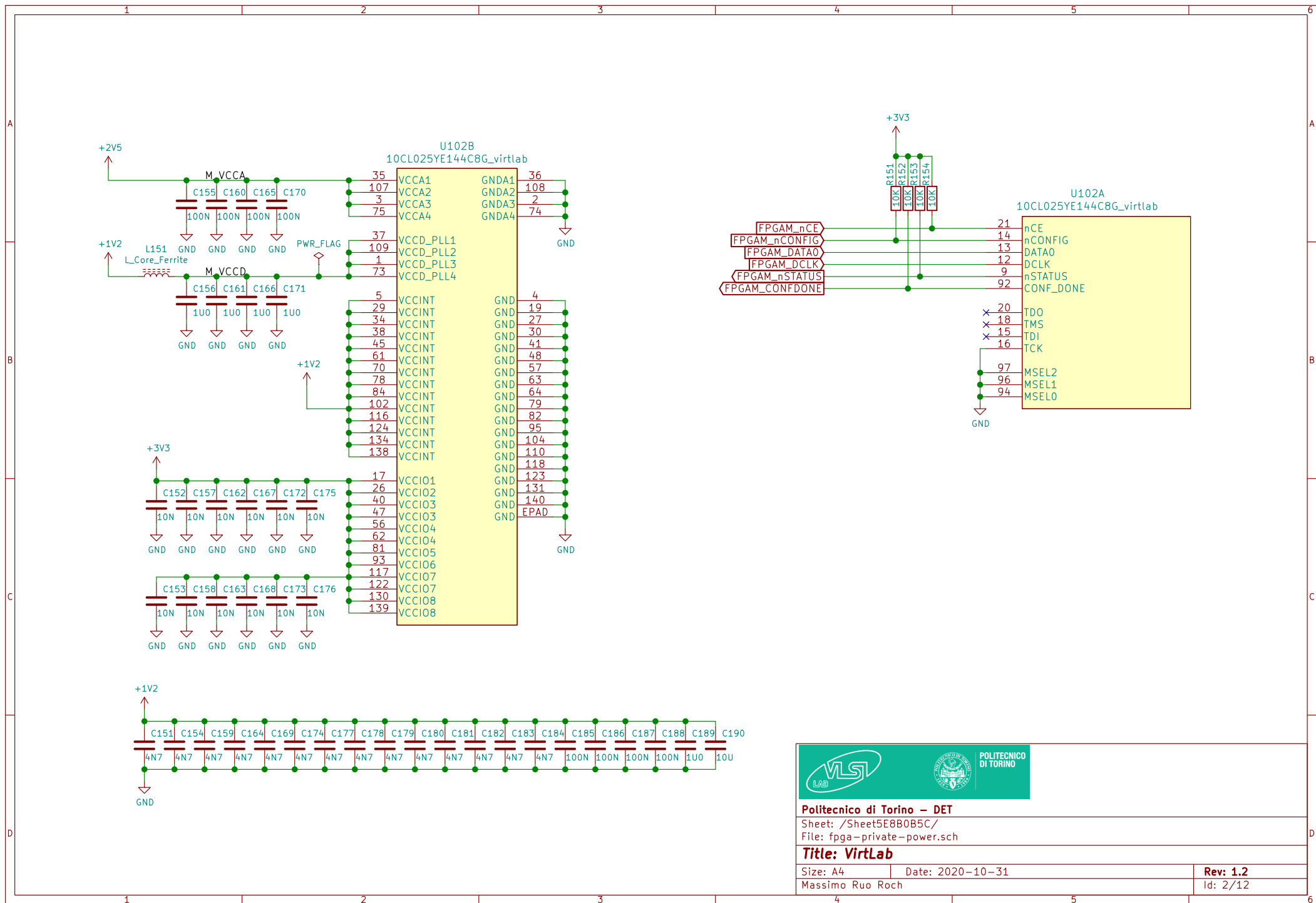
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Title: VirtLab

Size: A4 Date: 2020-10-31
Massimo Ruvo Roch

Rev: 1.2
Id: 1/12



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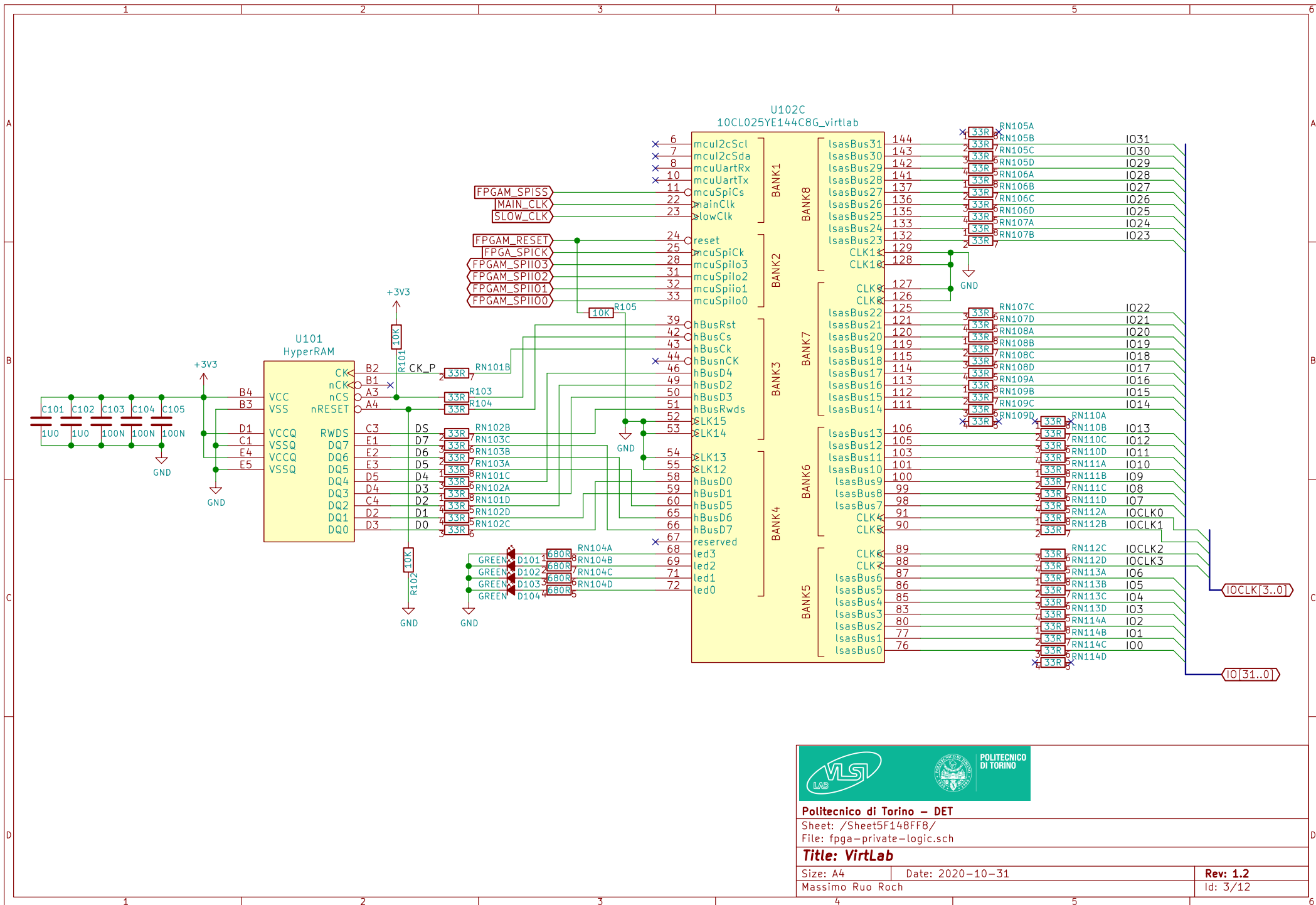
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Rev: 1.2

Id: 2/12



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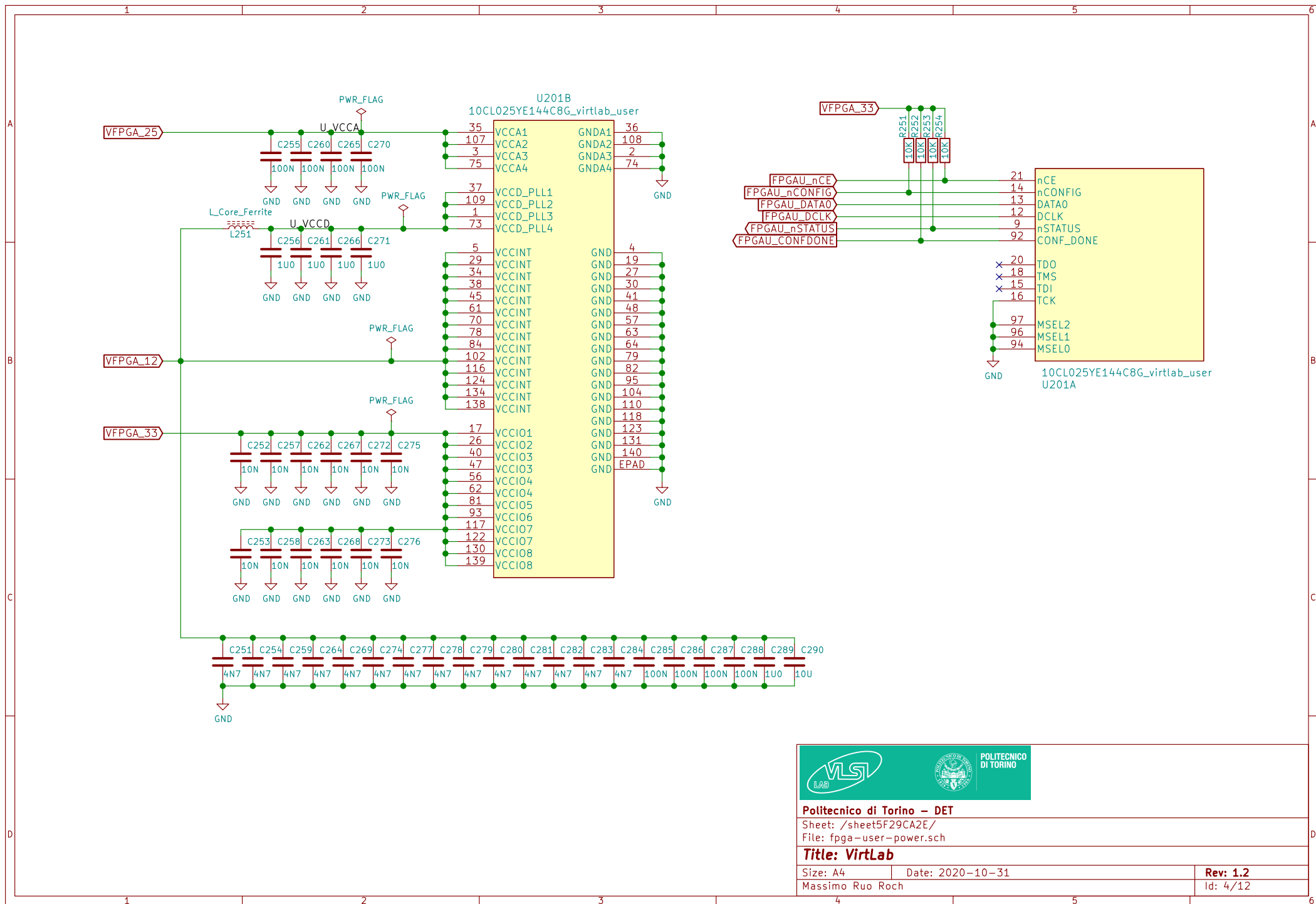
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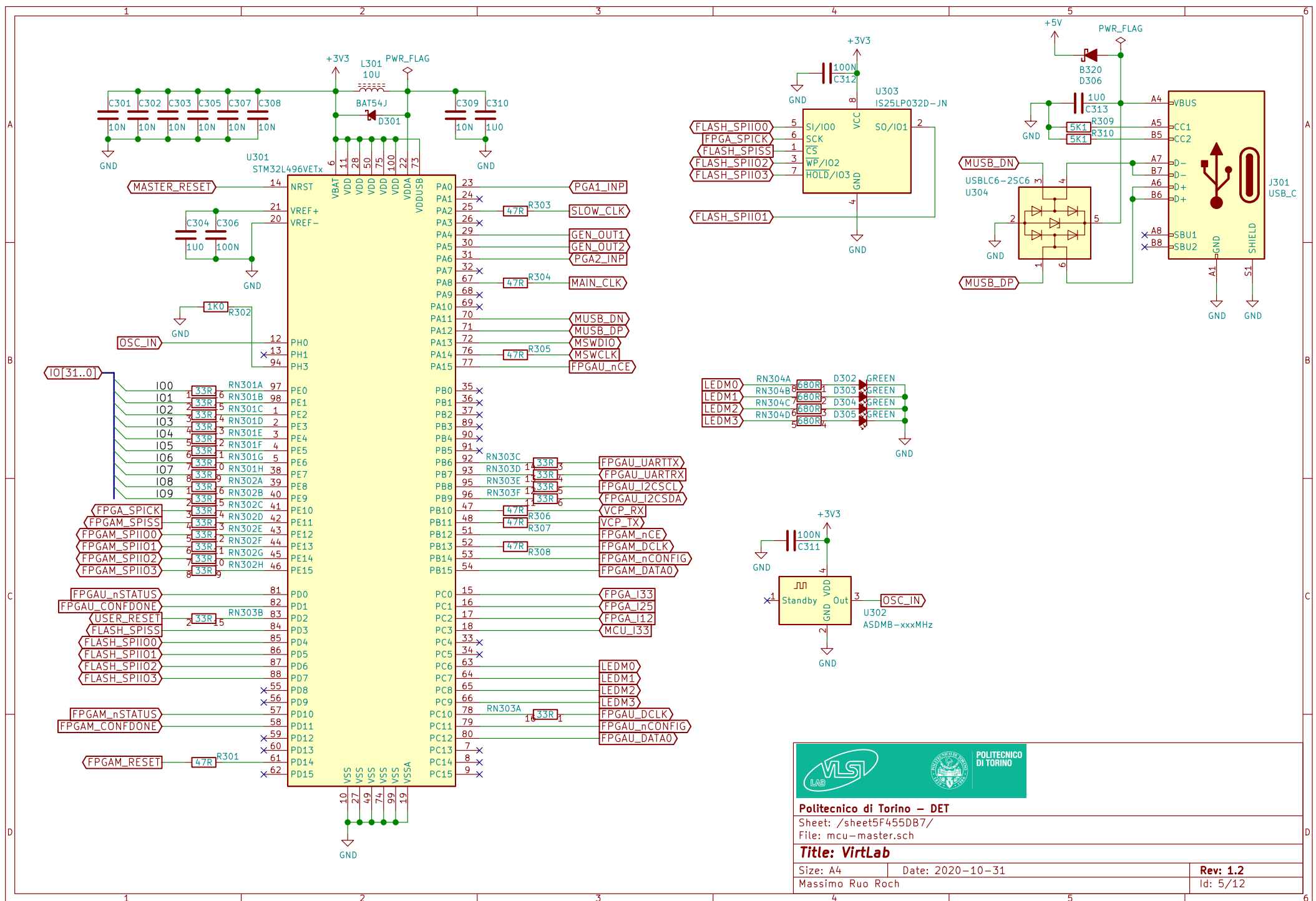
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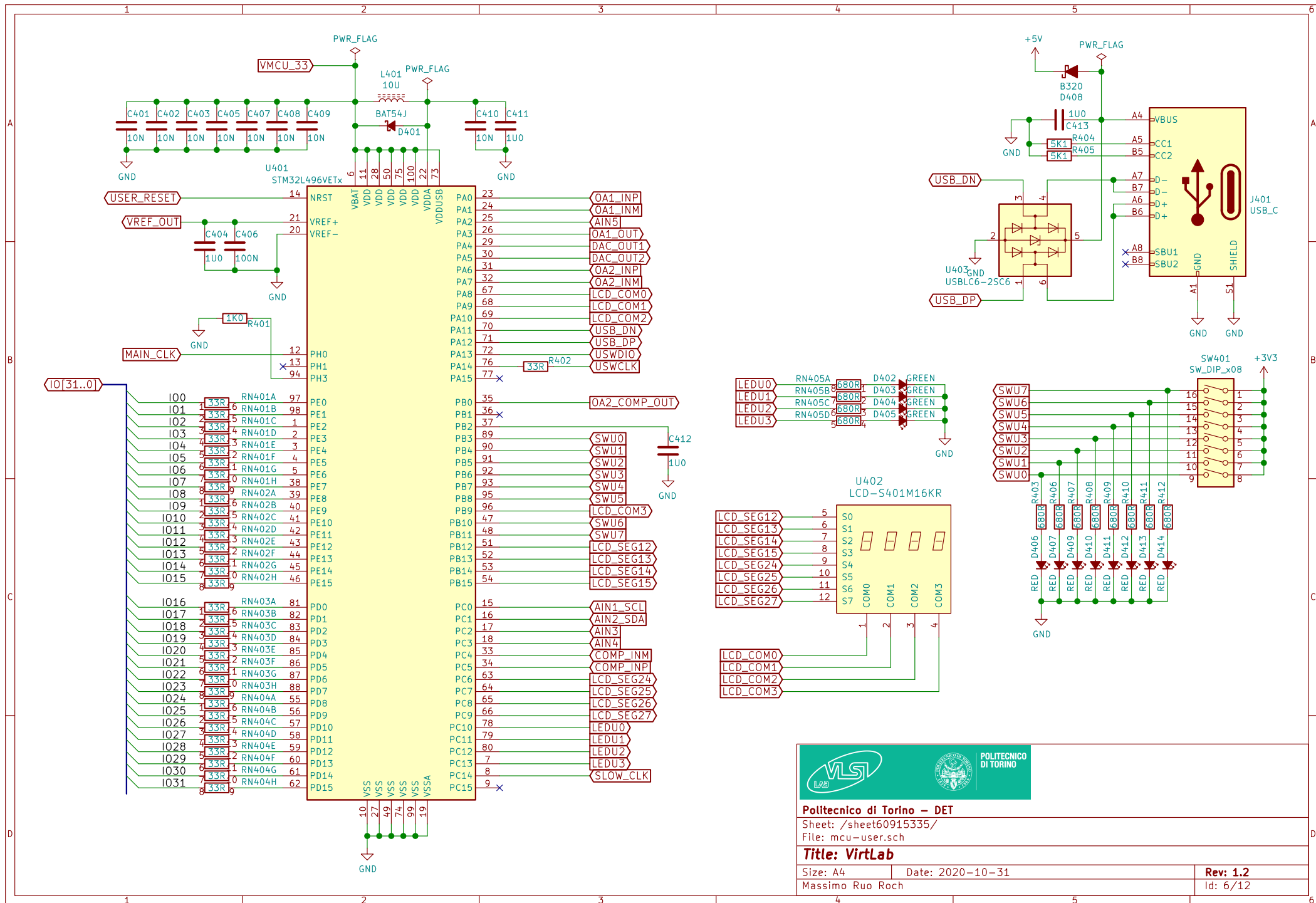
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Rev: 1.2

Id: 3/12







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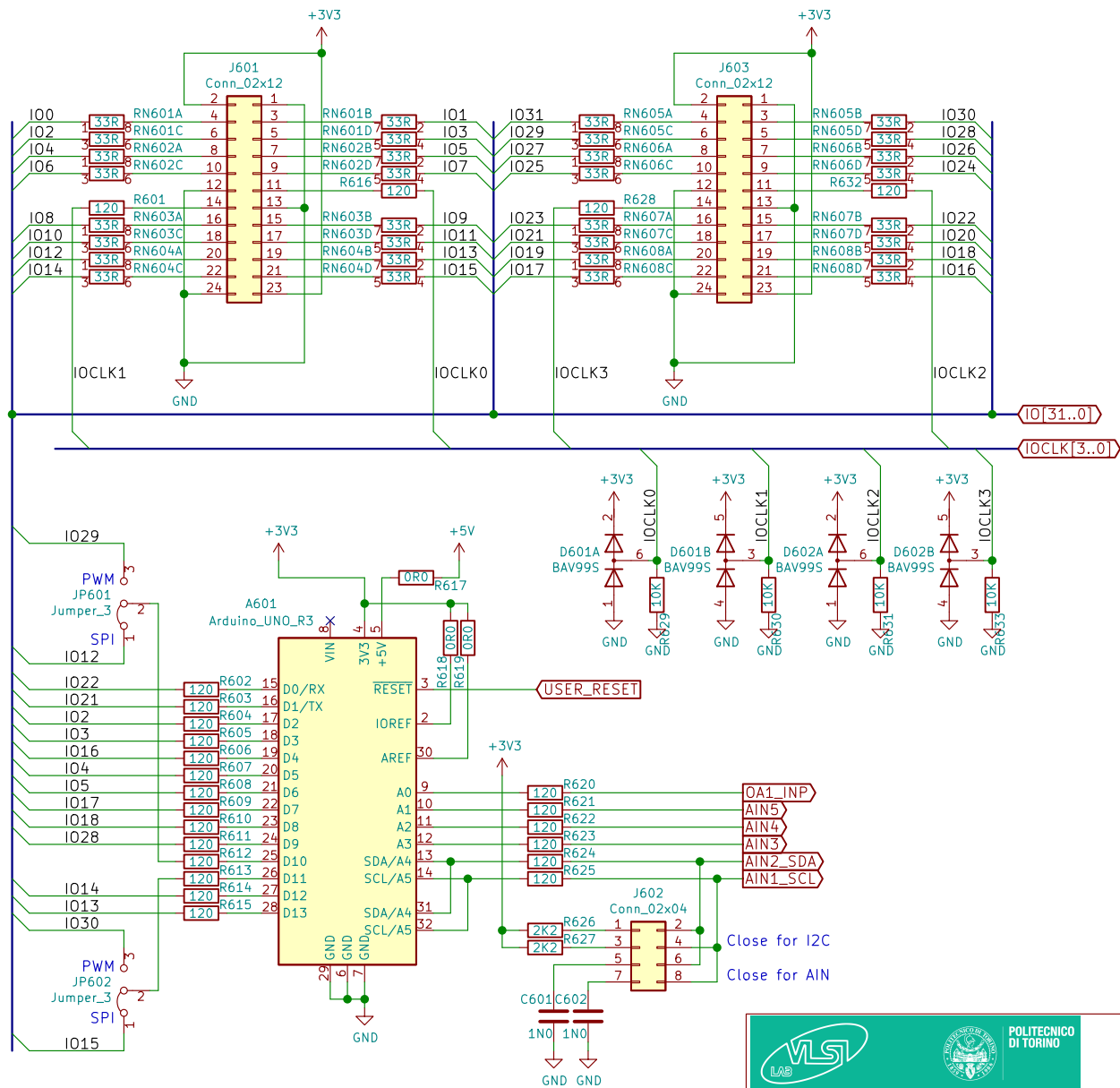
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Rev: 1.2

Id: 6/12



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Size: A4 Date: 2020-10-31

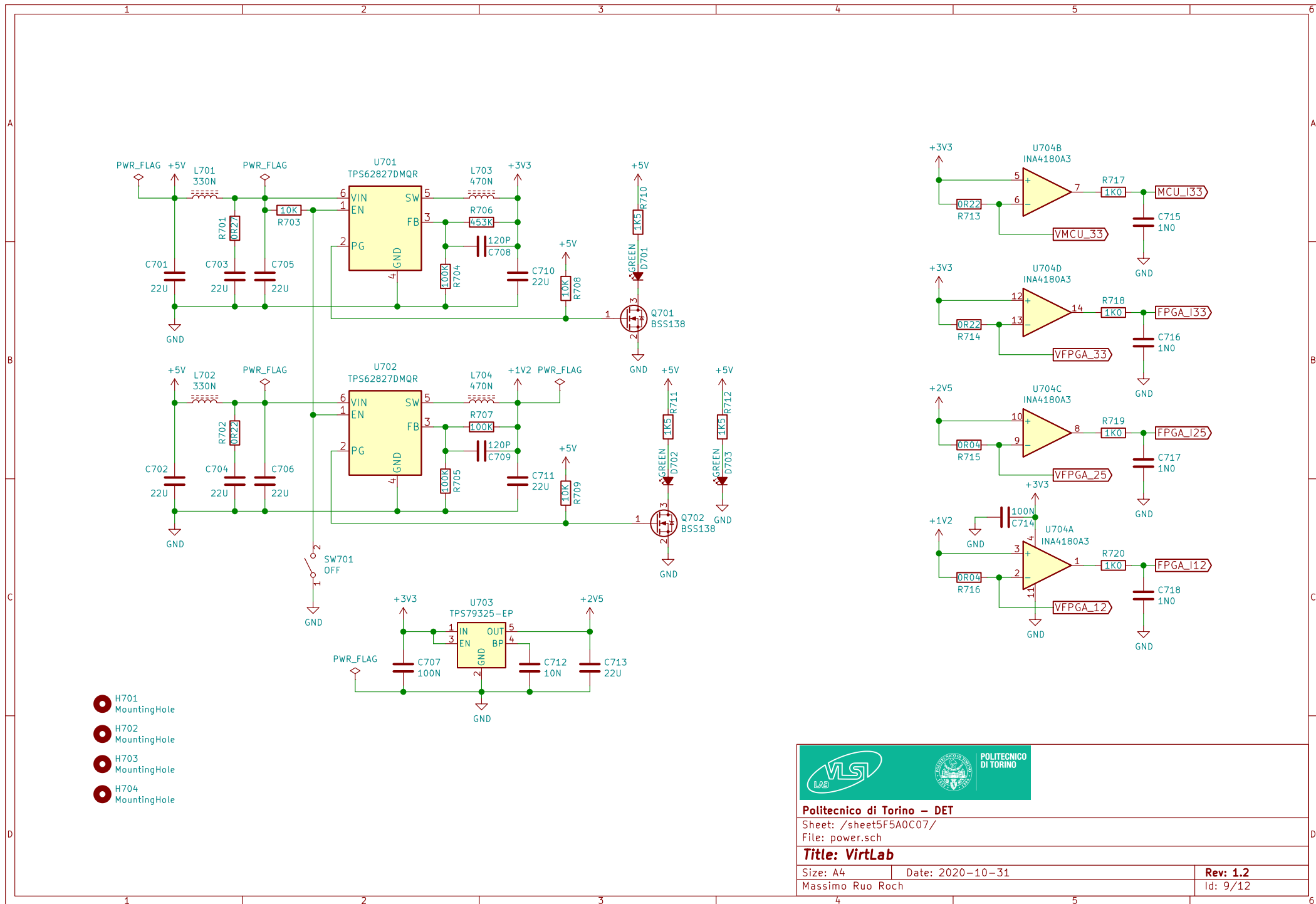
Massimo Ruco Roch

Rev: 1.2

Id: 7/12



Size: A4	
Massimo Ruotolo	



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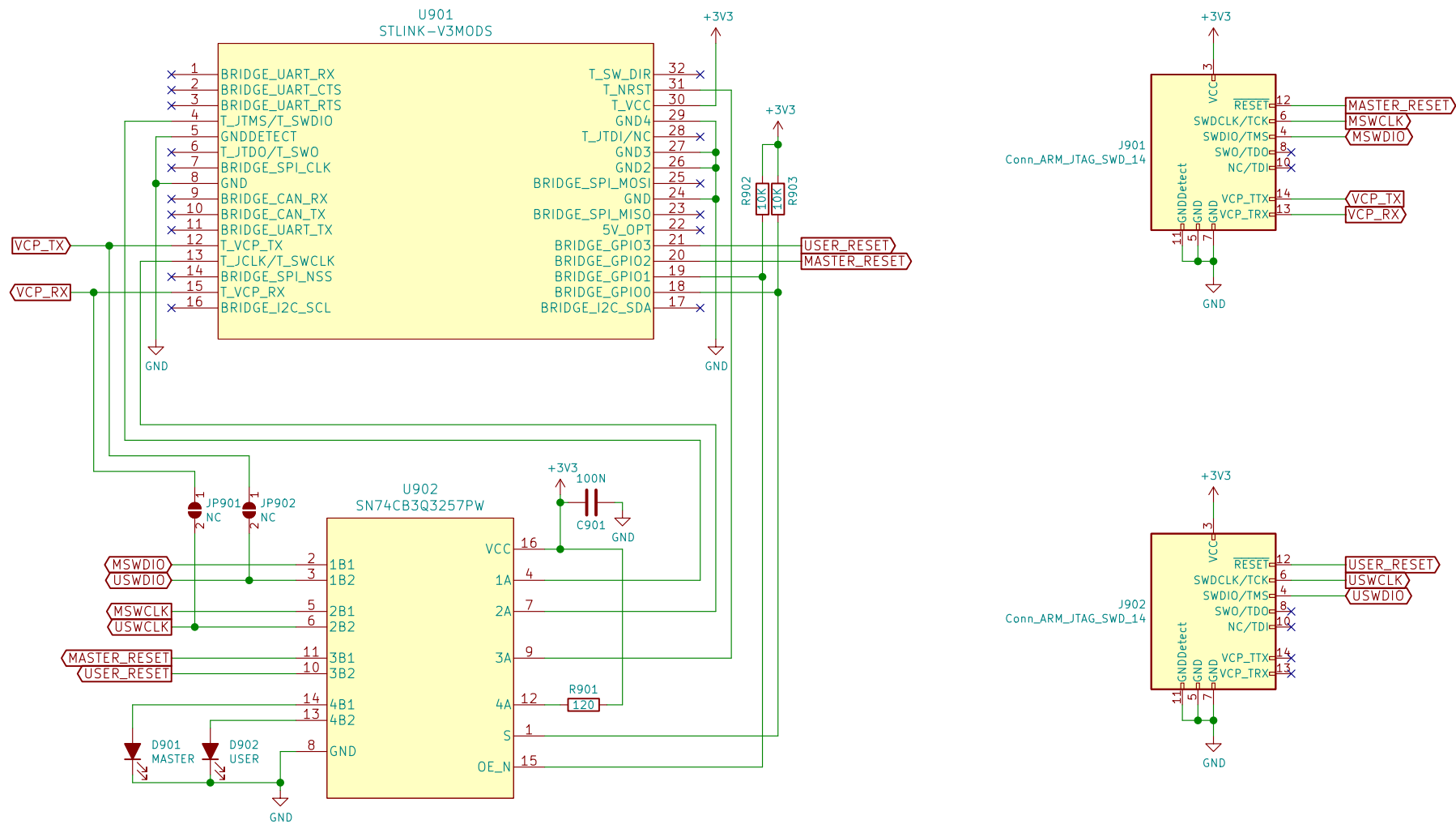
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Rev: 1.2

Id: 9/12



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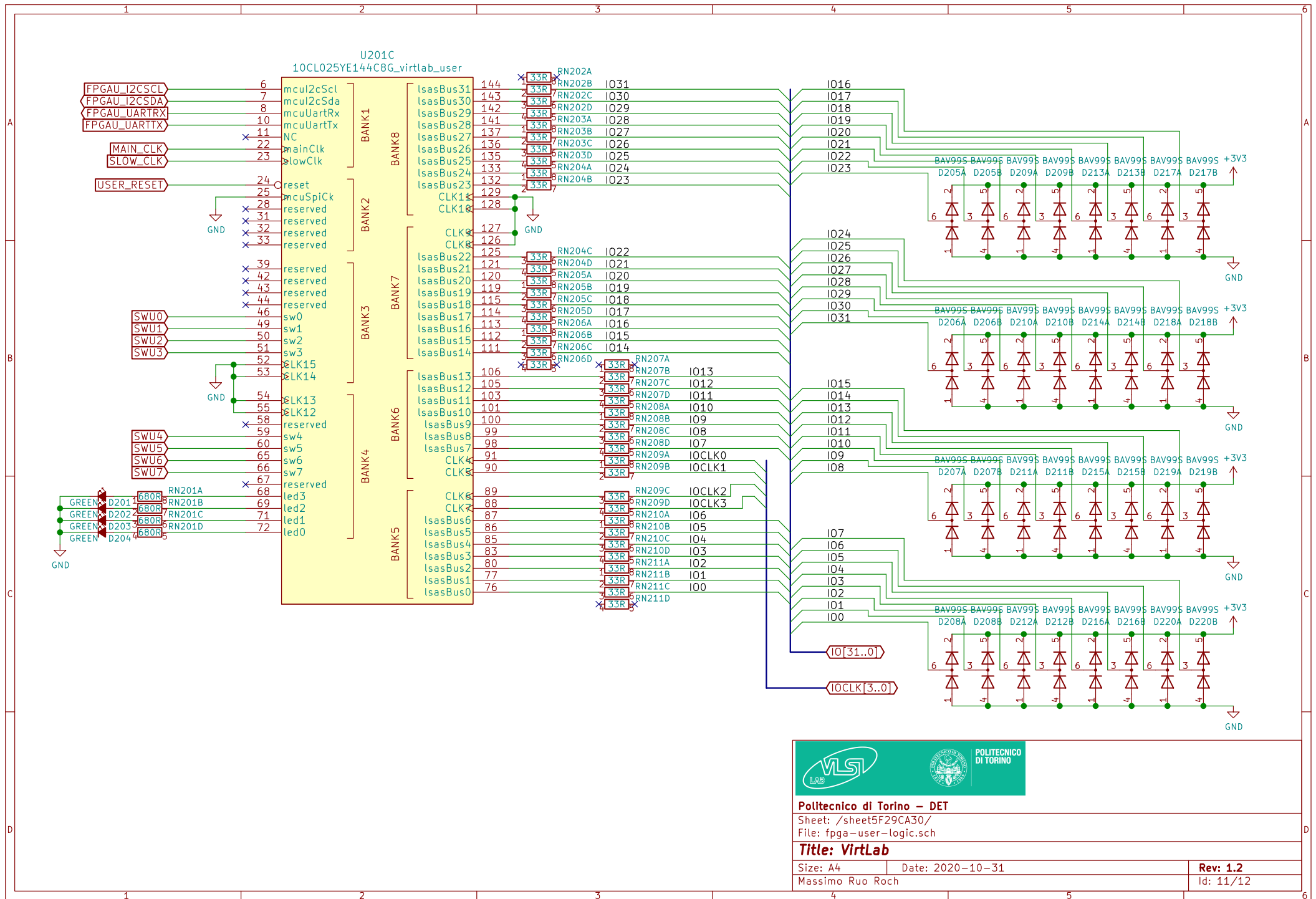
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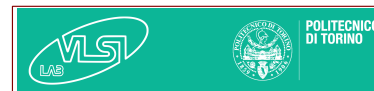
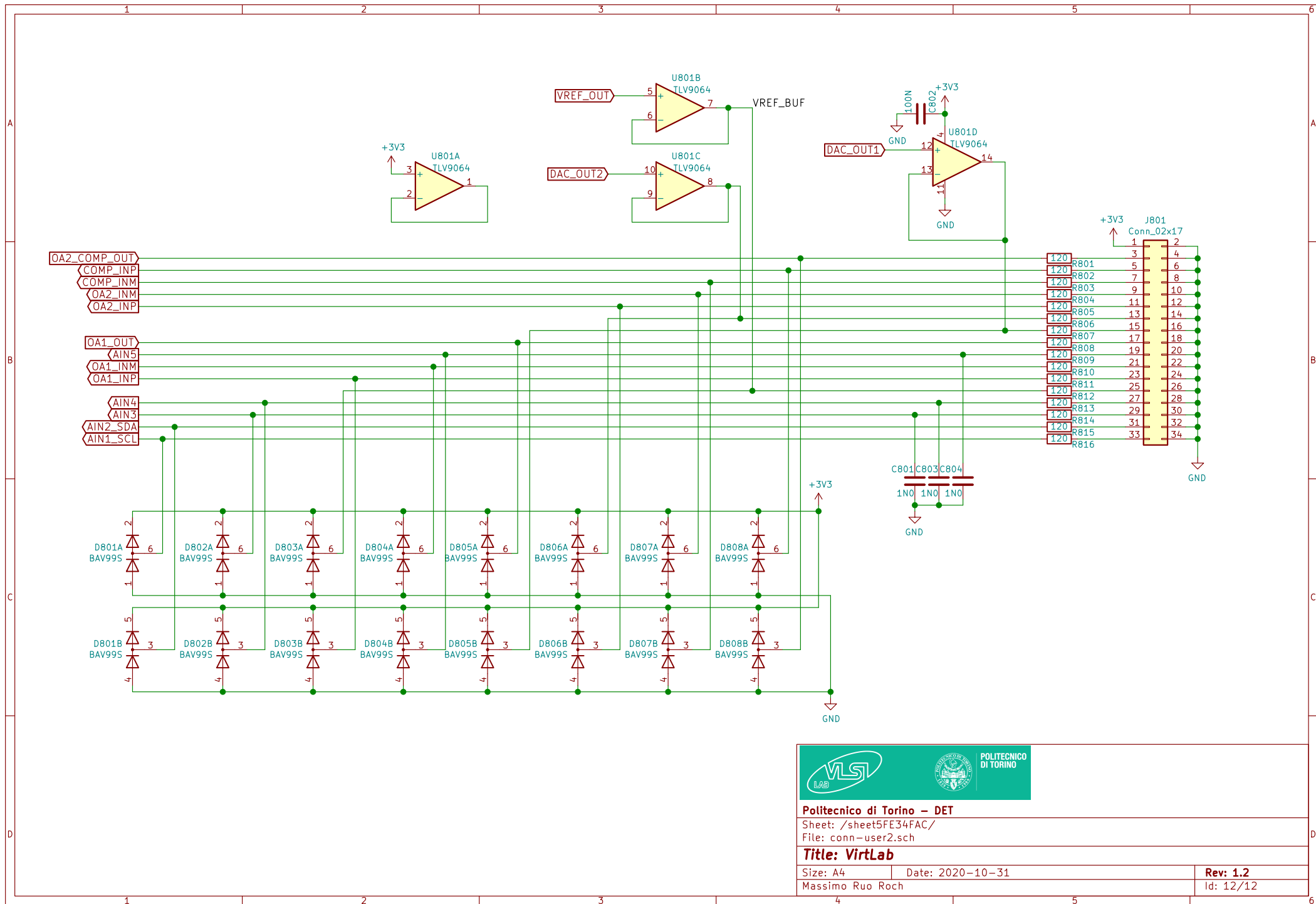
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Rev: 1.2

Id: 10/12





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Title: VirtLab

Size: A4 Date: 2020-10-31

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Id: 12/12