Impact of PCB Design on Switching noise and EMI of Synchronous DC-DC buck Converter

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***Abstract*— Synchronous DC-DC buck converters operate under a few MHz but generate broadband noise up to GHz range due to its switching operation. The noise causes EMI problem through radiation and switching noise at the converter output from direct conduction. To control EMI and switching noise at the converter output, proper PCB design plays a critical role. This paper evaluates three types of GND plane layout and three types of high-voltage AC node layout for synchronous DC-DC buck converter test benches with 4-layer stack-up PCB. Transverse electromagnetic (TEM) cell measurement and time-domain measurement of switching noise at the converters output were performed for the evaluation. The source of EMI, switching noise and magnitude difference over layouts were analyzed by the impedance measurement on the test benches.**

I. INTRODUCTION

Recent digital systems for mobile applications have to fulfill a low power requirement since the systems are often powered by batteries. The supply voltage of those systems gradually down to below 1V to meet the requirement. For those systems, a converter based on synchronous DC-DC buck topology is most widely used to step down the DC voltage with good power efficiency. Synchronous DC-DC buck converters are switching regulator. Switching regulators are known for superior power efficiency over linear regulators. However, there have been a lot of EMI issues caused by switching noise with broadband frequency range occur at the output node of DC-DC buck converter [1]-[2]. Various approaches have been addressed in the previous studies to resolve the EMI and switching noise issues. [3]-[6] introduce passive snubber circuit, input/output passive filters and external schottky diodes. Switching frequency modulation techniques were proposed in [7] and [8] to suppress the EMI and switching noise by spreading of spectral energy of the switching signal. These approaches are effective but cost additional passive components and area or advanced circuit design.

To control the EMI and switching noise without an extra cost, PCB design is another option designers can handle. It is generally known that PCB design greatly affect the generation of EMI and switching noise. Previous studies [9] and [10] give guidelines on design factors such as components placement, GND plane layout and high-voltage AC node layout which play a key role to control the EMI and switching noise. Those studies also introduce proper layout examples in 2-layer stack-up PCB for a switching regulator. However, previous guidelines are not enough to directly be applied on multi-layer stack-up PCB, which is widely used for digital systems for mobile applications. Because the multi-layer stack-up PCB has much more design factors to control than 2-layer stack-up PCB. Therefore, design of the key parts need to be evaluated in multi-layer stack-up PCB to ensure mitigation of excessive EMI and switching noise.

In this paper, layouts of GND plane and high-voltage AC node for synchronous DC-DC buck converter with 4-layer stack-up PCB are evaluated on their EMI and switching noise generation.

In chapter II, test benches of 4-layer stack-up PCB with three types of GND plane layout and three types of high-voltage AC node are explained.

In chapter III, transverse electromagnetic (TEM) cell measurement result and time-domain measurement result of switching noise at the converter output are presented.

Finally in chapter IV, the source of EMI and switching noise and magnitude difference over the layouts observed in chapter III are analyzed by the impedance measurement on the test benches.

II. TEST BENCH DESIGN

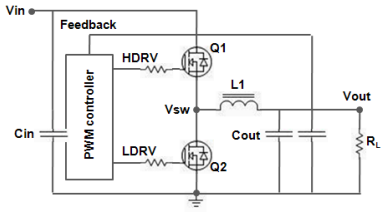


Fig. 1. Schematic of synchronous DC-DC buck converter for test benches

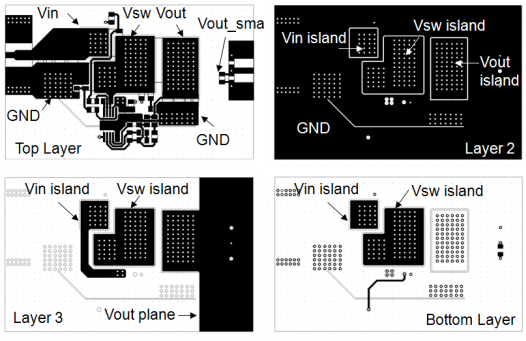


Fig. 2. Reference PCB layout of synchronous DC-DC buck converter for test benches

Fig.1 and 2 shows the schematic and reference PCB layout of synchronous DC-DC buck converter for test benches. The test benches are designed to have 4V to 5.5V voltage input, 2.5V output voltage and maximum 1A output current with 600 kHz switching frequency of PWM controller. R_L in Fig.1 is set to 5 ohm to have constant 0.5A load current at the output. PCB has 4-layer stack up; 0.1T-0.8T-0.1T. As shown in Fig.2, top and bottom layer are assigned for signal traces and Vin, Vout and GND. Layer 2 is assigned for solid GND plane including an island for Vin, Vsw and Vout nodes. Layer 3 is for Vout plane and an island for Vin and Vsw nodes. Because of the high current density at the Vin and Vsw nodes, Vin and Vsw nodes are laid out from top to bottom with bunch of through hole vias for the purpose of heat spreading [9]. Component placement and layout of the top layer is based on the evaluation board from the PWM controller vendor and modified to follow guidelines in [9]-[10].

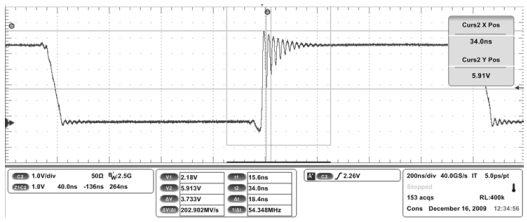


Fig. 3. Measured switching voltage waveform at Vsw node of the designed synchronous DC-DC buck converter

From a sequential turn-on and turn-off operations of Q1 and Q2, switching voltage waveform is measured at Vsw node as shown in Fig. 3. The switching voltage is high up to Vin and has broadband frequency components up to a few hundred MH. Accordingly, Vsw node becomes potential EMI and switching noise source and determines the amount of radiation and coupled noise at the output.

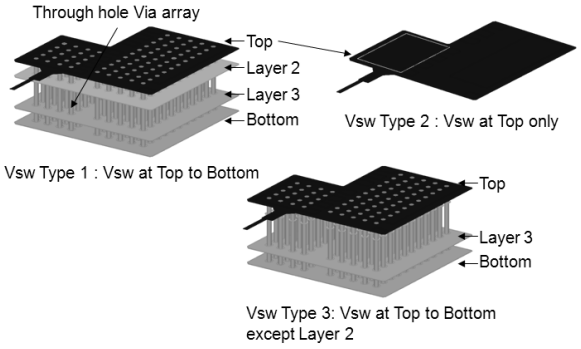


Fig. 4. Three types of Vsw node design for test benches

Fig. 4 shows three types of Vsw node designed for test benches. In the test benches, the exposed area of Vsw node on the top layer is kept as small as possible to reduce an electrical coupling to surround structure [11]. In Vsw Type 1, Vsw node is extended from top to bottom to compensate the heat spreading capability of the small exposed area on top, as forementioned in reference PCB design. In Vsw Type 2, Vsw node is only at the top layer. Vsw Type 2 is the control test bench to verify how the heat spreader affects the amount of EMI and switching noise at the output. In Vsw Type 1, the solid GND plane at layer 2 cannot locate right under Vsw node on top layer. This may affect EMI and amount of the switching noise by increasing of current loop inductance [5]. Vsw Type 3 is to verify the impact of solid GND plane underneath the Vsw node on the top in EMI and amount of the switching noise.

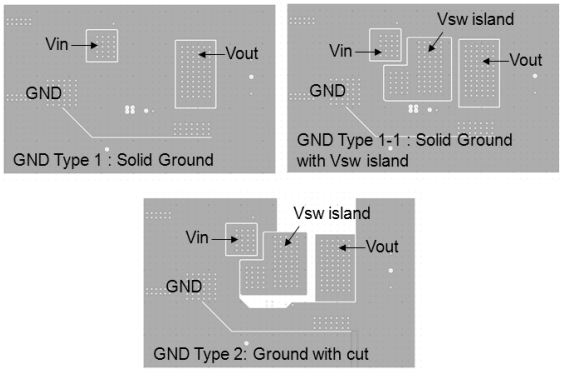


Fig. 5. Three types of GND plane design for test benches

For the intent to Vsw Type 3, three types of GND plane for layer 2 are designed for test benches as shown in Fig. 5. Table I summarizes total 5 types of test benches are designed by combination of the Vsw node designs and the GND plane designs. 'Ref_fill' is the reference PCB layout shown in Fig. 2.

TABLE I
TEST BENCH SUMMARY

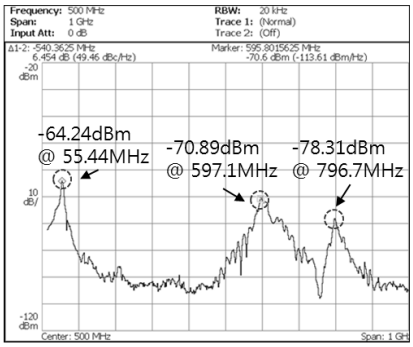
Type	**Composition**	
	Vsw type	**GND type**
Ref_unfill	Vsw type1	GND type 2
Ref_fill	Vsw type1	GND type 1-1
Top_unfill	Vsw type2	GND type 2
Top_fill	Vsw type2	GND type 1
Top_fill2	Vsw type3	GND type 1

III. MEASUREMENT RESULT

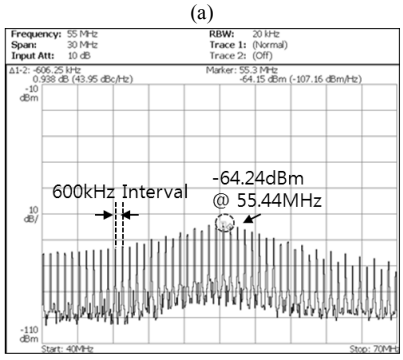
Over 5 test benches, TEM cell measurement was performed. 5V DC power is provided to the test benches from the outside of TEM cell to operate the test benches. Coupling between TEM cell and test benches are measured with Spectrum Analyzer from DC to 1 GHz. Then, the switching noise at the converter output was measured with the oscilloscope. The noise voltage is captured by a high-impedance probe at Vout_sma node in Fig. 2.

A. TEM cell measurement result

Fig. 6 shows measured coupling between TEM cell and 'Ref_unfill' test bench. From DC to 1 GHz, there is 3 high coupling peaks at 56 MHz, 616 MHz and 796 MHz. When the span is down to 30 MHz, it is revealed that each peak is a set of peaks of 600 kHz component, which is the switching frequency of the test benches, and its harmonics, as shown in Fig. 6 (b).



(a)



(b)

Fig. 6. TEM cell measurement result of 'Ref_unfill' (a) From DC to 1GHz (b) From 25MHz to 55MHz

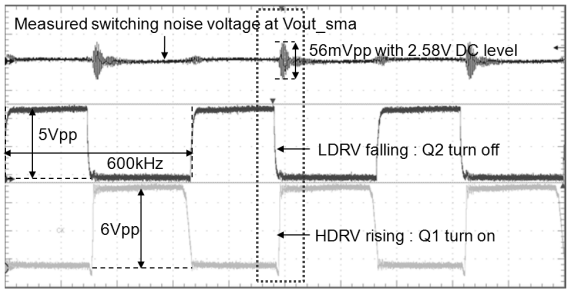
All test bench has 3 peaks as same as 'Ref_unfill' in Fig. 6. Only the frequency and magnitude of peaks differ from the test benches. The TEM cell measurement result over 5 test benches are summarized in Table II. 'Ref_unfill' and 'Top_unfill' have almost same frequency and magnitude of peaks. It means that the heat spreader for Vsw at layer 2, 3 and bottom (Vsw Type 2) doesn't affect the radiation when a solid GND plane is not located right under Vsw node on top layer (GND Type 2). On the contrary, with GND Type 1 and 1-1, test benches with Vsw Type 2 and 3 ('Top_fill' and 'Top_fill2') are superior to the test bench with Vsw Type 1 ('Ref_fill'). The origin of peaks and the difference between test benches will be explained in more detail in chapter IV.

TABLE II
SUMMARY OF TEM CELL MEASUREMENT RESULT OF TEST BENCHES

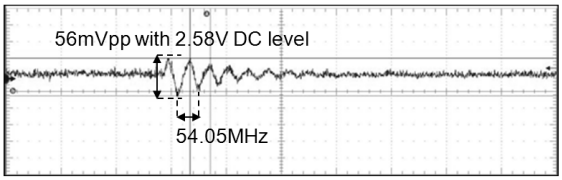
Type	Frequency and magnitude of peaks		
	1st peak	2nd peak	3rd peak
Ref_unfill	-64.24 dBm @ 55.44 MHz	-70.89 dBm @ 597.1 MHz	-78.31 dBm @ 796.7 MHz
Ref_fill	-66.99 dBm @ 56.86 MHz	-83.58 dBm @ 613.4 MHz	-87.78 dBm @ 795.3 MHz
Top_unfill	-64.81 dBm @ 51.45 MHz	-70.9 dBm @ 605.1 MHz	-81.18dBm @ 794.6 MHz
Top_fill	-71.21 dBm @ 67.75 MHz	-88.31 dBm @ 613.7 MHz	-91.35 dBm @ 795.5 MHz
Top_fill2	-70.27 dBm @ 64.77 MHz	-88.99 dBm @ 614.8 MHz	-93.07 dBm @ 795.5 MHz

B. Time-domain measurement result of switching noise at the converter output

Fig. 7 (a) shows the measured switching noise voltage at Vout_sma of 'Ref_unfill' with LDRV and HDRV signal. It tells that rising of HDRV signal is the source of the switching noise [5]. The frequency of the switching noise, 54.05 MHz, is almost same as the frequency of the first peak of TEM cell measurement result of 'Ref_unfill'. It means that the switching noise from HDRV rising is the origin of the 1st peak in TEM cell measurement. This is confirmed by the other test benches. Table III summarizes the frequency and the magnitude of measured switching noise over the test benches. All test bench showed similar shape of switching noise waveform at Vout_sma when HDRV signal rises. Same as 'Ref_unfill', the frequencies of the switching noise of the test benches match the frequency of the 1st peak in TEM cell measurement. Since it is revealed that the switching noise is the origin of the 1st peak in TEM cell measurement, it can be easily explained the magnitude variation of the switching noise over the test benches match the magnitude variation of the 1st peak in TEM cell measurement. A detailed analysis on the measurement result of switching noise will be described in chapter IV.



(a)



(b)

Fig. 7. Measured switching noise voltage at Vout_sma of 'Ref_unfill (a) Triggered with LDRV and HDRV signal (b) Detailed view of the measured switching noise

TABLE III
SUMMARY OF MEASURED SWITCHING NOISE VOLTAGE AT VOUT_SMA OF TEST BENCHES

Type	Frequency and magnitude of measured switching noise
Ref_unfill	54.05 MHz, 56.67mVpp
Ref_fill	57.14 MHz, 82.5mVpp
Top_unfill	54.05 MHz, 60.83mVpp
Top_fill	68.97 MHz, 19.17mVpp
Top_fill2	66.67 MHz, 20.83mVpp

IV. Analysis of Measurement Result the with Impedance Measurement of Vsw node

A. Analysis of TEM cell measurement result

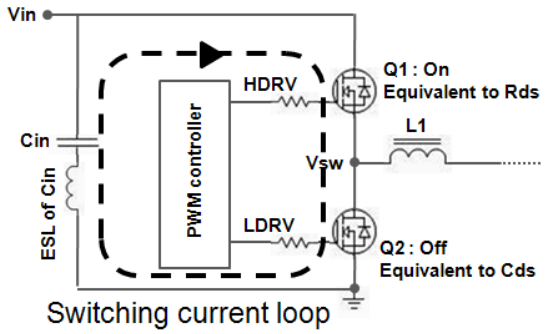


Fig. 8. Measured self-impedance (Z11) seen at Vsw node of test benches

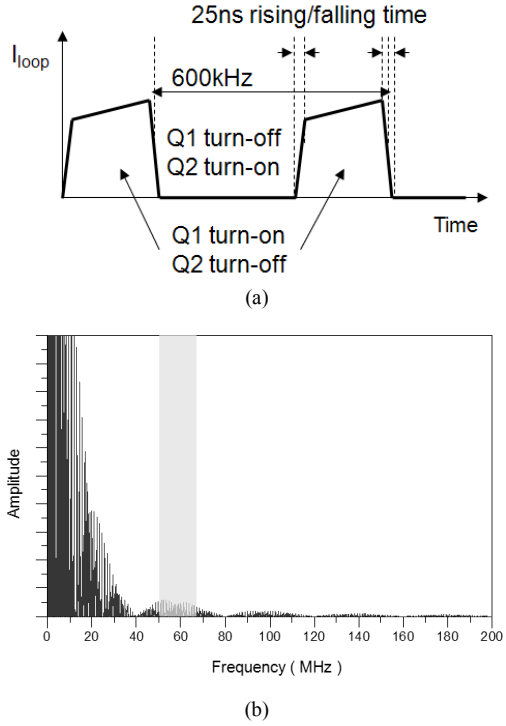


Fig. 9. (a) Time and (b) frequency domain waveform of the current flowing the switching current loop

It is revealed that the switching noise is the origin of the 1st peak in TEM cell measurement in chapter III. [5] reports that the switching noise is caused from a switching current loop shown in Fig. 8. Because the switching current flowing on the switching current loop is fixed as Fig. 9, a reactance of the switching current loop determines the magnitude of the switching noise and EMI. The switching current loop can be evaluated with a self-impedance measurement. Fig. 10 shows the measured self-impedance (Z11) from 300 kHz to 1 GHz at Vsw node of test benches. To see the impedance of the switching current loop, Q1 is forced to be on and Q2 is off during the measurement.

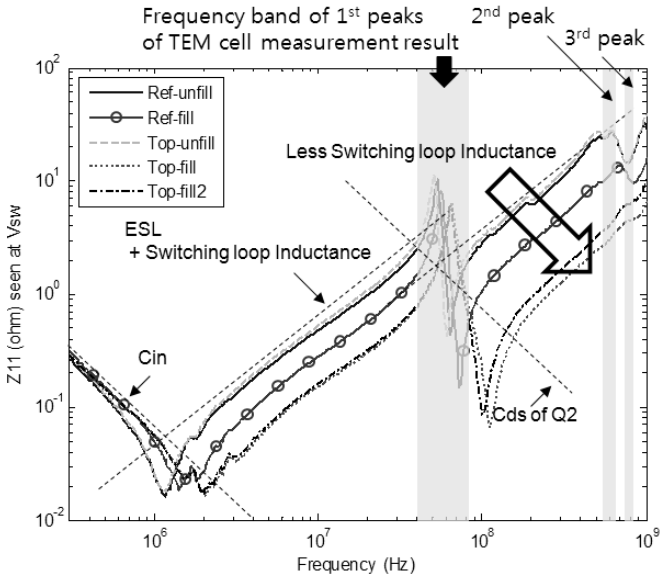


Fig. 10. Measured self-impedance (Z11) seen at Vsw node of test benches when Q1 is on and Q2 is off

Z11 for all test benches have the resonance peak around 50MHz. It is due to a parallel resonance of Cds of Q2 (~2nF), and the sum of switching loop inductance and ESL of Cin (~5nH). The 1st peaks of TEM cell measurement can be explained from the resonance peak.

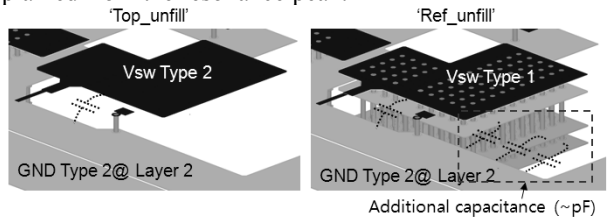


Fig. 11. The heat spreader of 'Ref_unfill" only gives additional pF order of capacitance.

'Ref_unfill' and 'Top_unfill' have almost same frequency and impedance of the resonance peak. This is why 'Ref_unfill' and 'Top_unfill' have the same 1st peak in TEM cell measurement result. Two test benches have same GND type (GND Type 2). The Vsw design doesn't affect the resonance peak since the additional capacitance by the heat spreader in 'Ref_unfill' is only a few pF as shown in Fig. 11. On the contrary, GND design directly affects the switching loop inductance. The same GND Type makes the same resonance peak; 'Ref_unfill' and 'Top_unfill'. Less switching loop inductance makes the resonance peak lower and moves the peak to higher frequency. Among the GND designs, GND Type 1 is the ground plane design which provides the lowest switching loop inductance. It explains why 'Top-fill' and 'Top-fill2' showed the lowest 1st peak in the highest frequency in TEM cell measurement.

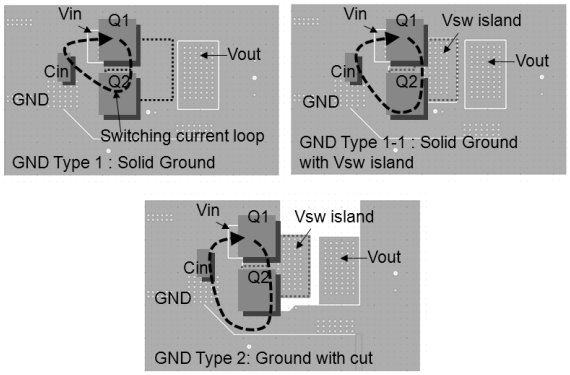


Fig. 12. Switching current loop size of each GND Types.

The self-impedance also can give an answer for the 2nd and 3rd peak of TEM cell measurement. Because the Vsw node acts like an antenna, the self-impedance of the Vsw node determines the amount of radiation of those peaks despite of the origin of those peaks; recovery of the body diode associated with Q2 [12]. For this reason, 2nd and 3rd peak is also the lowest in 'Top-fill' and 'Top-fill2'; 'Top-fill' and 'Top-fill2' have the lowest impedance at the frequency band of 2nd and 3rd peak as shown in Fig. 10.

B. Analysis of time-domain measurement result of switching noise at the converter output

Since the switching current is fixed, the measured switching noise at converter output (Vout_sma) can be explained with transfer-impedance (Z21) between Vsw node and Vout_sma. Fig. 13 shows the measured transfer-impedance between Vsw node and Vout_sma of test benches. Just same as the measured self-impedance, transfer-impedance shows the resonance around 60 MHz. The resonance frequency of transfer-impedance and its magnitude well match with the measured switching noise at Vout_sma. The transfer impedance is getting higher when the frequency goes over 100 MHz. However, the switching noise doesn't have much energy over 100 MHz as shown in Fig. 9 (b). That is why the measured switching noise at Vout_sma over test benches only has the frequency components around 60 MHz.

V. CONCLUSION

Layouts of the GND plane and the high-voltage AC node (Vsw) for a synchronous DC-DC buck converter with 4-layer stack-up PCB have been evaluated on their EMI and switching noise generation. From the TEM cell measurement and the time-domain measurement of switching noise at the converter output, it was found that the solid GND plane right under the Vsw is the best design for synchronous DC-DC buck convert with multi-layer stack-up PCB in terms of EMI and switching noise generation. Impedance measurement tells that a key to the best design is controlling the inductance of the switching current loop. It is found that a design which gives the lowest inductance for the switching current loop will have the lowest EMI and switching noise no matter what the source of EMI and switching noise is.

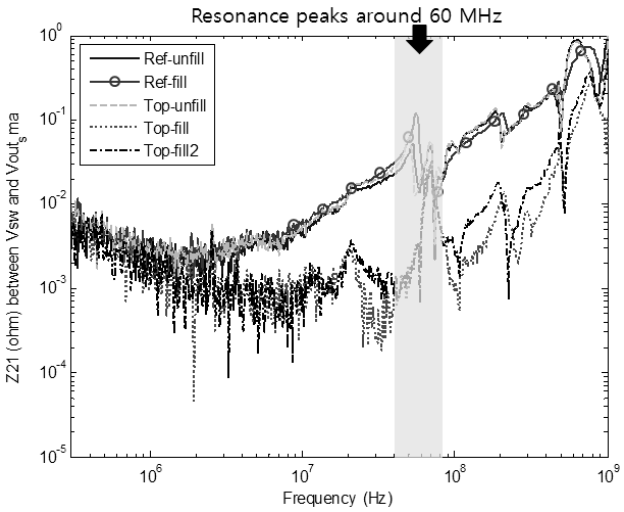


Fig. 13. Measured transfer-impedance (Z21) between Vsw node and Vout_sma of test benches

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