DC-DC Buck Converter EMI Reduction Using PCB Layout Modification

Ankit Bhargava, *Member, IEEE*, David Pommerenke, *Senior Member, IEEE*, Keong W. Kam, *Member, IEEE*, Federico Centola, and Cheng Wei Lam

***Abstract*—The paper treats the effect of layout on the electromagnetic interference (EMI) of buck converters. An optimized layout design for dc-dc synchronous buck converter is proposed for EMI reduction. Six different layout versions are analyzed with respect to loop area, loop inductance, radiating dipole moments, and far-field radiation. Optimizations are done with respect to field-effect transistor (FET), decoupling capacitor and via placement. Passive full-wave simulations are used to estimate and verify the loop inductance and far-field emissions. Those are compared with measurements. A gigahertz transverse electromagnetic (GTEM) cell is used to quantify the dipole moments in the printed circuit board (PCB) for estimating the far field and comparing to measurement.**

***Index Terms*—DC-DC buck converter, EMI/EMC, loop inductance, PCB layout.**

I. Introduction

THE switching nature of dc-dc synchronous buck converters can cause significant electromagnetic interference (EMI) issues. Three mechanisms contribute to the EMI:

1) the harmonics of the switching frequency, usually below 30 MHz;
2) the ringing of the phase voltage loop [1], [2], usually between 50–300 MHz; this problem is addressed in the following work; the ringing is caused by a loop formed from the high-side (HS) FET (on), the low-side (LS) FET (off), and the input decoupling capacitors;
3) and, the reverse recovery noise usually seen above 200 MHz [13].

There are circuit (KVL, KCL) and layout (electromagnetic) related methods for controlling the EMI. This paper mainly focuses on the layout related methods. However, it is worth to briefly review circuit related methods.

A popular choice to suppress the ringing is an RC snubber circuit, which is placed across the low-side FET to add RF loss [10], [11]. For low-inductance loops, an RL snubber added in series within the loop offers advantages in suppressing the ringing [3], or, the ESR of capacitors can be used to suppress the ringing.

The selection of MOSFETs and its drive circuitry will also affect the ringing. Ringing is influenced by the switching times, values of $C_{\mathrm{oss},}$ and losses in the output capacitance. To allow us to concentrate on layout effects, the same driver and FET combination was chosen throughout this paper: Intersil ISL6269IRZ as PWM controller, FDMS8692 as HS FET, and FDMS8672 as LS FET.

Another additional loss contributing to the attenuation of the ringing is the real part of the output capacitance C_{oss}. We assign a value "R_{oss}" to it, which can be determined by measurements [4], [14]. An equivalent circuit for the low-side FET, when it is turned OFF, can be realized, as shown in Fig. 1.

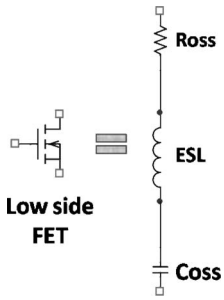

Fig. 1. Equivalent for the low side FET.

More layout-related known methods are:

1) Reducing the loop inductance: Two plausible, but not always valid lines of thought show that a reduced loop inductance is likely to reduce the EMI. The resonance frequency moves up, however, the excitation rolls off with frequency, thus the loop will be excited less strongly. Second, if the losses of the loop stay constant, then the attenuation will increase, as the ratio of L/R diminishes [2], [3].
2) Layout optimization for geometry-based design strategy.
3) Input and output filtering [2].

This paper mainly focuses on the layout optimization methods and gives an insight into the physical structure of the loops to suppress EMI. This way EMI issues can be dealt on the PCB level.

Fig. 2. shows the circuit schematic of a buck converter.

A synchronous buck converter is a step down dc-dc converter. It uses two complimentary switches and an inductor and a capacitor at the output stage. The two MOSFETs switch alternatively connecting the inductor to the source. The energy is stored in the inductor and then discharged into the load

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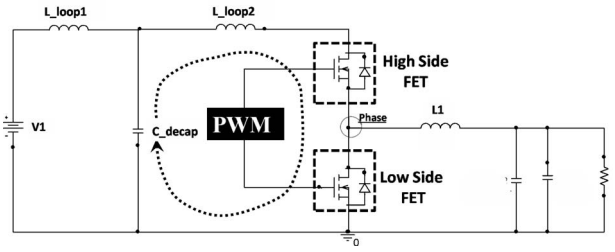


Fig. 2. Schematic of a buck converter.

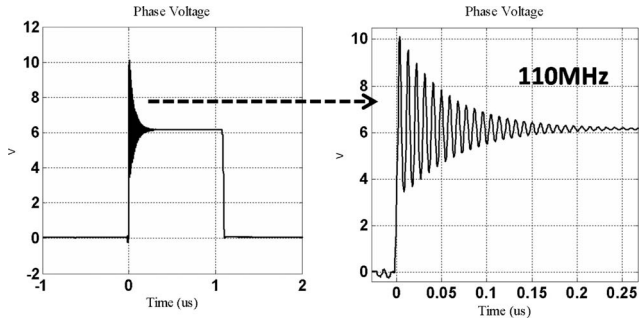


Fig. 3. Voltage measured at the phase node.

depending on the switching state. The duty cycle determines the output voltage [12].

The two MOSFETs switch alternatively. To understand the nature of the LC loop, consider a state when the high-side FET is "ON" and the low-side FET is "OFF." A loop is formed by the input decoupling capacitor (C_decap) and the two switching MOSFETs [2]. The low-side FET (off state) forms a capacitor, of which the value is given by $C_{\rm oss}$ in the datasheets. The inductance due to this loop is shown as a distributed inductance $L_{\rm \_loop2}$ while $L_{\rm \_loop1}$ is the inductance to the dc net.

To understand the excitation of the loop, we need to consider the moment at which the high-side FET turns ON. Two factors contribute to the excitation of the loop. Suddenly, current is provided by the input capacitance into the low-side FET capacitance, raising its voltage within usually a few nanoseconds. Second, the body diode of the low-side FET will undergo reverse recovery. Both factors contribute to overshoot and the ringing of the LC loop.

Most of the noise current will not reach the output side of the converter, as the main inductor will block this current. It is often at or close to self-resonance at the ringing frequency, thus it provides a high-impedance path, further filtered by the output capacitors. On the input side large currents flow through the input capacitor, thus, conducted noise coupling is more likely on the input side then on the output side of the buck converter. The lower the loop inductance, the more critical the input filtering will be. The ratio of loop inductance and effective inductance of the input capacitors determines the filtering. If, e.g., the loop has only 2 nH of inductance, and the effective inductance of the input capacitors is 0.5 nH, then the inductive 10 V ringing might lead to 2.5 V ringing on the input side. Of course, the distributed nature of the input filtering is not considered in this simplified illustration, but reducing the loop inductance places stronger demands on the filtering of the input side. Otherwise, the input voltage rail will distribute the ringing noise throughout the system. Besides conducted coupling, coupling can occur via the electric field from the PCB area that forms the phase voltage node, calling for a minimization of the surface area of this node. Finally, we need to consider magnetic field coupling caused by the current in the loop.

Fig. 3 shows the phase voltage node of the buck converter investigated.

To mitigate the EMI issue the loop inductance should be minimized. However, minimal inductance not necessarily leads to minimal EMI, since the noise coupling is not only dependent on the loop size but field distribution/orientation. A small loop might couple stronger to the surroundings than a large loop. In this investigation, three often used FET arrangements have been used. They differ in the orientation of the LC-loop. At first, each of the FET arrangements was optimized for minimum loop inductance, and then the EMI was compared.

The stack-up of the variants was as follows:

Layer 1: Signal Layer (PWM, inductor, FET (in one variant))

Layer 2: Solid Ground Plane

Layer 3: Solid Ground Plane

Layer 4: Signal Layer (FETs, decoupling capacitors)

II. Optimized PCB Layouts Under Investigation

The basic purpose of optimizing the PCB layouts was to minimize the loop inductance by the following methods:

1) The decoupling capacitors were placed as close as possible to the FETs [3].
2) The MOSFETs were also placed at a minimum distance from each other.
3) The vias were placed after carefully examining the current path in the loop. This is discussed in greater detail in Sections III and V.
4) The size of the phase plane was kept as small as possible to reduce electric field coupling [3].
5) The MOSFET package style influences the loop inductance, and for optimized layouts if the package style could, dominate the loop inductance. All investigations have been performed using the same, low-inductance POWER 56 package.

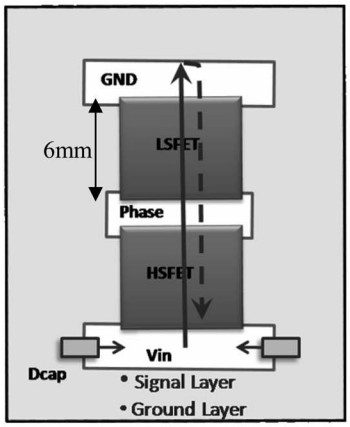
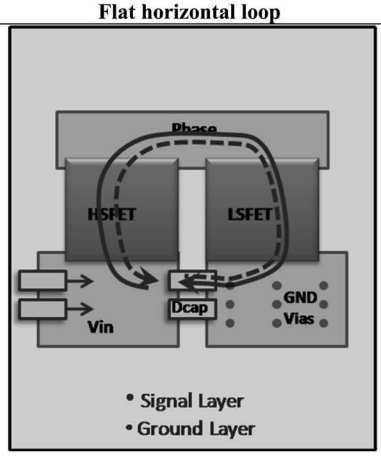
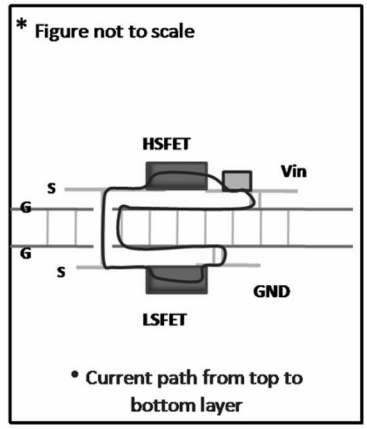
The next paragraph introduces the three main designs.

Table I compares the three PCB layout designs.

The vertical loop layout is designed by placing the FETs such that all the high-frequency current returns in the loop through the ground plane below the FETS, as shown in Fig. 4. The path for the high frequency noise current is shown using arrows where dashed lines show the return current path. The HF current flows from the input patch, passing the two FETs. The current loop is completed through the ground plane where the decoupling capacitors provide the return path to the Vin plane.

Goal for designing the flat horizontal loop was making the current flow horizontally above a ground plane. This is shown in the second column of Table I.

TABLE I
COMPARISON OF THE THREE PCB LAYOUT DESIGNS

	Vertical loop	Flat horizontal loop	Two sided vertical loop
PCB layouts designs			
Current paths	Vin→ HSFET→Phase plane→ LSFET→ GND plane→Dcaps→ Vin	1. Vin→HSFET→Phase plane →LSFET→GND→Dcaps→Vin 2. Vin→HSFET→Phase plane →LSFET→GND plane→ Dcaps→Vi	Vin→HSFET→Phase (top layer)→ phase (bottom layer) → LSFET→ GND plane→ Dcaps→ Vin
Loop area approximation	This can be considered as a horizontal rectangle with an area: A= 18mmX0.25mm = **4.5mm²**	This can be considered as a flat rectangle with an area: A= 6mmX6mm = **36mm²**	The area can be approximated by splitting into 3 rectangles: A= 8X0.2 5+ 1X0.4 + 8X0.25 = **4.4mm²**
L_{loop} (measured)	2.5nH	2.41nH	2.7nH

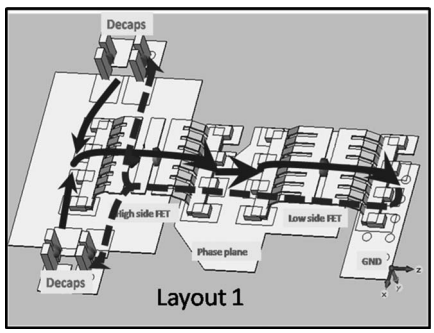


Fig. 4. Vertical loop in full wave.

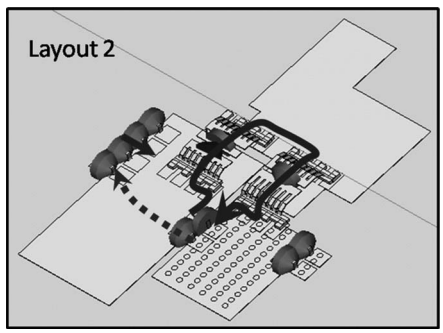


Fig. 5. Flat-horizontal loop in full-wave.

Most of the current returns directly on the top layer through the two decoupling capacitors connected between the ground fill and the Vin plane. However, there is a second current path: The current flows to the ground plane through GND vias and returns through the two decoupling capacitors on the left side of the high-side FET. In short, the noise current in the loop splits into a horizontal and a vertical path.

Measurements and simulations have shown that most current flows in the horizontal loop path. The horizontal loop design has a large loop area (36 mm^2 relative to 4.5 mm^2); however, its inductance is about the same. This is because of the current induced in the ground plane directly underneath the horizontal loop. This current compensates large parts of the magnetic field of the horizontal loop; however, the fraction of the current that flows in the remaining vertical loop is not compensated for.

The "both sided vertical loop" places the two FETs on top and bottom layers of the PCB, as shown in Fig. 6. Via placement is critical. Both ground planes are well-viaed together, such that no flux can penetrate between the planes. This reduces the inductance.

Table I shows that all loops have about the same inductance. The larger loop area of the horizontal loop design does not lead to larger inductance, due to the presence of the eddy current in the ground plane. Simulations using a perfectly flat package instead of the real package have shown that L_{loop} is dominated by the height of the package itself. Since we use the same package for all the designs, the inductances are similar.

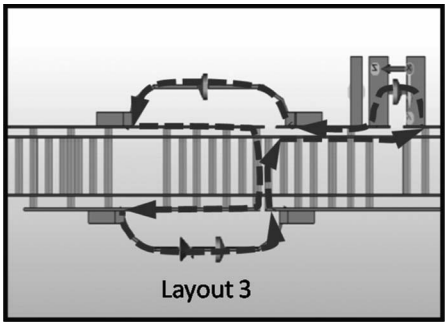


Fig. 6. Two-sided vertical loop 3 in full-wave.

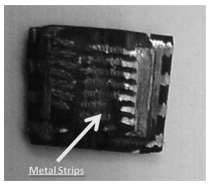


Fig. 7. Metal strip connection inside the FET package.

III. Full-Wave Modeling of DC-DC Buck Converters

Full-wave modeling of the passive structure and PCB layout of buck converter is an excellent method to analyze the parasitic loop inductance and EMI coupling. This section provides a simulation guideline and some key points to remember while modeling the structure. The three full-wave structures are as shown in Figs. 4–6

Simulating the complete circuit in a combined full wave and SPICE solver is not easy, as most power MOSFET models are not designed to provide valid results up to a few hundred MHz.

In spite of the large physical FETs the loop inductance is as small as 2 nH, thus small details inside the loop need to be modeled:

1) MOSFET Package: The lead frame and the connecting metal strips are part of the model, Fig. 7.
   If the FETs are modeled as ideally flat, the loop inductance drops from 2.4 nH to 0.5 nH.
2) The capacitors are modeled in their original dimensions using a discrete capacitor between both metal contacts.

Loop inductance simulation concept: The loop inductance is calculated via the resonance frequency. For this the high-side FET is set to $R_{\mathrm{ds(on)}}$, a few mOhm, while the low-side FET is set to be a capacitor having the value of C_{oss}. The loop is excited in time domain by a discrete port located in the high-side FET as well to obtain S_{11}. Using the known C_{oss} the inductance is determined from the observed resonance.

The impedance looking into the loop is shown in Fig. 8.

Besides S_{11} the far field was calculated. Both data sets are compared to measurement.

IV. Loop Inductance and Far-Field Measurement

All three layouts show similar phase voltage waveforms. Fig. 9 shows the ringing measured at the rising edge of the three layouts.

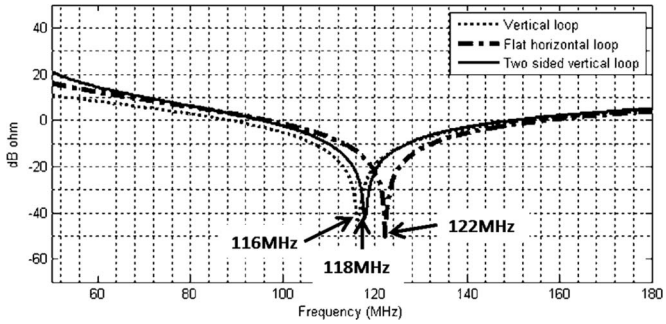


Fig. 8. Impedance looking into the loop.

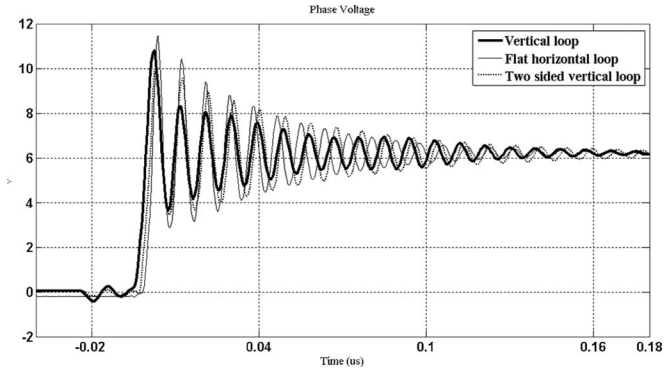


Fig. 9. Ringing measured at the ringing edge of the phase voltages.

TABLE II
Comparison of the Measured and Simulated Loop Inductances

	Loop Inductance comparison		
	Ringing Frequency (measured)	**L_{loop} (measured)**	**L_{loop} (simulation)**
Loop Layout 1	111MHz	2.5nH	2.4nH
Loop Layout 2	114MHz	2.4nH	2.4nH
Loop Layout 3	108MHz	2.7nH	2.5nH

A comparison of the measured and simulated loop inductances is as shown in Table II.

Table II shows that the loop inductances are similar. However, does this mean the far-field radiations are similar?

The far field is first verified using full-wave simulations. The dc feed cable was not considered. During the measurements, we added ferrites to the feed cable and verified that the cable position has no significant influence anymore. A broadband field monitor was used in a time domain full-wave solver (CST-MWS) to monitor the far-field radiation at a distance of 3 m. The radiation pattern at the resonance frequency was obtained in dBμV/m and the magnitudes of the major lobe were compared for all the three test boards. The frequency domain results in CST Microwave studio are normalized to 1 W of input power but the time domain results are not normalized [6].

The three radiation patterns were obtained in the x-y plane in horizontal polarization and the planes are shown in Fig. 10. The

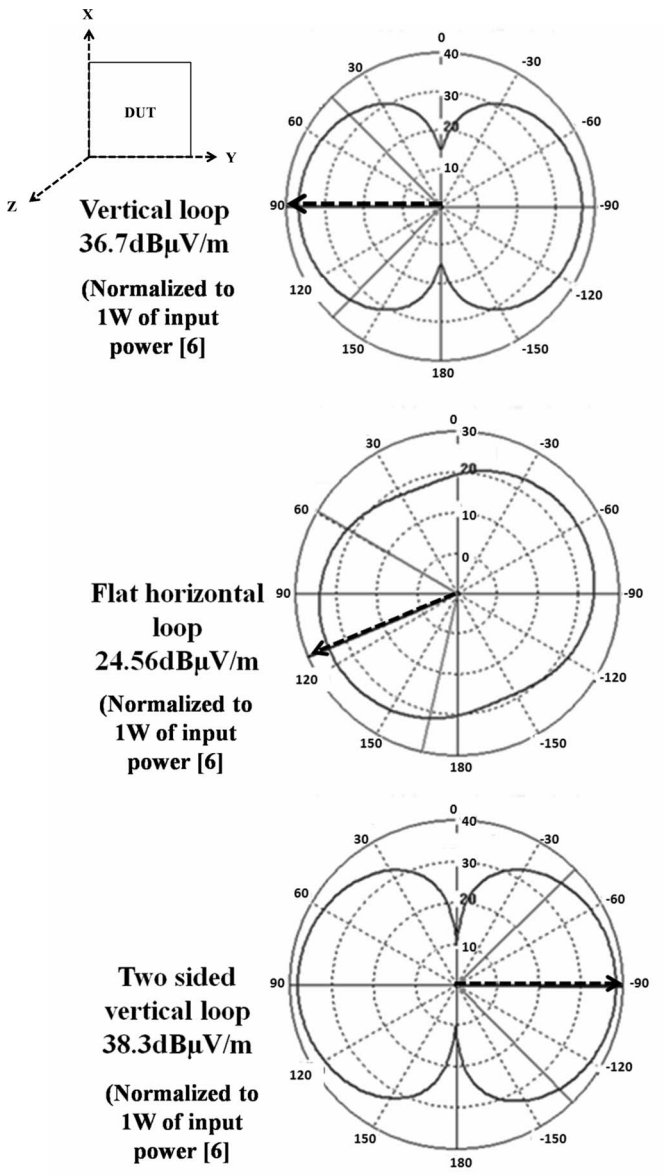


Fig. 10. Far-field radiation patterns from full-wave solver.

radiation pattern was obtained the at the resonance frequency and the magnitude of the major lobe was taken as the maximum radiated far field. Fig. 10 shows the radiation patterns as obtained in the full-wave far-field simulation of three test boards. The black dashed arrows show the direction of maximum radiation or the magnitude of the major lobe.

The simulation setup consists of the loop structure on a 10 cm $\times$ 10 cm printed circuit board. The simulation was performed in free space and, therefore, can be considered as fully anechoic. A similar setup was used for the far-field measurement. The floor in the measurement chamber was covered with ferrite tiles to eliminate the effect of the ground plane. The measurements were maximized with respect to the turn-table rotation and antenna height.

As stated before, the far-field simulation spectrum is normalized. In order to have a valid comparison between measurement

TABLE III
COMPARISON BETWEEN THE SIMULATIONS AND THE MEASUREMENTS

	Measurement (dB)	Simulation (dB)
Board 1	-34.25	-36.02
Board 2	-44	-44.20
Board 3	-34.5	-34.98

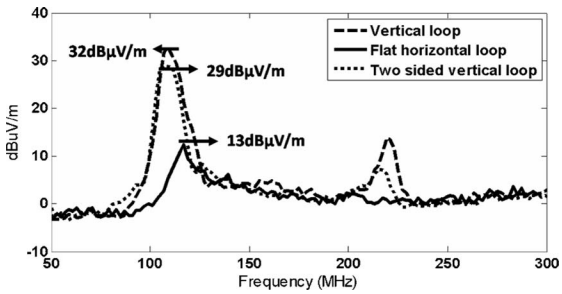


Fig. 11. Far-field comparison for three test boards.

and simulation, the transfer function (ratio) between the loop current and the far field were compared in both measurement and simulation. In the measurement, the loop current was calculated from the measured phase voltage spectrum with same instrument settings as the far-field measurement. The transfer functions obtained from the simulation and measurements are shown in Table III.

The comparison in Table III shows the similarity between the simulations and the measurements.

The simulation shows that the vertical loops have similar far-field radiation while flat horizontal loop has lower radiation by over 10 dB, as shown in Fig. 10. These are the values in the direction of maximum radiation at the resonance frequency.

Further, the standard far-field measurements were done in a semianechoic chamber using a log periodic antenna at a distance of 3 m from the DUT. A maximized far-field measurement was performed by placing the DUT in all possible orientations and by varying the height of the antenna. It is expected to receive maximum signal at the resonance frequency. The measured broadband far-field radiation is as shown in Fig. 11.

It can be clearly noticed that test board 2 (horizontal loop) radiates 10 dB less than the other designs. In the horizontal loop design compensation current is flowing in the ground plane directly underneath (image plane), generating a nearly equal but opposite vertical magnetic field [17]. The compensation loop helps to reduce the total H-field radiation and suppresses the EMI.

V. IMPACT OF GROUND VIA LOCATION

In the flat horizontal loop part of the HF noise current in the loop also returns through the ground plane. The ground vias near the low-side FET provide the path to the ground and carry all the noise current flowing on the ground layer. This might affect the signal integrity of a nearby signal. The noise current through the vias could easily couple to nearby signal vias. Also, it would reduce the HF noise current on the ground plane. The main goal in rearranging the ground vias is to force all the HF noise current on the top layer and minimize the current flowing

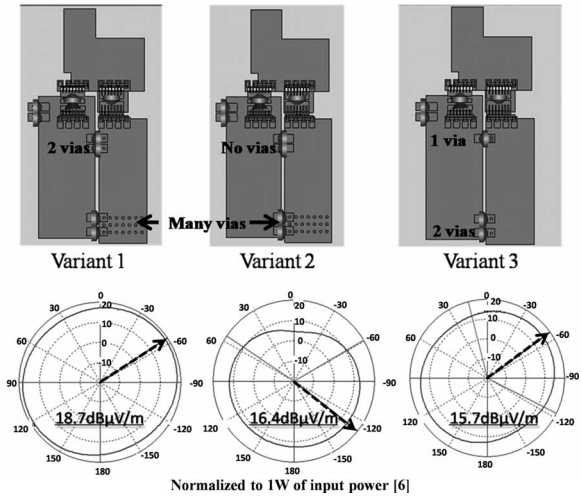


Fig. 12. Via arrangement variants for horizontal loop.

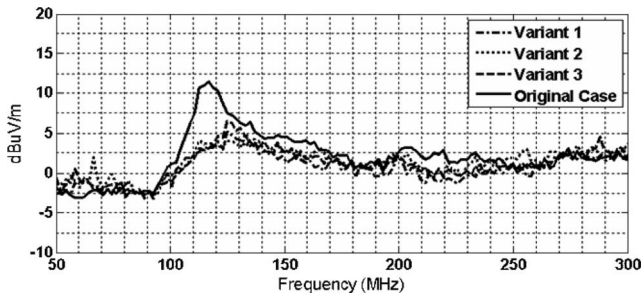


Fig. 13. Far-field measurements in comparison to original case.

through the ground vias. It is interesting to find the impact of via location on $L_{\rm loop}$ and far field. It can be achieved by shifting the ground vias away from their original location. In this case, the vias were shifted 1 cm away from their original position. Fig. 12 shows three different via configurations, their loop inductances and the far-field simulation results. These are further compared with measurement, which is shown in Fig. 13.

The variant 1 and 2 had many vias far away from the low-side FET and no or very few vias near the FET. Variant 3 had very few vias at both the ends. As the vias are shifted further away, more and more noise current is forced to flow on the top layer. However, small amount of noise current flows on the ground through the vias. The compensation loop in this case is more effective as most of the noise current flows on the top layer. Fig. 14 shows the current distribution at resonance through different capacitors in variant 2 (from full-wave simulation). G1, G2, and G3 are the decoupling capacitors while G4 are the bulk capacitors. Most of the noise current is forced to return through the horizontal loop.

The loop inductance reduces by 0.4 nH. The loop inductance measurement and simulation is 2 nH and 2.19 nH, respectively. The far-field measurement and simulation also show the effectiveness of the compensation loop. The far-field radiation further decreases by 5 dB, as shown in Fig. 13. It was also noticed that number of GND vias near the FETs does not really make a big difference in $L_{\rm loop}$ and far-field radiation.

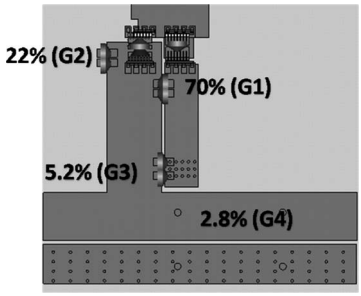


Fig. 14. Current distribution at resonance frequency in variant 2.

VI. Comparison on the Level of Dipoles Moments Using GTEM Cell

Radiation sources of a not too complex far field can often be modeled by a small set of elementary dipoles. Here, one needs to distinguish between the dipole moments of a circuit on a board, relative to the dipole moments of the board itself. In a TEM cell measurement, the board is mounted to the side of the TEM cell, making it electrically infinitely large [5], [15]. This measures the dipole moments of the circuit. In a GTEM cell the complete board is mounted in free space, thus the GTEM cell is excited by the board, not only by the circuit. Here, the circuit will excite the board and then couple to the GTEM cell.

The DUT can be placed and rotated inside the GTEM cell. Each test board can be represented as an equivalent E and H dipole moment. This way, all the layout designs can be compared on the level of dipole moments and dominating dipole moments can be identified. The measurements in the GTEM cell can be further used to correlate to the OATS results (in this case, measurements were done in the far-field chamber at 3 m).

P. Wilson [7] suggests three different methods to estimate the dipole moments in a GTEM cell. This paper uses nine measurement methods.

The EUT is modeled as a set of multipoles and only the initial dipole terms are retained as explained in [7]. The TEM cell measurements are used to determine the magnitude of the dipole moments. The DUT emissions in the free space or over a ground plane are simulated based on dipole moments.

For the nine measurement approaches, the EUT has to be placed in nine different orientations and the radiated power inside the GTEM cell is measured [7]. The measurement procedure is already explained well in [7]–[9]. The power measured at the port of the GTEM cell in nine measurements can be processed for calculation of E and H dipole moments. The radiation in the GTEM cell is well documented in [7]–[9] and, therefore, a summery of the theory is provided.

TEM mode will be excited in the cell according to [7]. The excitation coefficients for the TEM mode are given by (2).

$$\begin{pmatrix} a_o \\ b_o \end{pmatrix} = -\frac{1}{2}(Py \pm jk_o M_x)e_{oy} \tag{1}$$

where P and M are the electric and magnetic dipole moments, respectively. Eoy is the vertical component of the electric field at the EUT location [7], [8].

TABLE IV
VECTOR ADDITION OF CALCULATED VALUE OF E AND H DIPOLE MOMENTS ALONG EACH AXIS FOR THE THREE MAIN TEST BOARDS WITH DIFFERENT LOOP ORIENTATIONS

	Electric dipole moment P	Magnetic dipole moment koM
B1	0.236 μ	0.385 μ
B2	0.117 μ	0.107 μ
B3	0.25 μ	0.35 μ

The measured power at the GTEM cell port is normalized by $(1/4)e_{oy}^2$. $|a_o|^2$ and $|b_o|^2$ are the powers carried at the port of the GTEM cell [8]. The normalized power at the port is given by (3) [7].

$$|b_o(\alpha)|^2 = P_y^2 + k_o^2 M_x^2. \tag{2}$$

The nine measurements can be related to the electric and magnetic dipoles along *x*, *y,* and *z* axis using (2). Therefore, nine different equations are obtained. These equations can be solved simultaneously to obtain the values of *Px, Py, Pz, Mx, My,* and *Mz* as a function of frequency [7]. Once all the six unknowns are obtained, the vector magnitude of electric dipole moment *P* and magnetic dipole moment *M* can be found from (3).

$$P = \sqrt{P_x^2 + P_y^2 + P_z^2}$$
$$M = \sqrt{M_x^2 + M_y^2 + M_z^2}. \tag{3}$$

Table IV shows the vector addition of calculated valued of E and H dipole moments along each axis for the three main test boards with different loop orientations.

It is to be noted that *P* and k_oM have the same units and, therefore, they can be directly compared [7]. The magnetic dipole moments of the vertical loops are about three times stronger than the flat horizontal loop.

Maximum far-field strength can be predicted from the radiated power inside a GTEM cell. According to [7], the power measured in the three basic positions can be used to predict the maximized far-field strength using (4).

$$P_o = 10k_o^2(b_{11} + b_{22} + b_{33}) \tag{4}$$

where b_{11}, b_{22}, b_{33} are the powers measured at the GTEM cell port in three basic orientations.

The electric field in the far-field (at a distance r) due to a short dipole is given by (5) [7].

$$E_\theta = 30\sqrt{\frac{P_o}{10}}(\sin\theta)\frac{e^{-jkr}}{r}. \tag{5}$$

We assume that the total power radiated is due to a short dipole moment and is represented by the measurements in a GTEM cell. This is a good representation if the single dipole moment is dominant. Now, this dipole is located over a ground screen and vertical and horizontal electric fields are calculated. It should be noted that the geometry factors in (6) and (7) have to be maximized to obtain maximized far-field radiation [7], [8].

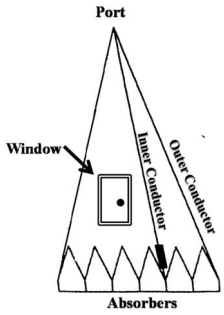


Fig. 15. GTEM cell.

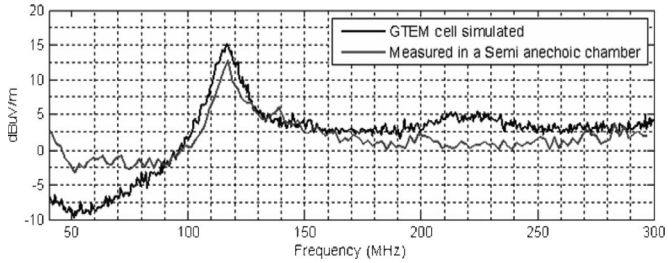


Fig. 16. Far-field prediction from GTEM cell in comparison with semianechoic chamber measurement.

$$E_h = 30\sqrt{\frac{P_o}{10}}\left(\frac{e^{-jkr1}}{r1} - \frac{e^{-jkr2}}{r2}\right) \tag{6}$$

$$E_v = 30\sqrt{\frac{P_o}{10}}\left(\frac{x^2}{r1^2}\frac{e^{-jkr1}}{r1} - \frac{x^2}{r2^2}\frac{e^{-jkr2}}{r2}\right). \tag{7}$$

The estimated far field for horizontal loop using the described method is shown below in Fig. 16.

Comparison of dipole moments in each test board shows that the magnetic dipole moments dominate slightly (by almost 30% or 2.5 dB). Therefore, it seems that the test boards are magnetically driven. The phase voltage plane on the printed circuit board causes direct electric field excitation. The phase voltage plane has the same area in all the three loop layouts. Therefore, one might think that this should lead to same electric field dipole moment. However, the GTEM cell measures the dipole moments of the boards. Thus a strong magnetic field circulating the board will cause a voltage across the board [16], which would again be seen as an electric dipole moment in the GTEM cell measurements. The magnetic dipole moments for test boards with vertical loops are three times stronger than the flat horizontal loop test board. Hence, the flat horizontal loop test board has the weakest emissions.

VII. Conclusion

This article suggested several dc-dc synchronous buck converter PCB layout modifications, which proved to be very effective in mitigation of the EMI problem. The parasitic loop inductance and the radiated emissions have been minimized by careful optimization of the PCB layout design. It was proved that a flat horizontal loop over a ground plane has the lowest radiated emissions. Also, the flat horizontal loop has very large area but a similar loop inductance as the vertical loops. The radiated emissions can be further suppressed by forcing the noise currents to stay in the horizontal loop.

In the end, a GTEM cell was used to model each test board as an equivalent E and H dipole moment. The test boards seem to be magnetically driven. The magnetic dipole moment of flat horizontal test board is the weakest, leading to weaker radiated emissions.

References

[1] A. Bhargava, D. Pommereneke, and K. Kam, "EMI Prediction in switched power supplies by full-wave and non-linear circuit co-simulation," in *Proc. IEEE Int. Symp. Electromagn. Compat*. Austin, TX, 17–21 Aug. 2009, pp. 41–46.

[2] K. W. Kam and D. Pommerenke, "EMI analysis methods for synchronous buck converter EMI root cause analysis," in *Proc. IEEE Int. Symp. Electromagn. Compat*. Detroit, MI, 18–22 Aug. 2008, pp. 1–7.

[3] K. Kam and D. Pommerenke, "EMC guideline for synchronous buck converter design," in *Proc. IEEE Int. Symp. Electromagn. Compat*. Austin, TX, 17–21 Aug. 2009, pp. 47–52.

[4] J. R. Warren, K. A. Rosowski, and D. J. Perreault, "Selection and design of a VHF DC-DC power converter," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 27–37, Jan. 2008.

[5] S. Deng, "Innovative applications of TEM cell measurements in predicting radiated emission due to common-mode current on printed circuit boards," Ph.D. dissertation, Dept. Electr. Eng., Univ. of Missouri – Rolla, 2007.

[6] *CST Computer Simulation Technology, CST Microwave Studio 2008*, CST, Germany, Feb. 27, 2008.

[7] P. Wilson, "On correlating TEM cell and OATS Enission measurements," *IEEE Trans. Electromagn. Compat.*, vol. EMC-37, no. 1, pp. 1–16, Feb. 1995.

[8] A. Nothofer and A. C. Marvin, "Aspects of GTEM to OATS measurement correlation," in *Proc. Int. Conf. Electromagn. Compat.*. Coventry, U.K, 1–3 Sep. 1997, pp. 170–174.

[9] A. K. Lee, "An advanced correlation algorithm between GTEM and OATS for radiated emission tests," *ETRI J.*, vol. 17, no. 3, pp. 45–63, Oct. 1995.

[10] K. Harada and T. Ninomiya, "Optimum design of RC snubbers for switching regulators," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-15, no. 2, pp. 209–217, Mar. 1979.

[11] C. U-Yaisom, W. Khanngern, and S. Nitta, "The study and analysis of the conducted EMI suppression on power MOSFET using passive snubber circuits," in *Proc. 3rd Int. Symp. Electromagn. Compat., 2002*, 21–24 May, 2002, pp. 561–564.

[12] M. H. Rashid, "Switched power supplies," in *Power Electronics Handbook*. London, U.K: Academic Press, 2001, pp. 211–223.

[13] Z. Li and D. Pommerenke, "EMI specifics of synchronous DC-DC buck converters," in *Proc. 2005 Int. Symp. Electromagn. Compat.*, 8–12 Aug., 2005, vol. 3, pp. 711–714.

[14] K. Kam, A. Bhargava, and D. Pommerenke, "Quantification of self damping of power MOSFET in synchronous buck converter," unpublished.

[15] S. Deng, T. H. Hubing, and D. Beetner, "Using TEM cell measurements to estimate the maximum radiation from PCBs with cables due to magnetic field coupling," *IEEE Trans. Electromagn. Compat.*, vol. 50, no. 2, pp. 419–423, May 2008.

[16] T. Hubing, "Printed circuit boards emi source mechanisms," in *Proc. 2003 IEEE Int. Symp. Electromagn. Compat.*, 18–22 Aug. 2003, vol. 1, pp. 1–3.

[17] J. T. Fessler, K. W. Whites, and C. R. Paul, "The effectiveness of an image plane in reducing radiated emissions," *IEEE Trans. Electromagn. Compat.*, vol. 38, no. 1, pp. 51–61, Feb. 1996.

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