

1 | **Silicon**

1.1 | **refirenry**

1.1.1 | **from sand**

1.1.2 | **melted**

1.1.3 | **small molten crystal "seed" lower into a vat**

1.1.4 | **crystal forms**

1.1.5 | **pull cylander from molten reigon**

1.1.6 | **ground to form ingots**

1.1.7 | **sawed with diamond blade to form wafers**

1.1.8 | **wafer scrubbed**

1.1.9 | **edges rounded and surfaces ground smooth and to create uniform thickness**

1.1.10 | **rinsed and etched in "chemicals" to remove impurities**

1.1.11 | **final polish on one side of the wafer**

1.1.12 | **all so that there are no scratches or contamination**

1.1.13 | **then, measured for resistivity**

1. function of dopant concentratian

1.1.14 | **electron beam machine**

1. etches patterns onto chrome plated glass plates in clean room

1.1.15 | **glass plates become masks used to transfer the circuit pattern onto the wafer**

1.1.16 | **usage of masks**

1. first mask creates divots
2. masks 4, 5 define source and drain reigons
3. mask 6 defines contact holes to allow aluminium to be inserted
4. mostly use 12-25 masks depending on complexity and type of circuit (much more now)

1.1.17 | **decontamination**

1. bunny suits
2. very high purity materials

1.1.18 | **fabrication techniques (4)**

1. formation of thin layers of silicon dioxide
2. introduction of dopants
3. deposition of thin layers of ?
4. something?

1.1.19 | **cleaning**

1. hot acids to clean wafers, repeated throughout process
2. rinsed in deionized water and spun dry in filtered nitrogen gas
3. grow layer of silicon dioxide in a vertical furnace
 - (a) protects silicon substrate beneath from unwanted reactions
 - i. pure oxygen used to grow silicon dioxide

1.2 | **design**

1.2.1 | **circuit design**

1.2.2 | **organization of design team**

1. based on organization of the chip
2. establish microarchitecture that regulates sequences and timings
3. design divided into areas
 - (a) each unit given to logic designer
 - (b) each functional block given to circuit designer who works at transistor level
4. mask designer draws out blueprints on paper

1.2.3 | **transistors**

1. represents digital zero or one
2. C-MOS transistors
 - (a) complementary metal oxidized transistor
 - (b) n type transistor
 - i. surrounded by n-type
 - ii. sandwiching a p-type layer

- iii. gate electrode is near but not connect to the p type reigon
- iv. a positive charge in gate attracts electrons and allows electrons to pass
- (c) both types can be made on the same chip using "complementary manufacturing?"
- (d) signals propogate through complex maze of switches

1.3 | **structure**

1.3.1 | **cubic atomic structure**

1.3.2 | **4 electrons valence shell**

1.3.3 | **perfect crystal will have no holes**

1.3.4 | **but at room temperature, free electrons can conduct**

1.4 | **impurities called dopants**

1.4.1 | **negative**

1. arsenic or phosphorus
2. one more valence
3. n type crystal because negative free carriers

1.4.2 | **positive**

1. boron
2. missing electron acts like positive carrier, "hole"

1.4.3 | **silicon can be either good or poor conductor (semiconductor)**

1. controlled by concentration of dopant