1 | Silicon

1.1 | refirenry

1.1.1 | from sand

1.1.2 | melted

1.1.3 | small molten crystal ”seed” lower into a vat

1.1.4 | crystal forms

1.1.5 | pull cylander from molten reigon

1.1.6 | ground to form ingots

1.1.7 | sawed with diamond blade to form wafers

1.1.8 | wafer scrubbed

1.1.9 | edges rounded and surfaces ground smooth and to create uniform thickness

1.1.10 | rinsed and etched in ”chemicals” to remove impurities

1.1.11 | final polish on one side of the wafer

1.1.12 | all so that there are no scratches or contamination

1.1.13 | then, measured for resistivity

1. function of dopant concentratian

1.2 | design

1.2.1 | circuit design

1.2.2 | organization of design team

1. based on organization of the chip
2. establish microarchitecture that regulates sequences and timings
3. design divided into areas
   (a) each unit given to logic designer
   (b) each functional block given to circuit designer who works at transistor level

1.2.3 | transistors

1. represents digital zero or one
2. C-MOS transistors

(a) complementary metal oxidized transistor

(b) n type transistor

i. surrounded by n-type
ii. sandwhiching a p-type layer
iii. gate electrode is near but not connect to the p type reigon
iv. a positive charge in gate attracts electrons and allows electrons to pass

(c) both types can be made on the same chip using ”complementary manufacturing?”

1.3 | structure

1.3.1 | cubic atomic structure

1.3.2 | 4 electrons valence shell

1.3.3 | perfect crystal will have no holes

1.3.4 | but at room temperature, free electrons can conduct

1.4 | impurities called dopants

1.4.1 | negative

1. arsenic or phospherus
2. one more valence
3. n type crystal because negative free carriers

1.4.2 | positive

1. boron
2. missing electron acts like positive carrier, ”hole”

1.4.3 | silicon can be either good or poor conductor (semiconductor)

1. controlled by concentration of dopant