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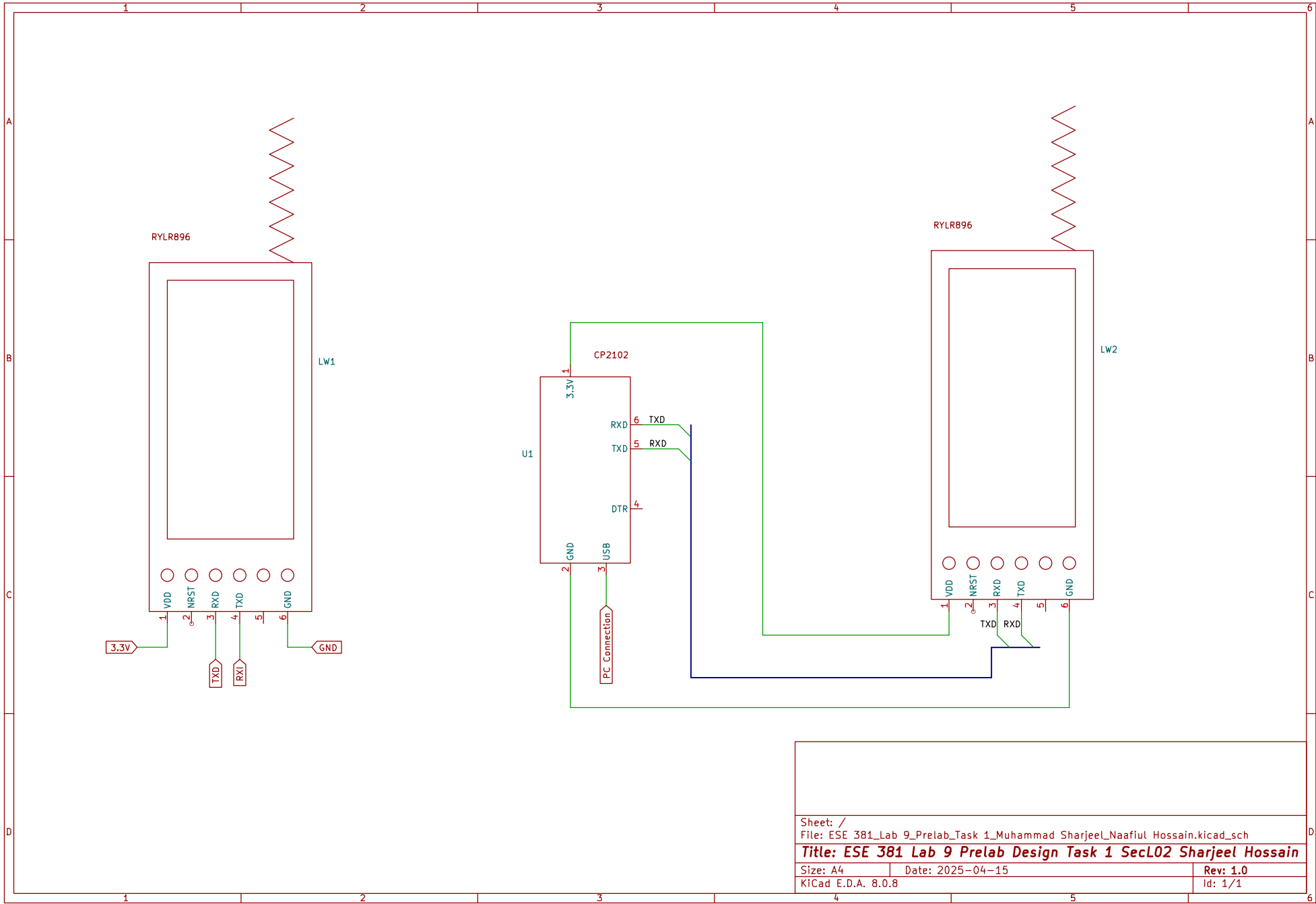
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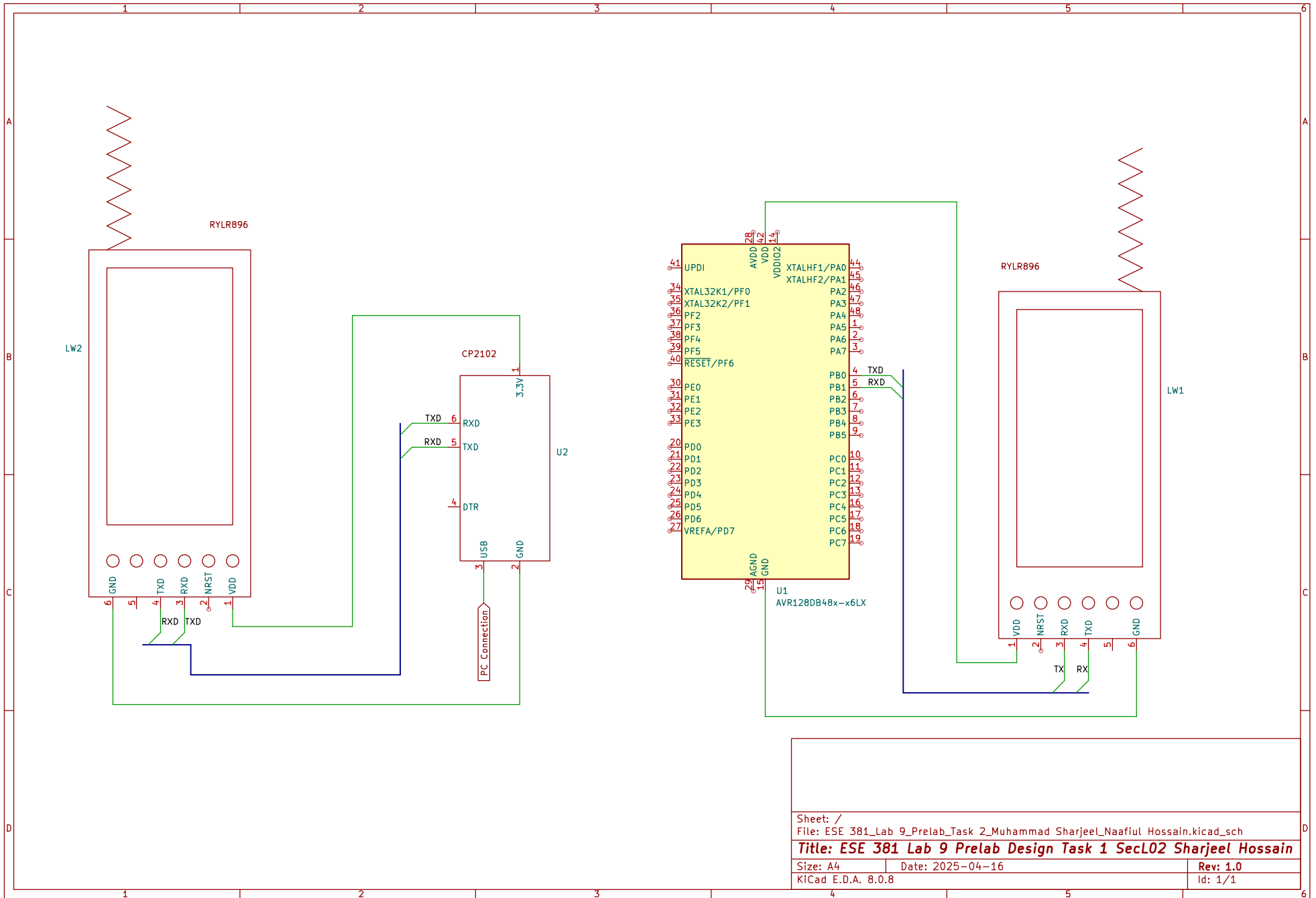
Pre-Lab 9: Asynchronous Serial (RS232) Communication Over a LoraWAN Channel

ESE 381 Section L02

Bench 7

Breadboard: K2





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File: ESE 381_Lab 9_Prelab_Task 2_Muhammad Sharjeel_Naafiul Hossain.kicad_sch		
<b>Title: ESE 381 Lab 9 Prelab Design Task 1 SecL02 Sharjeel Hossain</b>		
Size: A4	Date: 2025-04-16	Rev: 1.0
KiCad E.D.A. 8.0.8		Id: 1/1

```
1  /*
2  * receive_payload.c
3  * Task 2 - Receive message via LoRa (USART1), extract payload, send to PC via USART3
4  * Author: Naafiul Hossain
5  */
6
7  #include <avr/io.h>
8  #include <avr/interrupt.h>
9  #include <string.h>
10 #include <stdio.h>
11
12 #define F_CPU 4000000UL
13 #define BAUD_RATE 115200
14 #define USART_BAUD ((uint16_t)((float)(F_CPU * 64) / (16.0f * BAUD_RATE) + 0.5f))
15
16 #define RX_BUFFER_SIZE 80
17 #define TX_BUFFER_SIZE 40
18
19 // === RX and TX Buffers ===
20 char rxU1_buff[RX_BUFFER_SIZE] = {0}; // Incoming LoRa message
21 char txU3_buff[TX_BUFFER_SIZE] = {0}; // Payload to PC via USART3
22 uint8_t rxU1_index = 0;
23 uint8_t txU3_index = 0;
24 uint8_t rxU1_buff_dav = 0;
25 uint8_t txU3_buff_dav = 0;
26
27 // === Parsed Fields ===
28 char RCV_preamble[10];
29 char payload[40];
30 uint16_t txmtr_addr;
31 uint16_t rcv_data_len;
32 int16_t RSSI;
33 int16_t SNR;
34
35 void USART1_init(void); // RX from LoRa
36 void USART3_init(void); // TX to PC
37 void parse_rxU1_buff(void);
38
39 int main(void) {
40     USART1_init();
41     USART3_init();
42     sei(); // Enable global interrupts
43
44     while (1) {
45         if (rxU1_buff_dav) {
46             parse_rxU1_buff(); // Extract payload from received LoRa message
```

```
47         USART3.CTRLA |= USART_DREIE_bm; // Enable TX ISR to send to CoolTerm
48     }
49 }
50 }
51
52 // === Initialize USART1 (RX from LoRa) ===
53 void USART1_init(void) {
54     PORTC.DIRCLR = PIN0_bm; // PC0 = RX1
55     USART1.CTRLB = USART_RXEN_bm;
56     USART1.CTRLC = USART_CHSIZE_8BIT_gc;
57     USART1.BAUD = USART_BAUD;
58     USART1.CTRLA = USART_RXCIE_bm;
59 }
60
61 // === Initialize USART3 (TX to PC) ===
62 void USART3_init(void) {
63     PORTB.DIRSET = PIN0_bm; // PB0 = TX3
64     USART3.CTRLB = USART_TXEN_bm;
65     USART3.CTRLC = USART_CHSIZE_8BIT_gc;
66     USART3.BAUD = USART_BAUD;
67 }
68
69 // === ISR: USART1 RX Complete - Receive LoRa message ===
70 ISR(USART1_RXC_vect) {
71     char c = USART1.RXDATAL;
72
73     if (rxU1_index < RX_BUFFER_SIZE - 1) {
74         rxU1_buff[rxU1_index++] = c;
75
76         if (c == '\n') {
77             rxU1_buff[rxU1_index] = '\0';
78             rxU1_index = 0;
79             rxU1_buff_dav = 1;
80             USART1.CTRLA &= ~USART_RXCIE_bm; // Disable RX interrupt until
81             parsed
82         } else {
83             rxU1_index = 0; // Prevent overflow
84         }
85     }
86
87 // === ISR: USART3 DRE - Send payload one char at a time ===
88 ISR(USART3_DRE_vect) {
89     if (txU3_buff_dav && txU3_buff[txU3_index] != '\0') {
90         USART3.TXDATAL = txU3_buff[txU3_index++];
91     } else {
92         USART3.CTRLA &= ~USART_DREIE_bm;
93         txU3_buff_dav = 0;
```

```
94     }
95 }
96
97 // === Parse LoRa message and copy payload to txU3_buff ===
98 void parse_rxU1_buff(void) {
99     sscanf(rxU1_buff, "%[^]=%u,%u,%[^,],%d,%d",
100           RCV_preamble, &txmtr_addr, &rcv_data_len, payload, &RSSI, &SNR);
101
102     snprintf(txU3_buff, sizeof(txU3_buff), "%s\r\n", payload); // Add CRLF ↗
103     for terminal display
104
105     rxU1_buff_dav = 0;
106     txU3_buff_dav = 1;
107     txU3_index = 0;
108
109     memset(rxU1_buff, 0, sizeof(rxU1_buff));
110     USART1.CTRLA |= USART_RXCIE_bm; // Re-enable RX
111 }
```

```
1  /*
2   * LoRaWAN_reply.c
3   * Task 3 - AVR receives LoRa message and echoes payload back via AT+SEND
4   * Author: Naafiul Hossain
5   */
6
7  #include <avr/io.h>
8  #include <avr/interrupt.h>
9  #include <string.h>
10 #include <stdbool.h>
11 #include <stdio.h>
12
13 #define F_CPU 4000000UL
14 #define BAUD_RATE 115200
15 #define USART1_BAUD ((uint16_t)((float)(F_CPU * 64) / (16.0f * BAUD_RATE) + 0.5f))
16
17 #define BENCH_NUM 7
18 #define PC_ADDRESS (BENCH_NUM + 30) // Destination LW2 address (PC side)
19
20 #define RX_BUFFER_SIZE 80
21 #define TX_BUFFER_SIZE 64
22
23 // === RX and TX Buffers ===
24 char rxU1_buff[RX_BUFFER_SIZE] = {0}; // Receive from LW1
25 char *rxU1_ptr = rxU1_buff;
26 uint8_t rxU1_index = 0;
27 uint8_t rxU1_buff_dav = 0; // Data Available Flag
28
29 char txU1_buff[TX_BUFFER_SIZE] = {0}; // Transmit to LW1
30 char *txU1_ptr = txU1_buff;
31 uint8_t txU1_index = 0;
32 uint8_t txU1_buff_dav = 0; // Transmission ready flag
33
34 // === Parsed Message Fields ===
35 char RCV_preamble[10];
36 volatile uint16_t txmtr_address;
37 volatile uint16_t rcv_data_len;
38 char payload[40]; // Payload from message
39 volatile int16_t RSSI;
40 volatile int16_t SNR;
41 uint8_t payload_index = 0;
42
43 void USART1_init(void);
44 void parse_rxU1_buff(void);
45
46 int main(void) {
47     USART1_init();
48     sei(); // Enable global interrupts
```

```
49
50     while (1) {
51         if (rxU1_buff_dav) {
52             parse_rxU1_buff();           // Parse and prep reply
53             USART1.CTRLA |= USART_DREIE_bm; // Enable TX ISR
54         }
55     }
56 }
57
58 // === USART1 Initialization ===
59 void USART1_init(void) {
60     PORTC.DIRCLR = PIN0_bm; // PC0 = RX (input)
61     PORTC.DIRSET = PIN1_bm; // PC1 = TX (output)
62
63     USART1.CTRLB = USART_RXEN_bm | USART_TXEN_bm;
64     USART1.CTRLC = USART_CHSIZE_8BIT_gc;
65     USART1.BAUD = USART1_BAUD;
66     USART1.CTRLA = USART_RXCIE_bm; // Enable RX interrupt
67 }
68
69 // === USART1 RX ISR: Receives characters into rxU1_buff ===
70 ISR(USART1_RXC_vect) {
71     char c = USART1.RXDATAL;
72
73     if (rxU1_index < RX_BUFFER_SIZE - 1) {
74         rxU1_buff[rxU1_index++] = c;
75
76         if (c == '\n') {
77             rxU1_buff[rxU1_index] = '\0'; // Null terminate
78             rxU1_buff_dav = 1;           // Message complete
79             rxU1_index = 0;
80             USART1.CTRLA &= ~USART_RXCIE_bm; // Disable RX interrupt until
81                                     processed
82         }
83     } else {
84         rxU1_index = 0; // Prevent overflow
85     }
86 }
87
88 // === USART1 TX ISR: Transmit txU1_buff one byte at a time ===
89 ISR(USART1_DRE_vect) {
90     if (txU1_buff_dav && txU1_buff[txU1_index] != '\0') {
91         USART1.TXDATAL = txU1_buff[txU1_index++];
92     } else {
93         USART1.CTRLA &= ~USART_DREIE_bm; // Disable TX interrupt
94         txU1_buff_dav = 0;
95     }
96 }
```



```
97 // === Parse incoming +RCV=... and construct AT+SEND=... ===
98 void parse_rxU1_buff(void) {
99     sscanf(rxU1_buff, "%[^]=%u,%u,%[^,],%d,%d", RCV_preamble, &txmtr_address, ↵
        &rcv_data_len, payload, &RSSI, &SNR);
100
101     // Construct reply: AT+SEND=<dest_addr>,<length>,<payload>\r\n
102     snprintf(txU1_buff, sizeof(txU1_buff), "AT+SEND=%d,%d,%s\r\n", PC_ADDRESS, ↵
        rcv_data_len, payload);
103
104     // Clear flags and prep TX
105     rxU1_buff_dav = 0;
106     txU1_buff_dav = 1;
107     txU1_index = 0;
108
109     memset(rxU1_buff, 0, sizeof(rxU1_buff));
110     USART1.CTRLA |= USART_RXCIE_bm; // Re-enable RX
111 }
112
```