|  |  |  |
| --- | --- | --- |
|  | Z80000 | PA-RISC |
| 2. Kompiuterio/procesoriaus bazė |  |  |
| 3. Architektūra |  |  |
| 4. Kelių adresų mašinos |  |  |
| 5. Registrai, jų kiekis, plotis, paskirtis | The CPU features a general-purpose register file with sixteen 32-bit registers. The registers can be used as data accumulators, index values, or memory pointers. Two of the registers, the Frame Pointer and Stack Pointer, are used for procedure linkage with the Call, Enter, Exit, and Return instruc tions. |  |
| 6. Ar naudojami požymių bitai (flags), kokie? | Carry (C) indicates a carry out of the high-order bit position during an operation. Zero (Z) indicates that the result of an operation is zero. Sign (S) indicates whether the result of an operation is negative or positive. Parity/Overflow (PlY) indicates that the result of a logical operation has even parity or that overflow has occurred for arithmetic operations. Dec:iJllal-Adjust (D) is used in BCD arithmetic to indicate whether an addition or subtraction was last executed. Half Carry (H) is used in BCD ar i thmetic to con vert the result of a previous binary addition or subtraction to a decimal result. |  |
| 7. Duomenų plotis (mašininis žodis) | The instruction set offers a regular combination of nine general addressing modes with operations on numerous data types, including bits, bit fields, bytes (a bits), words (16 bits) , long words (32 bits) , and variable-length strings. |  |
| 8. Atminties išdėstymas, adresų erdvė | 1.2.2 Address Spaces susikonspektuot |  |
| Efektyvus adreso plotis |  |  |
| Maksimalus atminties kiekis | he CPU uses 32-bit logical addresses, permitting direct access to 4G bytes of memory. The logical addresses are translated by the memory management mechanism to the physical addresses used to access memory and peripherals. |  |
| Tipiškas atminties kiekis |  |  |
| 9. Virtualioji atmintis | Segmented mode supports two segment sizes--64K bytes and 16M bytes. Up to 32,76a of the small segments and 12a of the large segments are avail able. In segmented mode, address calculations do not affect the segment number, only the offset wi thin the segment. Allocating individual objects such as program modules, stacks, or large data structures to separate segments allows appli cations to benefit from the logical structure of a segmented memory space. The 32-bit addresses in linear mode provide uni form and unstructured access to 4G bytes of mem ory. Some applications benefit from the flexibil ity of linear addressing by allocating objects to arbitrary positions in the address space. |  |
| 10.Komandų sistema | The Z80,OOO CPU supports operations on nine data types: bit, bit field, aigned integer, unaigned integer, logical value, address, packed BCD inte ger, stack, and string. Integer and logical values can be byte, word, or longword in size. In addition, floating-point operations are imple mented through the Extended Processing Architec ture (EPA) facility by a coproceasor (ZB07D Arith metic Processing Unit) or by software emulation. Several instructiona are provided for important control structures. Conditional branches and jumps support "if-then", "while", and "repeat" constructions. The Decrement and Branch if Non Zero instruction can be used for loop control. Call, Enter, Exit, and Return instructions perform procedure linkage. The regular combination of addressing modes, operations, and data types offers a powerful instruction set that is well-suited for compila tion of high-level languages such as C, Pascal, and Ada. |  |
| Mašinos komandų kiekis, kokios jų klasės |  |  |
| Instrukcijų formatai |  |  |
| 11. Adresavimo būdai |  |  |
| 12. I/O | The CPU has two modes of operation--normal and system--used to isolate application programs from senaitive portions of the operating system. The mode is aelected by a bit in the Flag and Control Word regiater. Dnly programs in system mode are privileged to execute I/O instructions and access control regis ters. The memory management mechanism allows sys tem mode programs to accesa regions of memory pro tected from normal mode access. Further protec tion is provided with separate stacks for system and normal modes. Application programs use the system Call instruction and trap to request ser vices from the operating system. |  |
| 13. Pertraukimai | The Z80,OOO CPU supports four types of exceptions: reset, bus error, interrupts, and traps. A reset exception initializes the CPU state in response to an exter nal request, typically part of a power-on sequence. A bus error exception occurs when external hardware indicates an irrecoverable error, such as an uncorrectable memory error, on a bus transaction. An interrupt is an asynchronous event signalled externally, typically when a peripheral device needs attention. A trap is a condition detected by the CPU synChronously with execution of an instruction. When an exception occurs, the CPU saves the Pro gram Status registers of the executing process on the system stack. Then new values for the Program Status registers are read from a table in memory (Program Status Area), thus passing control to an exception handler. The CPU provides a flexible interrupt structure that includes three types of interrupts: nonmask able, vectored, and nonvectored. The nonmaskable interrupt, which is of highest priority, is typi cally reserved for the most critical requirements, such as sudden power failure. Both vectored and nonvectored interrupts can be separately masked by bits in the flag and Control Word register. Vec tored interrupts allow the CPU to branch to a specific exception handler selected by a code read from the peripheral. Nonvectored interrupts use a common exception handler. The CPU recognizes several trap conditions, all of which can be used to improve software reliabil ity. The System Call trap provides controlled access for application programs to operating sys tem functions. Traps for integer overflow, sub range out of bounds, and subscript out of bounds catch common run-time errors. The Address Trans lation trap allows the operating system to imple ment access protection and virtual memory. Traps for breakpoint and single instruction tracing are used during software development. The Conditional Trap instruction ia used for software definition of exception conditions not recognized by the CPU hardware. |  |
| 14. Duomenų tipai |  |  |
| 15. Greitaveika |  |  |
| 16. Cache memory |  |  |
| 17. Tipinės taikymo sritys |  |  |
| 18. Programinė įranga šiai architektūrai |  |  |
| 19. Emuliatioriai |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

**Šaltiniai:**

Z80000:

<https://bitsavers.trailing-edge.com/components/zilog/z80000/Z80000_CPU_Preliminary_Technical_Manual_Sep84.pdf>

<https://en.wikipedia.org/wiki/Zilog_Z80000>

PA-RISC:

<https://parisc.docs.kernel.org/en/latest/>

<https://en.wikipedia.org/wiki/PA-RISC>

Z80000, dar nesusisteminta info iš vikipedijos:

The **Zilog Z80000** is an unreleased [32-bit](https://en.wikipedia.org/wiki/32-bit) [processor](https://en.wikipedia.org/wiki/Central_processing_unit) designed by [Zilog](https://en.wikipedia.org/wiki/Zilog) and completed in 1986. The Z80000 is a 32-bit expansion of the [16-bit](https://en.wikipedia.org/wiki/16-bit) [Zilog Z8000](https://en.wikipedia.org/wiki/Zilog_Z8000) with [multiprocessing](https://en.wikipedia.org/wiki/Multiprocessing) capability, a six-stage [instruction pipeline](https://en.wikipedia.org/wiki/Instruction_pipeline), and a 256-byte [cache](https://en.wikipedia.org/wiki/CPU_cache). It can address 4 [gigabytes](https://en.wikipedia.org/wiki/Gigabyte) of [RAM](https://en.wikipedia.org/wiki/Random-access_memory), but cannot execute code written for the Z8000 or [Z80](https://en.wikipedia.org/wiki/Zilog_Z80).

Described at the time as a "[mainframe](https://en.wikipedia.org/wiki/Mainframe_computer) on a chip", the processor is in many ways an equivalent to [Intel](https://en.wikipedia.org/wiki/Intel)'s [80386](https://en.wikipedia.org/wiki/I386). Delays in the initial manufacturing pushed back its availability date to after that of the 386, and the Z80000 only made it to a test sampling phase without ever being released commercially.[[1](https://en.wikipedia.org/wiki/Zilog_Z80000#cite_note-1)

The processor includes a [memory management unit](https://en.wikipedia.org/wiki/Memory_management_unit) that provides [protected memory](https://en.wikipedia.org/wiki/Protected_memory), important for [multitasking](https://en.wikipedia.org/wiki/Computer_multitasking), and [virtual memory](https://en.wikipedia.org/wiki/Virtual_memory) addressing for temporary storage of RAM on a [hard disk](https://en.wikipedia.org/wiki/Hard_disk). The processor has three methods of accessing memory:

* compact mode – meant for small programs, could only access 64 KB (16-bit addresses, equivalent to the Z8000's non-segmented mode). Address bits 31-16 of all virtual addresses comes from address bits 31-16 of the program counter.
* segmented mode – 32,768 segments of 64 KB (16-bit address; comprising memory from 0-2GB) *and* 128 segments of 16 MB (24-bit address; comprising memory from 2GB-4GB), making a total of 4 GB (32-bit address) of accessible memory.
* linear mode – direct 4 GB (32-bit address) accessible memory

The processor is designed to interoperate with other [integrated circuits](https://en.wikipedia.org/wiki/Integrated_circuit) designed for use with the Z8000, such as the [Zilog Z8070](https://en.wikipedia.org/w/index.php?title=Zilog_Z8070&action=edit&redlink=1) [floating-point](https://en.wikipedia.org/wiki/Floating-point) [coprocessor](https://en.wikipedia.org/wiki/Coprocessor).

Gal reiks is dokumentacijos info:

he CPU supports three modes of address represen tation--compact, segmented, and linear--selected by two control bits in the Flag and Control Word register. Applications with an address space smaller than 64K bytes can take advantage of the dense code and efficient use of base registers with the 16-bit compact addresses. Although pro grams executing in compact mode can only manipu late 16-bit addresses, the logical address is extended to 32 bits by concatenating the 16 most significant bits of the Program Counter register. Compact mode is equivalent to the laOOO non-seg mented mode.

A diagram of a number

Description automatically generated with medium confidence