Computer Organization 2023 Lab

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Finished part:

已完成本次作業所有要求。

(A) basic score: 75 / 75

Congratulation. You pass TA's pattern

Problems you met and solutions:

1. Vivado 讀不到 ALU_1bit.v

明明有放入檔案但還是讀不到,後來上網爬文發現需勾入 Settings ->

Simulation -> Advanced -> Include all design sources for

simulation,如此方可解決,若助教遇到相同問題也請用同樣方式解決。

Compilation Elaboration Simulation Netlist Advanced

✓ Enable incremental compilation

Enables incremental compilation and preserves simulation files during successive simulation runs.

✓ Include all design sources for simulation

Selecting this option will ensure that all files from design sources - along with all files from the current simulation set - will automatically be used for simulation. If files are re-ordered, enabled/disabled or changed in any way in design sources, the same changes will automatically be picked up when launching behavioral simulation.

2. 接線接錯

隨著作業越來越複雜·Simple_Single_CPU.v 裡接錯的可能性就越大·解決辦法就是再細心一點,或是祈禱下輩子眼睛利索點。

If you create additional module, please give a short explanation here:

本次使用助教提供之模板,但是 ALU.v 是繼承上次作業助教提供的檔案,所以會多出 ALU_1bit.v 以及 Adder.v。

ALU_1bit.v: 1bit 的 ALU · 32bit ALU 即由 1 bit ALU 建構而成。

Adder.v: 簡單加法器,可輸出兩個輸入相加之值,1 bit ALU 的所需模組。