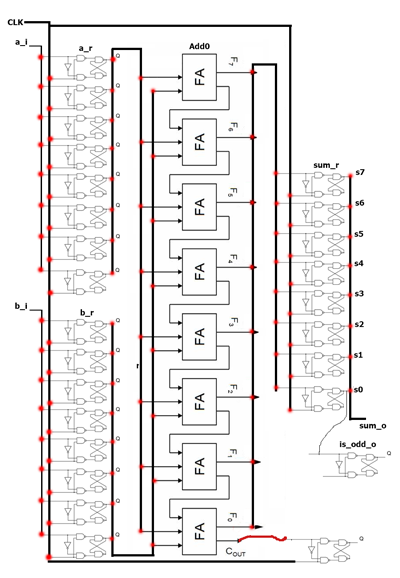
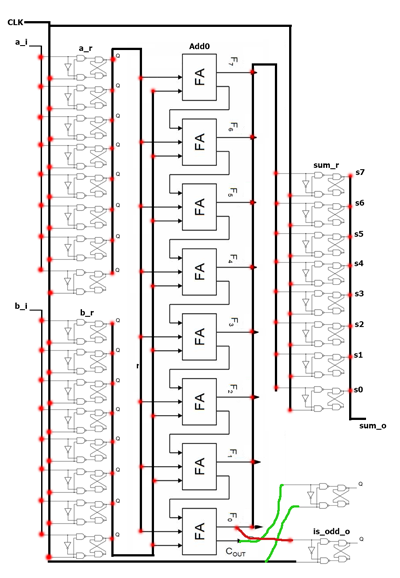
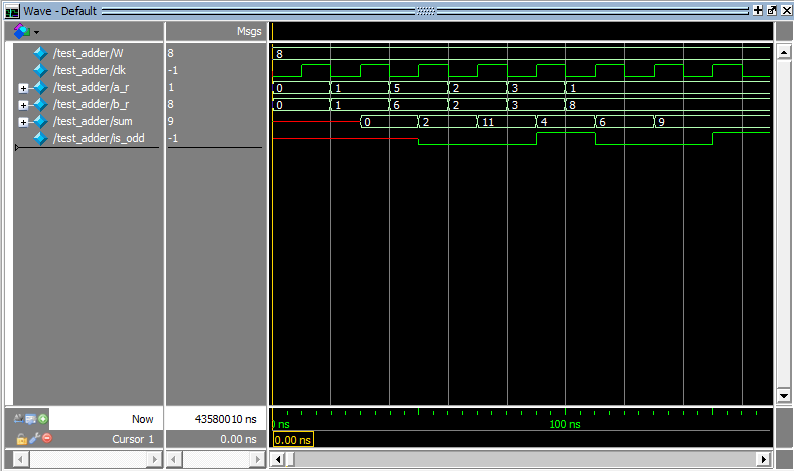
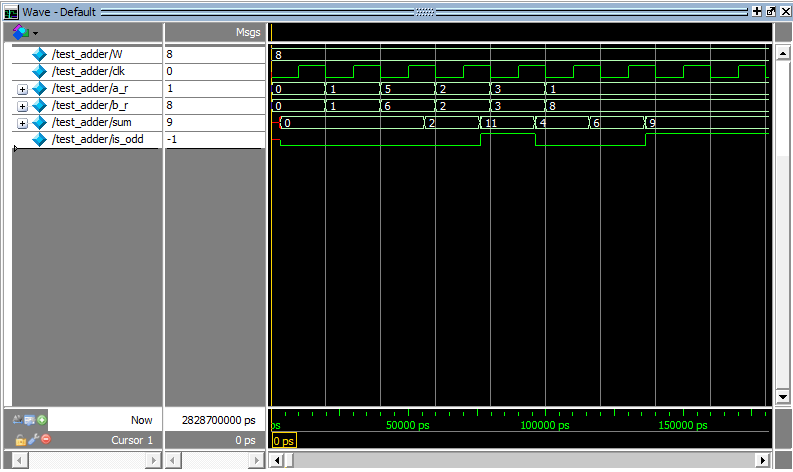
Q1)  


Q2)  


Q3)  
#flip-flops: **26**  
#EP4CE40F29C6 flip-flops: **39600**  
#logic elements: **26**  
#EP4CE40F29C6 logic elements: **39600**

Q4)  
*slow 1200mV 85C Model*  
Fmax: **547.35 MHz**  
Slack: **-0.827**

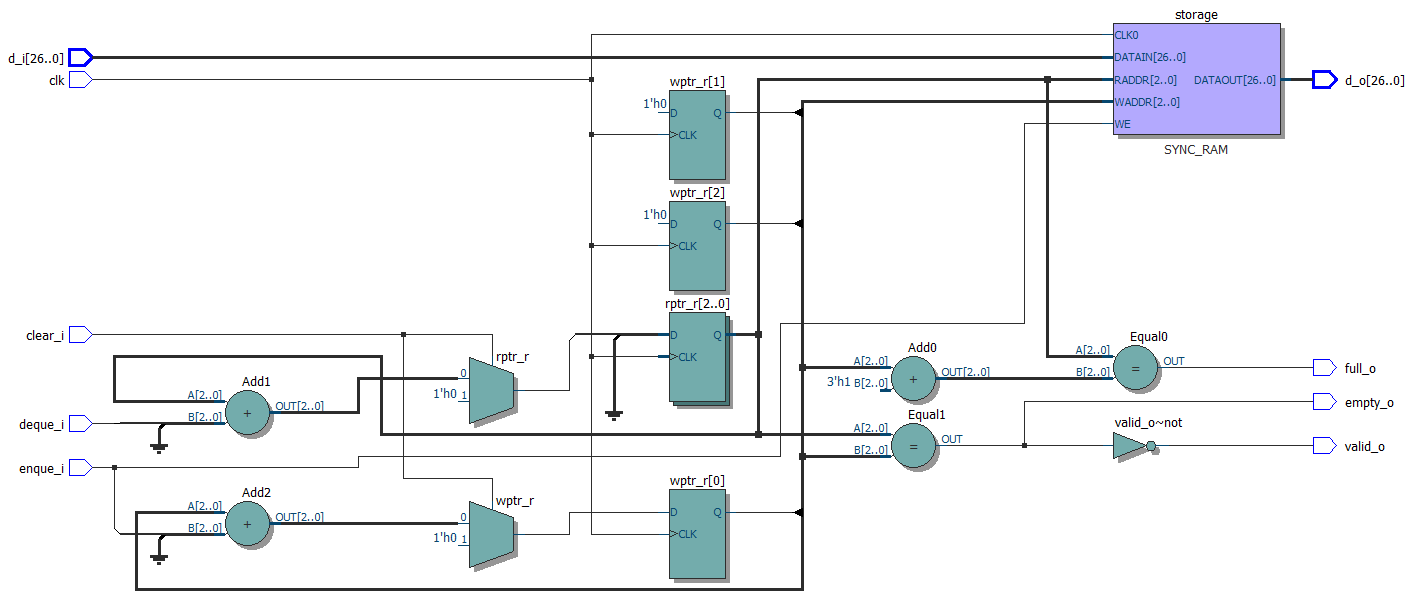
Q5)  
**The behavioral simulation was outputting the is\_Odd register a full clock cycle later than it was supposed to. This was fixed in the post-route simulation.  
  
  
  
**Q6)

|  |  |  |  |
| --- | --- | --- | --- |
| **Width** | **Max Freq** | **# of logic elements** | **# off registers used** |
| 8-bit | 547.35 MHz | 26 | 26 |
| 16-bit | 415.8 MHz | 50 | 50 |
| 32-bit | 308.17 MHz | 98 | 98 |
| 64-bit | 197.12 MHz | 194 | 194 |

Q7)  
The test bench sets the FPGA to accept write operation, then sets register 2 with a value of 5. On the next clock cycle it sets register 3 with a value of 6. On the next clock cycle both register 2 and register 3 are retrieved simultaneously to show two different registers can be read at the same time. On the next clock cycle, register 3 is retrieved twice to show that a register can be read on both read ports. This is repeated on the next clock cycle for register 2. On the next clock cycle, register 3 has the number 15 written to it while the register is being read to show that this operation is possible. Finally, writing is disabled and a write is attempted to register 3 followed by a read from register 3, demonstrating that the register is unaltered.

Q8)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Configuration** | **Max Freq** | **# of logic elements used** | **# of flip-flops used** | **# of embedded RAMs used** |
| 8 16-bit registers | n/a | 168 | 128 | n/a |
| 16 16-bit registers | 851.79 MHz | 29 | 29 | 256 |
| 32 16-bit registers | 1007.05 MHz | 32 | 32 | 512 |
| 32 64-bit registers | 823.05 MHz | 80 | 80 | 2048 |
| 256 32-bit registers | 843.17 MHz | 57 | 57 | 8192 |

Q9)  


Q10)  
instructions executed: **161**  
execution time = (instruction executed) \* (1/FMax) = **(161) \* (1/54.65MHz) = 2.946**  
wall clock time: **0.01 seconds**  
simulation: (wall clock time) / (simulation time) = (wall time) / (execution time) = = (**0.01 seconds) / [(161) \* (1/54.65MHz)] = 3.39\*10^(-3)**  
  
Q11)  
#flip-flops: **2086**#logic elements: **4838**max clock frequency: **55.25 MHz**slack: **-17.098**additional cores: **39600 / 4838 = ~8.1 == 8 cores.**

Q12)  
instructions executed: **161**  
execution time = (instruction executed) \* (1/FMax) = **(161) \* (1/55.25MHz) = 2.914**wall clock time: **60 seconds**simulation: (wall clock time) / (simulation time) = (wall time) / (execution time) = **(60 seconds) / [(161) \* (1/55.25Hz)] = 20.590**