

# CSCB58 - Lab 0

## Intro to the Lab & The DE2 Board

### Learning Objectives

This week we will be getting you familiar with the lab and the boards that we will be using in later labs. You will also learn how to use the Quartus software that is required in order to upload your verilog code onto the board.

### Resources

You can find many resources about the Altera DE2 board here <https://www.terasic.com.tw/cgi-bin/page/archive.pl?No=30>. The User Manual for the DE2 board can be downloaded from here: [https://www.terasic.com.tw/cgi-bin/page/archive\\_download.pl?Language=China&No=%20502&FID=cd9c7c1feaa2467c58c9aa4cc02131af](https://www.terasic.com.tw/cgi-bin/page/archive_download.pl?Language=China&No=%20502&FID=cd9c7c1feaa2467c58c9aa4cc02131af)

### Marks

Your TA must record the marks on this page as you complete each section of the lab. It is your responsibility to ensure that by the end of the lab, all work has been recorded appropriately.

Prelab	/4
Part I1 (in-lab)	/1
Part II (in-lab)	/1
Followed all directions and lab rules.	
Clean work-space with all materials returned to their original state	/2
<hr/> TOTAL	<hr/> /8

Write your name, UTorID, and student ID:

Name: \_\_\_\_\_

Student ID: \_\_\_\_\_

UTorID: \_\_\_\_\_

Write your partner's name, UTorID, and student ID:

Partner name: \_\_\_\_\_

Partner student ID: \_\_\_\_\_

Partner UTorID: \_\_\_\_\_

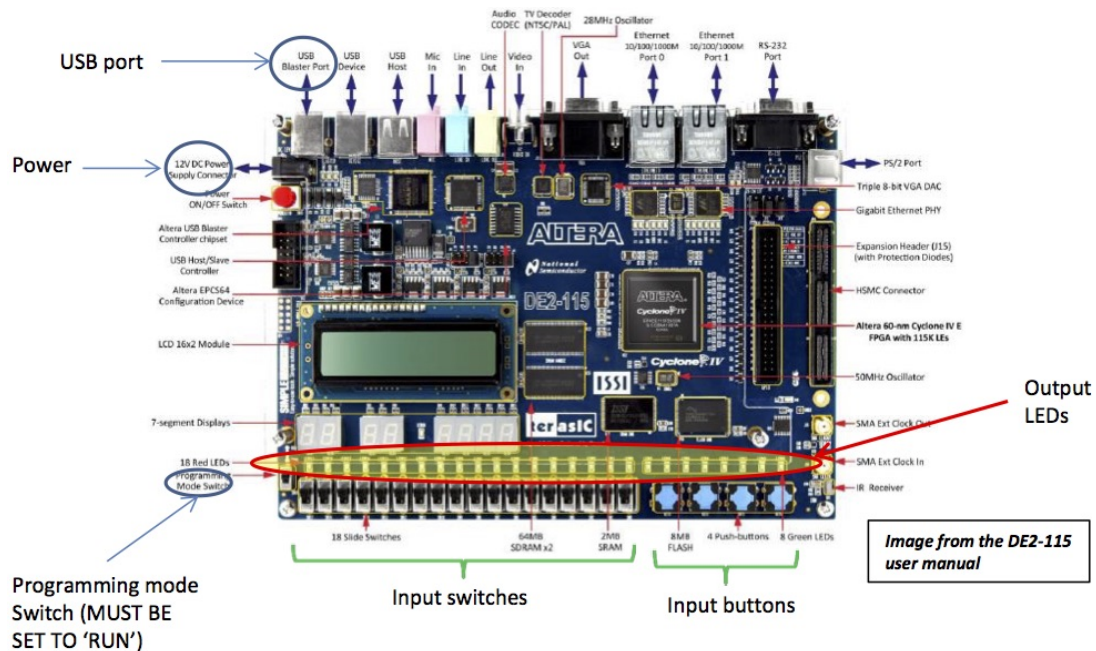
## Lab Rules

Since this is your first time here, it is appropriate to remind you of the rules and procedures governing the operation of the lab. Please read these carefully.

- No food or drinks are allowed inside the lab. Be sure to eat properly before your session, you can step out for water if you need to. Notify your TA since he/she is the only person that can grant you access to the lab.
- No laptops, notebook computers, tablets, or other electronic gizmos allowed during the session.
- Bags and backpacks must be stored at the front or back of the room.
- While in the lab, you are responsible for taking good care of all equipment.
- Treat everyone else in the lab with respect and consideration.
- You must listen and follow all instructions provided by your TA.

## Setting up the board

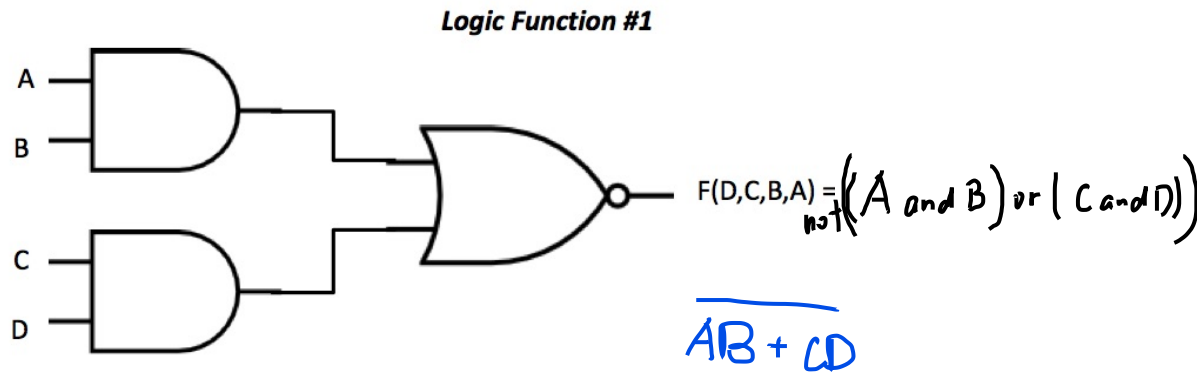
1. Carefully unpack the FPGA board and place it safely on the desk. Connect the power cable to the board and a desk outlet, connect the USB cable to the board's USB 'blaster' port and to a computer USB terminal. **DO NOT POWER UP THE BOARD yet.**



2. Familiarize yourself with the layout of the board, the location of input switches and buttons, output LEDs, and the programming mode switch. This is all we will use for this lab.
3. Open the Quartus II software. Close the initial information box. Create a new project from File -> New Project Wizard. Create a directory for the project on the Desktop, with name Lab\_0. Set the name of the project to Lab\_0. Click on Finish when done.

## Building a circuit

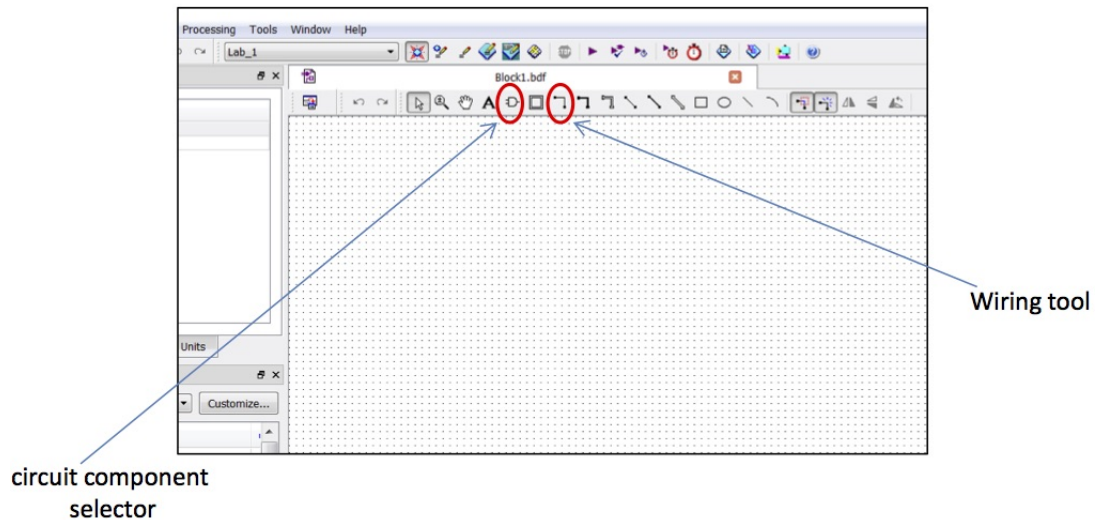
- Write the boolean expression for the function whose circuit is shown below (**PRELAB**)



- Complete the truth table for the function (**PRELAB**)

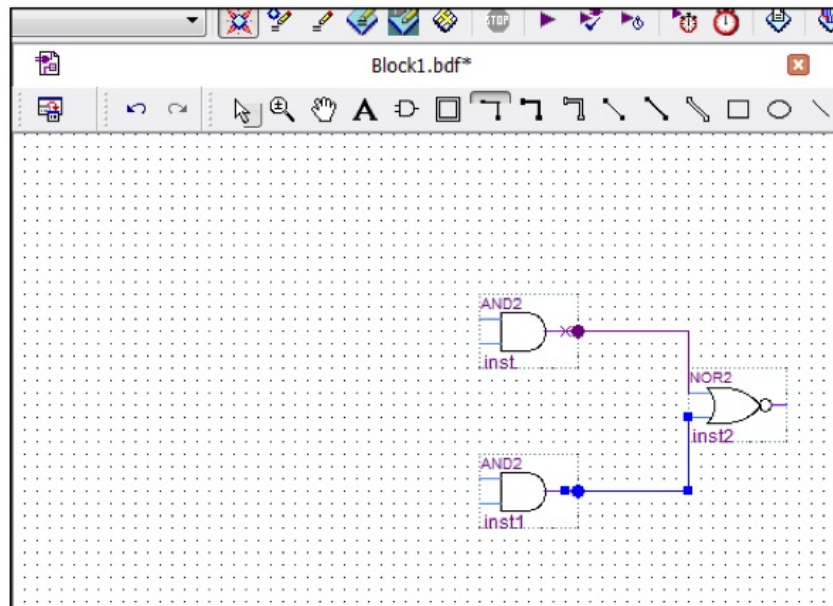
D	C	B	A	F(D, C, B, A)
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

3. Use the Quartus II graphical editor to implement the logic function from the previous page. To start the graphical editor, use File -> New -> Block Diagram/Schematic File. The graphical editor allows you to select and connect all sorts of logic functions and circuit components



For now, we will need only the circuit component selector, and the wiring tool. Click on the circuit component selector; this will bring up a menu with circuit components. Expand the contents of the Altera libraries, and find `primitives -> Logic`. There you will find a list of logic gates. Select and place on the graphical editor the gates needed for the circuit.

4. Use the wiring tool to connect the gates. You should have something like the image shown below.

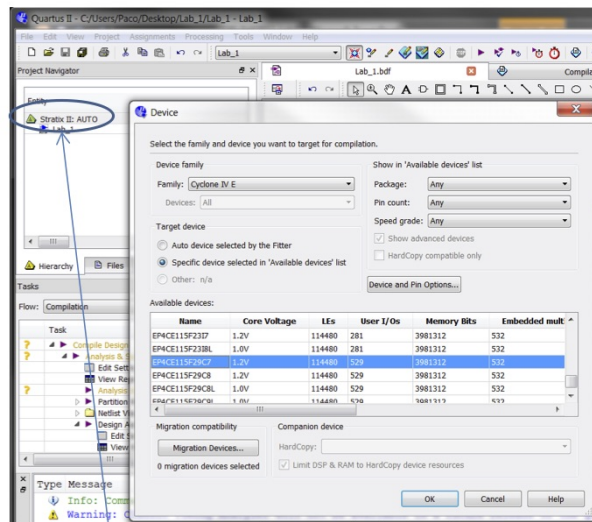


**TIP: make sure that the connections are properly set!** The wires in the schematic have a tendency to look connected even when they are not. Any wire that isn't connected to anything will have a small 'x' marked on it. (You may need to zoom in to make sure the wires are connected properly).

- Set the inputs and outputs for the circuit Use the circuit components selector, and go to primitives -> pin. You will need one input pin for each input variable, and one output pin for the output function. Set the pin names to the correct variable names. Make sure the inputs and output are properly connected to the gates At this point, save your work using File -> Save All Then go to Processing -> Start Compilation. If you did everything correctly your circuit will compile. If you get errors, check wiring and connections and compile again. **Do not proceed until your circuit compiles successfully.**
- Before programming the FPGA, we have to map inputs and outputs in our circuit to input and output elements in the DE2-115 board. We have at our disposal a set of 18 switches, and four push buttons to use as input. We also have 18 LEDs to use for output purposes. For this part we will use the four switches (SW0 to SW3) and one green LED (LEDG0). Locate these components on the FPGA board.

**Be very careful here, choosing the wrong device will void your design and possibly cause problems when attempting to program the device.**

On the Entity window, right-click on Stratix II (AUTO), select device. Select Cyclone IV E for family, click on Specific device selected... and choose EP4CE115F29C7 as the device.

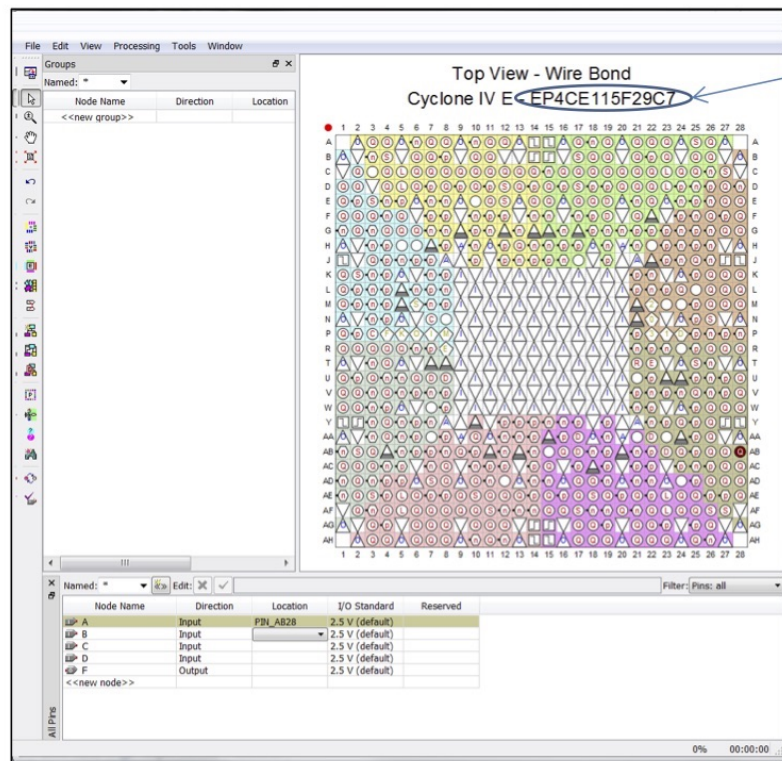


Right-click here



Double-check that the above matches the device type printed on the FPGA on the DE2-115 board

- Assign Your Pins In Quartus II, go to Assignments -> Pin Planner If you selected the device correctly, you will see a pin diagram for the FPGA, along with a list of the input and output pins in your circuit. Check the DE2-115 user manual for the mapping of switches and LEDs to pins, this can be found in Table 4-1, on page 35. For example, to assign input A to switch SW0, the manual indicates we should use PIN\_AB28. Double-click on the Location column for input A, and select PIN\_AB28 for this input.



Check you have  
the correct device

- Save your work, compile the project and fix any errors found at this stage. Turn your attention now to the DE2-115 board
  - Make sure power and USB connections are set up properly
  - Make sure the programming mode switch is set to RUN (see page 2)

Turn on the FPGA board by pressing the red power button.

You should see the welcome message on the LCD display, the numeric displays will be cycling digits, and the LEDs will be flashing. Wait a few seconds for the computer to recognize the board and load the appropriate drivers. Now in QuartusII go to Tools -> Programmer

Click on Hardware Setup... and choose USB Blaster

- Add the output file from your compilation (Add File -> Find your .sof file in your output\_files folder)  
To program your design onto the FPGA board, press Start.  
After the operation completes, the DE2-115 will have turned into the circuit you designed!

10. Now proceed to test that the circuit is indeed working to implement the logic function you designed.

Use SW0-SW3, to provide values for A, B, C, and D. The ordering of the variables should be such that A is the least-significant bit, and D is the most-significant bit.

Write the value of the output corresponding to all possible inputs (i.e. the truth table for the circuit) below.

D	C	B	A	Output (LED)
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

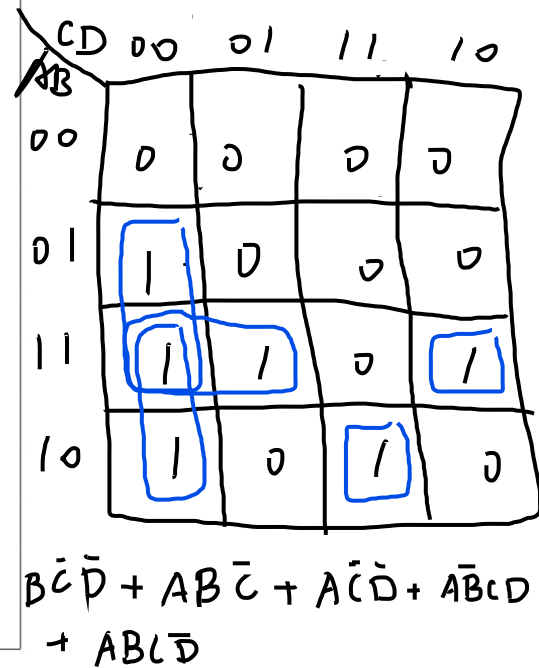
11. Show your work (and demonstrate your working code) to your TA



$$\overline{(B \bar{C} \bar{D})}$$

- $$(B+A) \bar{C} \bar{D} + A(B(\bar{C}+C\bar{D}) + \bar{B}CD)$$

D	C	B	A	F(D, C, B, A)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0


$$A \text{ and } B = (A \text{ and } B) \text{ and } (A \text{ and } B)$$

$A \text{ or } B = \neg A \text{ and } \neg B$   
and = not and  
or =

$$F(D,C,B,A) =$$

2. Simplify your function so that it can be implemented using nothing but NAND and NOT gates. Again, you'll just have to do this one manually for now (HINT: recall De Morgan's Law). We'll learn a more efficient way later. Draw the circuit diagram below. **(PRELAB)**

$$(B \wedge (\neg C) \wedge D) \vee (A \wedge B \wedge C) \vee (A \wedge (\neg C) \wedge (\neg D)) \vee (A \wedge B \wedge C \wedge D) \vee (A \wedge B \wedge C \wedge (\neg D))$$

$$\neg(\neg ① \wedge \neg ② \wedge \neg ③ \wedge \neg ④ \wedge \neg ⑤)$$

$$= \neg \{ (\neg ① \text{ nand } \neg ②) \text{ nand } (\neg ① \text{ nand } \neg ②) \}$$

$$\text{and } \{ (\neg ③ \text{ nand } \neg ④) \text{ nand } (\neg ③ \text{ nand } \neg ④) \}$$

$$\text{and } \neg ⑤$$

$$\begin{aligned} \neg ① &= (\neg B) \vee C \vee D = \neg(B \text{ and } \neg C) \text{ and } \neg D \\ \neg ② &= (\neg A) \vee (\neg B) \vee C = \neg(A \text{ and } B) \text{ and } \neg C \\ \neg ③ &= (\neg A) \vee C \vee D = \neg(A \text{ and } \neg C) \text{ and } \neg D \\ \neg ④ &= (\neg A) \vee B \vee (\neg C) \vee (\neg D) = \neg(A \text{ and } \neg B) \\ &\quad \text{and } \neg(C \text{ and } D) \\ \neg ⑤ &= (\neg A) \vee (\neg B) \vee (\neg C) \vee D \\ &= \neg(A \text{ and } B) \text{ and } \neg(C \text{ and } \neg D) \end{aligned}$$

3. Implement your new circuit on the FPGA board in a new project called `Lab_0b`
4. Test your code for each value in the truth table
5. Demonstrate your working code to your TA

## **1 Wrapping up**

1. Power down, and carefully store the DE2 board back in its original box. Boxes not neatly repackaged will not be accepted
2. Return your board to your TA
3. Take your code with you! On the desktop, locate the folders for `Lab_0` and `Lab_0b` . Select both folders and create a zip file containing all your work.
4. Submit the zip file on Quercus (to the Lab 0 assignment). You can do that after the lab, too. All partners have to submit to Quercus individually.