

# CSCB58 - Lab 2

## The *case* statement, Adders and ALUs

### Learning Objectives

In this lab you will design (a) multiplexers using the *case* statement, (b) a simple ripple-carry adder, and (c) an Arithmetic Logic Unit (ALU). You will also gain more practice with hierarchical design in Verilog and with using binary and hexadecimal numbers.

### Marks

Your TA must record the marks on this page as you complete each section of the lab. It is your responsibility to ensure that by the end of the lab, all work has been recorded appropriately.

Prelab	/3
Part I (in-lab)	/1
Part II (in-lab)	/1
Part III (in-lab)	/2
Clean work-space with all materials returned to their original state	/1
<b>TOTAL</b>	<b>/8</b>

### Preparation Before the Lab

Review the instructions in Lab 1 about preparations.

You are required to complete Parts I to III of the lab by designing your schematics, and writing your Verilog code. Show your schematics and well commented code to your TA at the beginning of the lab session.

**Note: you do not need to print-out the code/schematic.** It is OK to show the schematic and code on your laptop/tablet/web page/etc. It is also OK to have hand-drawn schematics on paper (as long as they are clear).

### In-lab Work

You are required to implement and test all of Parts I to III of the lab. You need to demonstrate all parts to the teaching assistants.

Write your name, UTorID, and student ID:

Name: \_\_\_\_\_

Student ID: \_\_\_\_\_

UTorID: \_\_\_\_\_

Write your partner's name, UTorID, and student ID:

Partner name: \_\_\_\_\_

Partner student ID: \_\_\_\_\_

Partner UTorID: \_\_\_\_\_

## Background

### Representing Constants

Verilog has a specific notation for representing constants (i.e., literal values). The following code snippet creates a 1-bit wire named `a`, which is connected to ground (logic-0).

```
wire a;  
assign a = 1'b0;
```

The number before the single quote is a decimal number representing the *bit width* (i.e., number of binary digits, bits). This is one for a single wire, but is higher for a vector or a bus (i.e., a collection of wires). The letter after the single quote is called the *radix* and specifies the base of the number that follows it. Possible values are `b` for binary, `d` for decimal (base 10) or `h` for hexadecimal (base 16). Octal is another valid representation albeit rarely used. Lastly, the value after the radix is the number in the numerical representation as specified by the radix.

For example, `2'b10` corresponds to the binary digits 10 meaning the number two, while `8'h1a` (or `8'h1A`) to the hexadecimal 1A meaning the number 26 in decimal. The latter can also be written in binary as `8'b0001_1010` and in decimal as `8'd26`. Verilog allows you to use underscores `_` to separate groups of bits to improve readability. Here we separated groups of 4-bits as they each correspond to a single hexadecimal digit.

### More Verilog Operators

This section presents various Verilog operators that you might find useful for this and future labs. You are also encouraged to refer to the Verilog tutorials on Quercus, as well as the collection of online Verilog material posted on Quercus.

- **Arithmetic operators:** `+` (addition), `-` (subtraction), `*` (multiplication), `/` (division), `%` (remainder), `**` (exponentiation).
- **Reduction operators:** These are unary operators that reduce a vector (multiple bits) to a single bit value. The operators are: `&` (AND all bits), `|` (OR all bits), and `^` (XOR all bits). You can prepend `~` to any of these to get reduction NAND (`~&`), NOR (`~|`) and XNOR (`~^`) operators. An example of a reduction XOR operation is `^ 3'b010` which will produce `1'b1`, the result of `0 ^ 1 ^ 0`.
- **Concatenation:** Verilog uses curly braces for concatenation. For example, `{2'b01, 1'b1}` will produce `3'b011`. Concatenation can also be used in the left hand side of an assignment statement.
- **Replication:** `{n{x}}` will replicate the value `x` `n` times. For example, `{3{2'b01}}` is equivalent to `6'b010101`.

## Part I

For this part of the lab, you will be learning how to use `always` blocks and `case` statements to design a 7-to-1 multiplexer.

Like a module, an `always` block can have inputs and outputs. A module can contain any number of `always` blocks just as any module can contain any number of other module instantiations. The difference is that an `always` block can only instantiate logic within the module where it is defined. A module can be instantiated in any other module, i.e., it can be reused.

Any output of an `always` block must have been declared as a **reg** type in the module containing the `always` block. Please note that you **cannot** use a **wire** for that purpose.

The model Verilog code for a 7-to-1 multiplexer built using a case statement is shown below. The seven inputs are from the signals named `Input [6:0]`. The output is called `Out`. The select lines are called `MuxSelect [2:0]`.

```

reg Out;          // declare the output signal for the always block

always @(*)       // declare always block with sensitivity *
begin
    case (MuxSelect[2:0]) // start case statement
        3'b000: Out = MuxInput[0]; // handle MuxSelect equals 0
        3'b001: Out = MuxInput[1]; // handle MuxSelect equals 1
        3'b010: Out = MuxInput[2]; // handle case 2
        3'b011: Out = ...           // case 3
        3'b100: Out = ...           // case 4
        3'b101: Out = ...           // case 5
        3'b110: Out = ...           // case 6
        default: Out = 1'b0;        // default case (all other cases)
    endcase
end

```

An `always` block is triggered to execute in simulation whenever there is a change in the *sensitivity list*. In the example above, this list is defined as the asterisk character (\*), meaning that whenever *any* input to the `always` block is changed, the code in the `always` block will be simulated. We can change the asterisk to certain inputs to limit when this code is triggered, but this can lead to simulations that do not match the real hardware. One of the (unfortunate) features of the Verilog language. The accepted practice today is to always use the asterisk in your `always` block for *combinational* logic, i.e., any logic where the outputs rely strictly on the inputs. You will learn more about *combinational* and *sequential* logic later. **For now, use the asterisk in the `always` block for a `case` statement as shown above.**

It is important to have a `default` case to ensure that all cases are covered. Otherwise, you can again have simulations that do not match the hardware. Yet another Verilog feature! Your goal is to write Verilog that will generate hardware that exactly matches the simulation, so **make sure to include the `default` statement**.

(If you want to know more, read on. When you execute an `always` block, the use of `if` and `case` statements can take you through different code paths. If you reach the end of the `always` block and there is an unassigned (**reg**) variable, then Verilog must create a memory element, a latch: since the meaning is that the variable keeps its previous value, Verilog infers a memory element is inferred. The problem becomes more subtle because if `MuxSelect` in the above example is three bits, there are actually more than eight cases! Each bit can be 1, 0, x (unknown value), or z (high-impedance) – so there are really  $4^3 = 64$  possible paths. Synthesis tools will likely assume only 1 or 0 and create the correct circuit, but the simulator may not do the same. **Always, always put in the `default` statement**. If you did not understand the above, at least you, hopefully, now see how Verilog can have subtle side effects that can cause problems. To avoid these issues, we will show you coding styles that help avoid most problems.)

Using  $SW_{6-0}$  as the data inputs and  $SW_{9-7}$  as the select signals, display on  $LEDR_0$  the output of a 7-to-1 multiplexer using the case statement style as shown above.

1. Draw a schematic showing your code structure with all wires, inputs and outputs labeled. Be prepared to explain it to the TA as part of your preparation. **(PRELAB)**
2. Create a new Quartus II project for your circuit.
3. Include your Verilog file for the circuit in your project. Use switches  $SW_{9-7}$  on the DE2 board as the `MuxSelect` inputs and switches  $SW_{6-0}$  as the Input data inputs. Connect the output to  $LEDR_0$ . **(PRELAB)**
4. Compile the project.
5. Download the compiled circuit into the FPGA chip. Test the functionality of the circuit by toggling the switches and observing the LEDs.
6. As always, demonstrate to the TA.

## Part II

Figure 2a shows a circuit for a *full adder*, which has the inputs  $a$ ,  $b$ , and  $c_i$ , and produces the outputs  $s$  and  $c_o$ . Parts b and c of the figure show a circuit symbol and truth table for the full adder, which produces the two-bit binary sum  $c_o s = a + b + c_i$ . Please note that the  $+$  operator here means addition and not logic-OR. Figure 2d shows how four instances of this full adder module can be used to design a circuit that adds two four-bit numbers. This type of circuit is called a *ripple-carry* adder, because of the way that the carry signals are passed from one full adder to the next. Write Verilog code that implements this circuit, as described below. Be sure to use what you learned about hierarchy in Lab 1 (e.g., build the solution from multiple copies of the same block).

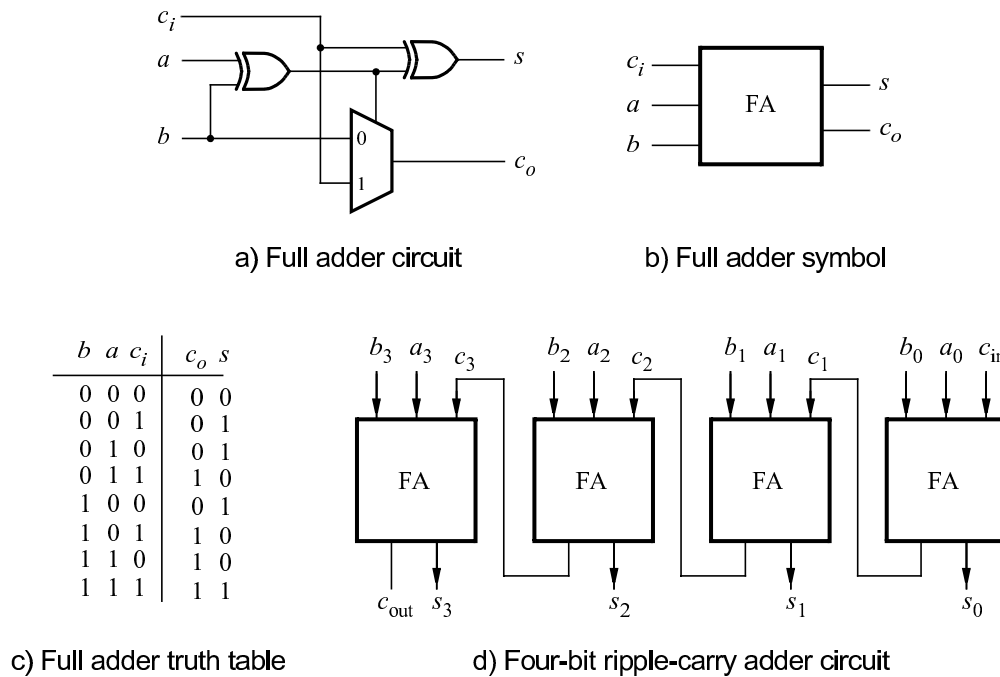


Figure 2. A ripple-carry adder circuit.

Perform the following steps:

1. Draw a schematic showing your code structure with all wires, inputs and outputs labeled. Your schematic should resemble Fig. 2d, though it should also contain module and signal labels, also showing external connections to the switches and LEDs. Be prepared to explain it to the TA as part of your preparation. **(PRELAB)**
2. Write a Verilog module for the full adder subcircuit and write a top-level Verilog module that instantiates four instances of this full adder. **You may not use the Verilog arithmetic operators (in particular  $+$ ) in your Verilog implementation of the full-adder.** Doing so will earn you 0 marks for this part. **(PRELAB)**
3. Use switches  $SW_{7-4}$  and  $SW_{3-0}$  to represent the inputs  $A$  and  $B$ , respectively. Use  $SW_8$  for the carry-in,  $c_{in}$ , of the adder. Connect the outputs of the adder,  $c_{out}$  and  $S$ , to the LEDs  $LEDR_9$  and  $LEDR_{3:0}$  respectively.
4. Compile the project.
5. Download the compiled circuit into the FPGA chip. Test the functionality of the circuit by toggling the switches and observing the LEDs. As always, demonstrate to the TA.

## Part III

Using Parts I and II from this lab and the HEX decoder from Lab 1 Part III, you will implement a simple Arithmetic Logic Unit (ALU). An ALU has two inputs and can perform multiple operations on the inputs such as addition, subtraction, logical operations, etc. The output of the ALU is selected by *function* bits that specify the function to be performed by the ALU. The easiest way to build an ALU is to implement all required functions and connect the outputs of the functions to a multiplexer. Choose the output value for the ALU using the ALU *function* inputs to drive the multiplexer select lines. The output of the ALU will be displayed on the LEDs and HEX displays.

Shown in the case statement below are the operations to be implemented in the ALU for each *function* value in pseudo code format. The ALU has two 4-bit inputs, *A* and *B* and an 8-bit output, called *ALUout[7:0]*. Note that in some cases, the output will not require the full 8 bits so do something reasonable with the extra bits, such as making them 0 so that the value is still correct.

```
always @(*)          // declare always block
begin
  case (function)    // start case statement
    0: A + B using the adder from Part II of this Lab
    1: A + B using the Verilog '+' operator
    2: A XOR B in the lower four bits of the output and A OR B in the upper four bits
    3: Output 1 (8'b00000001) if at least 1 of the 8 bits in the two inputs is 1 using a single OR operation
    4: Output 1 (8'b00000001) if all of the 8 bits in the two inputs are 1 using a single AND operation
    5: Make the inputs appear at the output, with A in the most significant four bits and B in the least significant four bits.
    default: ...     // default case, output 0
  endcase
end
```

Note that in this part of the lab, you will need to use Verilog concatenation for the additions, sign extension, and the Verilog reduction operations for ORing and ANDing multiple bits without typing out the operation for each bit individually.

The *A* and *B* inputs connect to switches *SW<sub>7-4</sub>* and *SW<sub>3-0</sub>* respectively. Use *KEY<sub>2-0</sub>* for the *function* inputs. Display *ALUout[7:0]* in binary on *LEDR<sub>7-0</sub>*; have *HEX0* and *HEX2* display the values of *B* and *A* respectively in hexadecimal and set *HEX1* and *HEX3* to 0. *HEX4* and *HEX5* should display *ALUout[3:0]* and *ALUout[7:4]* respectively in hexadecimal.

Perform the following steps:

1. Draw a schematic showing your code structure with all wires, inputs and outputs labeled. Your schematic should contain a block diagram of your design showing any design hierarchy. You should show the multiplexer that is implied by the case statement for your ALU as well as all inputs to this multiplexer. Also show all connections to switches and LEDs. Be prepared to explain it to the TA as part of your preparation. **(PRELAB)**
2. Write a Verilog module for the ALU including all inputs and outputs. **(PRELAB)**
3. Create a new Quartus II project for your circuit.
4. Compile the project.
5. Download the compiled circuit into the FPGA chip. Test the functionality of the circuit. Show to TAs.

### Notes:

- In your simulation, *KEY<sub>3-0</sub>* are inverted. Remember that the DE2 board recognizes an unpressed pushbutton as a value of 1 and a pressed pushbutton as a 0.
- Some boards have faulty buttons (for example, they might constantly flip values when pressed). If that happens, use a switch instead of a key.

Take all your code with you, and remember all partners have to submit to Quercus individually.