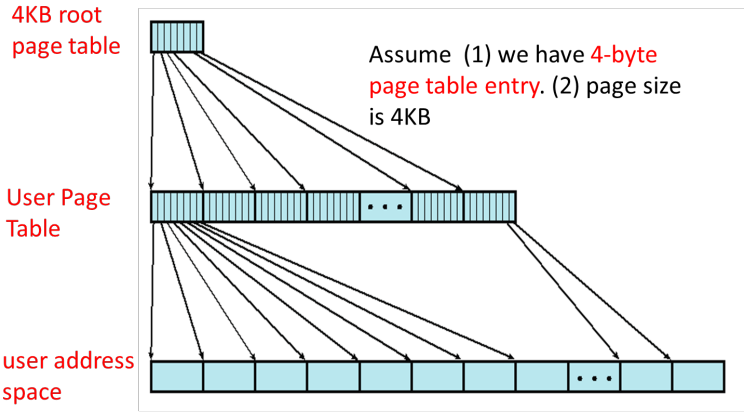
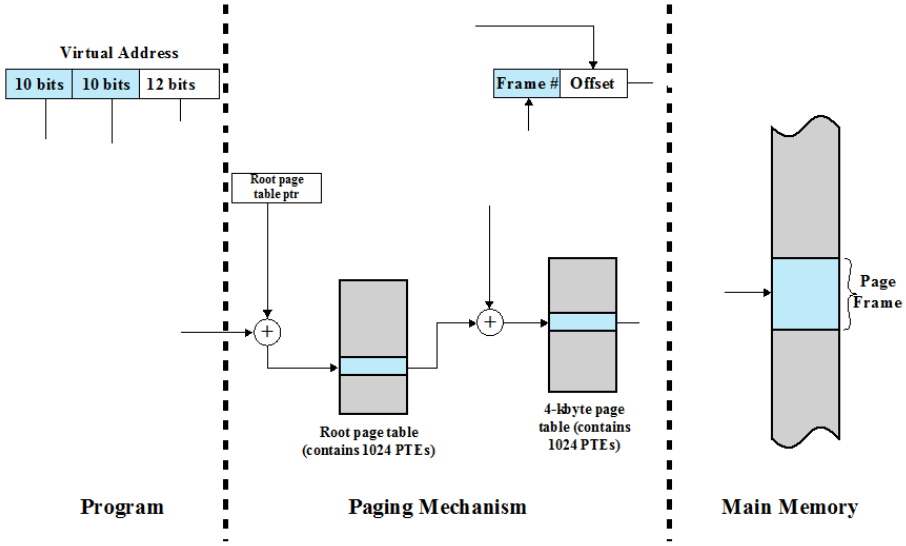
COMP3500: Translation Look-aside Buffers (TLB)– Exercises

Exercise 1: We assume each page table entry is 4 bytes, the page size is 4 KB.



Given a 4KB root page table, please answer the following three questions:
(1) How many root page table entries?
(2) How many user page table entries?
(3) How large is the user address space?

Exercise 2: How does the address translation work in the two-level paging system?



Exercise 3: Suppose you design a two-level page translation scheme where page size is 16MB and page table entry size is 16 bytes. What is the format of a 64-bit virtual address?

Exercise 4: (1) To load an instruction or data from main memory, how many memory accesses are required in the paging scheme? (2) What is the problem with respect to memory access? Solution?

Exercise 5: Consider a single-level paging scheme with no data cache. The TLB has 32 entries. The TLB access time is 10 ns; memory access time is 200ns.

5.1 How long does it take to access data in memory if there is a TLB hit?

5.2 How long does it take to access data in memory if there is a TLB miss?

5.3 What is the effective memory-access time if we have a TLB hit ratio of 80%?

5.4 What is the minimal hit ratio that guarantees the effective access time of at most 220ns?