COMP3500: Paging – Exercises

Exercise 1: How to use a page table to perform logical-to-physical address translations (Fig. 1)?

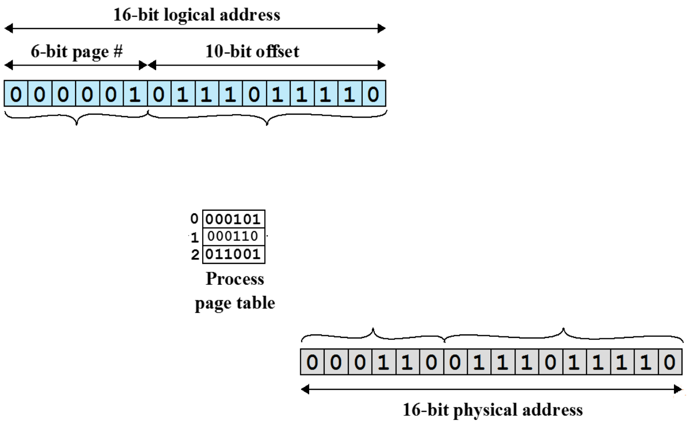

Fig. 1

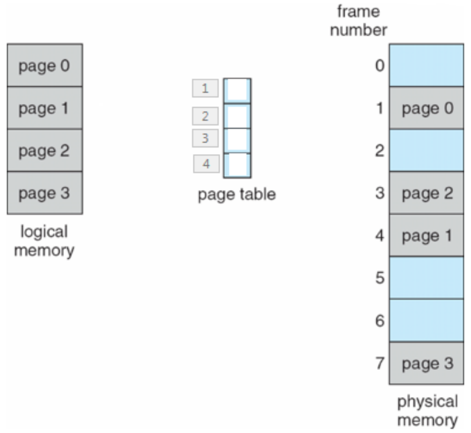

Fig. 2

Exercise 2: Please fill the page table up in Fig. 2.

Exercise 3: (1) What is the size of physical memory in Fig. 3? (2) What is the page size? (3) How many bits are used as an index into a page table? (4) How many bits are used for page offset? (5) How many bits are there in the logical address?

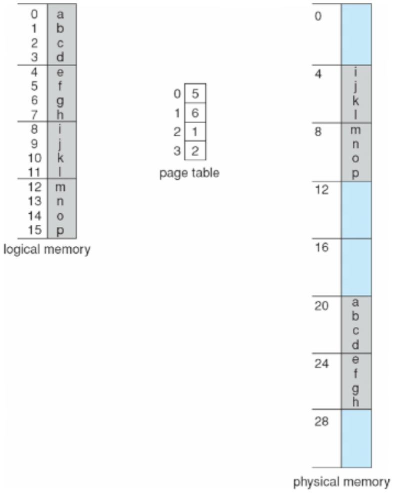

Fig. 3

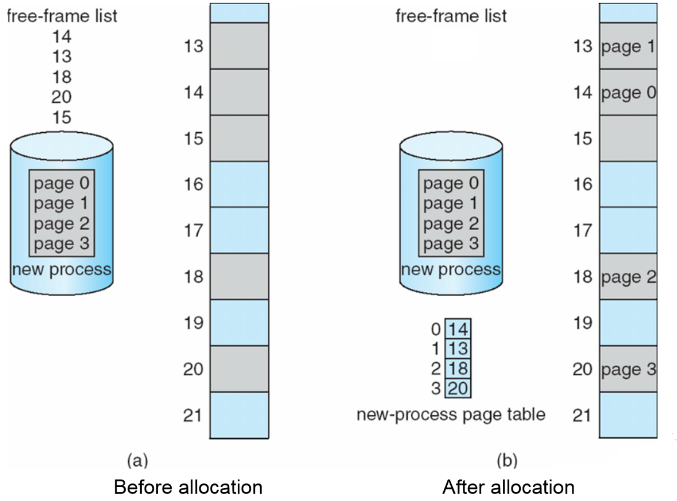

Fig. 4

Exercise 4: Assume that page size is 2,048 bytes and a process size is 72,766 bytes. (1) How many pages are there in this process? (2) How many bytes are there in the last page? (3) What is the internal fragment?(4) What is the worst case fragmentation? (5) What is the average fragmentation?

Exercise 5: Is it a good idea to keep frame size very small? Why?

Exercise 6: What is the free-frame list after allocation in Fig. 4?

Exercise 7: (1) Where should we keep page tables? (2) Where does the *Page-table base register (PTBR)* point at? (3) The *Page-table length register (PTLR)* indicates size of the page table. Why the *Page-table length register (PTLR)* is important?

Exercise 8: (1) To load an instruction or data from main memory, how many memory accesses are required in the paging scheme? (2) What is the problem with respect to memory access? Solution?