COMP 4300 Exam Review 2

Internal Memory

- SRAM/DRAM
    - DRAM – Dynamic RAM
        - Made with cells that store data as charge on capacitors
        - Presence or absence of charge in capacitor is interpreted as a binary 1 or 0.
        - Requires periodic charge refreshing to maintain data storage
        - Tendency of the stored charge to leak away, even with power continually applied (hence the term dynamic)
        - Simpler to build
        - More dense (smaller cells = more cells per unit area)
        - Less expensive
        - Requires supporting refresh circuitry
        - Tend to be favored for large memory requirements
        - Used for main memory
    - SRAM – Static RAM
        - Digital device uses the same logic elements used in the processor
        - Binary values are stored using traditional flip-flop logic gate configurations
        - Will hold its data as long as power is supplied to it
        - Faster
        - Used for cache memory
- ROMS/PROMS/EEPROMS
    - Read Only Memory (ROM)
        - Data cannot be changed or added to
        - No power source required to maintain the bit values in memory
        - Data or program is permanently in main memory and never needs to be locate din secondary memory
        - Data is actually wired into the chip as part of the fabrication process
            - Disadvantage
                - No room for error
                - Data insertion has a relatively large cost

- Programmable Read Only Memory (PROM)
  - Less expensive alternative
  - Nonvolatile
  - May be written to once
  - Provides flexibility and convenience
  - Writing process is performed electrically and may be performed at a later time than the original chip fabrication
- Electrically Erased Programmable Read Only Memory (EEPROM)
  - Can be written into at any time without erasing prior contents
  - Combines non-volatility with the flexibility of being updatable in place
  - More expensive than EPROM and less dense
- Flash
  - Uses an electrical erasing technology like EEPROM except it is much faster
  - Memory cells erased in a single action, hence "flash"
  - NOR
    - Cells connected in parallel o the bit lines so that each cell can be read/write/erased individually
    - Bit line goes low if any memory cell of the device is turned on b the corresponding word line
  - NAND
    - Organized in transistor array with 16 or 32 transistors
    - Bit line goes low only if **all** transistors in the corresponding word lines are turned on

- Refresh Operation
  - Used in DRAM
  - Problems
    - Capacitors do not hold their charge indefinitely
      - Can cause memory to be lost
        - Point of refresh operation
- Interleaved Memory
  - Banks

        - A number of chips can be grouped together to form a memory bank
        - Each bank is able to complete a memory read or write request on its own.
    - Not random, rather spatial, temporal localities
- Hamming Codes and Parity
    - Soft Errors
        - Random, non-destructive even that alters the contents of one or more memory cells
        - No permanent damage to memory
        - Causes
            - Power supply problems
            - Alpha particles
    - Hard Errors
        - Permanent physical defect
        - Memory cell(s) affected cannot reliably store data but become stuck at 0 or 1 or switch erratically between the two.
        - Causes
            - Harsh environmental abuse
            - Manufacturing defects
            - Wear
- SDRAM & DDR-SDRAM
    - SDRAM – Synchronous DRAM
        - One of the most widely used forms of DRAM
        - Exchanges data with the processor synchronized to an external clock signal that runs at full speed of the processor/memory bus without imposing wait states.
        - Other tasks can safely be done while SDRAM is processing.
    - DDR-RAM – Double Data Rate SDRAM
        - Widely used in desktop computers and servers
        - Achieves higher data rates in three ways
            - Data transfer is synchronized to both rising and falling clock edges instead of just rising edge
            - Uses a higher clock rate on the bus to increase the transfer rate
            - A buffering scheme is used

External Memory

- Magnetic Disks Function
    - Disk constructed of nonmagnetic material coated with a magnetizable material
        - Substrate, nonmagnetic material, is generally aluminum or aluminum allot material
        - Glass substrates recently introduced
            - Benefits
                - Improvement of uniformity of the magnetic film surface to increase disk reliability
                - Reduction is overall surface defects reducing read-write errors
                - Ability to support lower fly heights
                - Better stiffness to reduce disk dynamics
                - Greater ability to withstand shock and damage
- Seek time, rot delay, track, sector, access time, transfer time
    - Seek time – time it takes to position the head at the track
    - Rotational delay – time it takes for the beginning of the sector to reach the head
    - Track – Organizations of data in a concentric set of rings located on the platter.
        - There are thousands of tracks per surface
    - Sector – Data transfers to and from the disk in sectors
        - There are usually hundreds of sectors in a single track with either a fixed or variable length
    - Access time – Time it takes to get into position to read or write
        - Seek Time + Rotational Delay = Access Time
    - Transfer time – Time it takes for the data to be transferred
- Circular redundancy check
- RAID Error Control
    - parity, Hamming Code, mirroring
        - Parity
            - Bits are updated each time a write occurs
                - Each strip write = 2 reads and 2 writes
                    - User data must also be updated
            - Parity Strip

        - To calculate the new parity strip, must read old user strip and old parity strip
    - Hamming Code
        - Correct single-bit errors
        - Detect double –bit errors
    - Mirroring
        - Data striping is used but each logical strip is mapped to two separate physical disks so that every disk in the array has a mirror disk that contains the same data
- SSD Disks
    - Block level erase, write
        - Before the block can be written back to flash memory, the entire block must be erased.
    - Wear leveling
        - Wear-leveling algorithms help evenly distribute writes across block of cells
    - Front interface with cache
        - Allows to delay and group write operations
- CD/DVD – basic CD and CD R/W operation
    - CD
        - Non-erasable
        - Stores digitized audio information
    - CD-RW
        - Erase and rewrite to the disk multiple time
- Tapes
    - Uses same reading and recording techniques as disk systems
    - Medium is flexible polyester tape coated with magnetizable material
    - Serial Recording
        - Data is laid out as a sequence of bits along each track
    - Data is read and written in contiguous blocks
        - Physical records
    - Blocks on tape are separated by gaps
        - Inter-record gaps

I/O

- Major functions of I/O Module
  - Two Major functions
    - Interface to the processor and memory via the system bus or central switch
    - Interface to one or more peripheral devices by tailored data links
- Programmed I/O, interrupt driven I/O, DMA
  - Figure 7.4

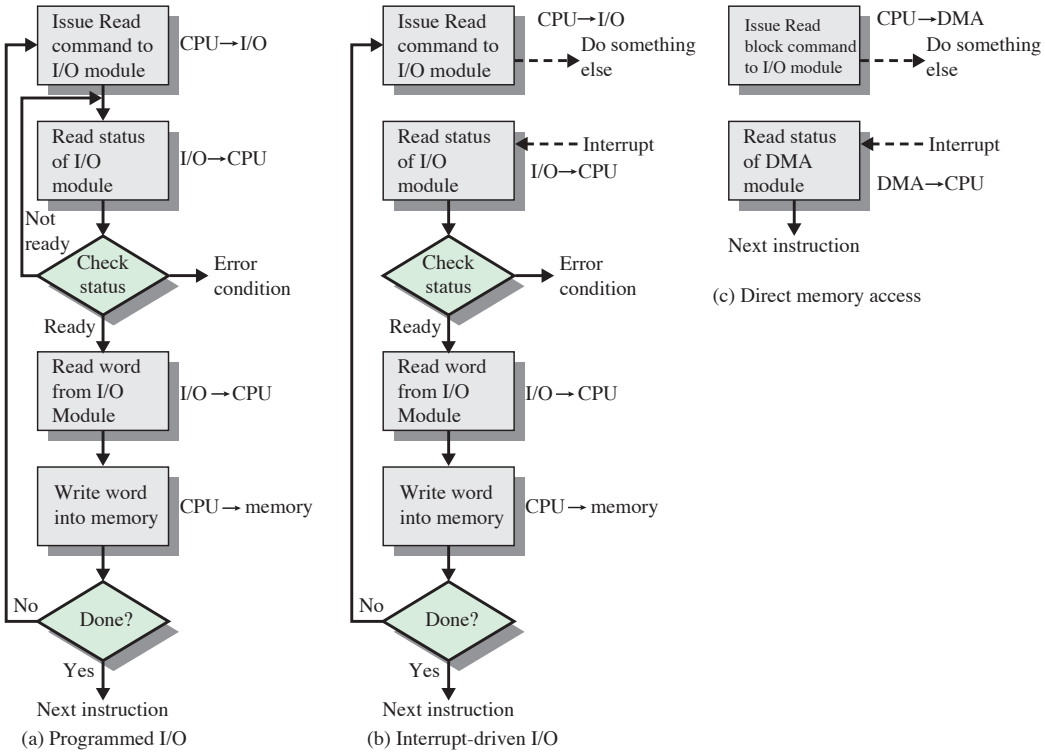

Figure 7.4 Three Techniques for Input of a Block of Data

  - Compare and contrast techniques
    - Programmed I/O
      - Processor executes a program that gives it control over the I/O operation. If a command is issued, the processor must wait until the I/O operation is completed.
    - Interrupt-Driven I/O
      - Processor is interrupted by the I/O module when a command has been issued

        - Direct Memory Access (DMA)
            - I/O module and main memory exchange data directly without processor involvement
            - More efficient technique when large volumes of data need to be moved
- Memory mapped I/O, isolated I/O
    - Memory Mapped I/O
        - Devices and memory share an address space
        - I/O looks just like memory read/write
        - No special commands for I/O
            - Large selection of memory access commands available
    - Isolated I/O
        - Separate address spaces
        - Need I/O or memory select lines
        - Special commands for I/O
            - Limited set
- Device Identification – ways to find a who caused an interrupt
    - Multiple interrupt lines
        - Most straightforward approach
        - If multiple lines are used, it is likely that each line will have multiple I/O modules attached to it
    - Software poll
        - When the processor detects an interrupt it branches to an interrupt service routine whose job is to poll each I/O module to determine which module caused the interrupt
            - Time consuming
    - Daisy chain (hardware poll, vectored)
        - Interrupt acknowledge line is daisy chained through the modules
        - Vector – address of the I/O module or some other unique identifier
        - Vectored Interrupt
            - Processor uses the vector as a pointer to the appropriate device-service routine avoiding the need to execute a general service routine first.
    - Bus arbitration (vectored)

        - I/O module must first gain control of thus bus before it can raise the interrupt request line
        - When the processor detects the interrupt, it responds on the interrupt acknowledge line
        - Then the requesting module places its vector on the data lines
- USB/FireWire (IEEE-1394)
    - USB
        - Widely used for peripheral connections
        - Default interface for slower speed devices
        - Commonly used high-speed I/O
    - FireWire Serial Bus
        - IEEE standard 1394, for a High Performance Serial Bus
        - Alternative to small computer system interface for small computers, workstations, and servers
        - Objective:
            - Meet the increasing demands for high I/O rates while avoiding the bulky and expensive I/O channel technologies developed for mainframe and supercomputer systems
        - 1022 FireWire buses can be interconnected using bridges
        - Hot plugging
            - Allows for connection and disconnection of peripherals without having to power the computer system down or reconfigure the system
        - Automatic configuration to assign addresses
        - No terminations
- DMA/breakpoints – Figure 7.13, 7.15
    - 7.13

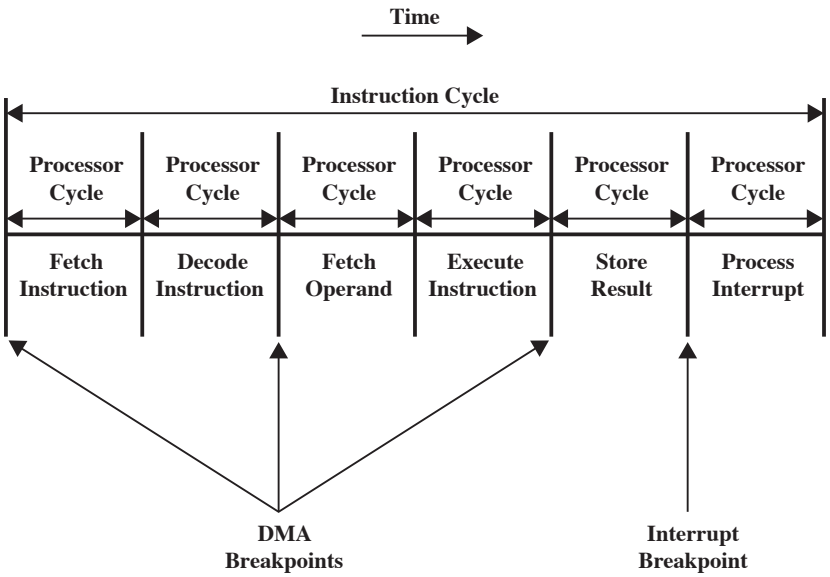

Figure 7.13 DMA and Interrupt Breakpoints During an Instruction Cycle

- 7.15

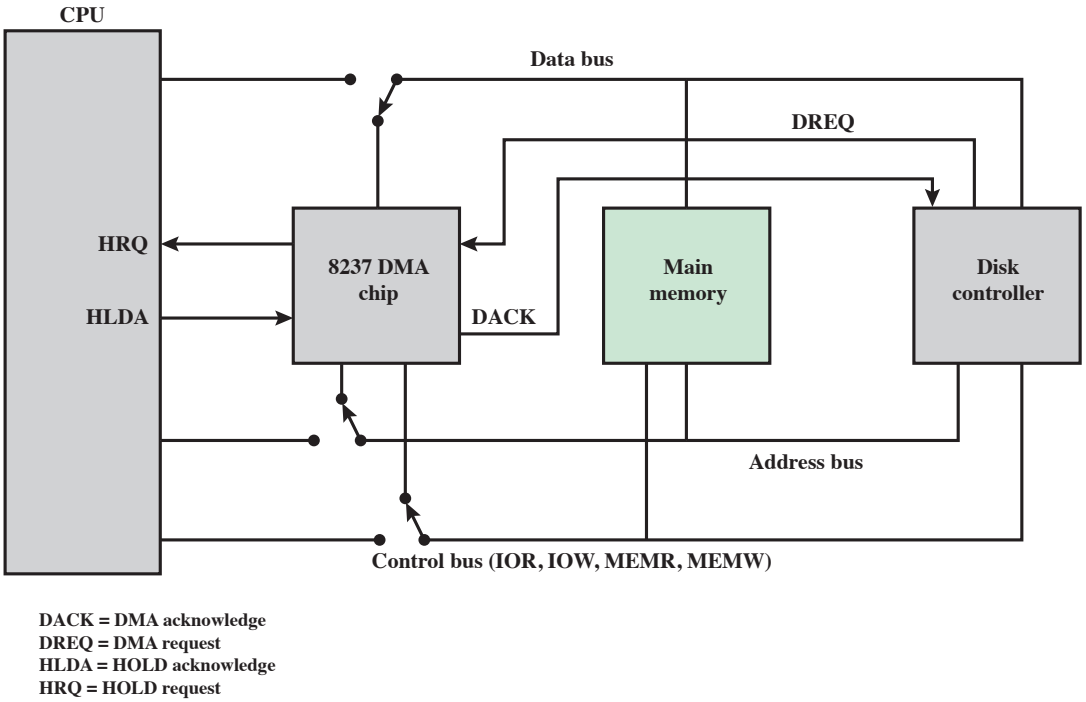

Figure 7.15 8237 DMA Usage of System Bus

- Problems from class and in homework