ACTIVITY 18

Suppose:
- Memory addresses are **8 bits**.
- The cache is **2-way** set-associative.
- Cache lines are **8 bytes**.
- There are **8 rows** in the cache.

1. How large is the address space? (How many bytes of memory can be addressed?) What is the address of the first byte of memory? The last byte?

2. The addresses of the first 32 bytes of memory are shown to the right. Which memory addresses will be in block 0? block 1? block 2? etc.

3. How many bits of the 8-bit memory address are used for the block number? Why?

4. Show how the following memory address is divided into a *block number* and an offset within the block.

   0 0 0 1 0 1 1 0

5. The cache is shown below. Indicate which rows correspond to which sets.

	Tag	Data
0		
1		
2		
3		
4		
5		
6		
7		

6. How many bits of the 8-bit memory address are used for the set number? Why?

7. Show how the following memory address is divided into a tag, index (set number), and offset within the block.

   0 0 0 1 0 1 1 0

8. Suppose the processor reads memory address 00010110. When the corresponding block of data is copied from main memory into the cache...

   a. Which row(s) of the cache could the data from main memory be copied into?

   b. How many bytes of data are copied from main memory into the cache?

   c. The data from which memory addresses are copied into the cache?

00000000 = 0
00000001 = 1
00000010 = 2
00000011 = 3
00000100 = 4
00000101 = 5
00000110 = 6
00000111 = 7
00001000 = 8
00001001 = 9
00001010 = A
00001011 = B
00001100 = C
00001101 = D
00001110 = E
00001111 = F
00010000 = 10
00010001 = 11
00010010 = 12
00010011 = 13
00010100 = 14
00010101 = 15
00010110 = 16
00010111 = 17
00011000 = 18
00011001 = 19
00011010 = 1A
00011011 = 1B
00011100 = 1C
00011101 = 1D
00011110 = 1E
00011111 = 1F
...

As before, suppose:

- Memory addresses are **8 bits**.
- The cache is **2-way** set-associative.
- Cache lines are **8 bytes**.
- There are **8 rows** in the cache.

Furthermore, suppose the cache is populated as follows:

	Row	Tag (Binary)	Data (Hexadecimal)
Set 0	0	011	0A 0B 0C 0D 0E 0F 0F 0F
	1	101	F0 A0 B0 C0 F0 12 13 1F
Set 1	2	100	00 00 00 00 00 00 00 00
	3	000	FF FE FD FC FB FA 00 00
Set 2	4	011	3C 12 D8 F7 33 **6F** 2D 5C
	5	110	11 22 33 44 55 66 77 88
Set 3	6	111	F0 A0 **B0** C0 F0 12 13 1F
	7	110	E8 F3 27 5C BA D3 CC F8

9. Suppose the processor reads memory address 01111000. Is this byte in the cache? Explain.

10. Suppose the processor reads memory address 01100000. Is this byte in the cache? Explain.

11. Suppose the processor reads memory address 01110010. Is this byte in the cache? Explain.

12. In row 4, the byte value 6F is shown in bold and underlined. What memory address was this byte loaded from?

13. In row 6, the byte value B0 is shown in bold and underlined. What memory address was this byte loaded from?

14. What is the maximum amount of data that can be stored in this cache? If it is completely full, what fraction of main memory is cached?

15. My MacBook Pro has 8 GB of RAM. Its largest cache—the L3 cache—is 4 MB. What percentage of main memory can be in the L3 cache at any point in time?