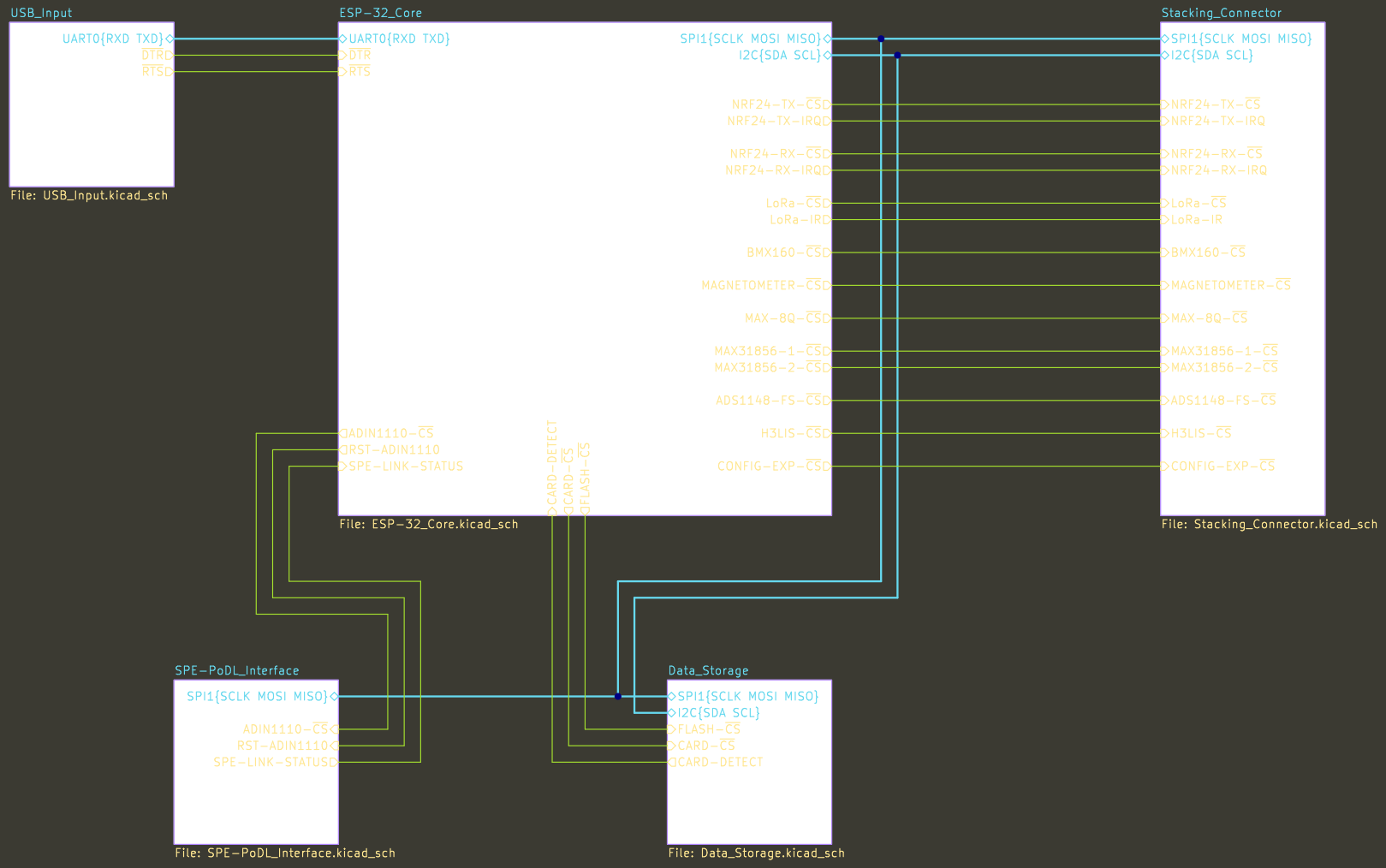


Sheet: /
File: Forerunner-Cubic-Mainboard.kicad_sch

Title: Overview

Size: A4	Date: 2024-01-21	**Rev: 1.0.1**
KiCad E.D.A. kicad 7.0.7		Id: 1/7

Power Rail Caps

+3V3 +3V3 +3V3 +1V1 +1V1

C14 100nF C15 10nF C16 10nF C17 100nF C18 10nF C19 100nF C20 100nF C22 680nF

GND GND GND GND GND GND GND GND GND

AVDD_H AVDD_L VDDIO DVDD_1P1 DLDO_1P1

Oscillator

CL = 18pF, Assume Cstray = 3pF (1pF5 on each pin per ADIN1110 datasheet)
CL = (C1 * C2) / (C1 + C2) + Cstray
C1, C2 = 30pF ->

X1
ABRACON_ABM8-25.000MHZ-12-D2Y

XTAL-I XTAL-O

C24 30pF NPO C25 30pF NPO

GND GND GND

TDK SPE Applications Overview
(NOTE: Using Line-Side Injection for Power Class 15 in this design)
https://product.tdk.com/en/techlibrary/applicationnote/single-pair-ethernet.html

PoDL Line-Side Injection

+24V 24V_RTN

F2 FAST 32V 3A

3µH6 L2 3µH6 L3

C28 15nF 50V

Line side injection allows for more compact choke, as it does not require 1500mA capacity

fc: 500kHz
Drives boost converter freq

CONTACT POSITION	SIGNAL PER IEC 63171-6
1	BI_DA+
2	BI_DA-

Mfr. Recommended Hybrid w/DC Blocking Caps

R26 49R9 0402

TX_N RX_N RX_P TX_P

R27 5K1 0402 C26 220nF 50V 0402 DATA-

R28 5K1 0402 C27 220nF 50V 0402 DATA+

R29 49R9 0402

R24 10K2 0402 R25 10K2 0402

100R 100R_PoE

L1
350mA
25%
250R
279nH

Place network as close to IC pins as possible

Cap voltage rating defined by 24V PoDL Req. and 40V TVS

+3V3 +1V1 DLDO1P1 powers DVDD1P1 from internal LDO

U6

AVDDH AVDDH AVDDL DLDO1P1 DVDD1P1 VDDIO

RST-ADIN1110D RST

XTAL-I XTAL-O CLK25REF

SPI1.MISO SPI1.MOSI SPI1.SCLK ADIN1110-CSD SPI-CFG1 SDO/SPI-CFG0 SDI SCLK CS SPI-CFG1

INT-ADIN1110 INT

DNC DNC DNC

EP GND

TX_N RX_N RX_P TX_P

LED0 LED1 LINK-ST TX2P4_EN SWPD_EN

SPE-LED

LED1 disabled by default

SPE-LINK-STATUS

TX2P4 Pulled down internally for 2V4p-p mode

CEXT2 CEXT3

TEST1 TEST2

TS-CAPT TS-TIMER

DNC DNC DNC DNC DNC DNC

C21 0603 1uF C23 0603 100nF

GND GND

AD_ADIN1110CCPZ

RST has Internal Pull-Up

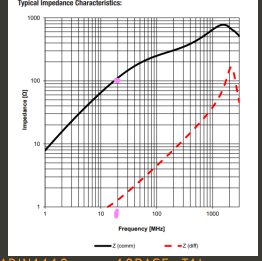
SPI1{SCLK MOSI MISO}

Trace Impedance Calcs

File: Trace_Impedance_Calcs.kicad_sch

Wurth Elektronik 744230251

Typical Impedance Characteristics:



D8 TVS 40V D9 TVS 40V

GND GND GND

Optional 0603 FP to float or use cap to termination shield

R30 0R

J2

SHLD1 SHLD2 SHLD3 SHLD4

AMP_MSPE-J2L0-B01

Only need to connect drain at 1 shield pin

ADIN1110 uses 10BASE-T1L:
- Speccing a CMC for 100R @ 20MHz
Due to board size constraints, will NOT be adopting
IEEE 802.3 insulation requirements (i.e. no isolating transformer)
IEC 62368-1:
- Withstand 1500VAC for 60s
- Withstand 2250VDC for 60s

The SPE electrical requirements are specified in the following IEEE standards:

- IEEE 802.3cg (10BASE-T1) with bandwidth from 0.1 to 20 MHz and reach up to 1000 m.
- IEEE 802.3bw (100BASE-T1) with bandwidth 0.3 to 66 MHz and reach up to 40 m.
- IEEE 802.3bp, (1000BASE-T1) with bandwidth 1 to 600 MHz and reach up to 40 m.

SPE Standard Basic Info:
https://single-pair-ethernet.com/sites/default/files/2021-03/202103speapplikationnotespe-integrationv10en_anp085.pdf

Status LED, Active Low Config

+3V3 +3V3

R19 5K1 0603 R20 121R

SPE-LED D7 2V85 5mA Blue

(3.3-2.85)/121 = 3.7mA
LED Max = 15mA
Pin Max = 8mA @ 3V3

Pull-Ups/Config

+3V3 +3V3 +3V3

R21 1K5 R22 1K5 R23 5K1

INT-ADIN1110 TEST1 SPI-CFG1

SPI Configs are PULLED AT BOOT-UP!
- Careful when initializing devices

SPI_CFG0 (MISO) is pulled down by IC by default
SPI_CFG1 desires 4K7 pull ups; using 5K1 for BoM optimization

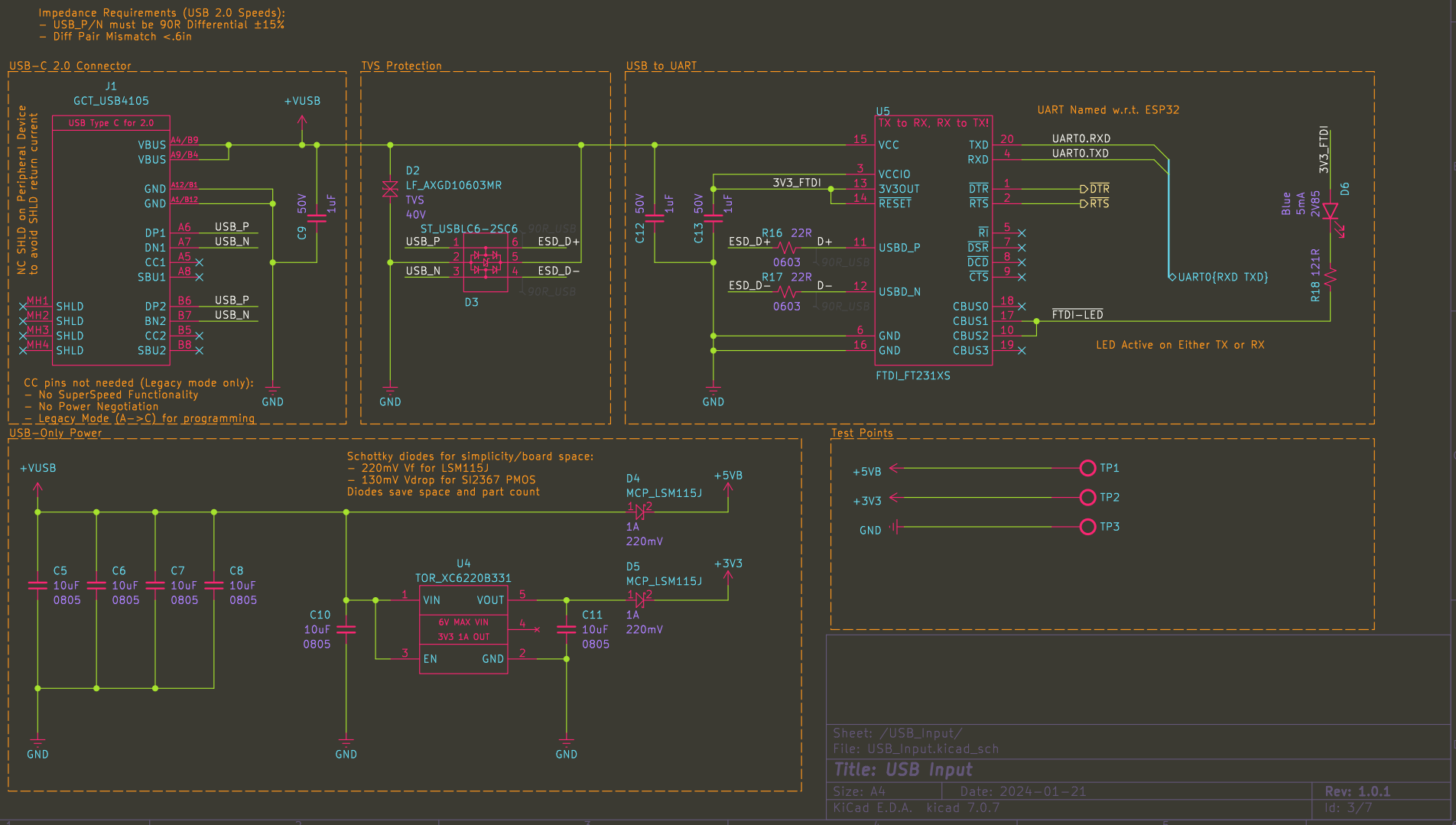
Table 16. SPI Protocol (Hardware Configuration)

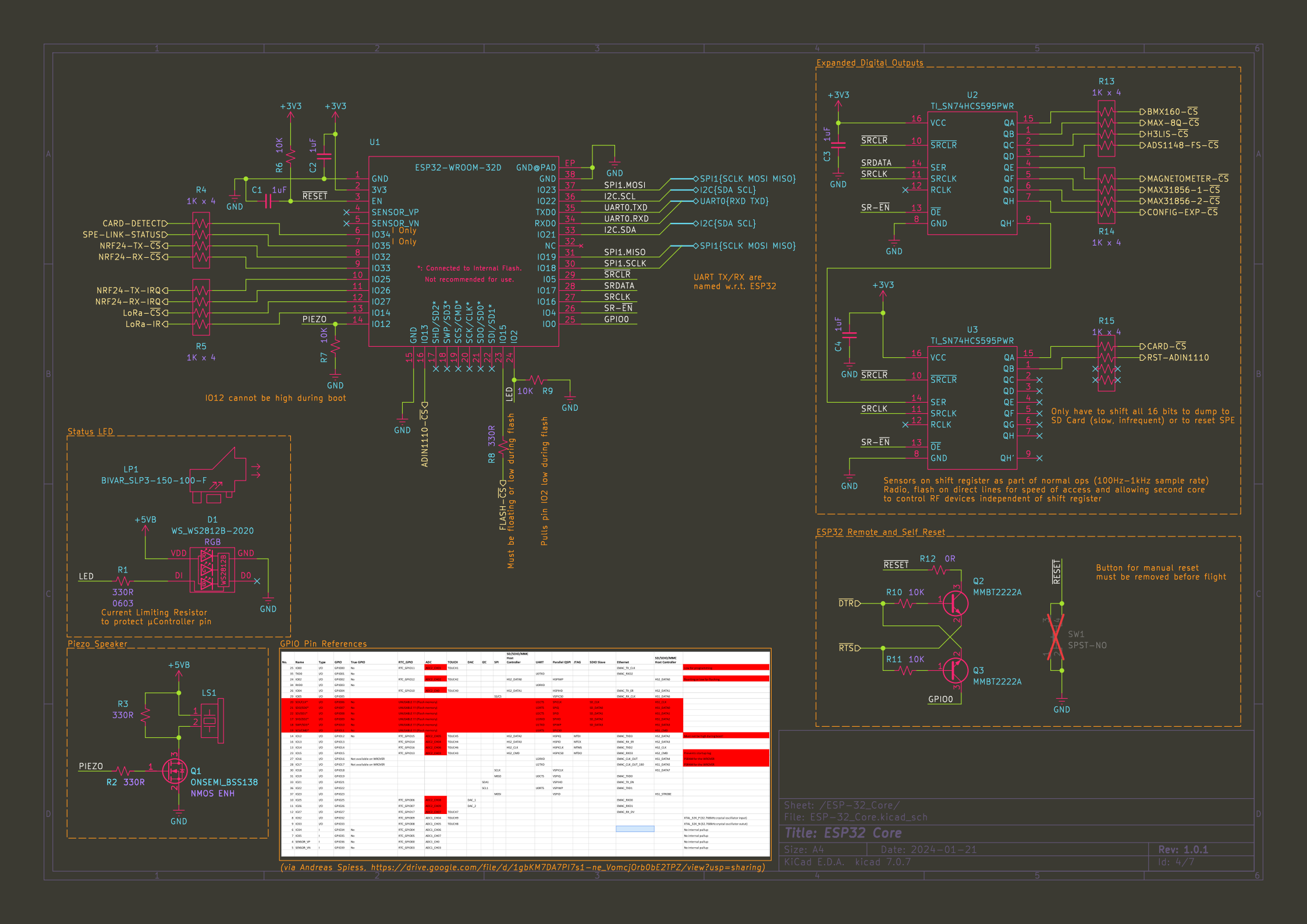
SPI Protocol	SPI_CFG1	SPI_CFG0
OPEN Alliance with Protection	0	0
OPEN Alliance Without Protection	0	1
Generic SPI with 8-bit CRC	1	0
Generic SPI Without 8-bit CRC	1	1

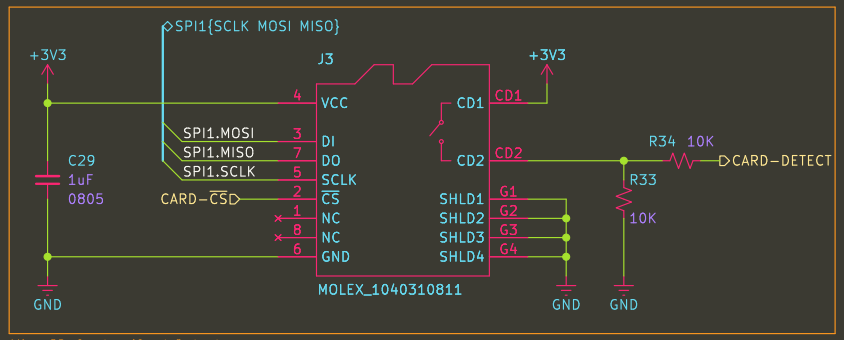
Sheet: /SPE-PoDL_Interface/
File: SPE-PoDL_Interface.kicad_sch

Title: SPE with PoDL Implementation

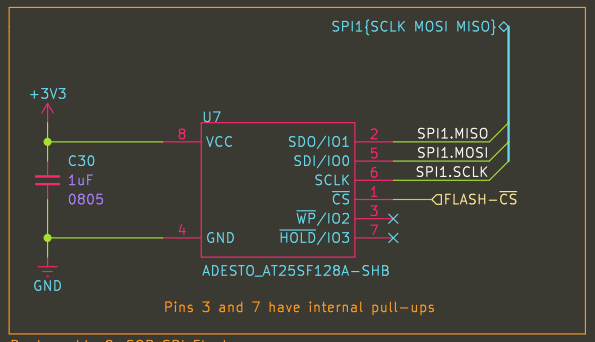
Size: A4 | Date: 2024-01-21 | Rev: 1.0.1
KiCad E.D.A. kicad 7.0.7 | Id: 2/7


Impedance Requirements (USB 2.0 Speeds):
– USB_P/N must be 90R Differential ±15%
– Diff Pair Mismatch <.6in
USB-C 2.0 Connector
J1
GCT_USB4105
USB Type C for 2.0
NC SHLD on Peripheral Device to avoid SHLD return current
VBUS
GND
DP1
DN1
CC1
SBU1
DP2
BN2
CC2
SBU2
SHLD
MH1
MH2
MH3
MH4
USB_P
USB_N
+VUSB
C9 50V 1uF
CC pins not needed (Legacy mode only):
– No SuperSpeed Functionality
– No Power Negotiation
– Legacy Mode (A->C) for programming
TVS Protection
D2
LF_AXGD10603MR
TVS
40V
ST_USBLC6-2SC6
D3
ESD_D+
ESD_D–
USB to UART
U5
TX to RX, RX to TX!
FTDI_FT231XS
VCC
VCCIO
3V3OUT
RESET
USBD_P
USBD_N
TXD
RXD
DTR
RTS
RI
DSR
DCD
CTS
CBUS0
CBUS1
CBUS2
CBUS3
3V3_FTDI
C12 50V 1uF
C13 50V 1uF
R16 22R 0603
R17 22R 0603
UART Named w.r.t. ESP32
UART0.RXD
UART0.TXD
UART0{RXD TXD}
FTDI–LED
LED Active on Either TX or RX
Blue 5mA 2V85
D6
R18 121R
USB-Only Power
Schottky diodes for simplicity/board space:
– 220mV Vf for LSM115J
– 130mV Vdrop for SI2367 PMOS
Diodes save space and part count
D4
MCP_LSM115J
1A
220mV
+5VB
D5
MCP_LSM115J
1A
220mV
+3V3
U4
TOR_XC6220B331
6V MAX VIN
3V3 1A OUT
VIN
VOUT
EN
C5 10uF 0805
C6 10uF 0805
C7 10uF 0805
C8 10uF 0805
C10 10uF 0805
C11 10uF 0805
GND
Test Points
TP1
TP2
TP3
Sheet: /USB_Input/
File: USB_Input.kicad_sch
Title: USB Input
Size: A4
Date: 2024-01-21
Rev: 1.0.1
KiCad E.D.A. kicad 7.0.7
Id: 3/7

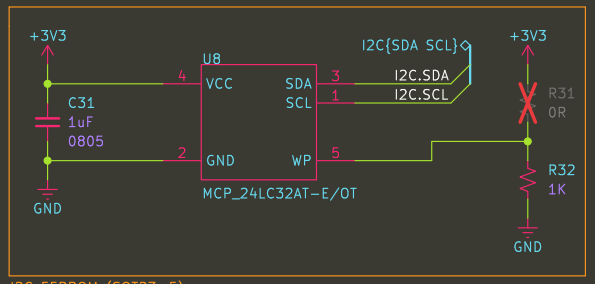

Expanded Digital Outputs
U1
ESP32-WROOM-32D
U2
TI_SN74HCS595PWR
U3
TI_SN74HCS595PWR
R13
1K x 4
R14
1K x 4
R15
1K x 4
R4
1K x 4
R5
1K x 4
BMX160-CS
MAX-8Q-CS
H3LIS-CS
ADS1148-FS-CS
MAGNETOMETER-CS
MAX31856-1-CS
MAX31856-2-CS
CONFIG-EXP-CS
CARD-CS
RST-ADIN1110
CARD-DETECT
SPE-LINK-STATUS
NRF24-TX-CS
NRF24-RX-CS
NRF24-TX-IRQ
NRF24-RX-IRQ
LoRa-CS
LoRa-IR
SPI1{SCLK MOSI MISO}
I2C{SDA SCL}
UART0{RXD TXD}
I2C{SDA SCL}
SPI1{SCLK MOSI MISO}
UART TX/RX are named w.r.t. ESP32
*: Connected to Internal Flash.
Not recommended for use.
IO12 cannot be high during boot
ADIN1110-CS
FLASH-CS
Must be floating or low during flash
Pulls pin IO2 low during flash
Sensors on shift register as part of normal ops (100Hz-1kHz sample rate)
Radio, flash on direct lines for speed of access and allowing second core
to control RF devices independent of shift register
Only have to shift all 16 bits to dump to
SD Card (slow, infrequent) or to reset SPE
Status LED
LP1
BIVAR_SLP3-150-100-F
D1
WS_WS2812B-2020
Current Limiting Resistor
to protect µController pin
Piezo Speaker
LS1
Q1
ONSEMI_BSS138
NMOS ENH
ESP32 Remote and Self Reset
Q2
MMBT2222A
Q3
MMBT2222A
SW1
SPST-NO
Button for manual reset
must be removed before flight
GPIO Pin References
(via Andreas Spiess, https://drive.google.com/file/d/1gbKM7DA7PI7s1-ne_VomcjOrb0bE2TPZ/view?usp=sharing)
Sheet: /ESP-32_Core/
File: ESP-32_Core.kicad_sch
Title: ESP32 Core
Size: A4
Date: 2024-01-21
Rev: 1.0.1
KiCad E.D.A. kicad 7.0.7
Id: 4/7



MicroSD Card w/Card Detect



Replaceable 8-SOP SPI Flash
Base Model: 128MBit

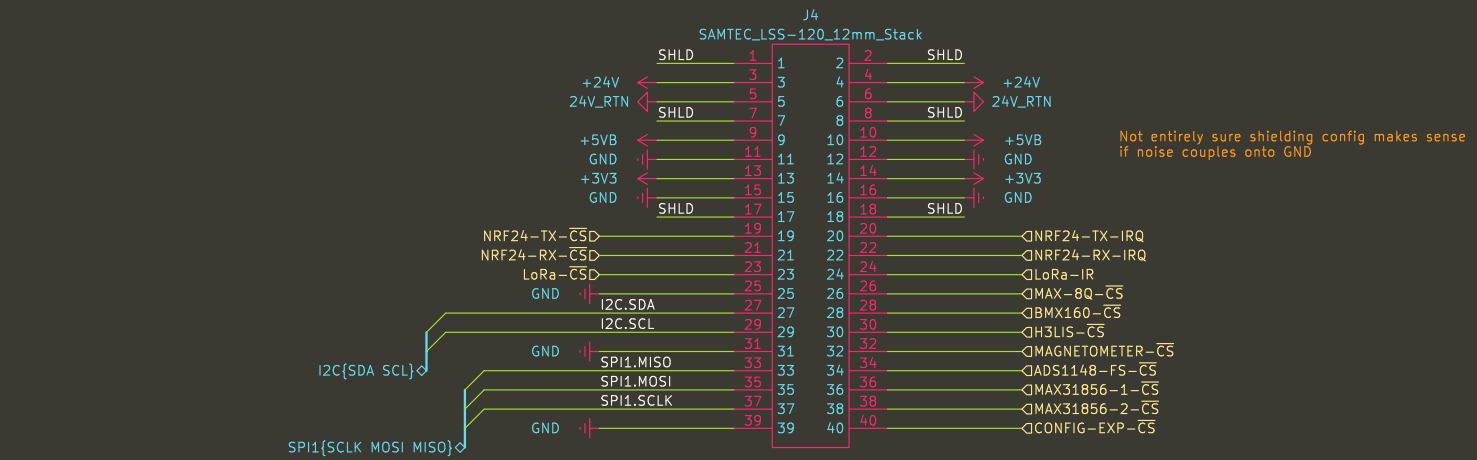


I2C EEPROM (SOT23-5)
Base Model: 32KBit

Sheet: /Data_Storage/
File: Data_Storage.kicad_sch

Title: Data Storage and EEPROM

Size: A4	Date: 2024-01-21	**Rev: 1.0.1**
KiCad E.D.A. kicad 7.0.7		Id: 5/7

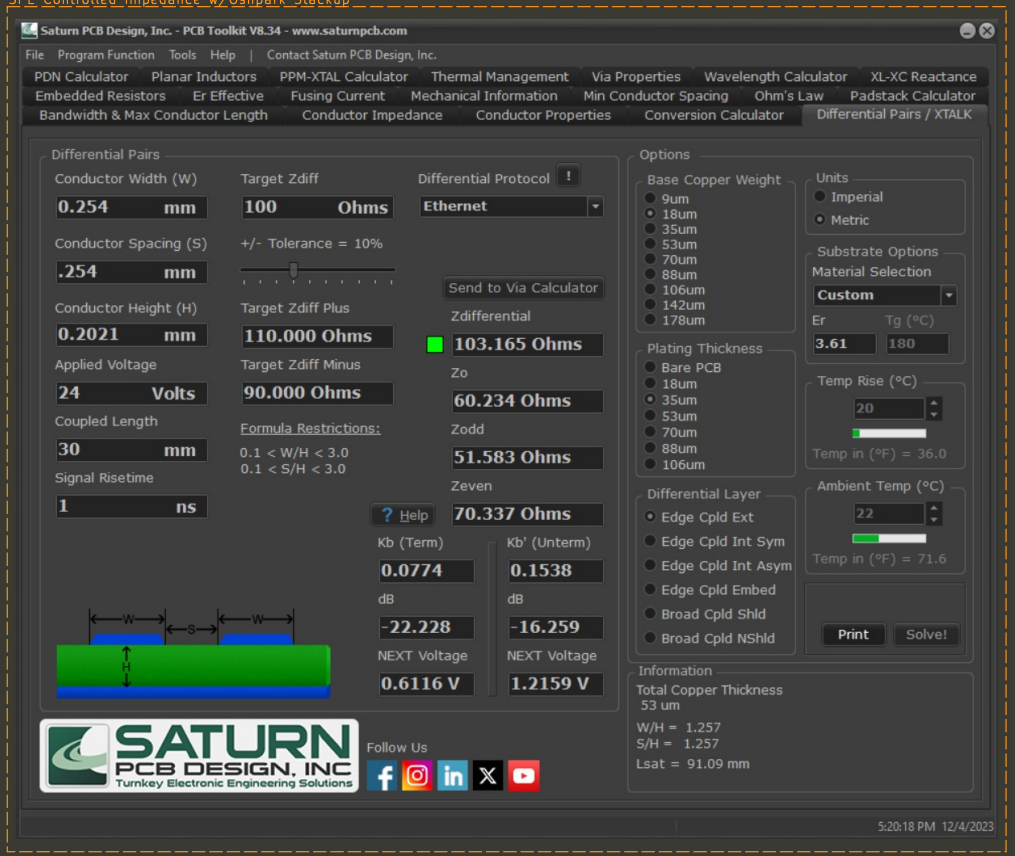


Sheet: /Stacking_Connector/
File: Stacking_Connector.kicad_sch

Title: Stacking Connector

Size: A4	Date: 2024-01-21	**Rev: 1.0.1**
KiCad E.D.A. kicad 7.0.7		Id: 6/7

SPE Controlled Impedance w/Oshpark Stackup



USB Controlled Impedance w/Oshpark Stackup

Impedance Requirements (SPE):
- 100R characteristic impedance, selecting 10% tolerance
- Maintaining through run between lumped hybrid network, through CMC, and to pins
- Not controlling impedance on PoE injection traces

Impedance Requirements (USB 2.0 Speeds):
- USB_P/N must be 90R Differential ±15%
- Diff Pair Mismatch <.6in

Sheet: /SPE-PoDL_Interface/Trace Impedance Calcs/
File: Trace_Impedance_Calcs.kicad_sch

Title: SPE and USB Trace Impedance Calculations

Size: A4	Date: 2024-01-21	Rev: 1.0.1
KiCad E.D.A. kicad 7.0.7		Id: 7/7