Tronlong®

TL6678ZH-EVM

Revision History

Revision No.	Description of Change	Author(s)	Data
A1	Initial Version of TL6678ZH-EVM-A1	DYZ	2020/06/29
A2	1.Optimize JTAG circuit. 2.Modify ZYNQ PS RGMII LED and PHY address circuit. 3.Modify DSP BOOTSET circuit. 4.Optimize ZYNQ system clock circuit.	Charles	2020/12/18
A2.1	1.Modify DSP and ZYNQ communicate circuit. 2.Modify DSP PCIE RC reset control circuit	Charles	2021/02/04
A2.2-000	1.Delete R481-R485,R503-R507 to solve SFP+ communication problems. 2.Modify CameraLink CC2 and CC4 channels sinal problems. 3.Update power tree and power up sequence	Charles	2021/11/18

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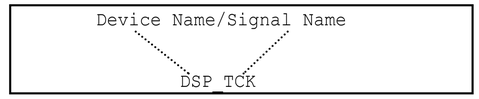
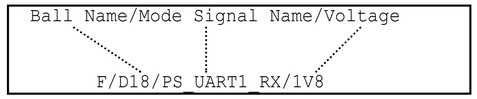
DSP Naming Rules



ZYNQ Naming Rules



CAUTION1:

Signals have this symbol routing with 100 ohm differential impedance

DSP I2C ADDRESS:	
AT24CM01-SSHM-T(SOM)	50H 51H
PS I2C0 ADDRESS:	
TMP102AIDRLT(SOM)	49H
12V Current/Power Monitor	41H
5V Current/Power Monitor	40H
DS1340	68H
SIL9022A	3BH 62H
HDMI Screen	50H
ADV7611	4CH
FMC	X
CDCM6208V1RGZR	54H
PL I2C ADDRESS:	
SFP MODULE	50H 51H
MT9V034	48H

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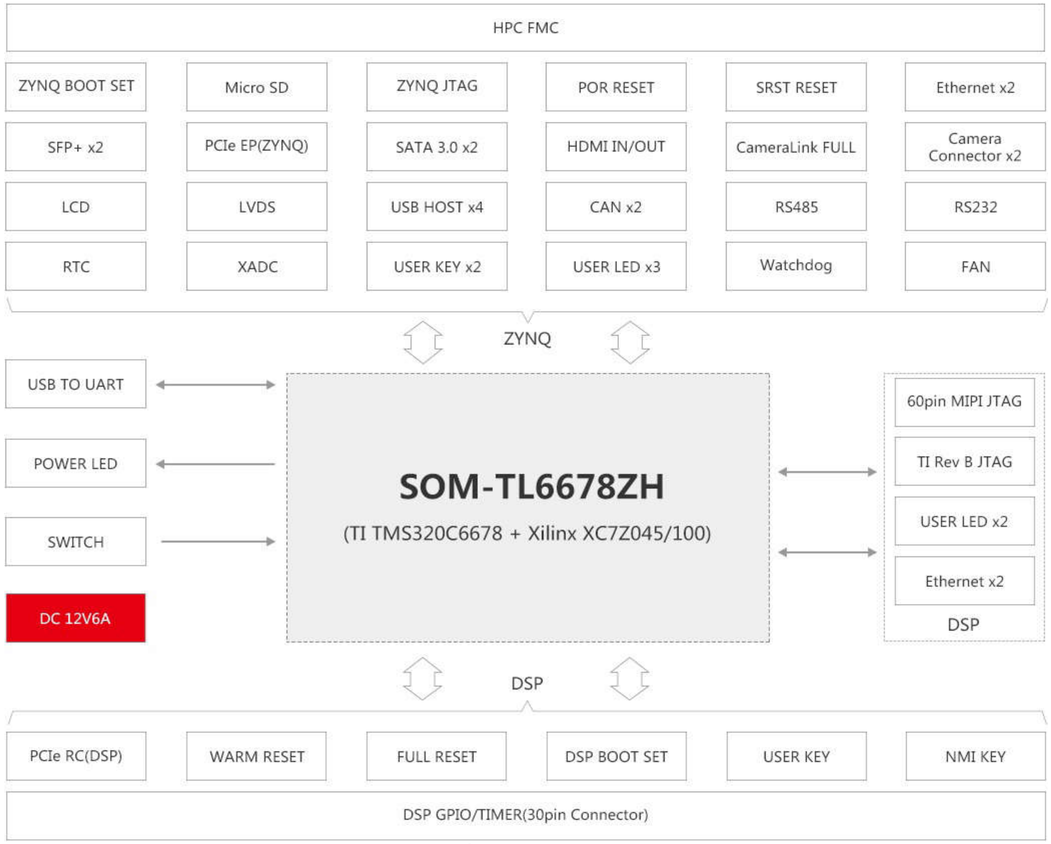
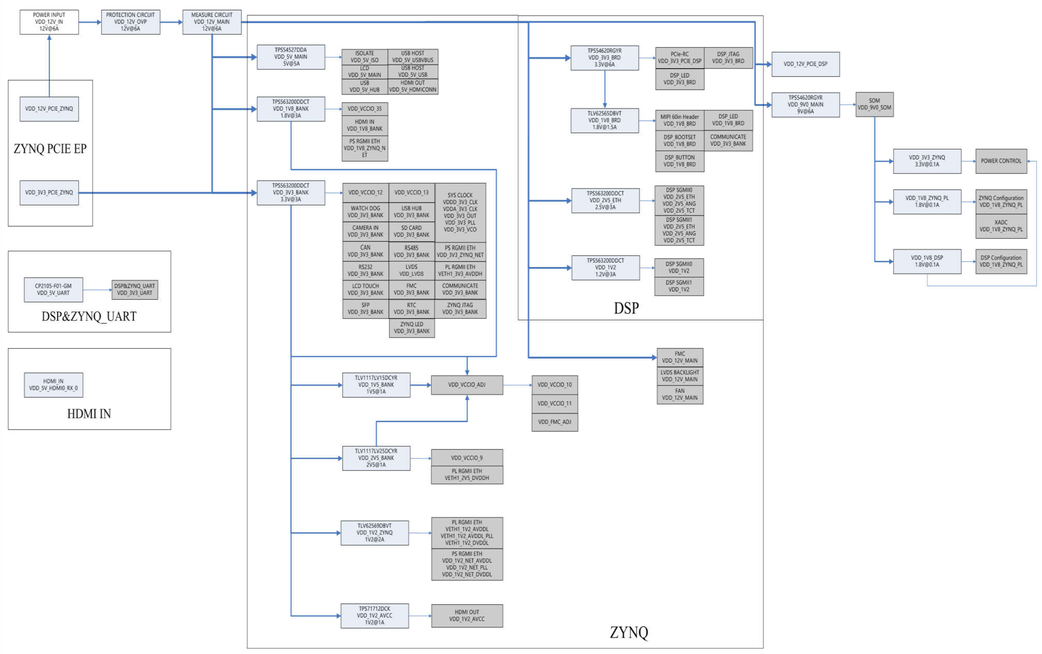
BLOCK DIAGRAM

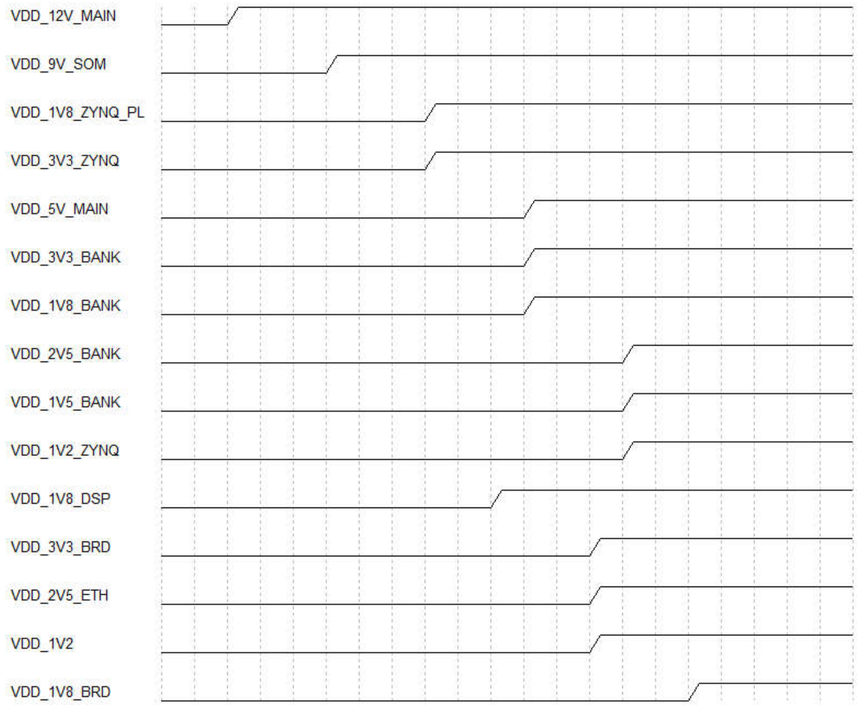


POWER TREE



BANK	VOLTAGE
PL-BANK0	3.3V
PL-BANK9	2.5V
PL-BANK10	USER_VOL
PL-BANK11	USER_VOL
PL-BANK12	3.3V
PL-BANK13	3.3V
PL-BANK33	1.5V
PL-BANK34	1.5V
PL-BANK35	1.8V
PS-BANK500	3.3V
PS-BANK501	1.8V
PS-BANK502	1.5V

POWER UP SEQUENCE



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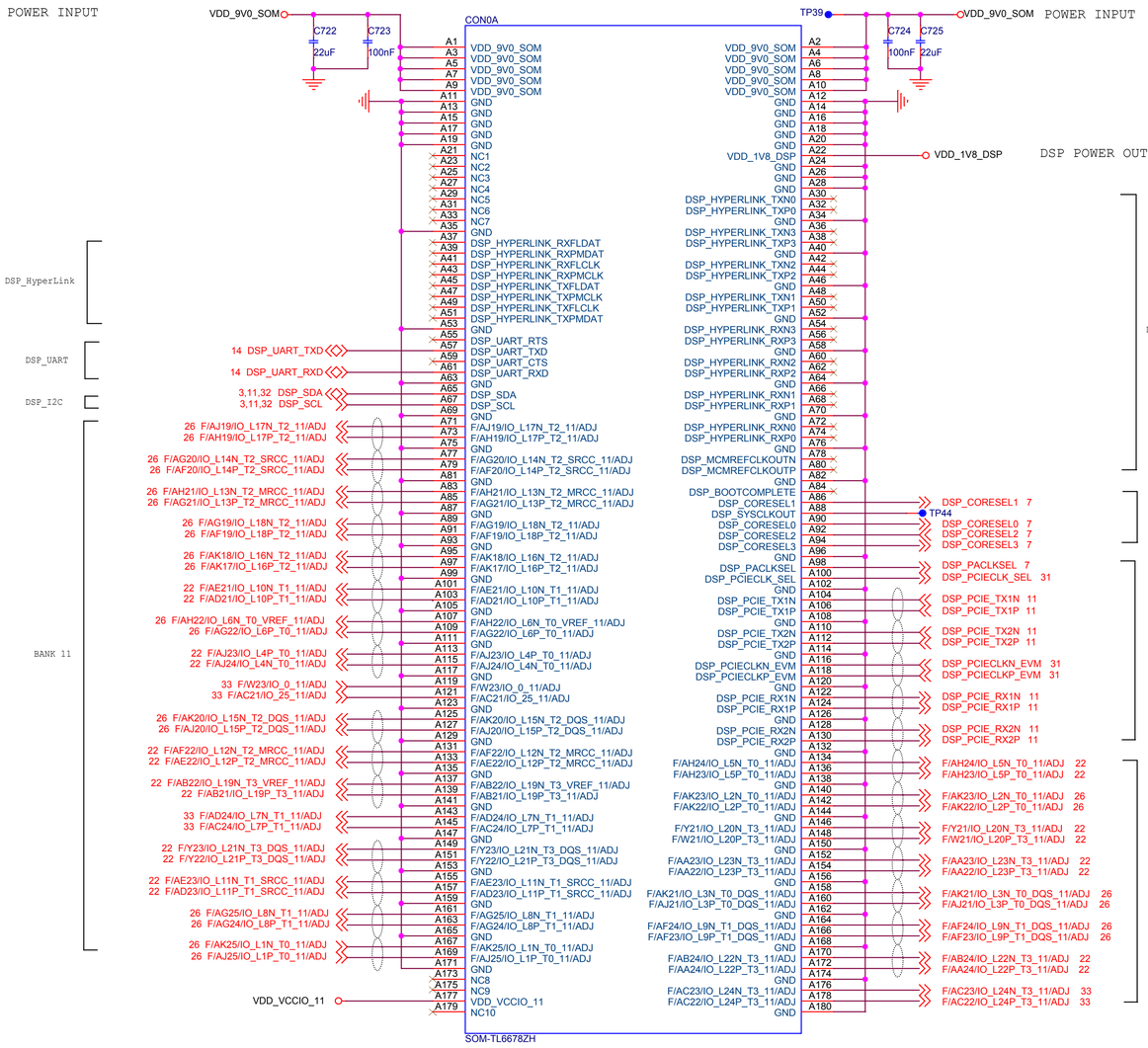
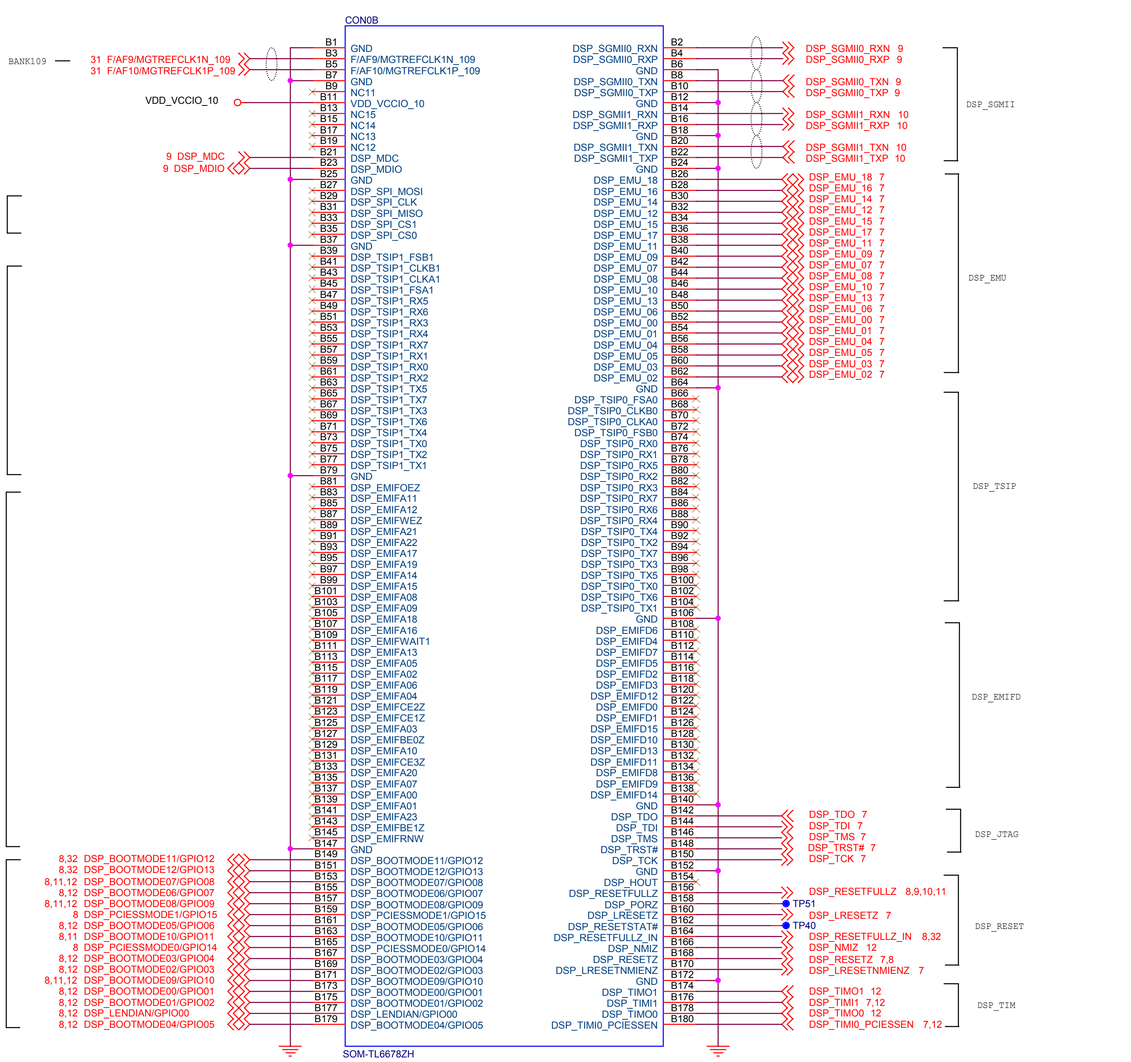
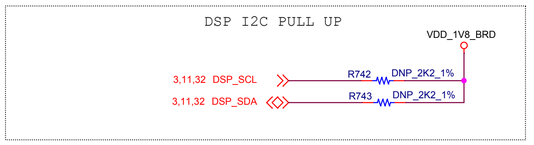
DSP/ZYNQ PS MALE CONNECTOR

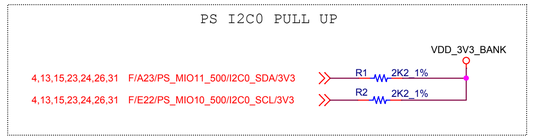


Signal ends P/N routing with 100 ohm differential impedance



Signal ends P/N routing with 100 ohm differential impedance





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ZYNQ_FEMALE CONNECTOR

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Title	ZYNQ_MALE CONNECTOR
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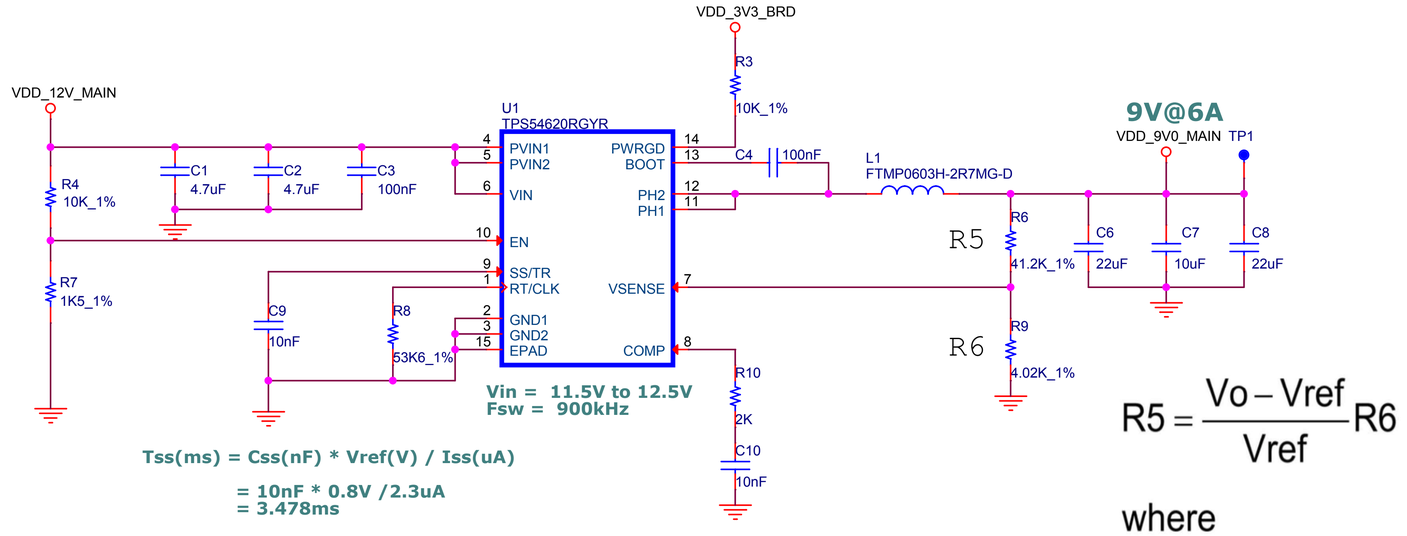
12V TO VDD_9V0_MAIN

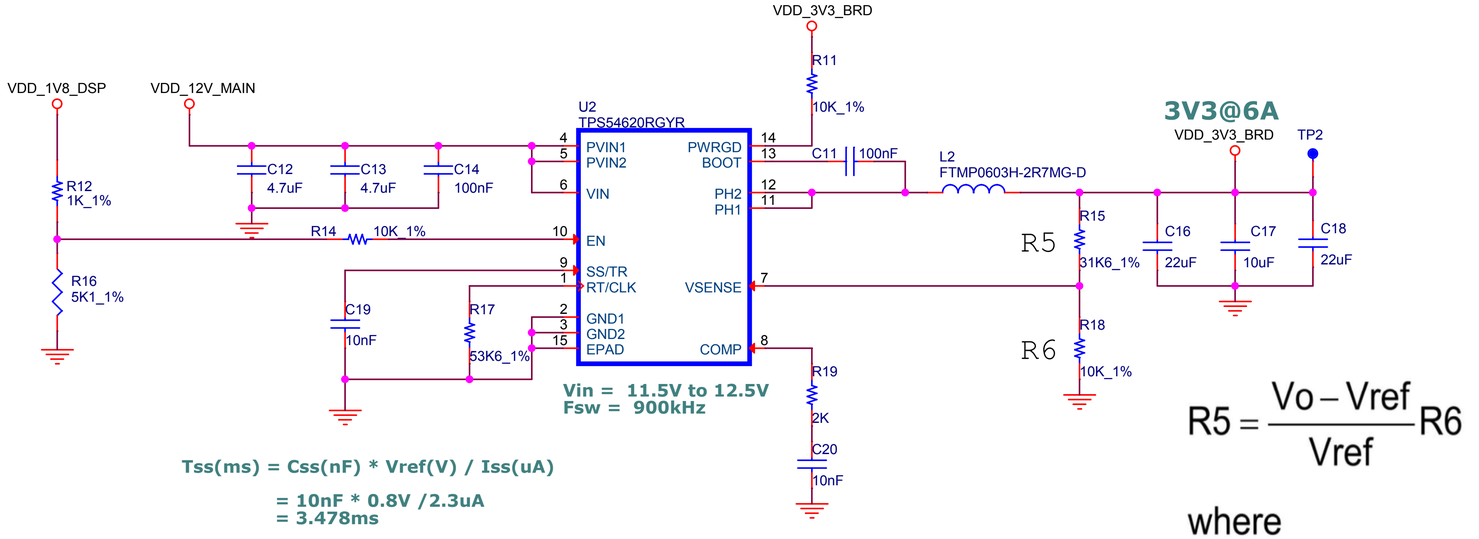


$$R5 = \frac{Vo - Vref}{Vref} R6$$

where

- Vref = 0.8V

12V to VDD_3V3_BRD



$$R5 = \frac{Vo - Vref}{Vref} R6$$

where

- Vref = 0.8V

ALL POWER Layout Note:
All the power circuit need to be placed according to SCH explanation.

All the power trace wide set to more than 10mil except for control signal.

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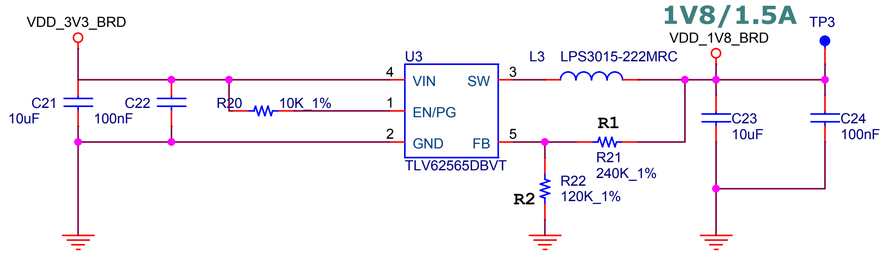
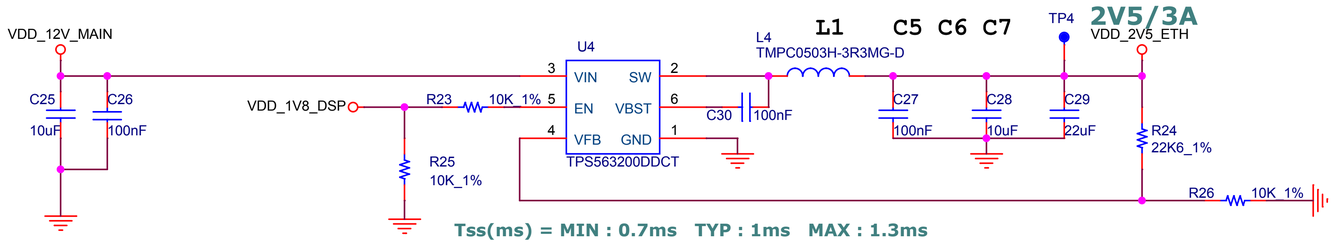
3.3V TO VDD_1V8_BRD



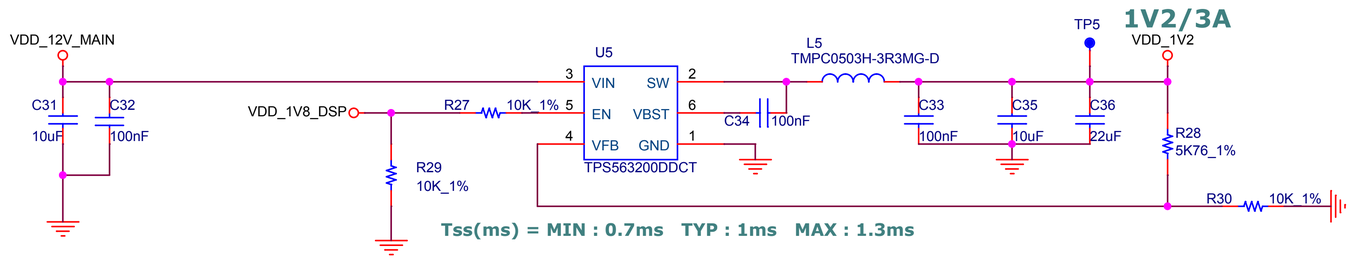
$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.6V \times \left(1 + \frac{R1}{R2}\right)$$

Vout =0.6x(1+R1/R2)
=0.6*(1+240/120)
=1.8

12V TO VDD_2V5_ETH



12V TO VDD_1V2



ALL POWER Layout Note:
All the power circult need to be placed according to SCH explanation.

All the power trace wide set to more than 10mil except for control signal.

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Title	DSP_POWER01
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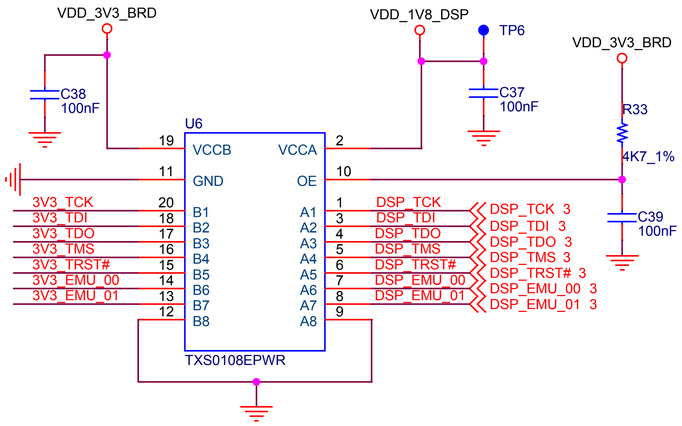
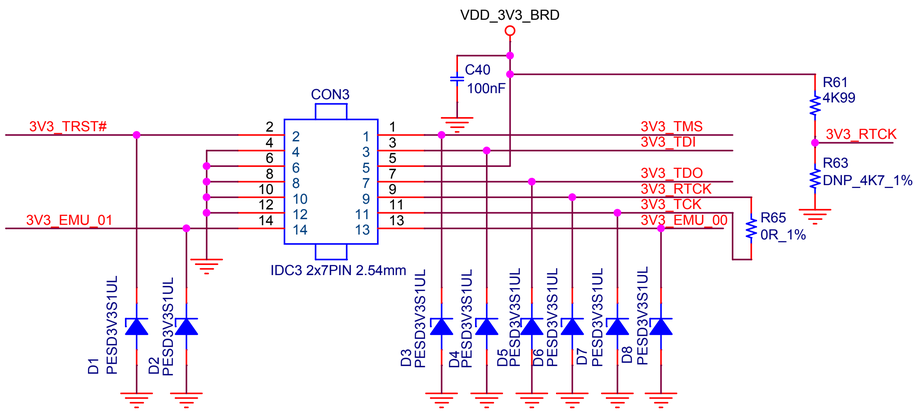
DSP_JTAG



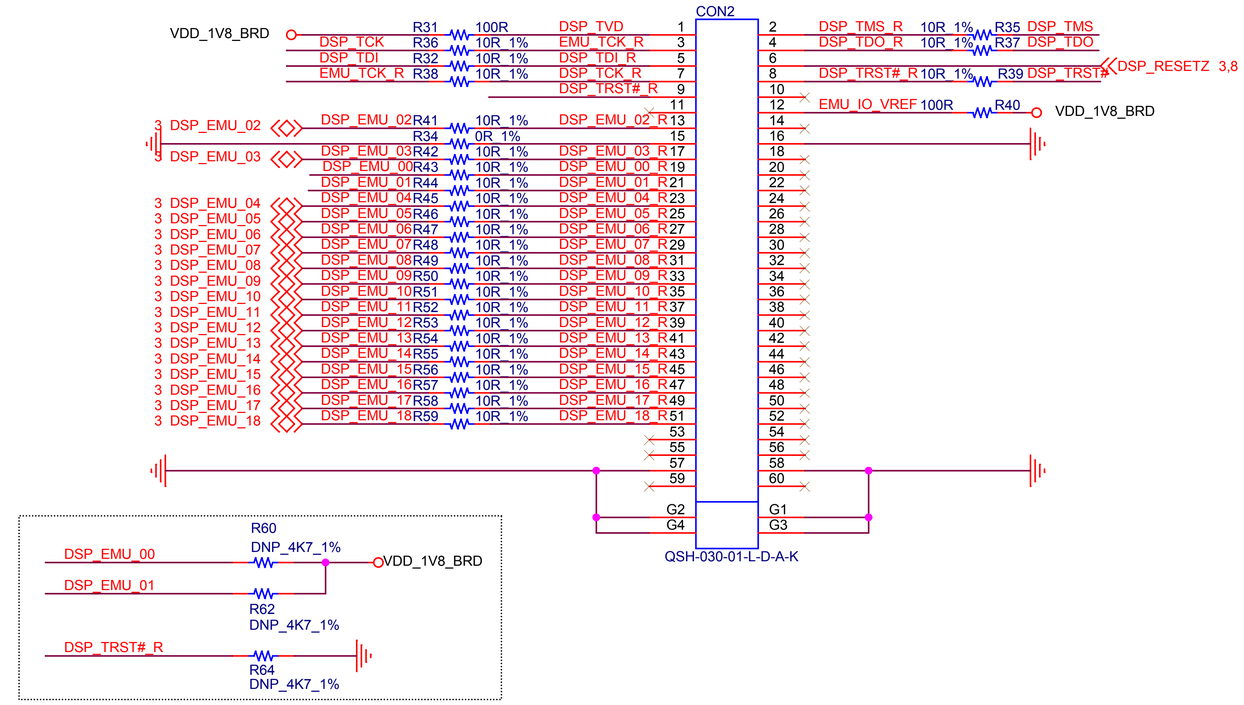
DSP_JTAG Voltage Converter

Clock frequency:29.4MHz



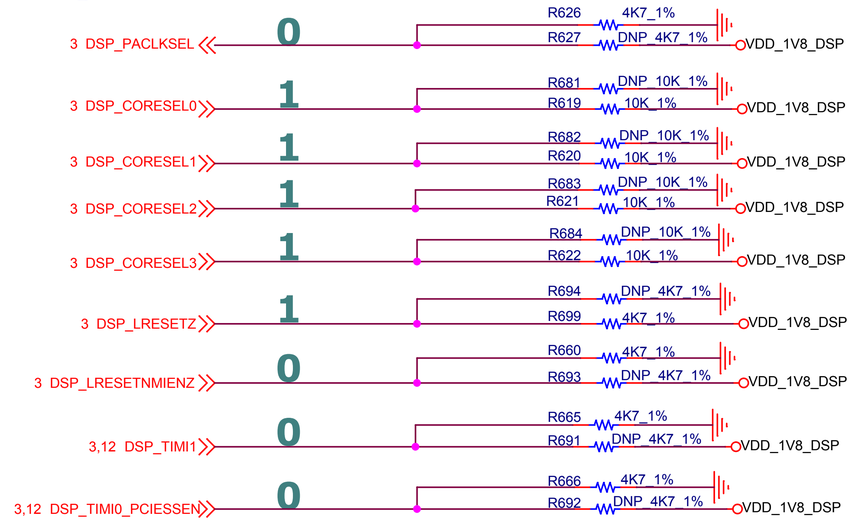
TI Rev B JTAG

MIPI 60Pin Header



Clock frequency:29.4MHz

DSP Configuration



DSP_PACLKSEL

L	USE INTERNAL PASSCLK
H	USE EXTERNAL PASSCLK

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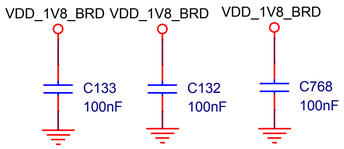
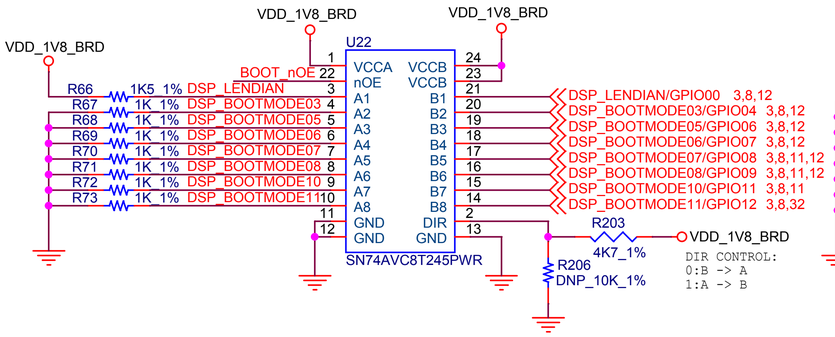
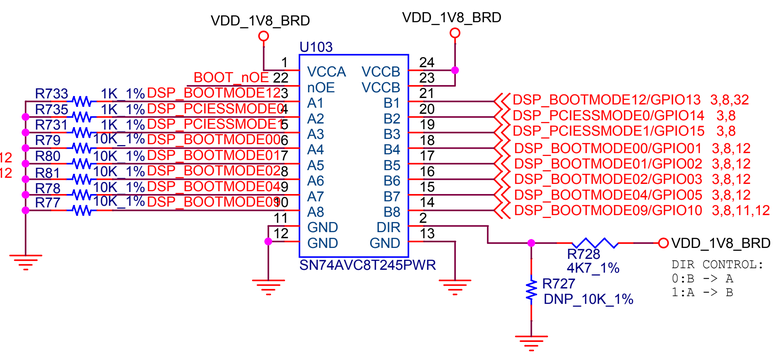
DSP_BOOTSET

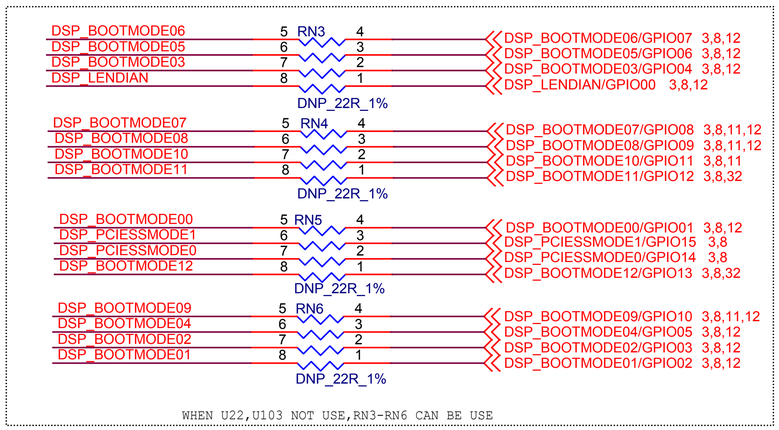


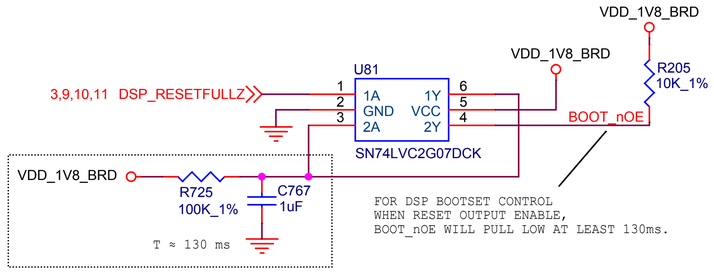
Boot Mode Pin Decoding

Boot Mode Pins												
12	11	10	9	8	7	6	5	4	3	2	1	0
PLL Mult I2C /SPI Ext Dev Cfg					Device Configuration					Boot Device		

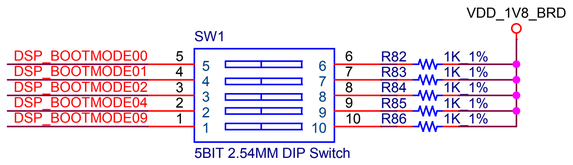








DSP RESET CONTROL BOOTMODE CIRCUIT



DSP BOOT SET

BOOT MODE	BOOTMODE SWH	9 1	4 2	2 3	1 4	0 5
No Boot		OFF	OFF	OFF	OFF	OFF
I2C BOOT	IBL NOR	OFF	OFF	ON	OFF	ON
	IBL NAND	OFF	ON	ON	OFF	ON
SPI BOOT	IBL NOR	ON	OFF	ON	ON	OFF
	IBL NAND	ON	ON	ON	ON	OFF
		P.S:ON = 1 , OFF = 0				

Boot Mode Pins: Boot Device Values

BOOTMODE[2:0]	Boot Device	BOOTMODE[2:0]	Boot Device
000	EMIF16 / No Boot	100	PCIe
001	Serial Rapid I/O	101	I2C
010	Ethernet (PA driven from core clk)	110	SPI
011	Ethernet (PA driven from PA clk)	111	HyperLink

No Boot Configuration

BOOTMODE	VALUE	FUNCTION/CONFIGURATION
LENDIAN	0b0	ENDIANESS: Little Endian
BOOTMODE[2:0]	0b00	Boot Device: No Boot
BOOTMODE[3]	0b0	Reserved
BOOTMODE[5:4]	0b0	Sub mode selection:No boot
BOOTMODE[6]	0b0	Reserved
BOOTMODE[7]	0b0	Extended Wait mode for EMIF16:Wait enable disabled (EMIF16 sub mode)
BOOTMODE[9:8]	0b00	Reserved

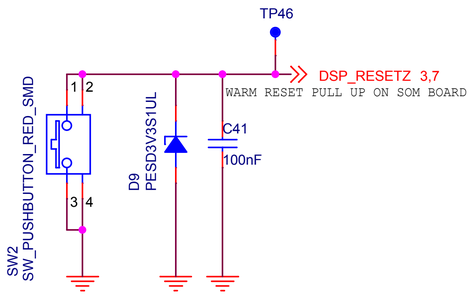
I2C Boot Configuration

BOOTMODE	VALUE	FUNCTION/CONFIGURATION
LENDIAN	0b0	ENDIANESS: Little Endian
BOOTMODE[2:0]	0b101	Boot Device: I2C
BOOTMODE[7:3]	0b00000/ 0b00010	Parameter Intex: IBL NOR/IBL NAND
BOOTMODE[9:8]	0b00	Mode: Master Mode
BOOTMODE[10]	0b00	Address/0x50
BOOTMODE[11]	0b0	Speed: CORECLK/5000
BOOTMODE[12]	0b0	Reserved

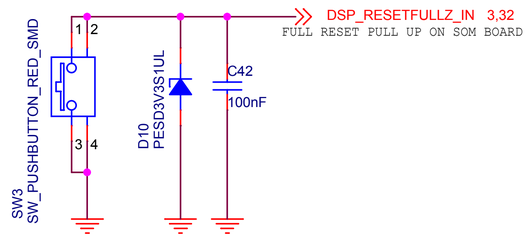
SPI Boot Configuration

BOOTMODE	VALUE	FUNCTION/CONFIGURATION
LENDIAN	0b0	ENDIANESS: Little Endian
BOOTMODE[2:0]	0b110	Boot Device: SPI
BOOTMODE[6:3]	0b0000/ 0b0010	Parameter Intex: IBL NOR/IBL NAND
BOOTMODE[8:7]	0b00	Chip Select: CS0 and CS1 are both active
BOOTMODE[9]	0b01	Addr Width: 24-bit address
BOOTMODE[10]	0b0	Mode: 4 Pin
BOOTMODE[12:11]	0b00	Clk Pol / Phase: Data is output on the rising edge of SPICLK. Input data is latched on the falling edge.

DSP_RESET



WARM RESET



FULL RESET

Tronlong®	Guangzhou Tronlong Technology Co., Ltd.
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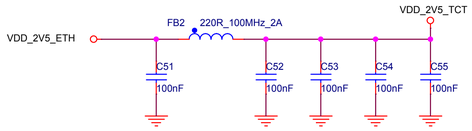
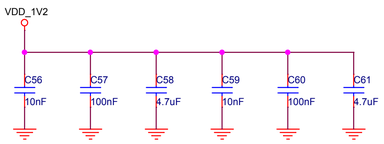
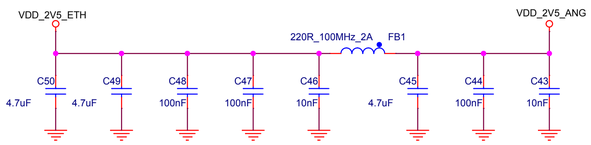
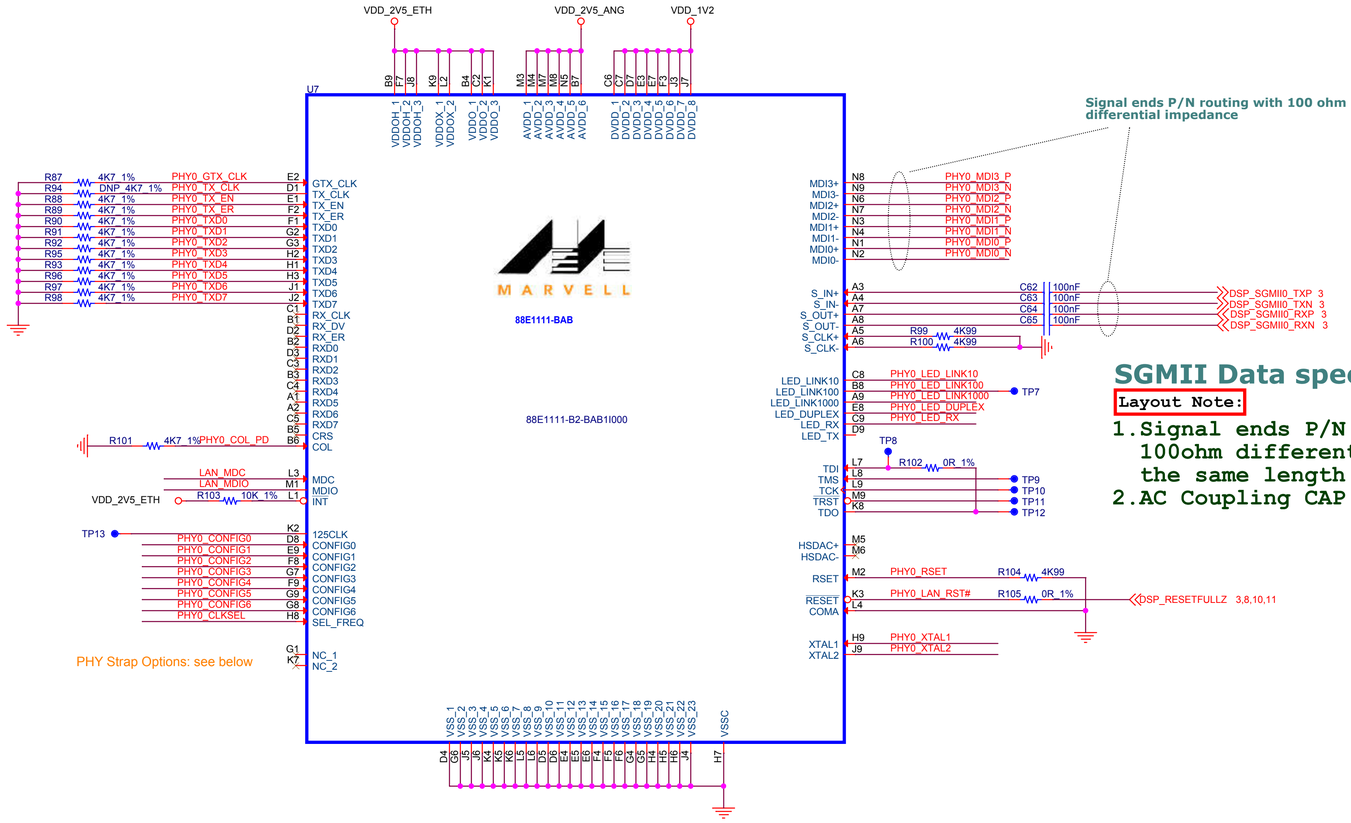
DSP_SGMII0_ETH





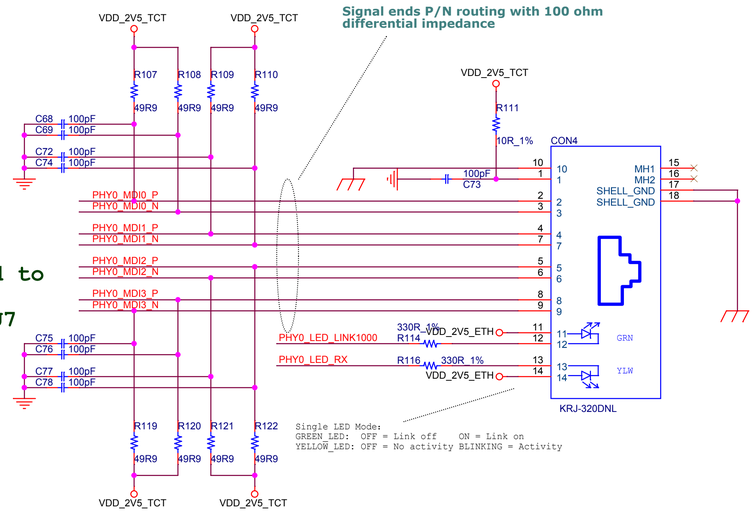


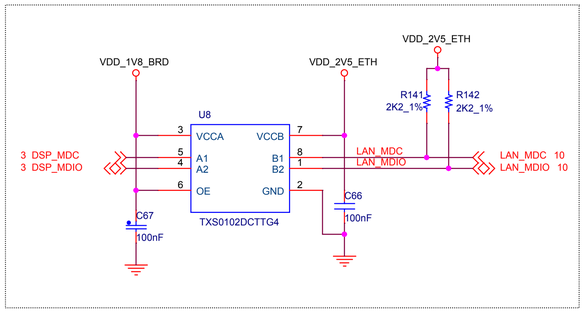


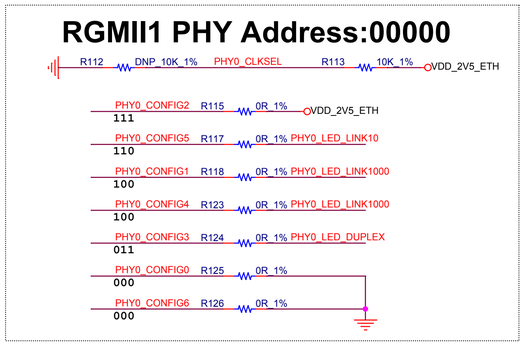
SGMII Data speed:1.25Gbaud

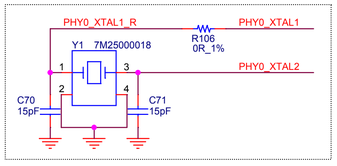
Layout Note:

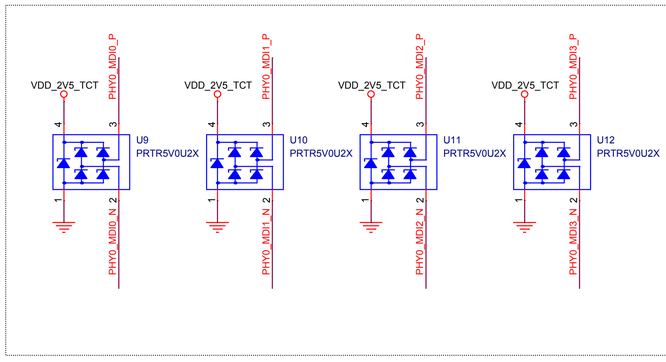
1. Signal ends P/N routing with 100ohm differentialimpedance,need to the same length with ±10mil;
2. AC Coupling CAP should close to U7











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Title	DSP_ETHERNET_SGMII0	
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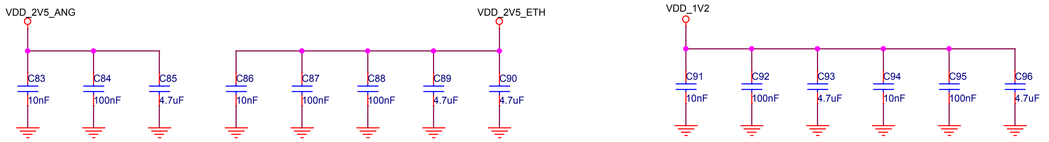
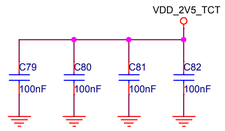
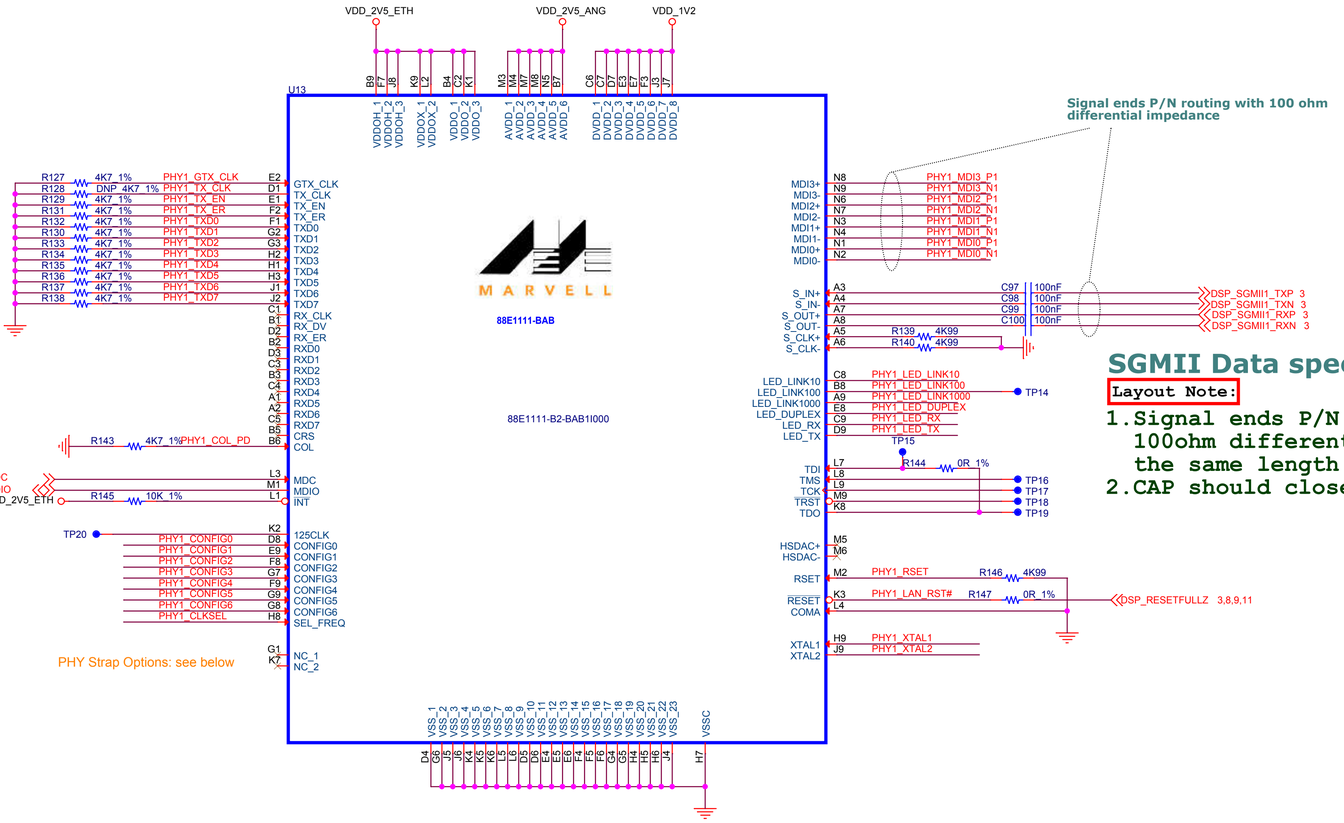
DSP_SGMII1_ETH



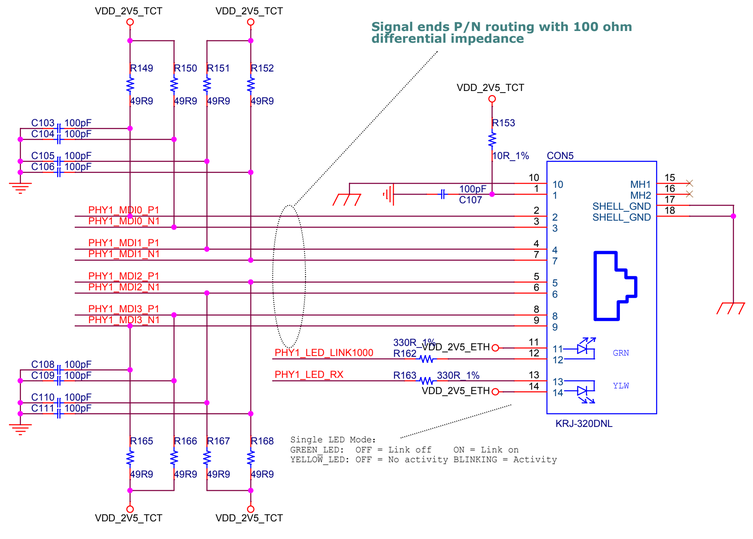




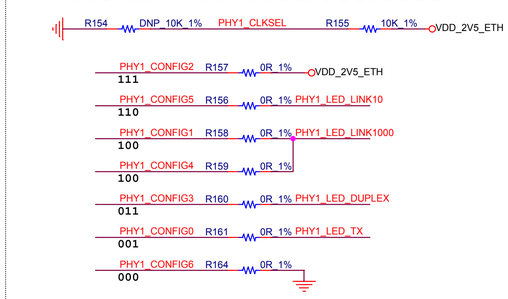
SGMII Data speed:1.25Gbaud

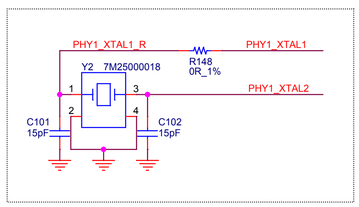
Layout Note:

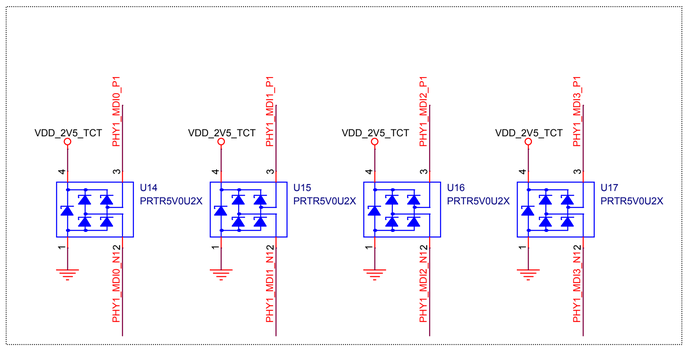
1. Signal ends P/N routing with 100ohm differentialimpedance,need to the same length with ±10mil;
2. CAP should close to U13



RGMII1 PHY Address:00001







Tronlong®	Guangzhou Tronlong Technology Co., Ltd.	
Title	DSP_ETHERNET_SGMII1	
Size A2	Document Number TL6678ZH-EVM	
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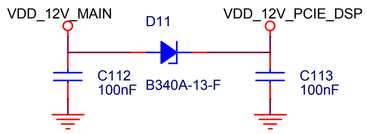
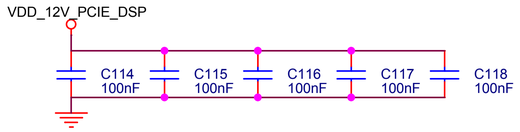
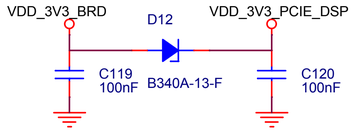
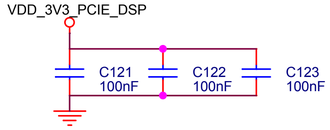
DSP_PCIE_RC





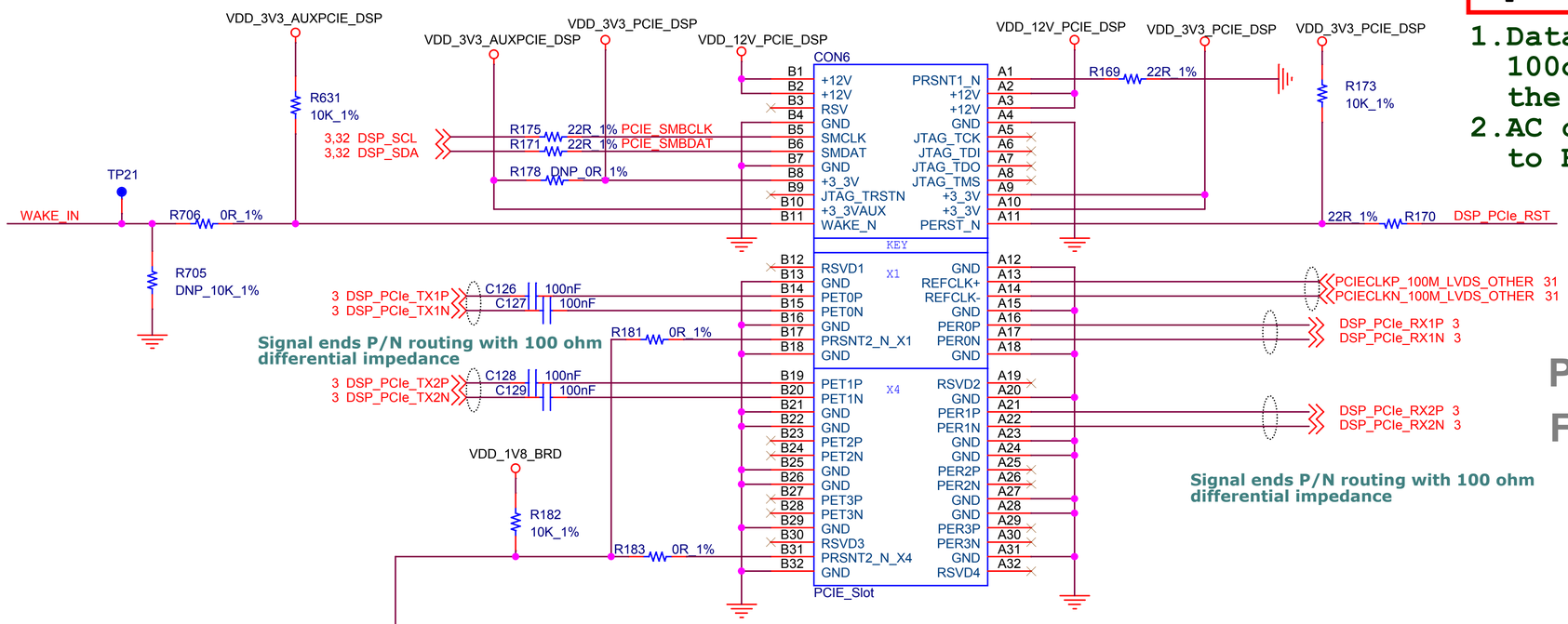




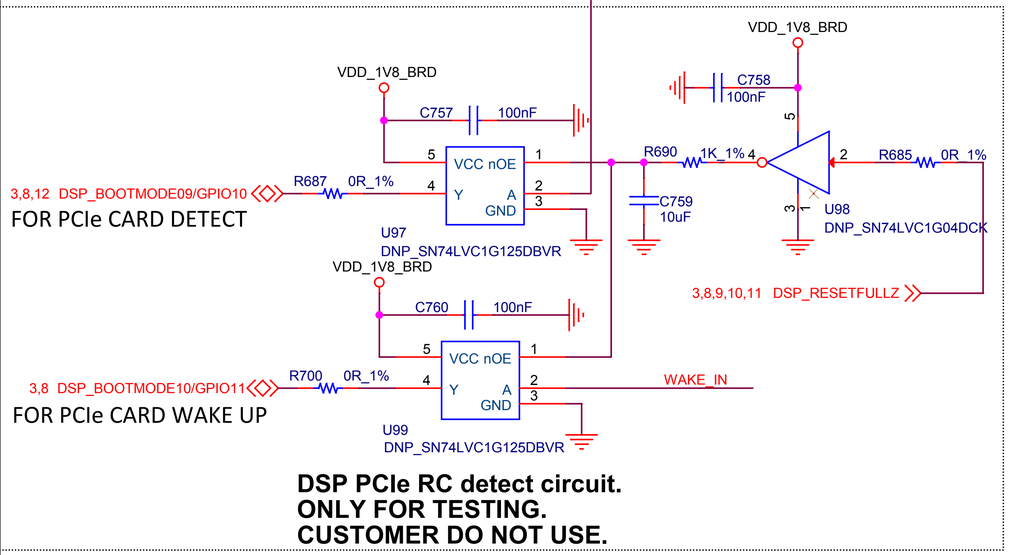
Data speed:5Gbaud/Lane

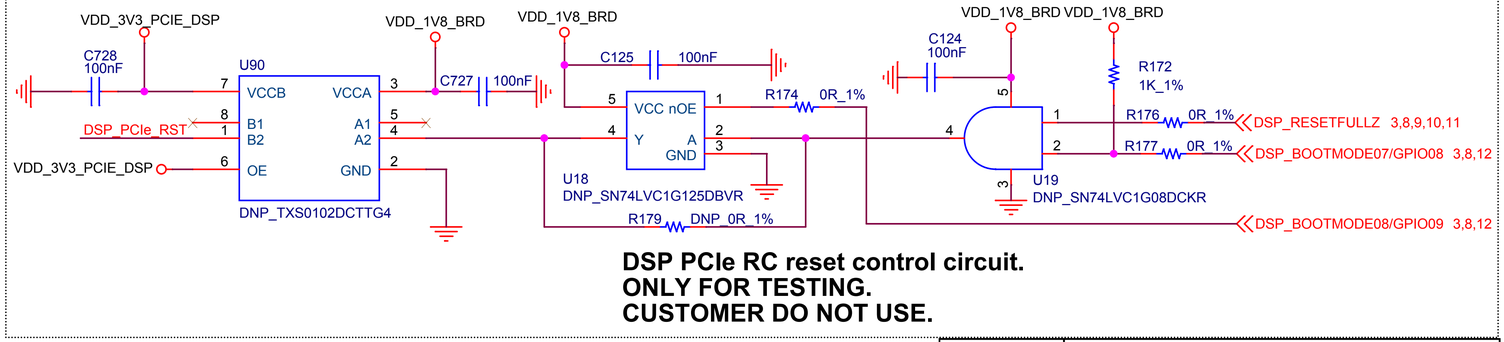
Layout Note:

1. Data signal ends P/N routing with 100ohm differentialimpedance,need to the same length with ±1mil;
2. AC coupling CAP should be placed close to Edge Connector



PCI Express x4 Edge Connector FOR RC MODE





Tronlong®	Guangzhou Tronlong Technology Co., Ltd.		
Title	DSP_PCIE_RC		
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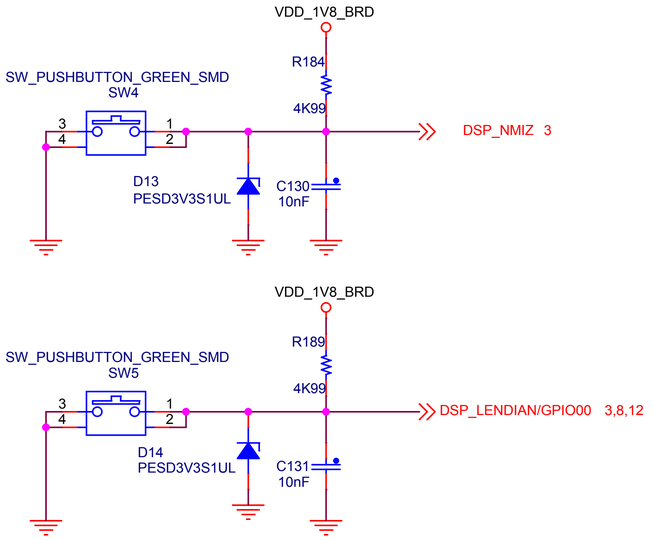
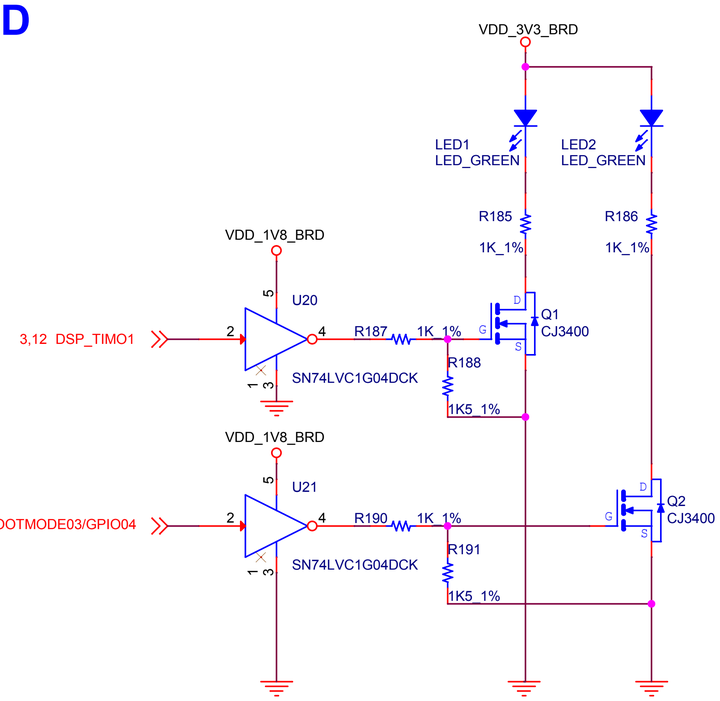
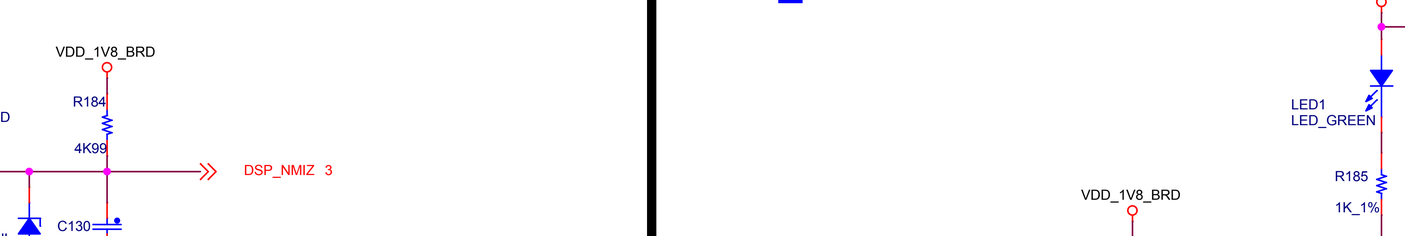
DSP_BUTTON

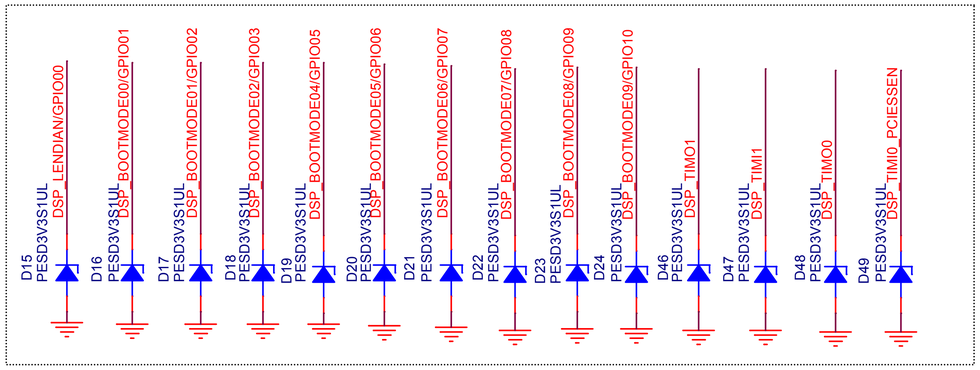


DSP_LED



DSP_GPIO





Tronlong®	Guangzhou Tronlong Technology Co., Ltd.	
Title	DSP_LED/KEY/GPIO	
Size A3	Document Number TL6678ZH-EVM	
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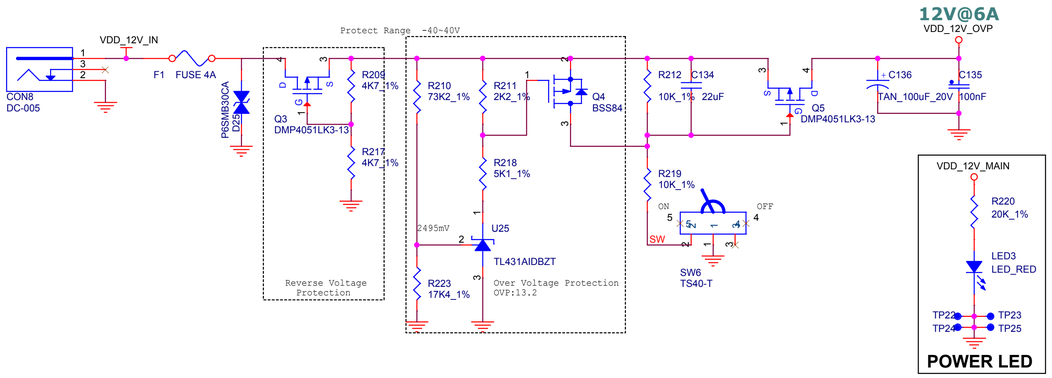
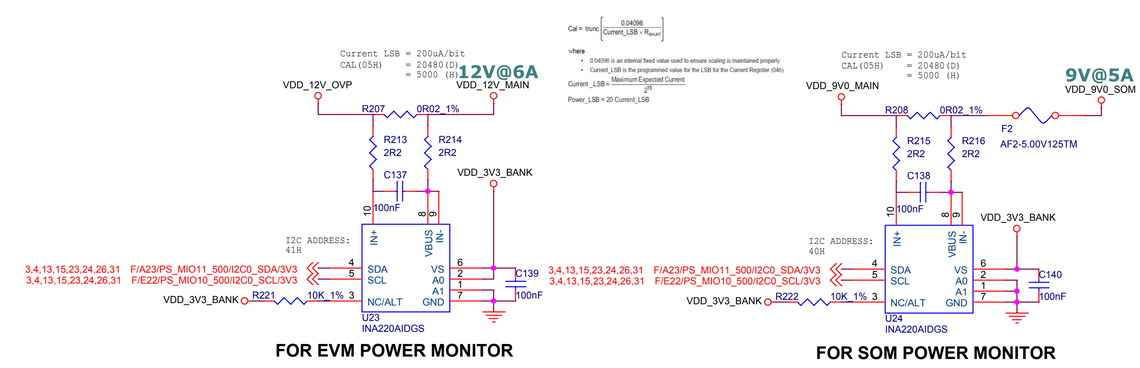
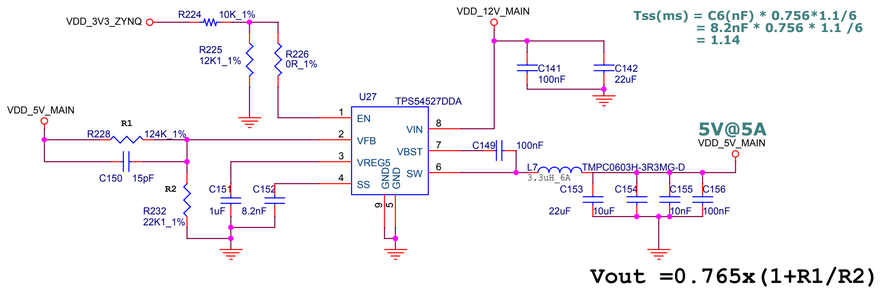
POWER INPUT



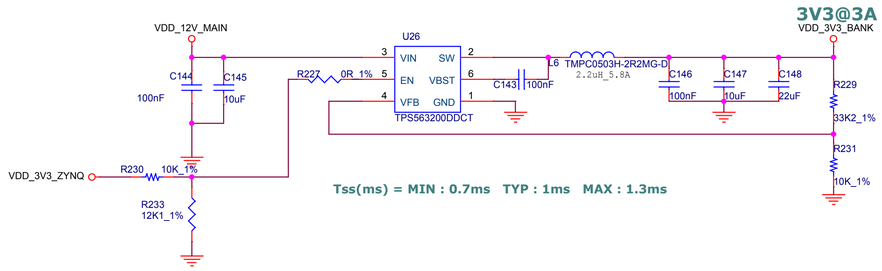
Current/Power Monitor



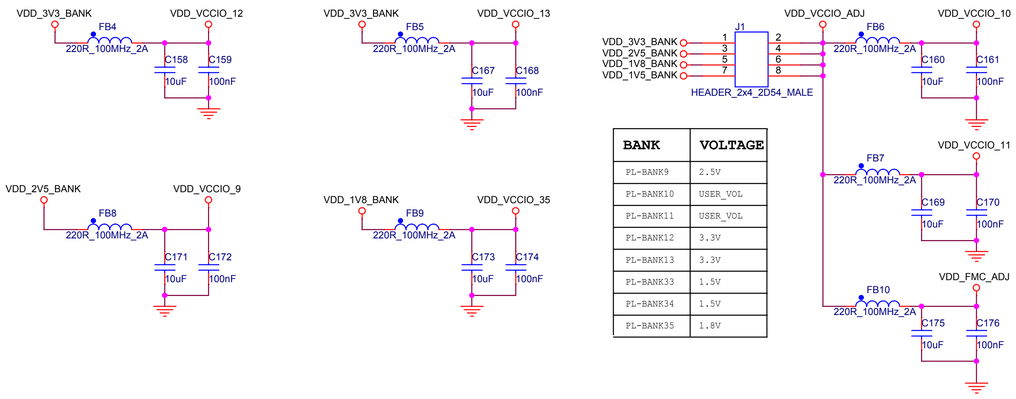
12V TO VDD_5V_MAIN



12V TO VDD_3V3_BANK



BANK POWER



BANK	VOLTAGE
PL-BANK9	2.5V
PL-BANK10	USER_VOL
PL-BANK11	USER_VOL
PL-BANK12	3.3V
PL-BANK13	3.3V
PL-BANK33	1.5V
PL-BANK34	1.5V
PL-BANK35	1.8V

12V TO VDD_1V8_BANK

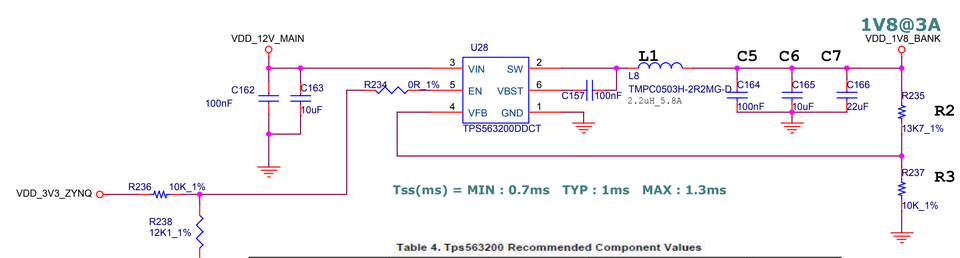
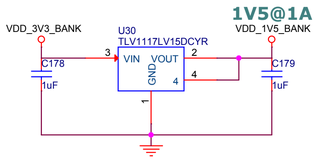


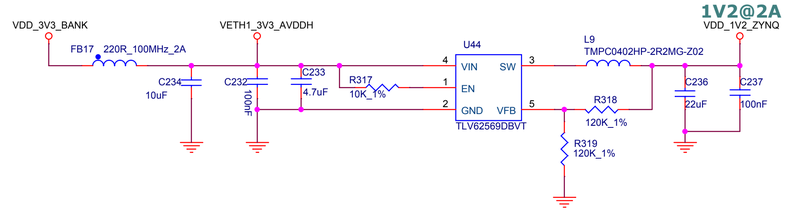
Table 4. Tps563200 Recommended Component Values

Output Voltage (V)	R2 (kΩ)	R3 (kΩ)	L1 (µH) MIN	L1 (µH) TYP	L1 (µH) MAX	C5 + C6 + C7 (µF)
1	3.09	10.0	1.0	1.5	4.7	20 - 68
1.05	3.74	10.0	1.0	1.5	4.7	20 - 68
1.2	5.76	10.0	1.0	1.5	4.7	20 - 68
1.5	9.53	10.0	1.0	1.5	4.7	20 - 68
1.8	13.7	10.0	1.5	2.2	4.7	20 - 68
2.5	22.6	10.0	1.5	2.2	4.7	20 - 68
3.3	33.2	10.0	1.5	2.2	4.7	20 - 68
5	54.9	10.0	2.2	3.3	4.7	20 - 68
6.5	75	10.0	2.2	3.3	4.7	20 - 68

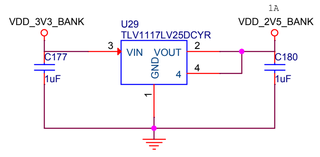
3.3V TO VDD_1V5_BANK



3.3V TO VDD_1V2_ZYNQ



3.3V TO 2.5V



ALL ZYNQ POWER Layout Note:
All the power circuit need to be placed according to Tronlong's requirement.

All the power trace wide set to more than 10mil except for control signal.

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Title	ZYNQ_POWER00
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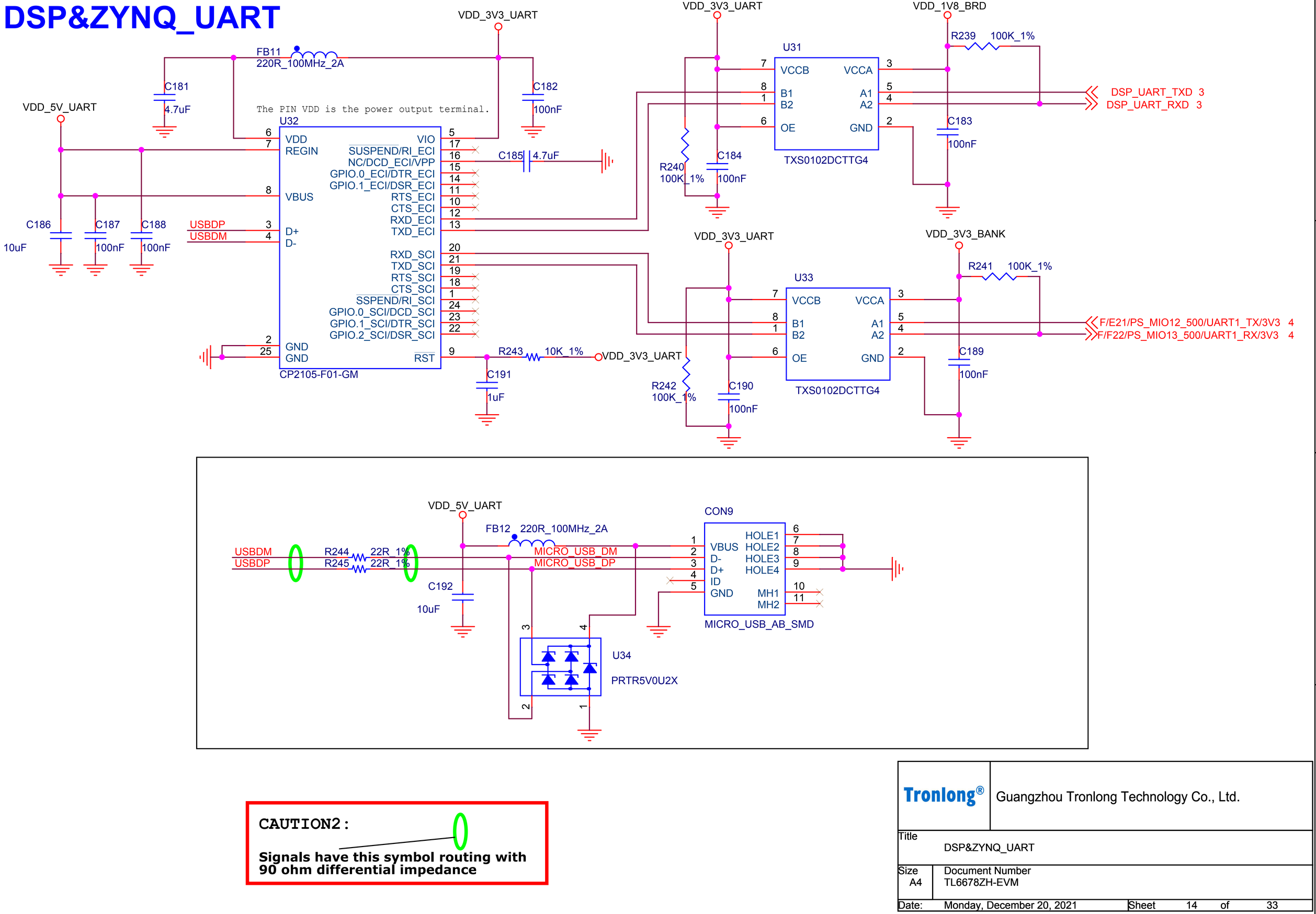
DSP&ZYNQ_UART



CAUTION2:

Signals have this symbol routing with 90 ohm differential impedance

Tronlong®	Guangzhou Tronlong Technology Co., Ltd.
Title	DSP&ZYNQ_UART
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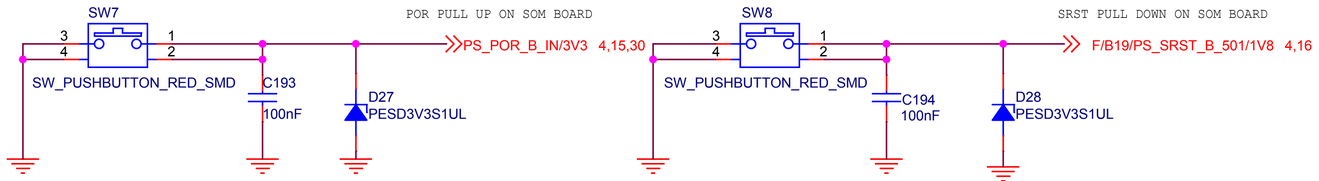
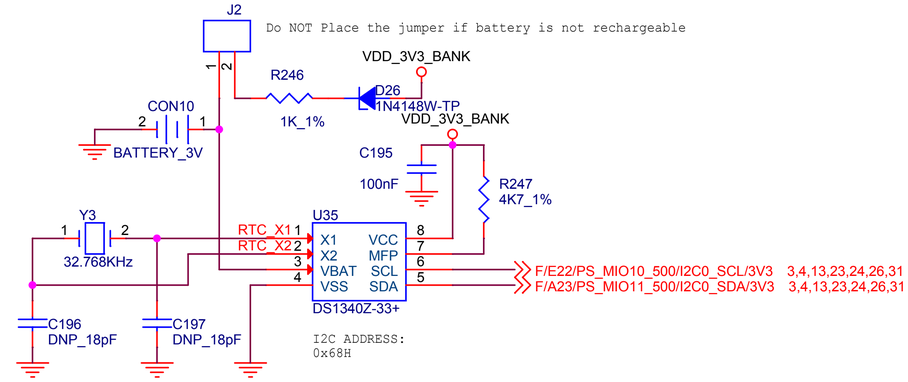
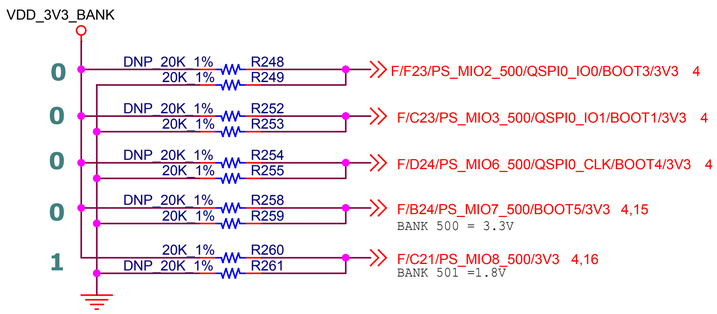
ZYNQ POR/SRST RESET

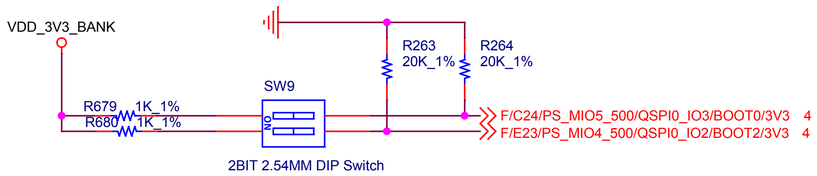


RTC



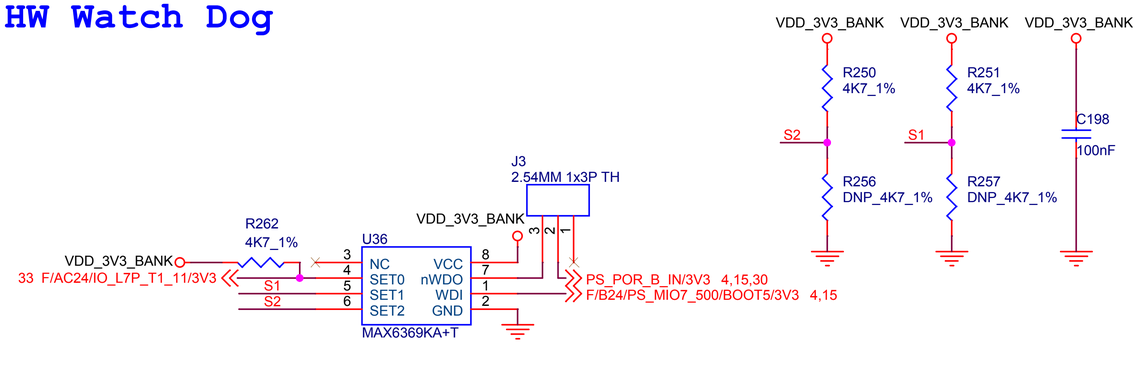
BOOTSET





ZYNQ BOOT SET			
Boot Mode	MIO	5	4
	SWITCH	1	2
JTAG Mode		0	0
Quad-SPI		1	0
SD Card		1	1
ON = 1 , OFF = 0			

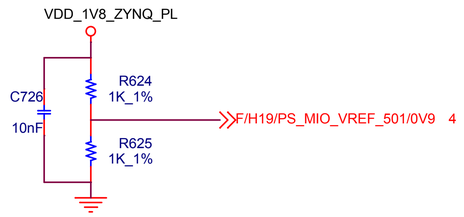
HW Watch Dog



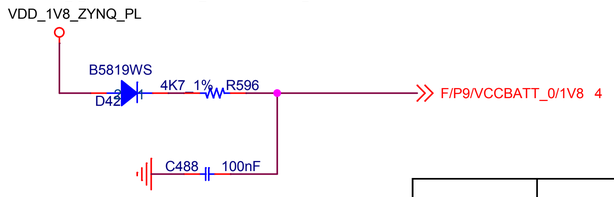
For the default setting,during the first startup,
when watchdog time out after 210s without any control of WDI,nWDO will pull low.
Then the time will become 90s.

ZYNQ Configuration

MIO BANK VOLTAGE CONFIG



Encryption Key Backup Circuit



Tronlong® Guangzhou Tronlong Technology Co., Ltd.

Title: ZYNQ_RTC/WD/BOOTSET/RESET/CONFIG

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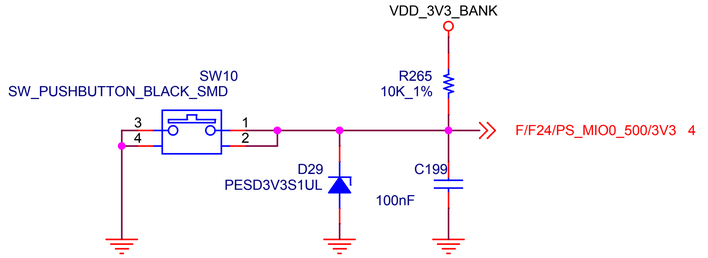
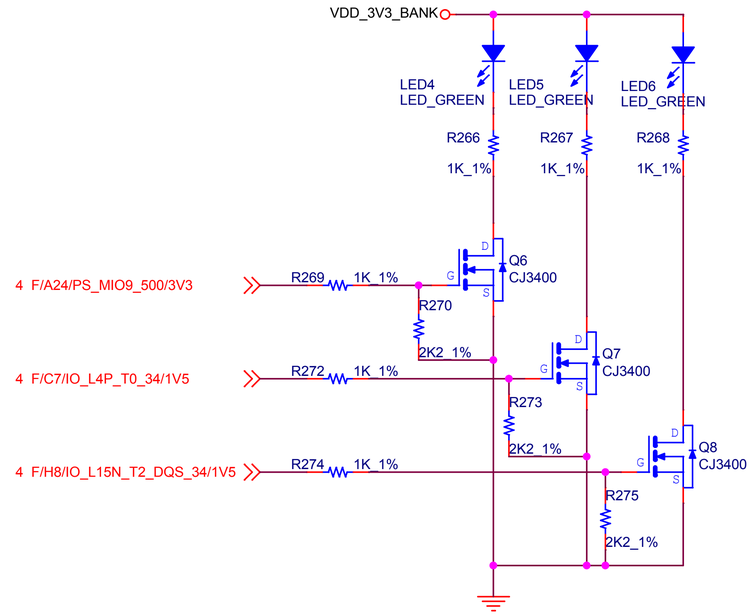
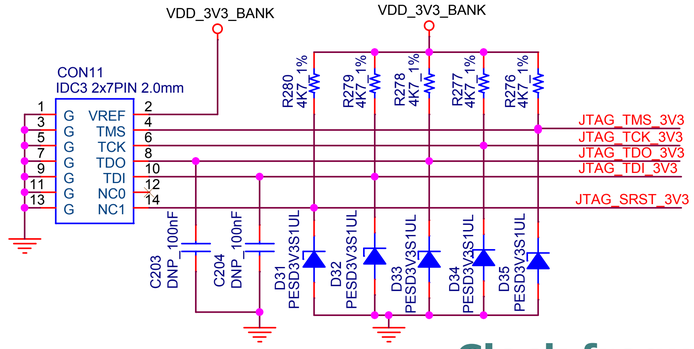
KEY



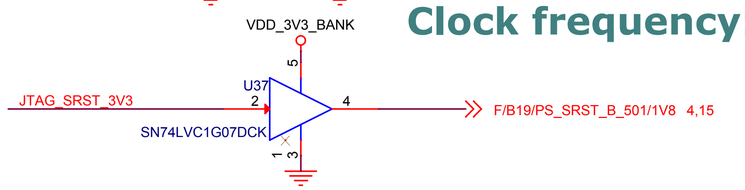
LED

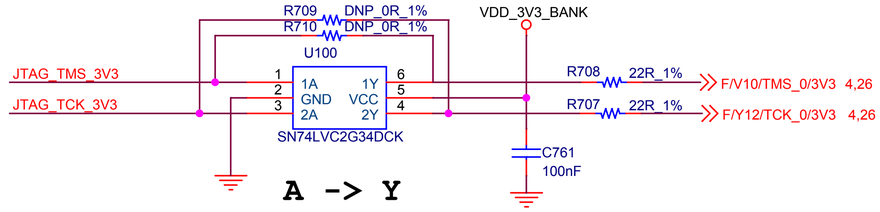


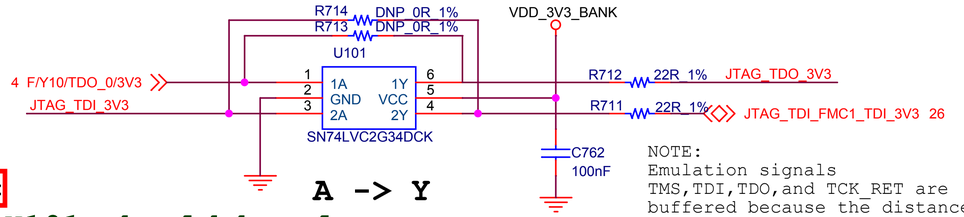
JTAG



Clock frequency:12MHz





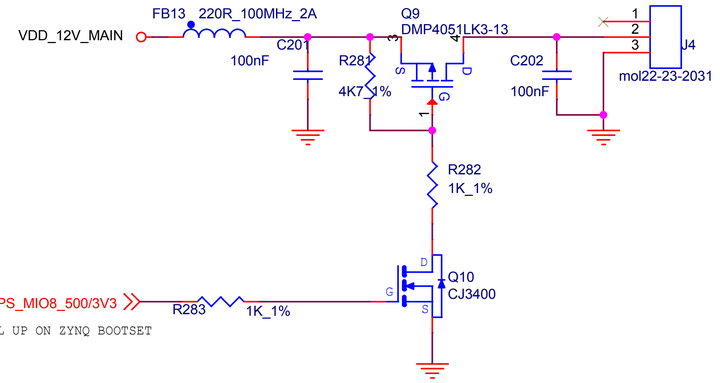


Layout Note:

U37,U100,U101 should be place in the middle of CON11 and CON0.

NOTE:
Emulation signals TMS,TDI,TDO,and TCK_RET are buffered because the distance between the emulation header and the processor is greater than six inches.

FAN



Tronlong®	Guangzhou Tronlong Technology Co., Ltd.		
Title	ZYNQ_JTAG/KEY/SRST/LED/FAN		
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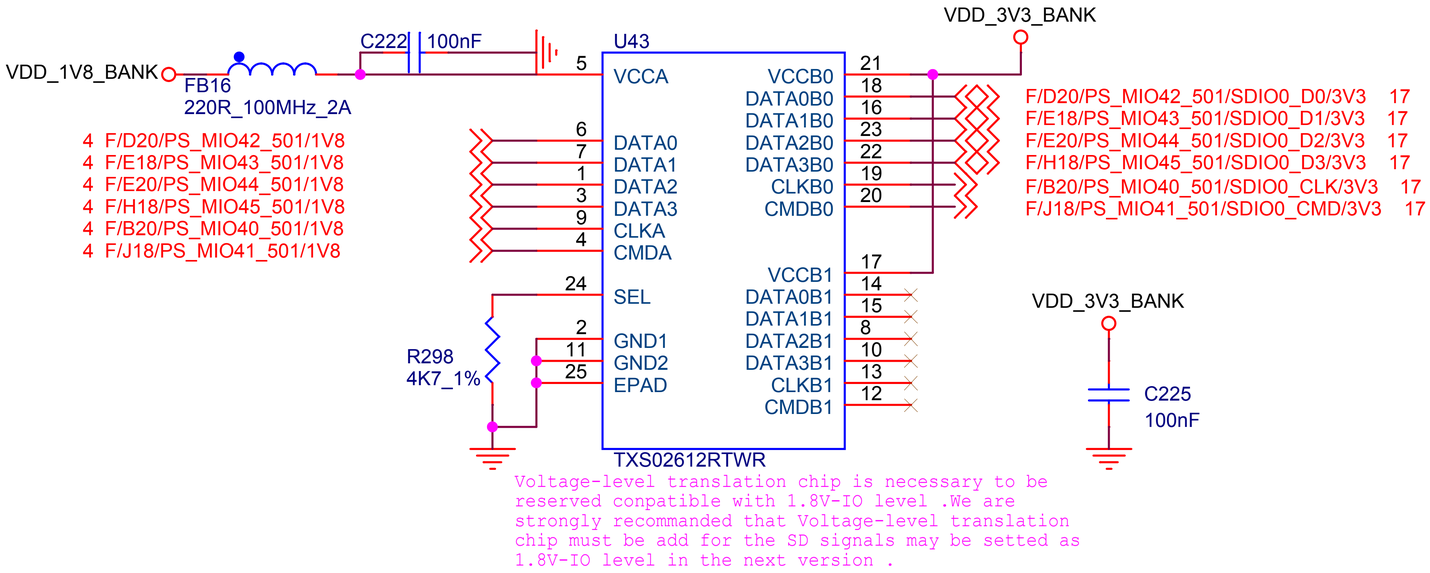
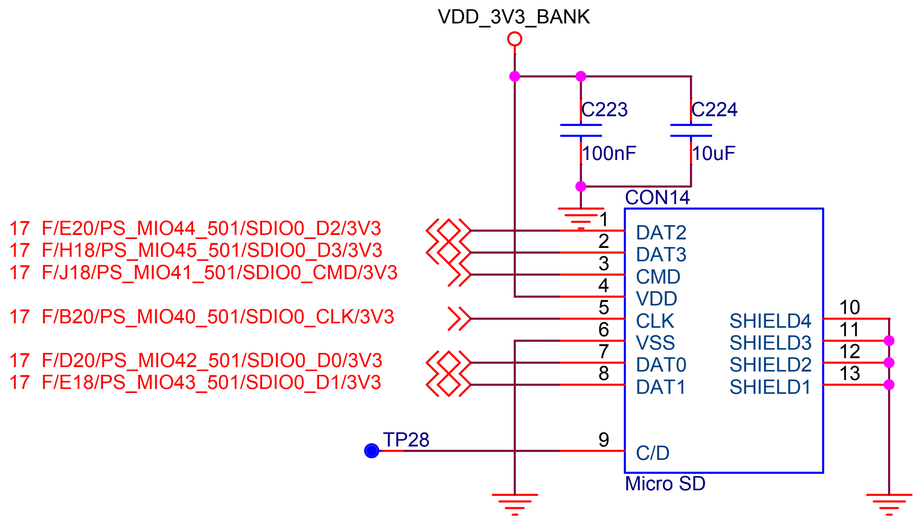
SD CARD



Voltage-level translation chip is necessary to be reserved conpatible with 1.8V-IO level .We are strongly recommanded that Voltage-level translation chip must be add for the SD signals may be setted as 1.8V-IO level in the next version .



CLK frequency:50MHz

Layout Note:

SD CARD should be routed according to Tronlong's requirement.

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Title	ZYNQ_SD_CARD/USB_HUB
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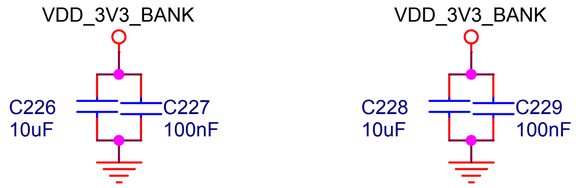
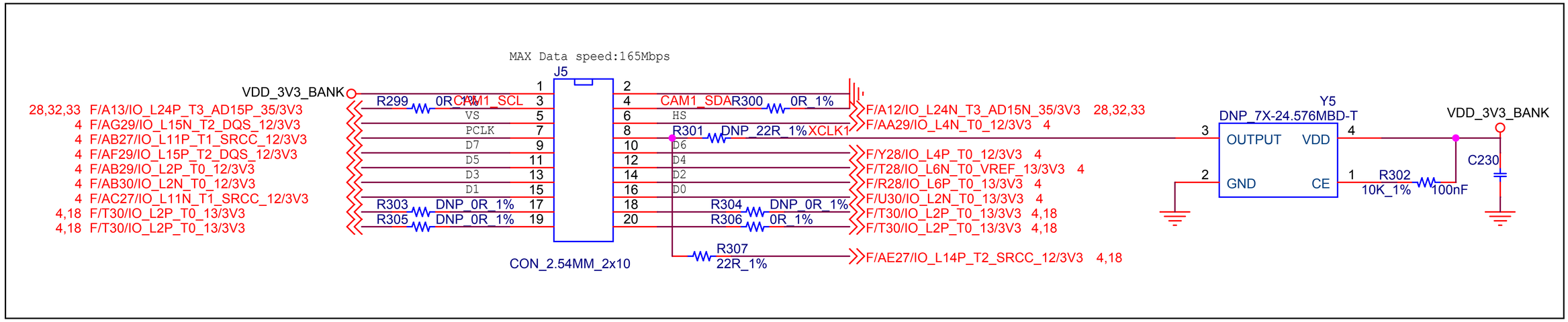
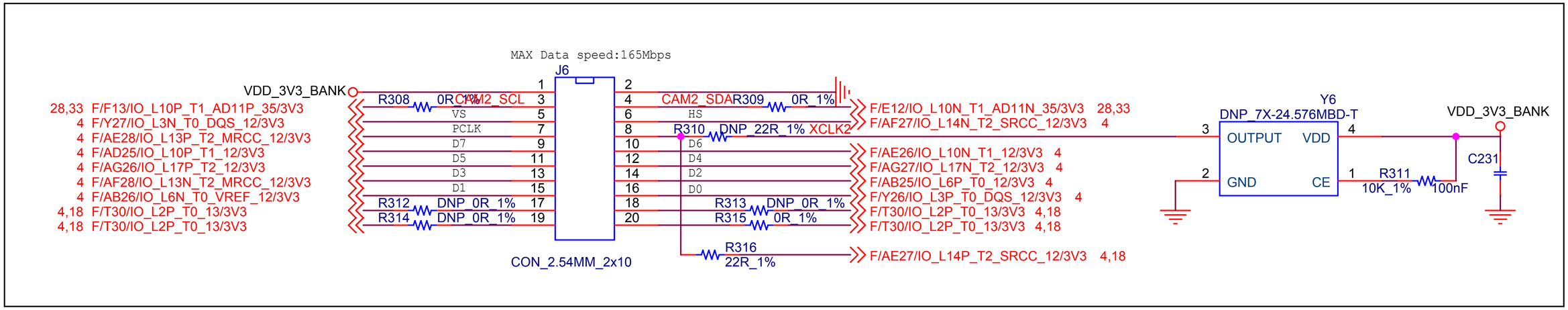
CAMERA_IN

Clock frequency:26.667MHz





MT9V034 I2C ADDRESS: 48H



Tronlong®

Guangzhou Tronlong Technology Co., Ltd.

Title	ZYNQ_CAMERA			
Size A4	Document Number TL6678ZH-EVM			
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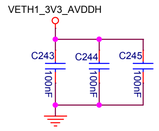
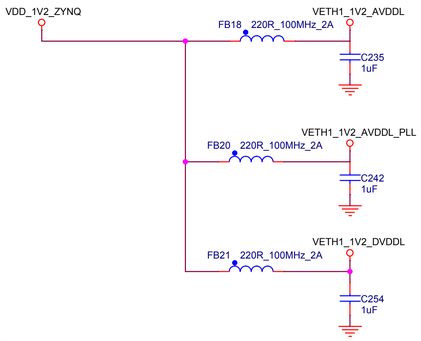
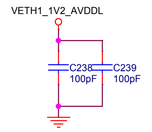
PL RGMII ETH

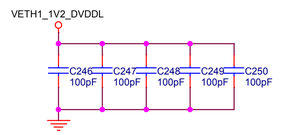
Data speed:1000Mbps

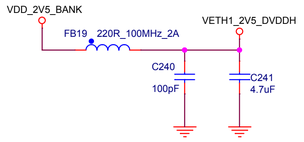
RGMII1_TD[3..0] & RGMII1_RD[3..0] Should be routed in Group and route same length reference to TXC & RXC with with ±10mil.

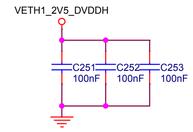


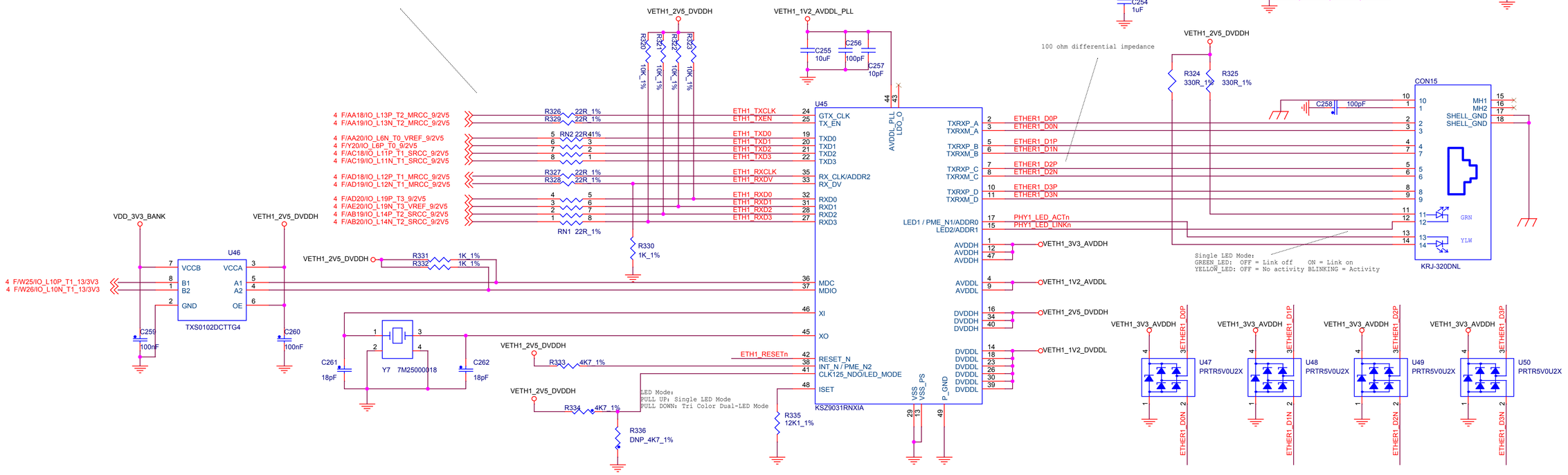


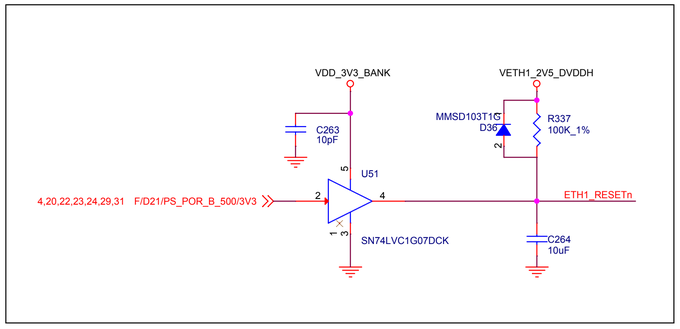


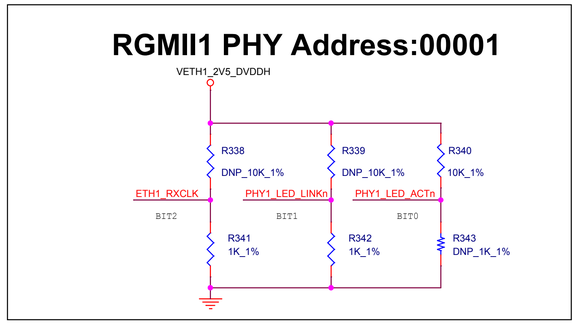












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Title	ZYNQ_ETH	
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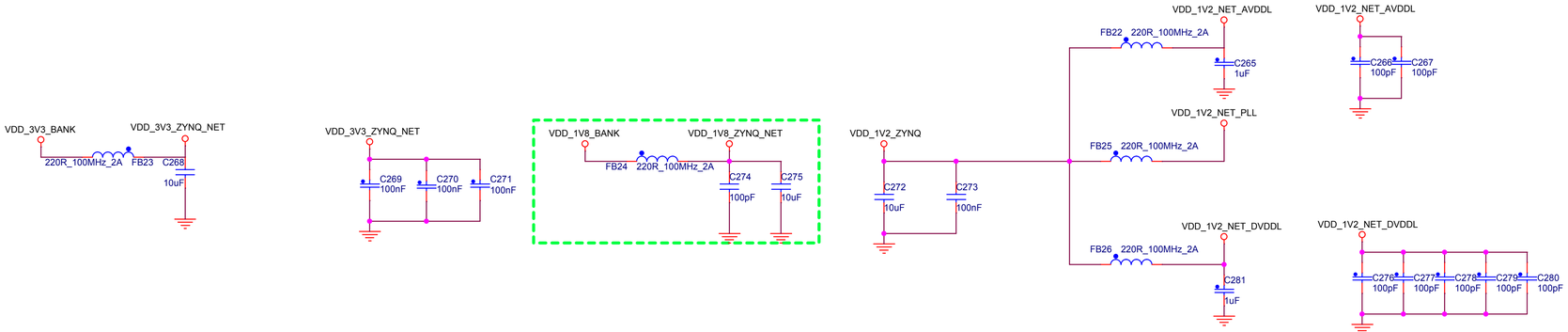
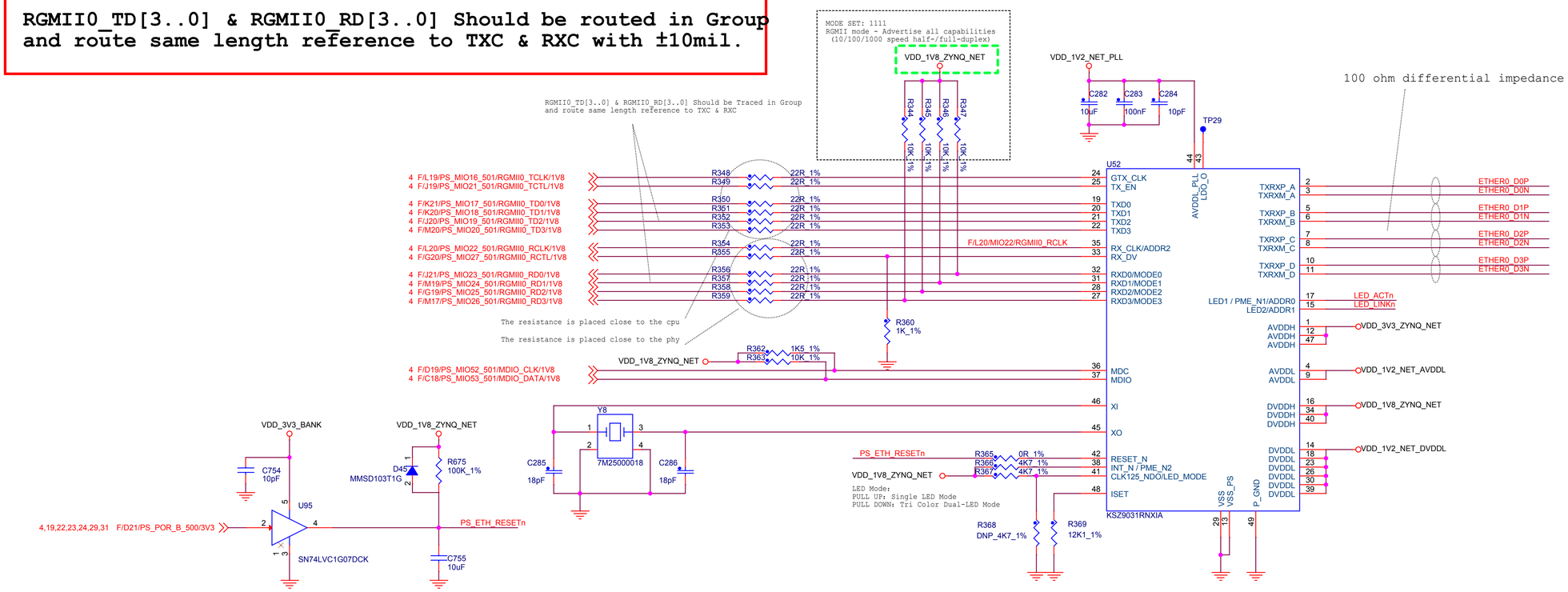
PS RGMII ETH



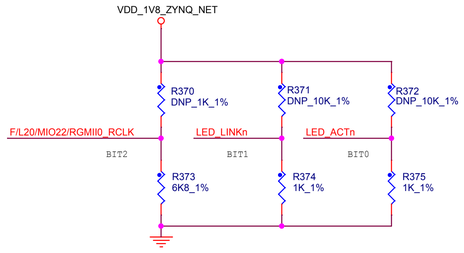
Clock frequency:125MHz

RGMII0_TD[3..0] & RGMII0_RD[3..0] Should be routed in Group and route same length reference to TXC & RXC with ±10mil.

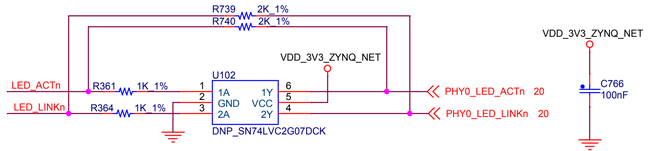


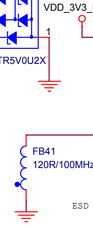
RGMII0 PHY Address:00000

PHY Address Bits [4:3] are always set to '00'



LED CONTROL





Tronlong®	Guangzhou Tronlong Technology Co., Ltd.
Title	ZYNQ_ETH
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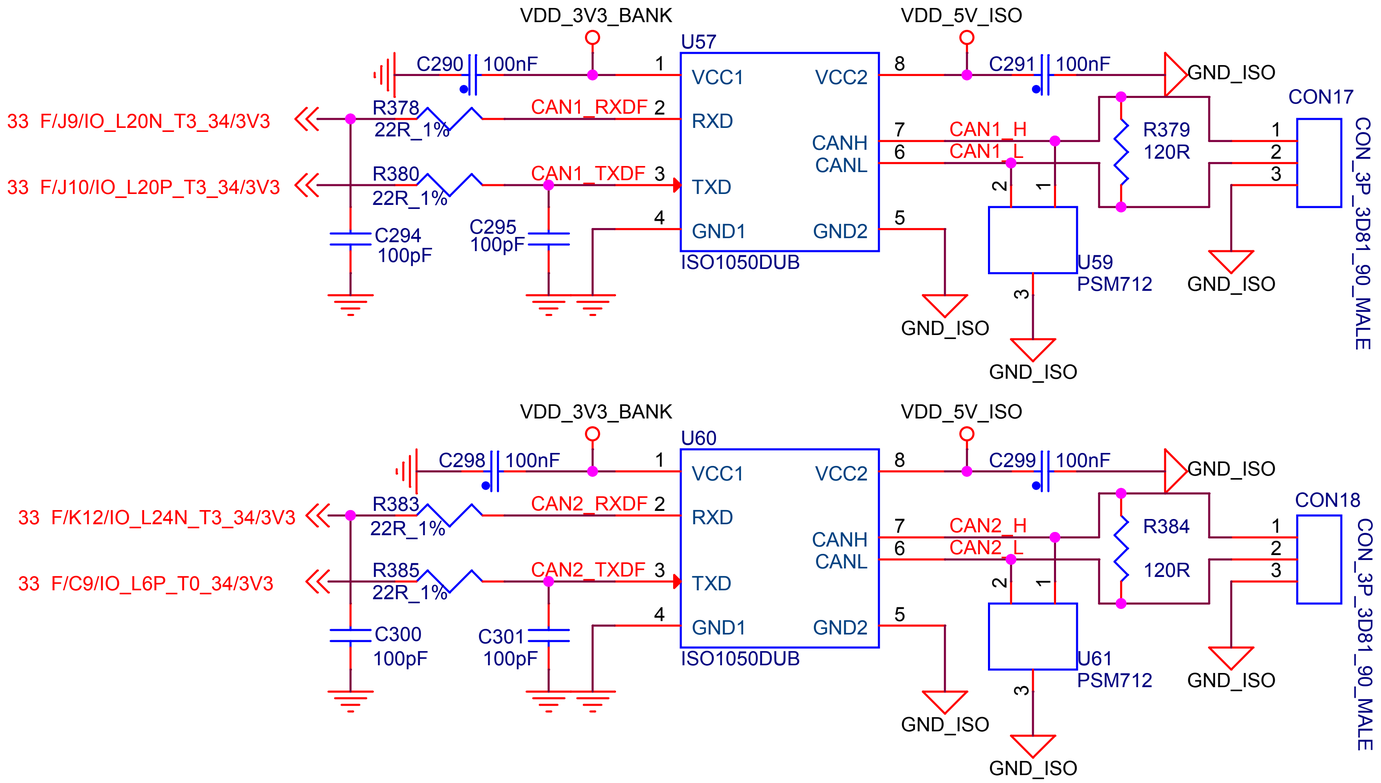
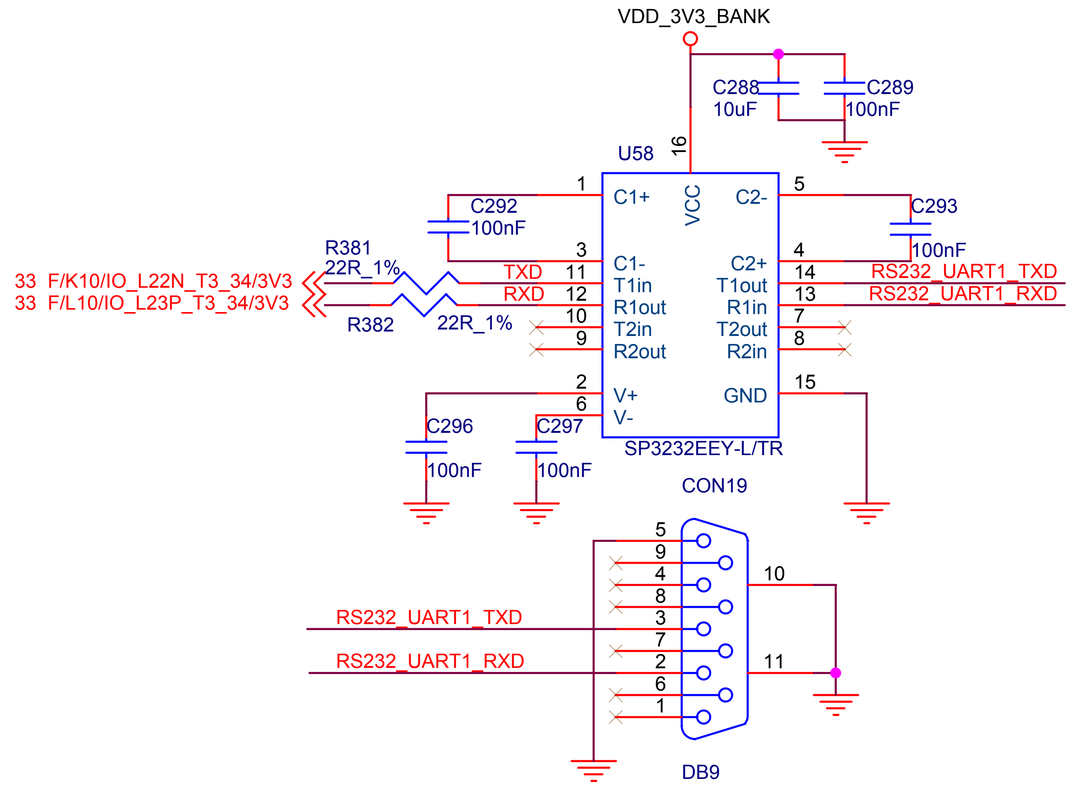
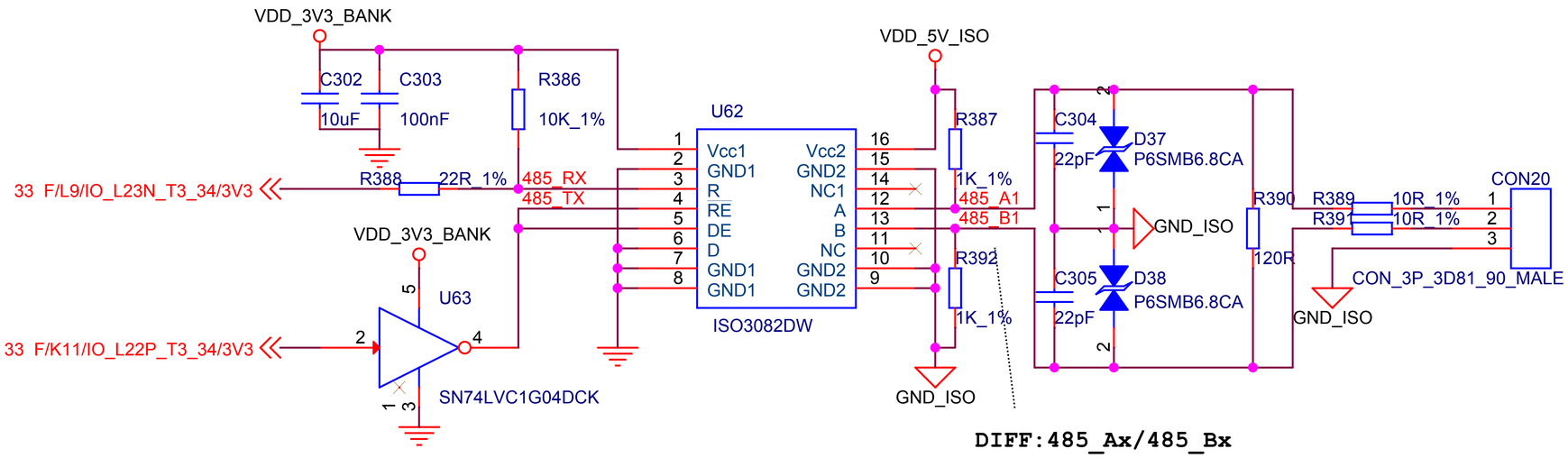
CAN



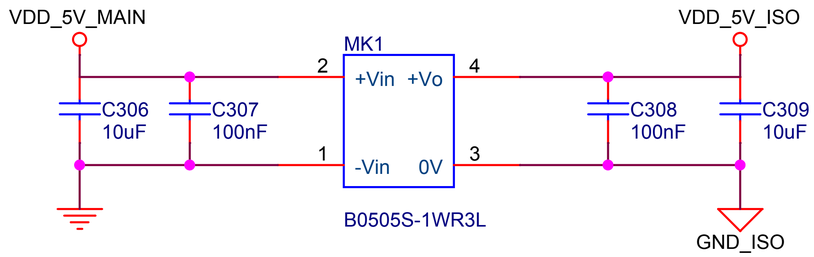
RS232



RS485



ISOLATE POWER



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Title	ZYNQ_RS485/CAN/RS232
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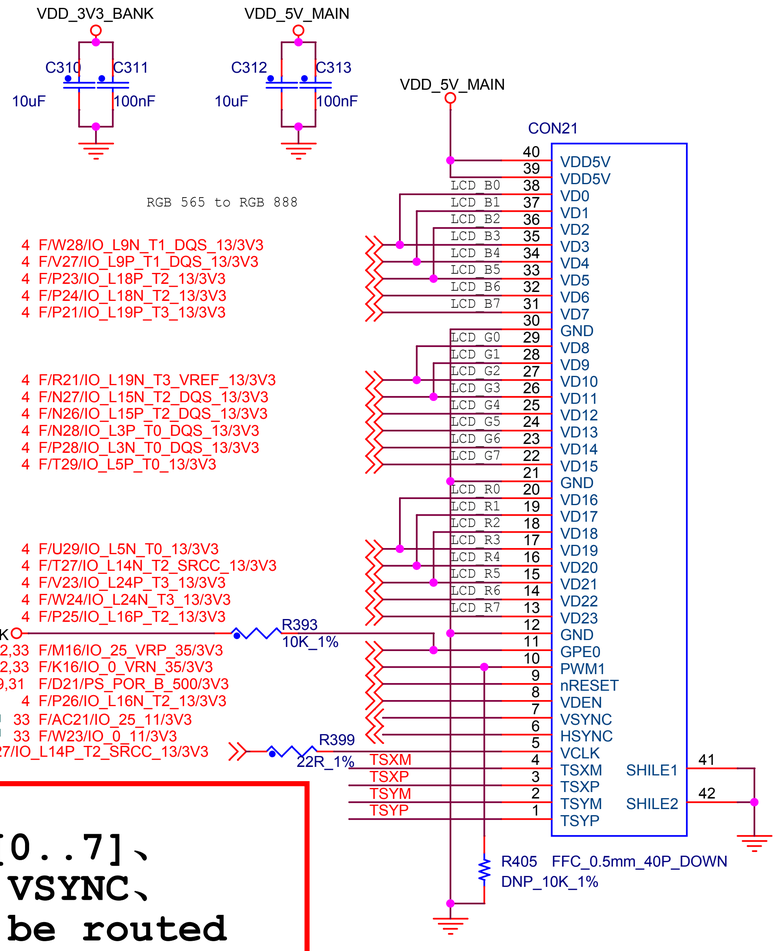
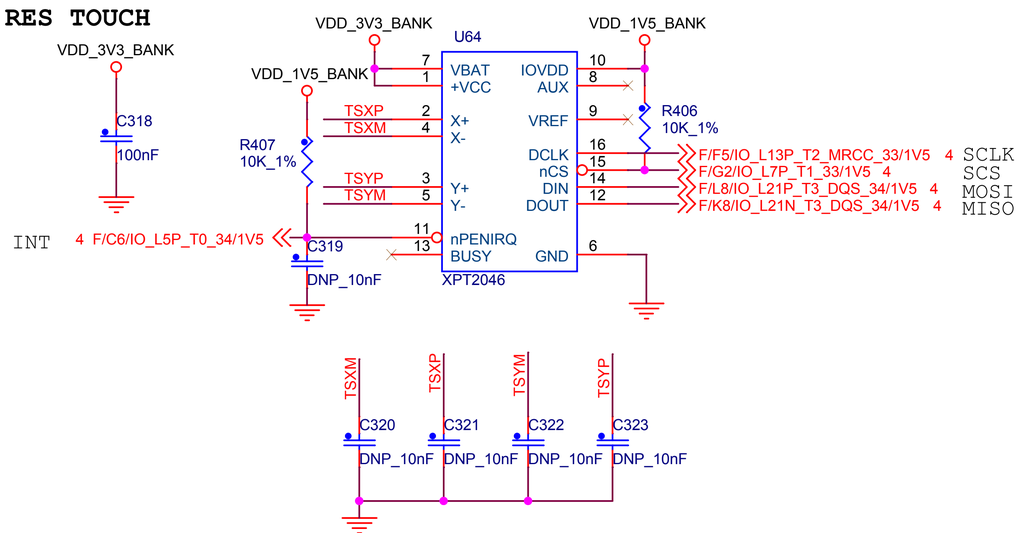
RES LCD



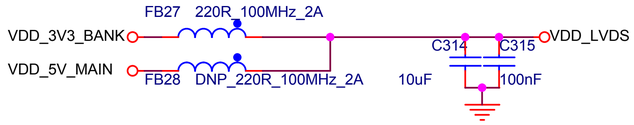
RGB Clock frequency: 148.5MHz

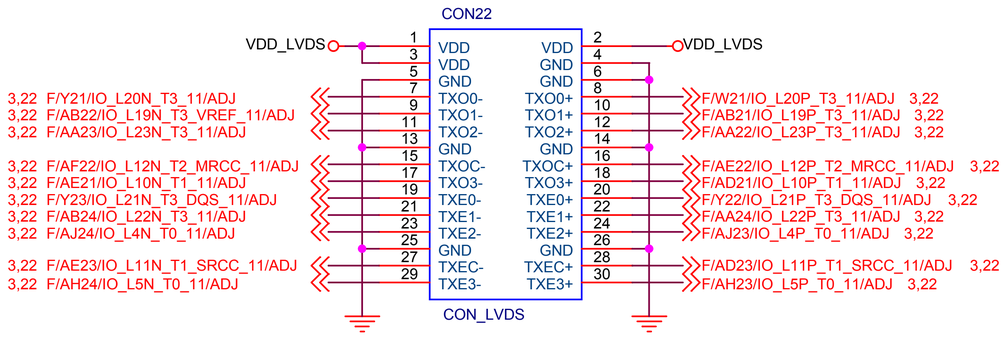
Layout Note:
LCD_B[0..7]、LCD_G[0..7]、LCD_R[0..7]、VDEN、VSYNC、HSYNC、VCLK should be routed in Group with same length.

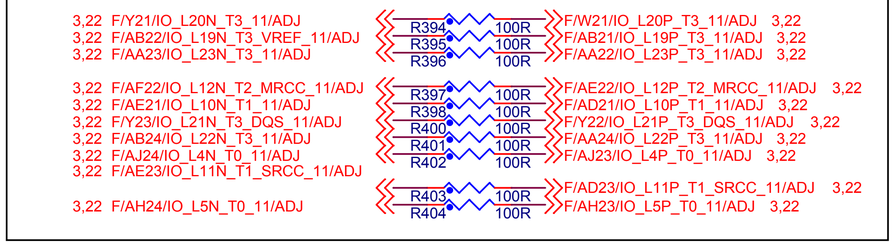
RES TOUCH



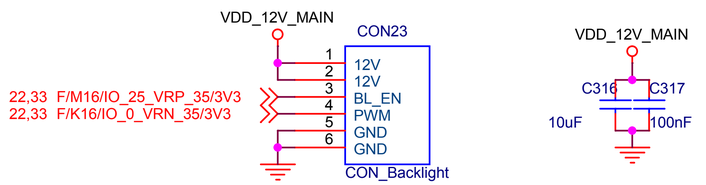
LVDS







BACKLIGHT POWER



Clock frequency: 74.25MHz
data speed: 519.75Mbps

Layout Note:

Data signal ends P/N routing with 100ohm differentialimpedance, need to the same length with ±15mil;

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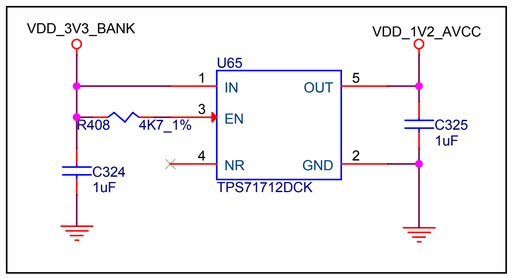
HDMI OUT



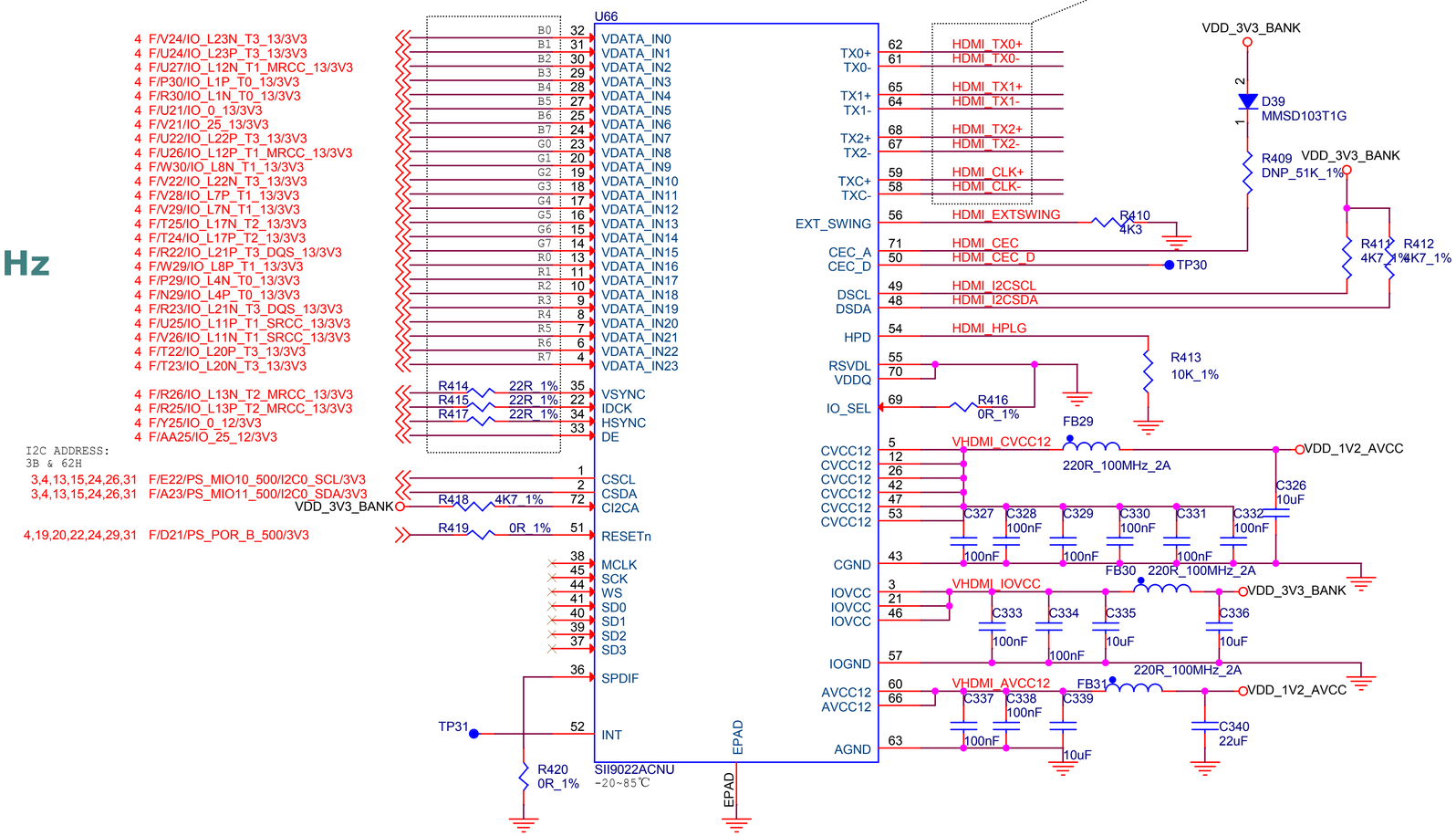
Clock frequency:148.5MHz

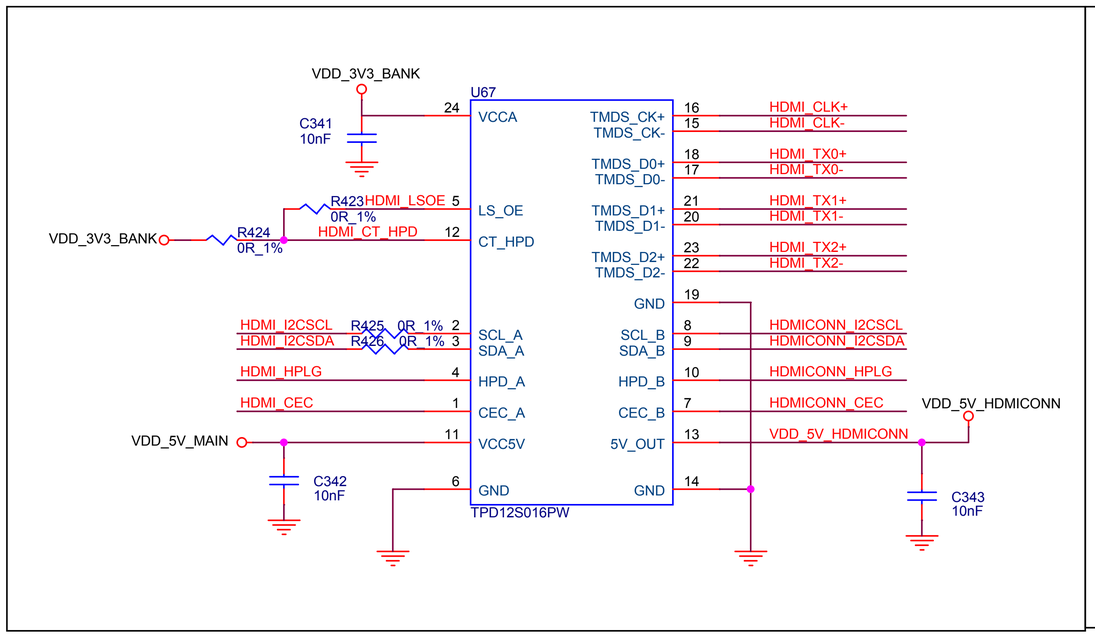
Layout Note:

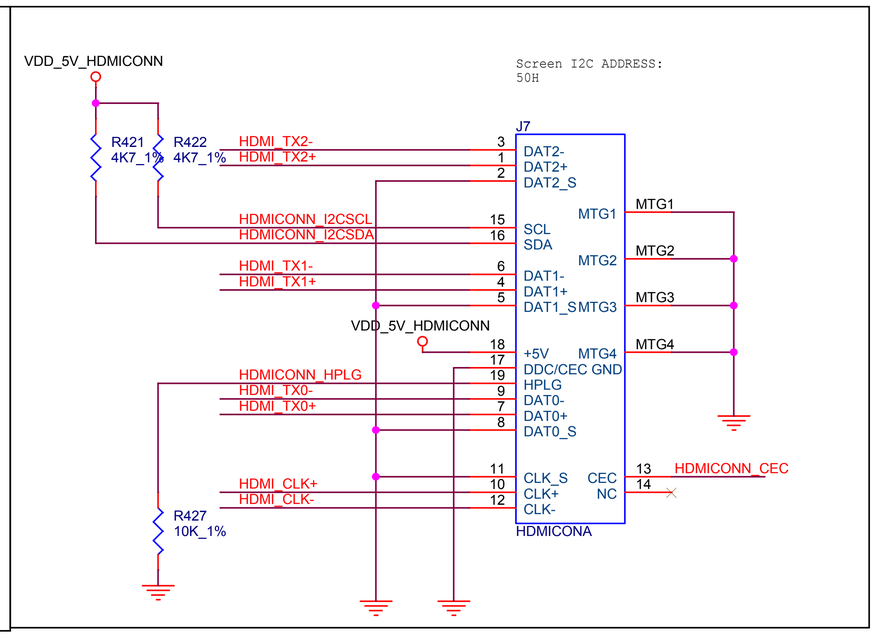
Should be routed in Group and need to the same length with ±10mil

Layout Note:

HDMI_TX0+/-、HDMI_TX1+/-、HDMI_TX2+/-、HDMI_CLK+/-
100 ohm differential impedance matching control







Tronlong®	Guangzhou Tronlong Technology Co., Ltd.		
Title	ZYNQ_HDMI_OUT		
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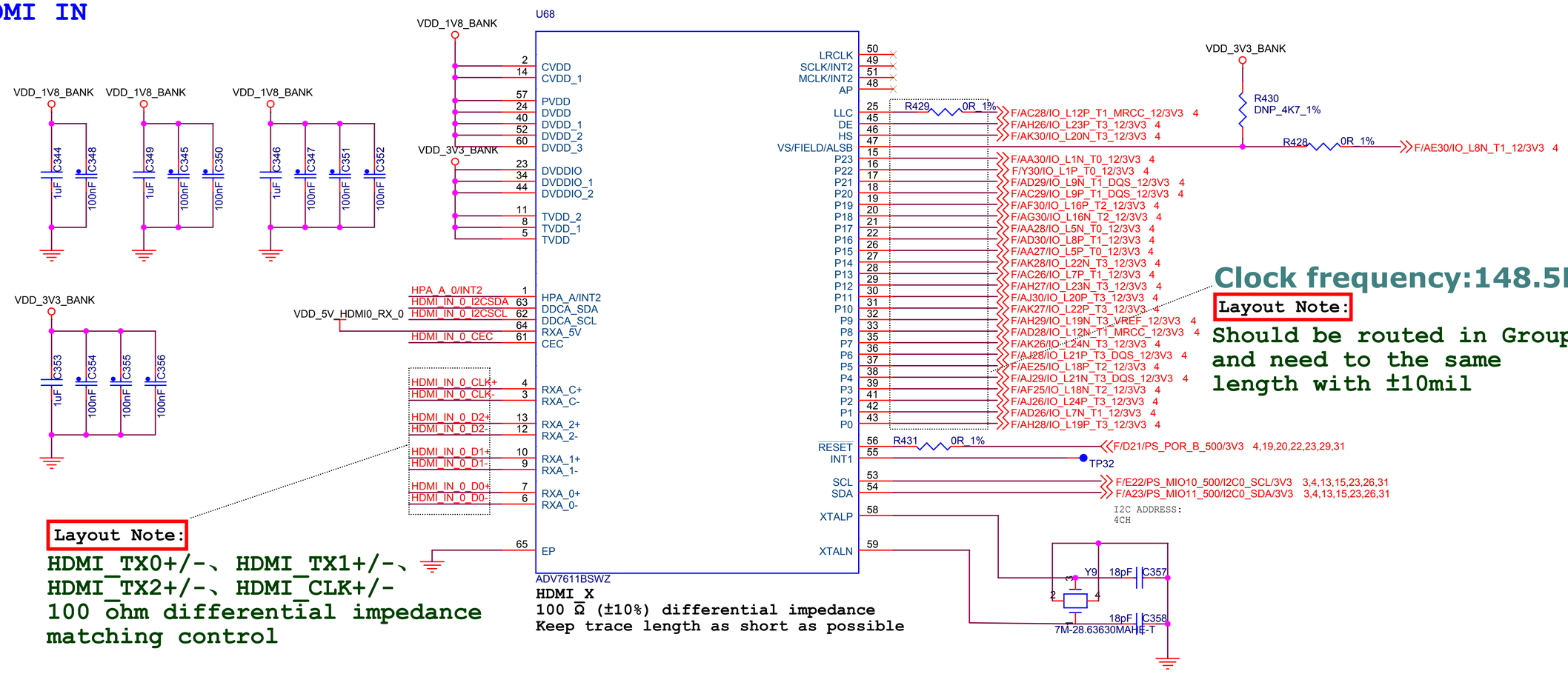
HDMI IN



Layout Note:

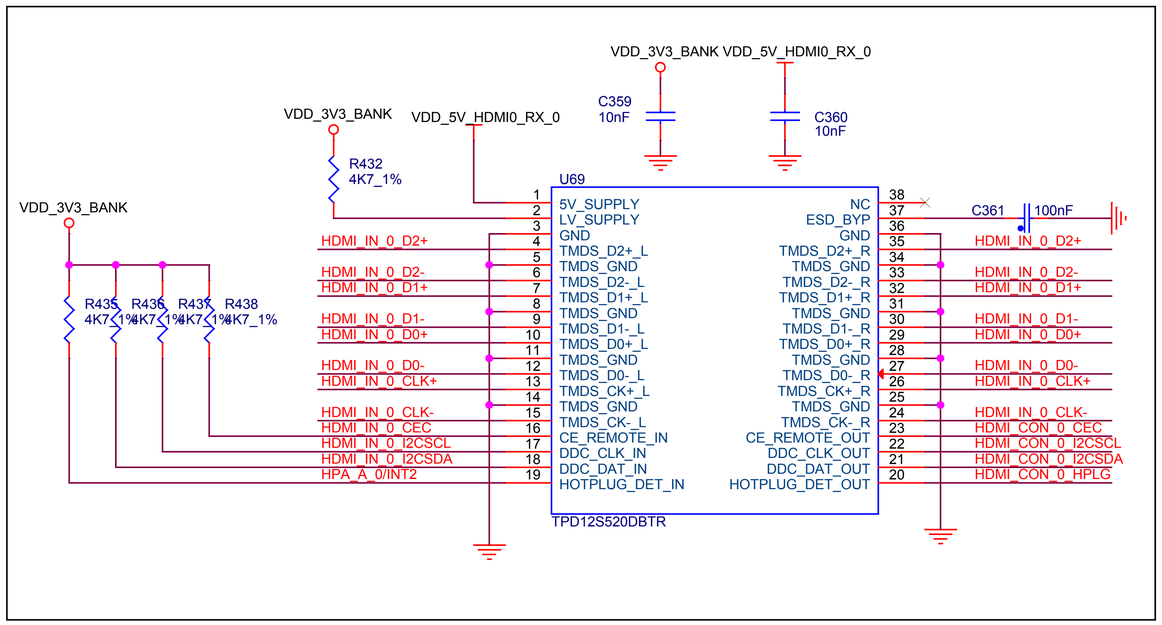
HDMI_TX0+/-、HDMI_TX1+/-、
HDMI_TX2+/-、HDMI_CLK+/-
100 ohm differential impedance
matching control

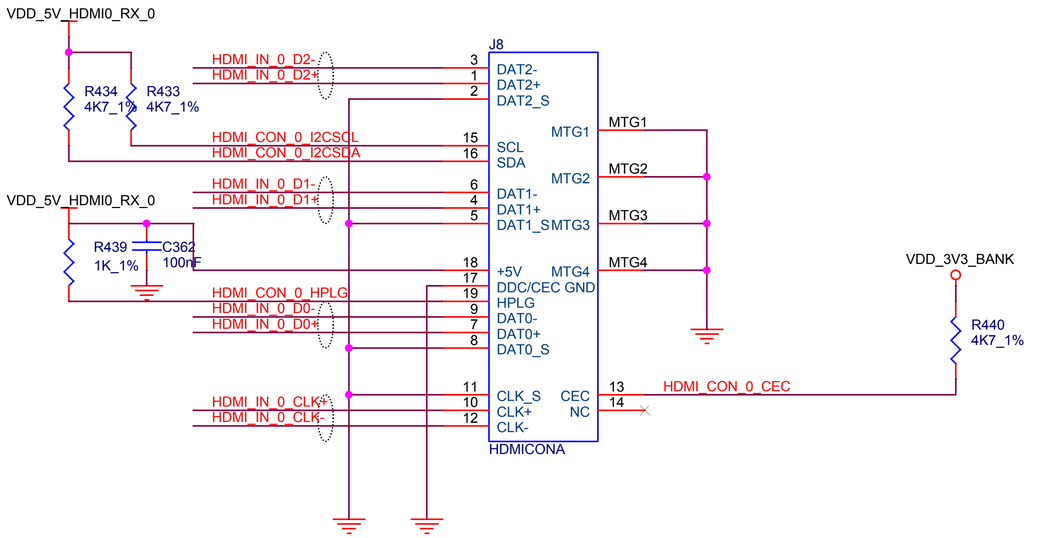
HDMI_X
100 Ω (±10%) differential impedance
Keep trace length as short as possible

Clock frequency:148.5MHz

Layout Note:

Should be routed in Group
and need to the same
length with ±10mil





Tronlong®	Guangzhou Tronlong Technology Co., Ltd.	
Title	ZYNQ_HDMI_IN	
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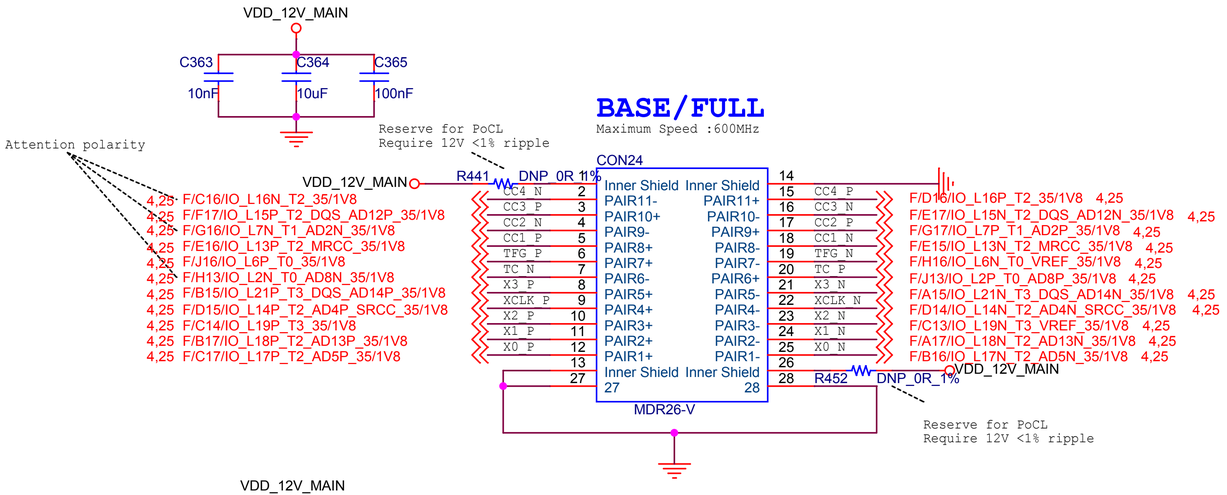
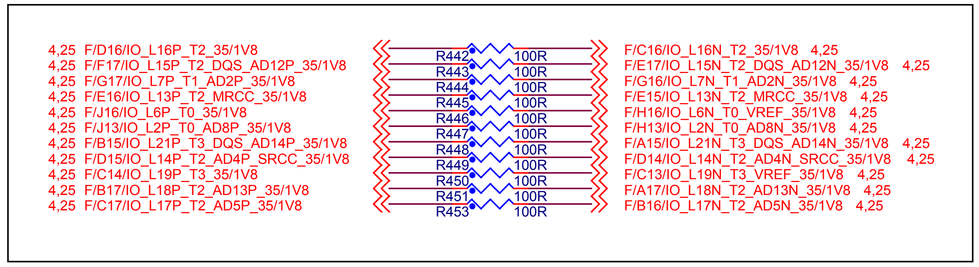
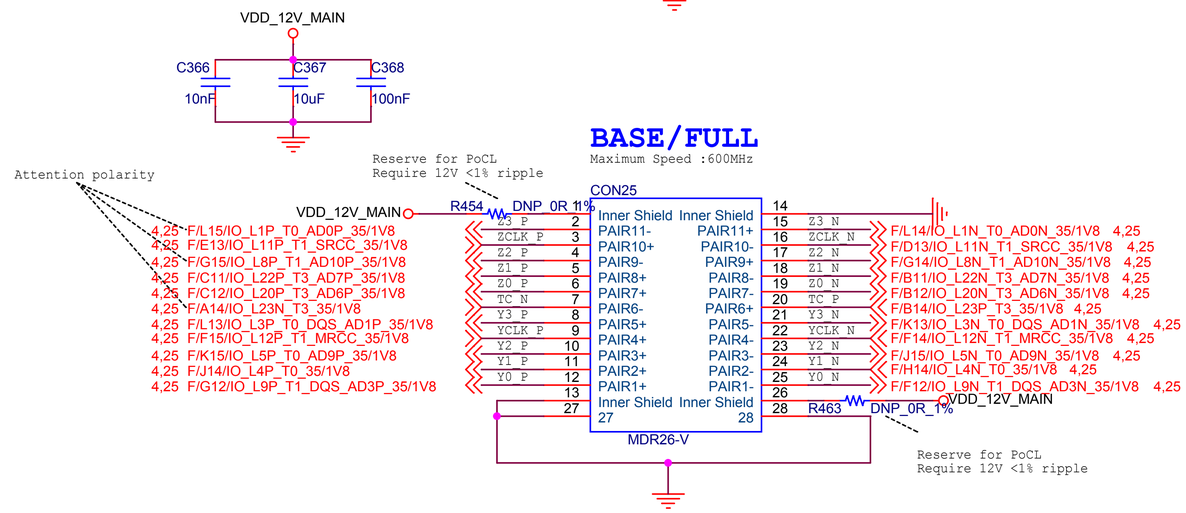
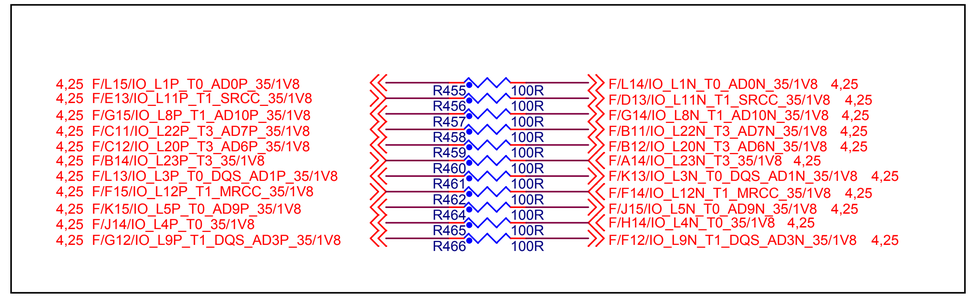
CAMERALINK









Cable Name	Base Configuration (with Camera Control and Serial Communications)			Medium, Full and 80 Bit Configurations		
	Camera Connector	Frame Grabber Connector	Channel Link Signal	Camera Connector	Frame Grabber Connector	Channel Link Signal
Inner Shield	1	1	inner shield	1	1	inner shield
Inner Shield	14	14	inner shield	14	14	inner shield
PAIR1-	2	25	X0-	2	25	Y0-
PAIR1+	15	12	X0+	15	12	Y0+
PAIR2-	3	24	X1-	3	24	Y1-
PAIR2+	16	11	X1+	16	11	Y1+
PAIR3-	4	23	X2-	4	23	Y2-
PAIR3+	17	10	X2+	17	10	Y2+
PAIR4-	5	22	Xclk-	5	22	Yclk-
PAIR4+	18	9	Xclk+	18	9	Yclk+
PAIR5-	6	21	X3-	6	21	Y3-
PAIR5+	19	8	X3+	19	8	Y3+
PAIR6+	7	20	SerTC+	7	20	100 Ω
PAIR6-	20	7	SerTC-	20	7	terminated
PAIR7-	8	19	SerTFG-	8	19	Z0-
PAIR7+	21	6	SerTFG+	21	6	Z0+
PAIR8-	9	18	CC1-	9	18	Z1-
PAIR8+	22	5	CC1+	22	5	Z1+
PAIR9+	10	17	CC2+	10	17	Z2-
PAIR9-	23	4	CC2-	23	4	Z2+
PAIR10-	11	16	CC3-	11	16	Zclk-
PAIR10+	24	3	CC3+	24	3	Zclk+
PAIR11+	12	15	CC4+	12	15	Z3-
PAIR11-	25	2	CC4-	25	2	Z3+
Inner Shield	13	13	inner shield	13	13	inner shield
Inner Shield	26	26	inner shield	26	26	inner shield

Data speed:595Mbps

Layout Note:

Signal ends P/N routing with 100ohm differentialimpedance, All differential pairs need to the same length with ±15mil;

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FMC A

Maximum Speed :10Gbps

CAUTION 2:

Signals held by this symbol should be rounted with 100 ohm differential impedance

CON26-2

DP0_C2M_P C2 → F/V2/MGTXTXP3_111 4
DP0_C2M_N C3 → F/V1/MGTXTXN3_111 4
DP0_M2C_P C6 → F/AA4/MGTXRXP3_111 4
DP0_M2C_N C7 → F/AA3/MGTXRXN3_111 4
LA06_P C10 → F/AE16/IO_L16P_T2_10/ADJ 4
LA06_N C11 → F/AE15/IO_L16N_T2_10/ADJ 4
LA10_P C14 → F/AJ15/IO_L5P_T0_10/ADJ 4
LA10_N C15 → F/AK15/IO_L5N_T0_10/ADJ 4
LA14_P C18 → F/AC17/IO_L23P_T3_10/ADJ 4
LA14_N C19 → F/AC16/IO_L23N_T3_10/ADJ 4
LA18_P_CC C22 → F/AF15/IO_L14P_T2_SRCC_10/ADJ 4
LA18_N_CC C23 → F/AG15/IO_L14N_T2_SRCC_10/ADJ 4
LA27_P C26 → F/AJ20/IO_L15P_T2_DQS_11/ADJ 3
LA27_N C27 → F/AK20/IO_L15N_T2_DQS_11/ADJ 3
SCL C30 — R467 22R 1% → F/E22/PS_MIO10_500/I2C0_SCL/3V3 3,4,13,15,23,24,31
SDA C31 — R468 22R 1% → F/A23/PS_MIO11_500/I2C0_SDA/3V3 3,4,13,15,23,24,31
GA0 C34 — R470 DNP 0R 1%; R469 0R 1% → VDD_3V3_BANK
12P0V_1 C35 → VDD_12V_MAIN
12P0V_2 C37
3P3V_1 C39 → VDD_3V3_BANK

ASP_134486_01

I2C Addressing(FMC):0bxxxxx01
Attetion:
I2C Address should not be set as 0bxxxxx00
if the HDMIOUT function circuit needed,otherwise.
That will be conflicted with the address of E2PROM (0x50) .

VDD_FMC_ADJ
C377 100nF
C378 10uF

CON26-3

PG_C2M D1 — R472 1K 1% → VDD_3V3_BANK
GBTCLK0_M2C_P D4 → GBTCLK0_M2C_P 26
GBTCLK0_M2C_N D5 → GBTCLK0_M2C_N 26
LA01_P_CC D8 → F/AE13/IO_L11P_T1_SRCC_10/ADJ 4
LA01_N_CC D9 → F/AF13/IO_L11N_T1_SRCC_10/ADJ 4
LA05_P D11 → F/AJ14/IO_L3P_T0_DQS_10/ADJ 4
LA05_N D12 → F/AJ13/IO_L3N_T0_DQS_10/ADJ 4
LA09_P D14 → F/AD14/IO_L9P_T1_DQS_10/ADJ 4
LA09_N D15 → F/AD13/IO_L9N_T1_DQS_10/ADJ 4
LA13_P D17 → F/AE18/IO_L17P_T2_10/ADJ 4
LA13_N D18 → F/AE17/IO_L17N_T2_10/ADJ 4
LA17_P_CC D20 → F/AG17/IO_L13P_T2_MRCC_10/ADJ 4
LA17_N_CC D21 → F/AG16/IO_L13N_T2_MRCC_10/ADJ 4
LA23_P D23 → F/AK13/IO_L1P_T0_10/ADJ 4
LA23_N D24 → F/AK12/IO_L1N_T0_10/ADJ 4
LA26_P D26 → F/AG22/IO_L6P_T0_11/ADJ 3
LA26_N D27 → F/AH22/IO_L6N_T0_VREF_11/ADJ 3
TCK D29 — R473 22R 1% → F/Y12/TCK_0/3V3 4,16
TDI D30 — R474 22R 1% → JTAG_TDI_FMC1_TDI_3V3 16,26
TDO D31 — R475 22R 1% → F/P10/FMC1_TDO_ZYNQ_TDI/3V3 4,26
3P3VAUX D32
TMS D33 — R476 22R 1% → F/V10/TMS_0/3V3 4,16
TRST_L D34
GA1 D35 — R477 DNP 0R 1%; R478 0R 1% → VDD_3V3_BANK
3P3V_2 D36
3P3V_3 D38
3P3V_4 D40 → VDD_3V3_BANK

ASP_134486_01

CON26-7

CLK0_C2M_P G2 → F/AG21/IO_L13P_T2_MRCC_11/ADJ 3
CLK0_C2M_N G3 → F/AH21/IO_L13N_T2_MRCC_11/ADJ 3
LA00_P_CC G6 → F/AF14/IO_L12P_T1_MRCC_10/ADJ 4
LA00_N_CC G7 → F/AG14/IO_L12N_T1_MRCC_10/ADJ 4
LA03_P G9 → F/AH18/IO_L2P_T0_10/ADJ 4
LA03_N G10 → F/AJ18/IO_L2N_T0_10/ADJ 4
LA08_P G12 → F/AE12/IO_L7P_T1_10/ADJ 4
LA08_N G13 → F/AF12/IO_L7N_T1_10/ADJ 4
LA12_P G15 → F/AB17/IO_L24P_T3_10/ADJ 4
LA12_N G16 → F/AB16/IO_L24N_T3_10/ADJ 4
LA16_P G18 → F/AC14/IO_L19P_T3_10/ADJ 4
LA16_N G19 → F/AC13/IO_L19N_T3_VREF_10/ADJ 4
LA20_P G21 → F/AB15/IO_L22P_T3_10/ADJ 4
LA20_N G22 → F/AB14/IO_L22N_T3_10/ADJ 4
LA22_P G24 → F/AJ16/IO_L4P_T0_10/ADJ 4
LA22_N G25 → F/AK16/IO_L4N_T0_10/ADJ 4
LA25_P G27 → F/AF19/IO_L18P_T2_11/ADJ 3
LA25_N G28 → F/AG19/IO_L18N_T2_11/ADJ 3
LA29_P G30 → F/AF23/IO_L9P_T1_DQS_11/ADJ 3
LA29_N G31 → F/AF24/IO_L9N_T1_DQS_11/ADJ 3
LA31_P G33 → F/AJ21/IO_L3P_T0_DQS_11/ADJ 3
LA31_N G34 → F/AK21/IO_L3N_T0_DQS_11/ADJ 3
LA33_P G36 → F/AJ25/IO_L1P_T0_11/ADJ 3
LA33_N G37 → F/AK25/IO_L1N_T0_11/ADJ 3
VADJ_3 G39 → VDD_FMC_ADJ

ASP_134486_01

VDD_3V3_BANK
R471 2K2 1%
FMC_PRSNTn

CON26-8

VREF_A_M2C H1
PRSNT_M2C_L H2
CLK0_M2C_P H4 → F/AF20/IO_L14P_T2_SRCC_11/ADJ 3
CLK0_M2C_N H5 → F/AG20/IO_L14N_T2_SRCC_11/ADJ 3
LA02_P H7 → F/AH17/IO_L6P_T0_10/ADJ 4
LA02_N H8 → F/AH16/IO_L6N_T0_VREF_10/ADJ 4
LA04_P H10 → F/AG12/IO_L10P_T1_10/ADJ 4
LA04_N H11 → F/AH12/IO_L10N_T1_10/ADJ 4
LA07_P H13 → F/AH14/IO_L8P_T1_10/ADJ 4
LA07_N H14 → F/AH13/IO_L8N_T1_10/ADJ 4
LA11_P H16 → F/AF18/IO_L15P_T2_DQS_10/ADJ 4
LA11_N H17 → F/AF17/IO_L15N_T2_DQS_10/ADJ 4
LA15_P H19 → F/AD16/IO_L18P_T2_10/ADJ 4
LA15_N H20 → F/AD15/IO_L18N_T2_10/ADJ 4
LA19_P H22 → F/AB12/IO_L21P_T3_DQS_10/ADJ 4
LA19_N H23 → F/AC12/IO_L21N_T3_DQS_10/ADJ 4
LA21_P H25 → F/AA15/IO_L20P_T3_10/ADJ 4
LA21_N H26 → F/AA14/IO_L20N_T3_10/ADJ 4
LA24_P H28 → F/AK17/IO_L16P_T2_11/ADJ 3
LA24_N H29 → F/AK18/IO_L16N_T2_11/ADJ 3
LA28_P H31 → F/AH19/IO_L17P_T2_11/ADJ 3
LA28_N H32 → F/AJ19/IO_L17N_T2_11/ADJ 3
LA30_P H34 → F/AG24/IO_L8P_T1_11/ADJ 3
LA30_N H35 → F/AG25/IO_L8N_T1_11/ADJ 3
LA32_P H37 → F/AK22/IO_L2P_T0_11/ADJ 3
LA32_N H38 → F/AK23/IO_L2N_T0_11/ADJ 3
VADJ_4 H40 → VDD_FMC_ADJ

ASP_134486_01

CON26-1

Maximum Speed :13GHz

DP1_M2C_P A2 → F/Y6/MGTXRXP2_111 4
DP1_M2C_N A3 → F/Y5/MGTXRXN2_111 4
DP2_M2C_P A6 → F/AB6/MGTXRXP1_111 4
DP2_M2C_N A7 → F/AB5/MGTXRXN1_111 4
DP3_M2C_P A10 → F/AC4/MGTXRXP0_111 4
DP3_M2C_N A11 → F/AC3/MGTXRXN0_111 4
DP4_M2C_P A14
DP4_M2C_N A15
DP5_M2C_P A18
DP5_M2C_N A19
DP1_C2M_P A22 → F/W4/MGTXTXP2_111 4
DP1_C2M_N A23 → F/W3/MGTXTXN2_111 4
DP2_C2M_P A26 → F/Y2/MGTXTXP1_111 4
DP2_C2M_N A27 → F/Y1/MGTXTXN1_111 4
DP3_C2M_P A30 → F/AB2/MGTXTXP0_111 4
DP3_C2M_N A31 → F/AB1/MGTXTXN0_111 4
DP4_C2M_P A34
DP4_C2M_N A35
DP5_C2M_P A38
DP5_C2M_N A39

ASP_134486_01

CON26-4

CLK_DIR B1
DP9_M2C_P B4
DP9_M2C_N B5
DP8_M2C_P B8
DP8_M2C_N B9
DP7_M2C_P B12
DP7_M2C_N B13
DP6_M2C_P B16
DP6_M2C_N B17
GBTCLK1_M2C_P B20 → GBTCLK1_M2C_P 26
GBTCLK1_M2C_N B21 → GBTCLK1_M2C_N 26
DP9_C2M_P B24
DP9_C2M_N B25
DP8_C2M_P B28
DP8_C2M_N B29
DP7_C2M_P B32
DP7_C2M_N B33
DP6_C2M_P B36
DP6_C2M_N B37
RES0 B40

ASP_134486_01

Data speed:DP 10Gbps
LA 2Gbps

Layout Note:

1. LA Data signal ends P/N routing with 100ohm differential impedance,need to the same length with ±5mil;
2. DP Data signal ends P/N routing with 100ohm differential impedance,need to the same length with ±1mil;

VDD_3V3_BANK
C383 100nF
R479 DNP 0R 1%
U70 NC7SZ66P5X
VCC 5
1 A
B 2 → F/P10/FMC1_TDO_ZYNQ_TDI/3V3 4,26
16,26 JTAG_TDI_FMC1_TDI_3V3
FMC_PRSNTn 4 OE
GND 3
R480 DNP 0R 1%
When OE = 1
Switch is Closed

26 GBTCLK1_M2C_P — C379 100nF → F/U8/MGTREFCLK0P_111 4
26 GBTCLK1_M2C_N — C380 100nF → F/U7/MGTREFCLK0N_111 4

26 GBTCLK0_M2C_P — C381 100nF → F/W8/MGTREFCLK1P_111 4
26 GBTCLK0_M2C_N — C382 100nF → F/W7/MGTREFCLK1N_111 4

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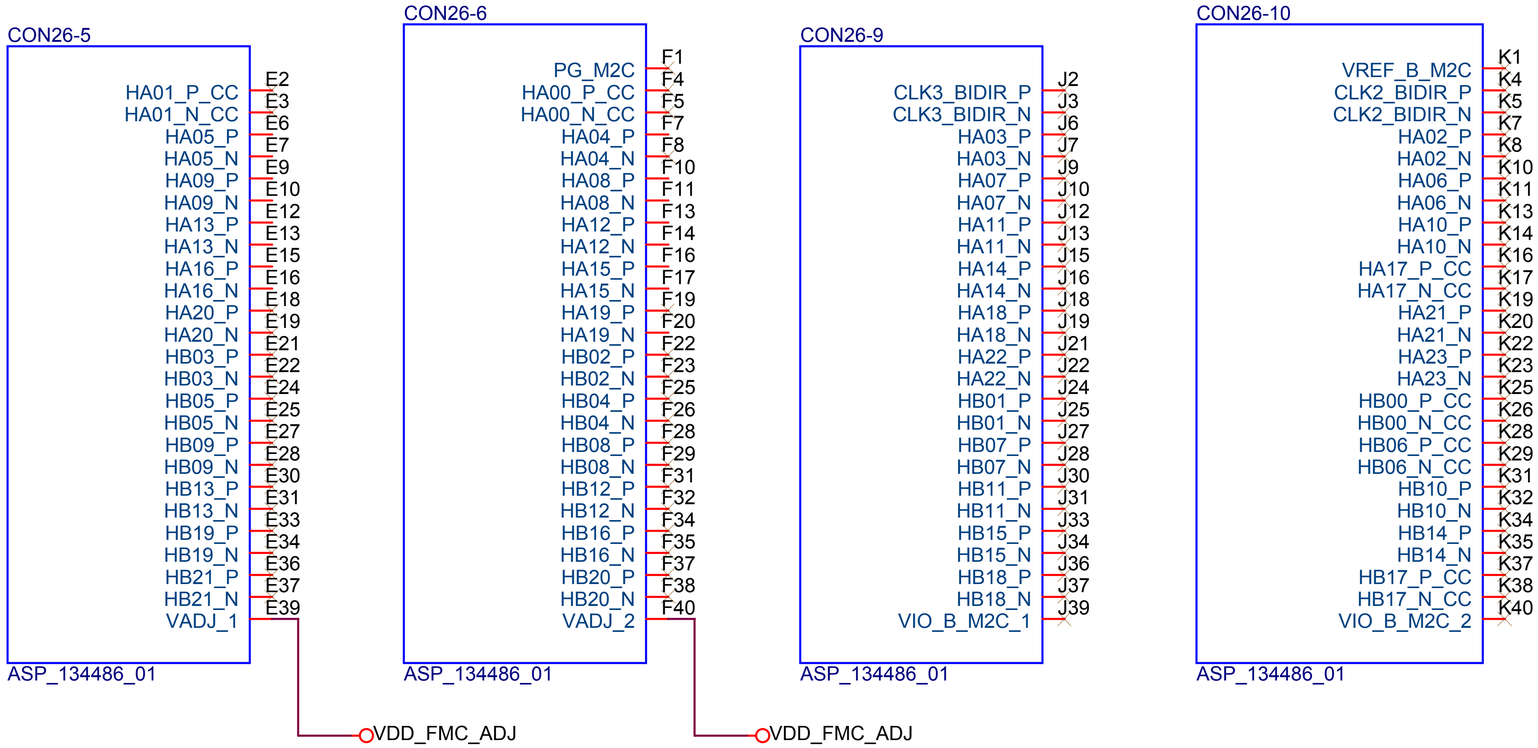
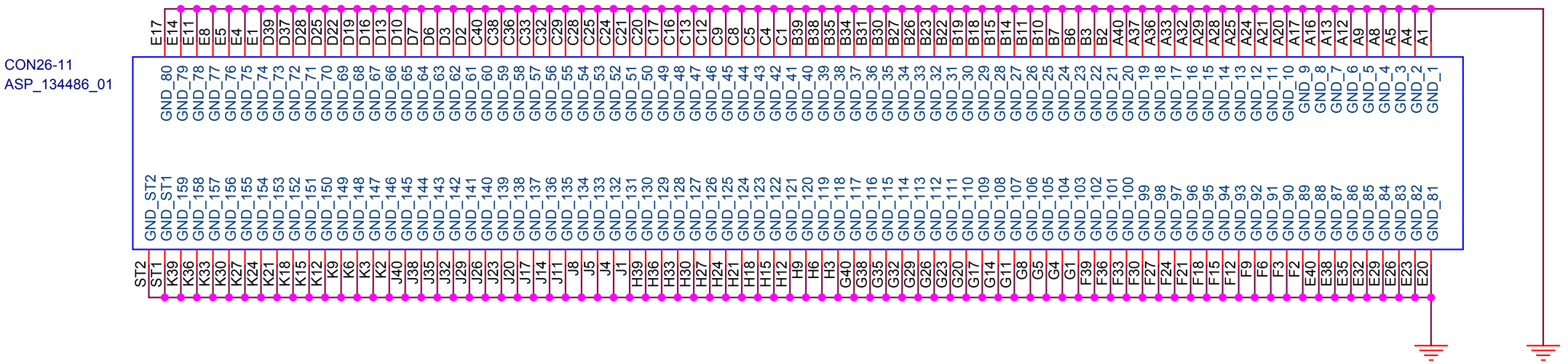
FMC B





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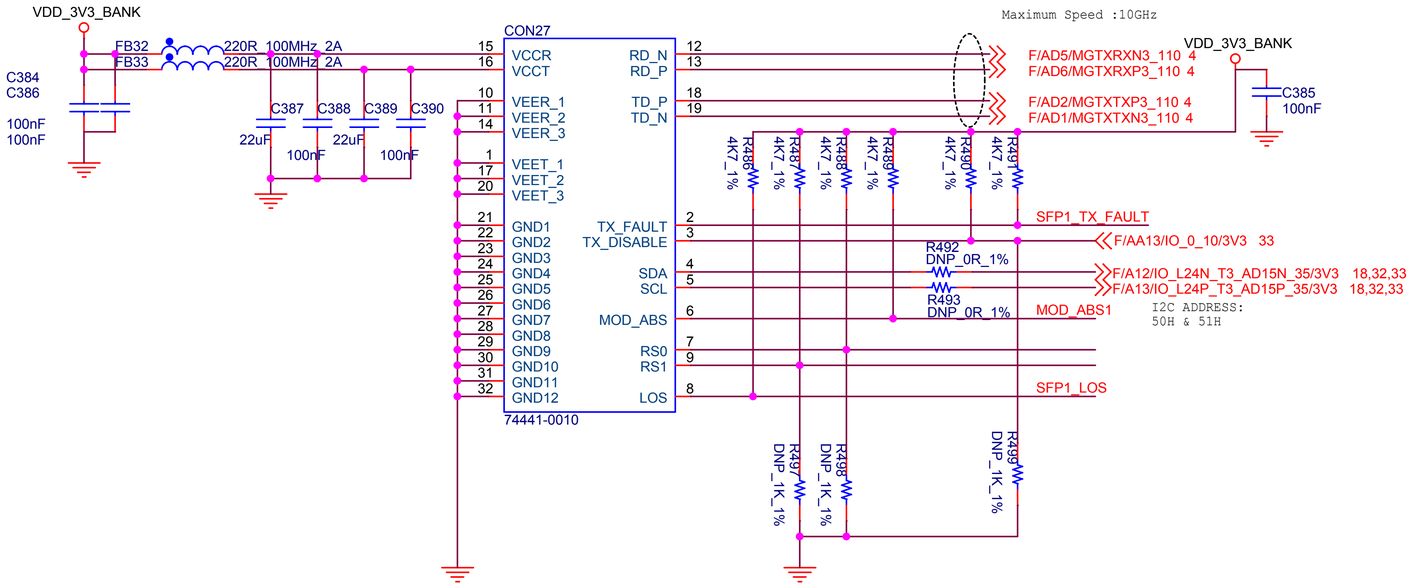
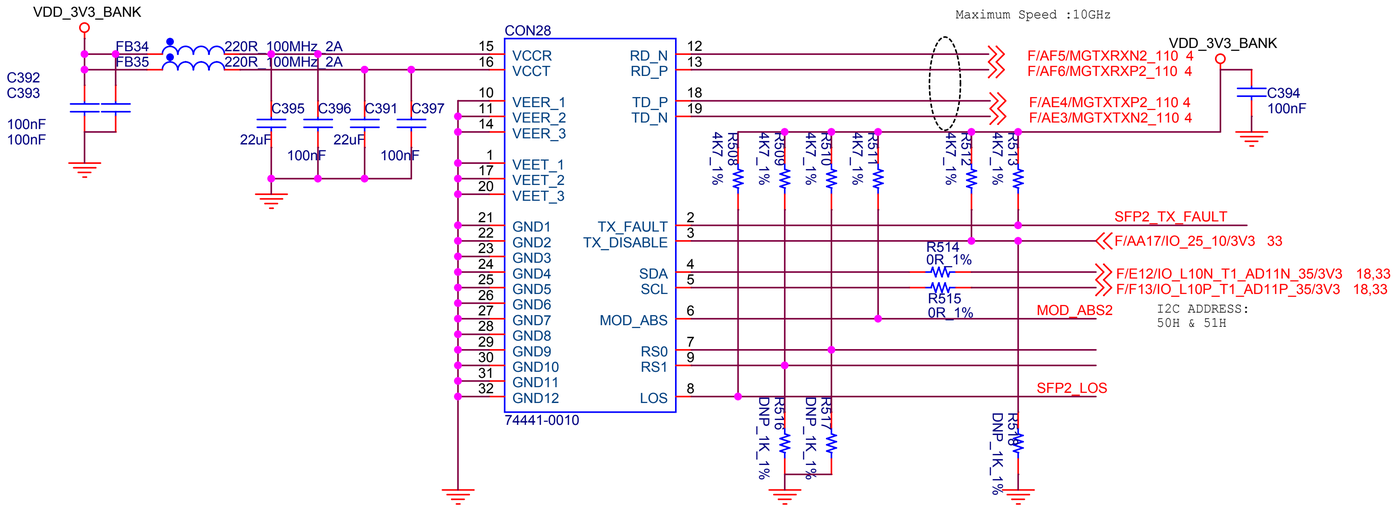
SFP+

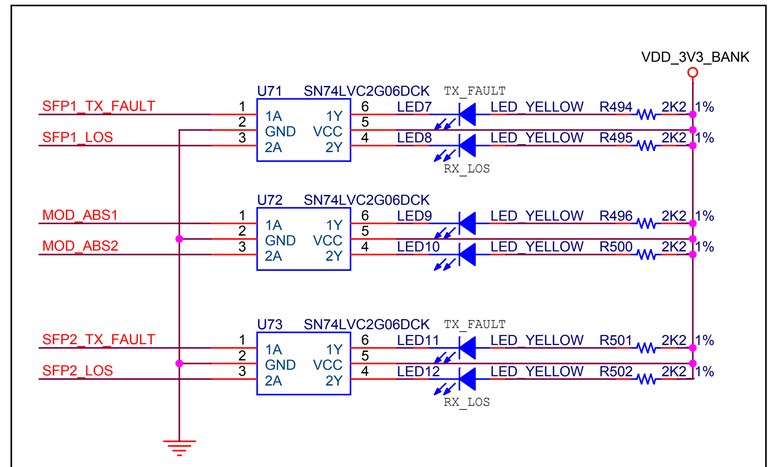




Data speed:10Gbps

Layout Note:

Signal ends P/N routing with 100ohm differentialimpedance,need to the same length with ±2mil;



MODULE STATE	IO STATE	LED STATE
TX_FAULT Nomal Operation	TX_FAULT=1 TX_FAULT=0	ON OFF
RX_LOS & Module Absent Nomal Operation	RX_LOS=1 RX_LOS=0	ON OFF

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USB HOST

Data speed:480Mbps

Layout Note:
ULPI trace need to the same length in group with ±50mil.

All the single trace impedence is 50 ohm.

VDD_5V_MAIN — FB36 220R_100MHz_2A — VDD_5V_USB; C402 100nF

VDD_5V_MAIN: C403 4.7uF, C404 470nF

VDD_5V_MAIN — R284 1K_1% — VDD_5V_USBVBUS

VDD_1V8_BANK: C398 100nF, C399 10uF

VDD_1V8_BANK: C400 100nF, C401 10uF

VDD_5V_USBVBUS: C694 100nF

VDD_1V8_BANK

U74 USB3320C-EZK

32	VDDIO	RESETB	27 — R519 0R_1% — USB_PHY_RSTn
4 F/L18/PS_MIO30_501/USB0_STP/1V8	29 STP	VBAT	21 — C405 2.2uF — VDD_5V_USB
4 F/H21/PS_MIO31_501/USB0_NXT/1V8	2 NXT	VDD33	20
4 F/H22/PS_MIO29_501/USB0_DIR/1V8	31 DIR	VDD18_1	30
		VDD18_2	28 — VDD_1V8_BANK
4 F/H17/PS_MIO36_501/USB0_CLK/1V8	R520 22R_1% 1 CLKOUT	VBUS	22 — VDD_5V_USBVBUS
		CPEN	17 — 90ohm differential impedance
4 F/K17/PS_MIO32_501/USB0_DATA0/1V8	3 DATA0	DM	19 — USB0_DM 29
4 F/G22/PS_MIO33_501/USB0_DATA1/1V8	4 DATA1	DP	18 — USB0_DP 29
4 F/K18/PS_MIO34_501/USB0_DATA2/1V8	5 DATA2		
4 F/G21/PS_MIO35_501/USB0_DATA3/1V8	6 DATA3	ID	23 — 0R_1% R285
4 F/L17/PS_MIO28_501/USB0_DATA4/1V8	7 DATA4		
4 F/B21/PS_MIO37_501/USB0_DATA5/1V8	9 DATA5	SPL_L	15 — Default Host: Connect to GND
4 F/A20/PS_MIO38_501/USB0_DATA6/1V8	10 DATA6	SPK_R	16 — Device: Connect to Power
4 F/F18/PS_MIO39_501/USB0_DATA7/1V8	13 DATA7		
		REFCLK	26
R522 8K06_1% 24	RBIAS	XO	25 — VDD_1V8_ZYNQ_PL — R523 1M_1% — Y1 7M24000036 — C406 20pF, C407 20pF
	12 NC	REFSEL0	8 — R524 0R_1%
	33 GND	REFSEL1	11 — R525 0R_1%
		REFSEL2	14 — R526 0R_1%

VDD_3V3_BANK

U38 GL852GT-MNG

100nF C211, 100nF C212, 100nF C213, 100nF C214	34 DVDD	DP4	22 — HUB_USB4_DP
	38 DVDD	DM4	21 — HUB_USB4_DM
R286 10K_1%	44 SEL27#	DP3	18 — HUB_USB3_DP
R287 10K_1%	25 SEL48#	DM3	17 — HUB_USB3_DM
FB15 220R_100MHz_2A		DP2	10 — HUB_USB2_DP
22uF C215, 100nF C216, 100nF C217, 100nF C218, 100nF C219	1 AVDD	DM2	9 — HUB_USB2_DM
	7 AVDD	DP1	6 — HUB_USB1_DP
	12 AVDD	DM1	5 — HUB_USB1_DM
	16 AVDD		90 ohm differential impedance
	19 AVDD		
90 ohm differential impedance			
4,19,20,22,23,24,29,31 F/D21/PS_POR_B_500/3V3 — R288 0R_1%	26 RESET#	OVCUR4#	28 — R289 10K_1%
29 USB0_DM	3 DM0	OVCUR3#	30 — R290 10K_1%
29 USB0_DP	4 DP0	OVCUR2#	40 — R291 10K_1%
		OVCUR1#	42 — R292 10K_1%
C220 22pF — Y4 NC/NC0 — R294 1M_1% — C221 22pF — CJ13-120001220B30	R293 680R_1% 11 RREF	PWREN4#	29
		PWREN3#	31
	14 X1	PWREN2#	41
		PWREN1#	43
	15 X2	PGREEN4	23
		PGREEN3	32
		PGREEN2	35
		PGREEN1	45
TP26	47 V5	PAMBER4	24
TP27	48 V33	PAMBER3	33
		PAMBER2	36
		PAMBER1	46
VDD_3V3_BANK — R296 10K_1% — R297 DNP_10K_1%	R295 100K_1% 39 PGANG	AGND	20
	37 PSELF	AGND	13
		AGND	8
	27 TEST	AGND	2

VDD_5V_MAIN — FB14 220R_100MHz_2A — VDD_5V_HUB; C205 22uF, C206 22uF, C207 100nF

VDD_5V_HUB: C208 22uF, C209 22uF, C210 100nF

VDD_5V_HUB — U39 PRTR5V0U2X: 4 — HUB_USB1_DP 3, 2 — HUB_USB1_DM

VDD_5V_HUB — U40 PRTR5V0U2X: 4 — HUB_USB2_DP 3, 2 — HUB_USB2_DM

VDD_5V_HUB — U41 PRTR5V0U2X: 4 — HUB_USB3_DP 3, 2 — HUB_USB3_DM

VDD_5V_HUB — U42 PRTR5V0U2X: 4 — HUB_USB4_DP 3, 2 — HUB_USB4_DM

CON12 DOUBLE_USB_A_TYPE

4	4, 8
HUB_USB1_DP	3, 7
HUB_USB2_DP	
HUB_USB1_DM	2, 6
HUB_USB2_DM	
VDD_5V_HUB	1, 5
	9, 10, 11, 12

CON13 DOUBLE_USB_A_TYPE

4	4, 8
HUB_USB3_DP	3, 7
HUB_USB4_DP	
HUB_USB3_DM	2, 6
HUB_USB4_DM	
VDD_5V_HUB	1, 5
	9, 10, 11, 12

VDD_3V3_BANK VDD_1V8_BANK

C756 10pF

R676 100K_1%

U96 SN74LVC1G07DCK

4,19,20,22,23,24,29,31 F/D21/PS_POR_B_500/3V3 — 2 — 4 — USB_PHY_RSTn

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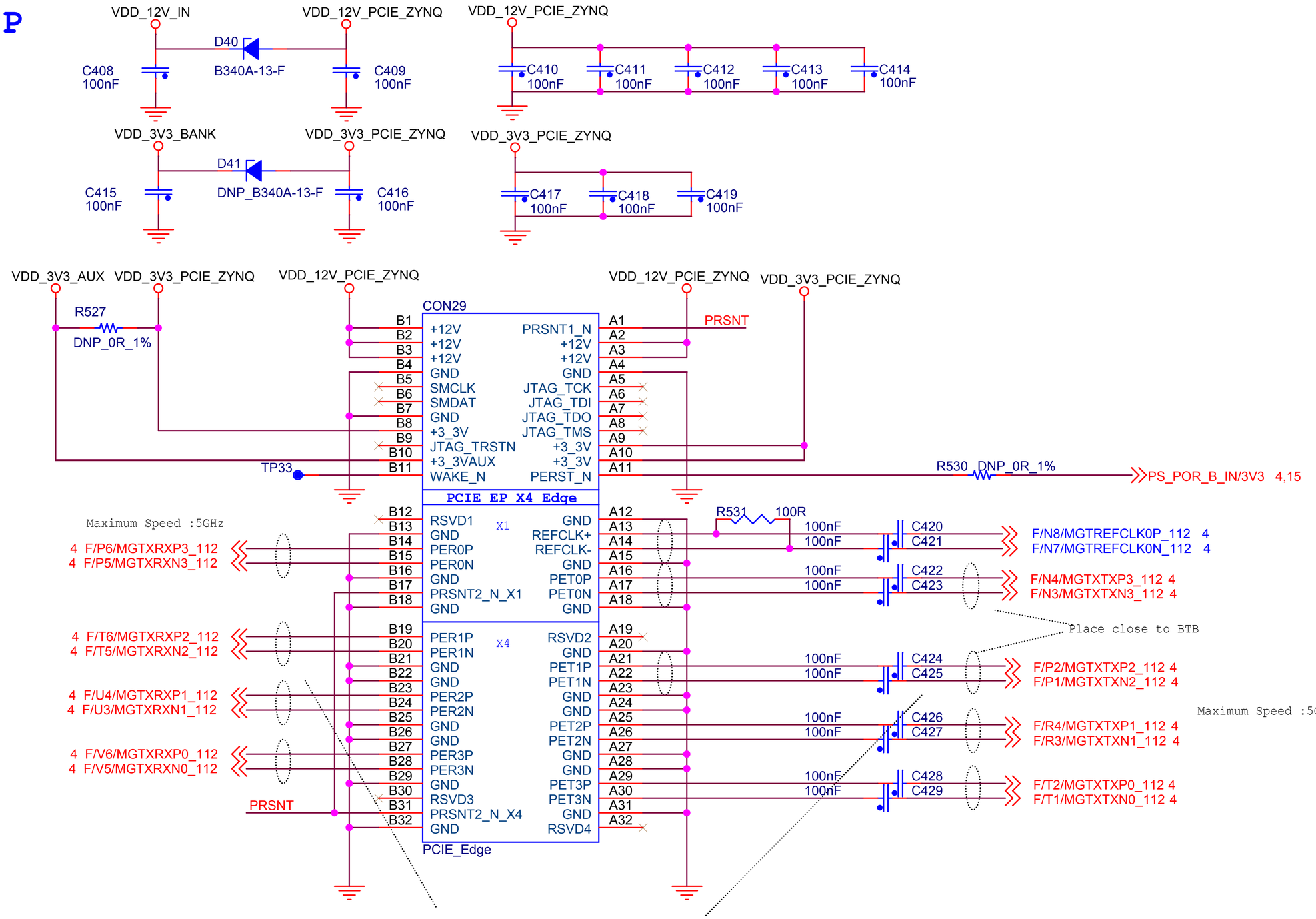
ZYNQ PCIE EP



PCIE_X
100 Ω (±10%) differential impedance
Keep trace length as short as possible

Data speed:5Gbaud/Lane

Layout Note:

1. Data signal ends P/N routing with 100ohm differentialimpedance,need to the same length with ±1mil;
2. AC coupling CAP should be placed close to Connector

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Title	ZYNQ_PCIE_EP
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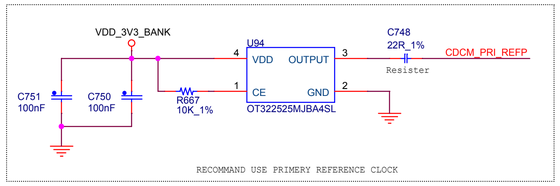
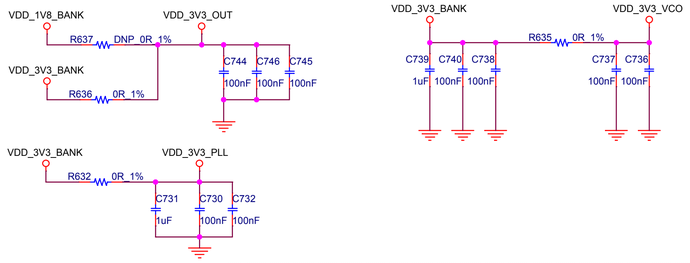
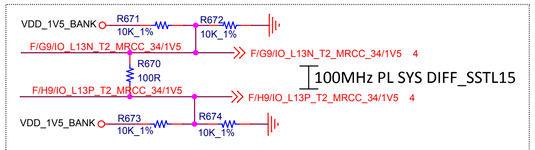
ZYNQ REF CLOCK

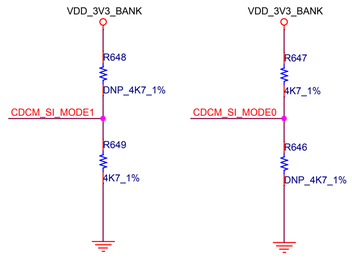






Layout Note:
Signal ends P/N routing with 100 ohm differential impedance

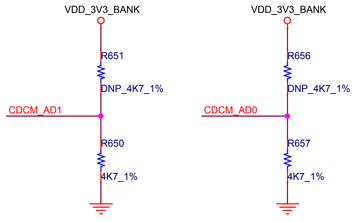
MODE SELECTION



MODE Configuration

SI_MODE[1:0]	*MODE*
00	SPI
01	I2C
10	Pin Mode

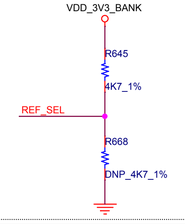
I2C ADDRESS OFFSET



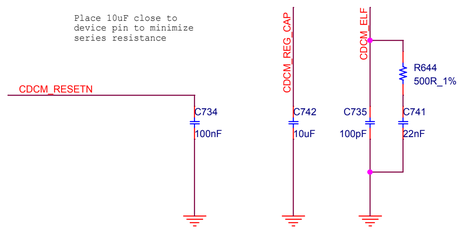
I2C ADDRESS:
1010100(54H)

The device slave address is 10101xx(the two LSBs are determined by the AD1 and AD0 pins). The five MSBs are hard-wired, while the two LSBs are set through pins on device power up.

REF_SEL Configuration



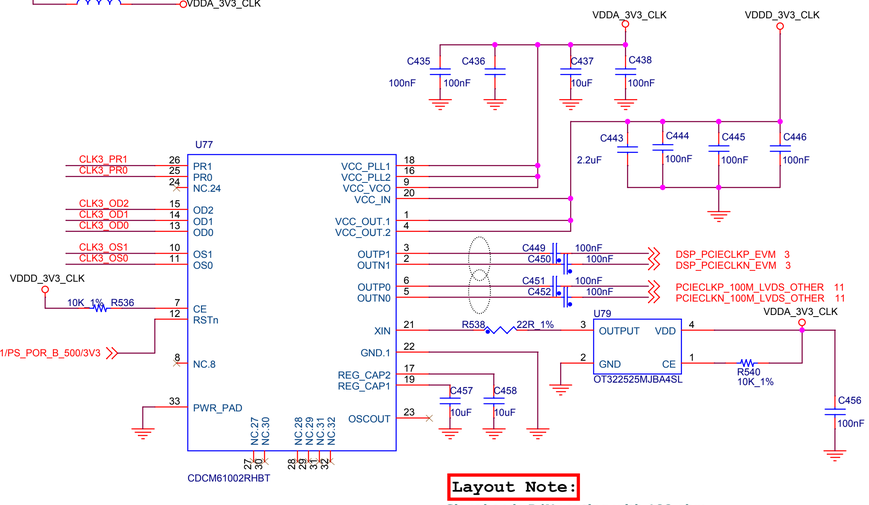
SI_MODE1 PIN NO. 47	REGISTER 4 BIT 13 SMUX_MODE_SEL	REGISTER 4 BIT 12 SMUX_REF_SEL	REF_SEL PIN NO. 6	SELECTED INPUT	
0 (SPI/I2C mode)	0	X	X	Auto Select Priority is given to Primary Reference input.	
	1	0	1	Primary input	input select through SPI/I²C
		1		Secondary input	
		1	0	Primary input	input select through external pin
			1	Secondary input	
1 (pin mode)	not available		0	Primary or Auto (see Table 6)	
			1	Secondary or Auto (see Table 6)	



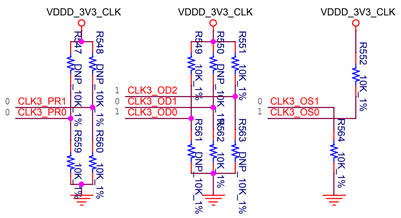
Default output

CHANNEL	*Frequency(MHz)*	*Type*
Y0	156.25	CML
Y1	156.25	CML
Y2	125.00	LVDS
Y3	125.00	LVDS
Y4	66.66	LVDS
Y5	66.66	LVDS
Y6	100.00	LVDS
Y7	100.00	LVDS

DSP PCIE REFCLK

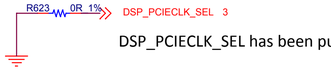


Layout Note:
Signal ends P/N routing with 100 ohm differential impedance



100M_CLK Configuration

SET Bit	*Value (100MHz)*	*Description*
PR 1:0	00	Prescaler Divider:3 | Feedback Divider:24
OD 2:0	101	Output Divider:6
OS 1:0	01	LVDS | OSC_OUT Off



DSP_PCIECLK_SEL has been pulled up on the SOM

DSP_PCIECLK_SEL

DSP_PCIECLK_SEL	*OPTION*
0	PCIe reference clock provided by EVM
1	PCIe reference clock provided by SOM

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Title: ZYNQ_SYS_CLK

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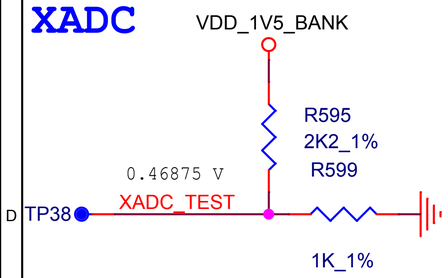
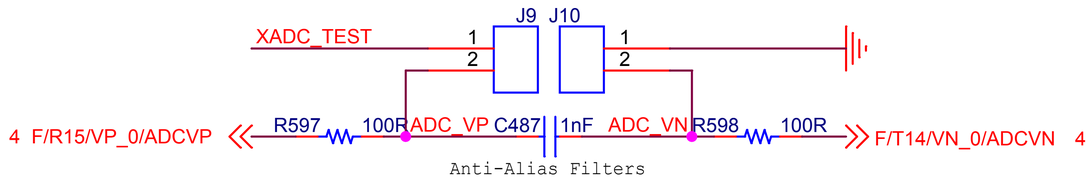
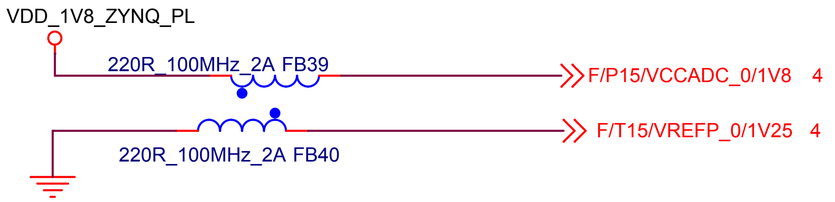
XADC

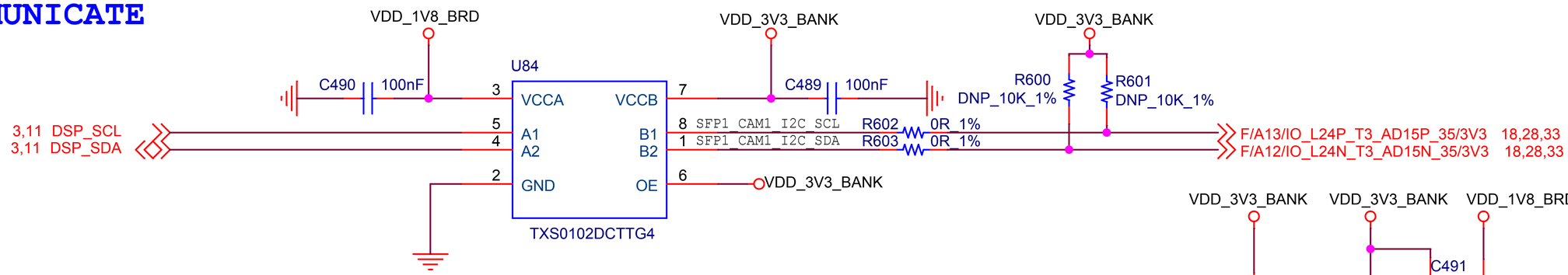


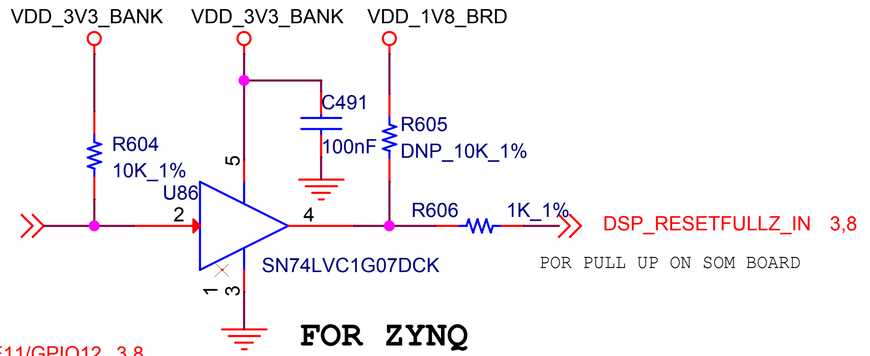
XADC Input Voltage Range is 0~1V or -0.5V~0.5V

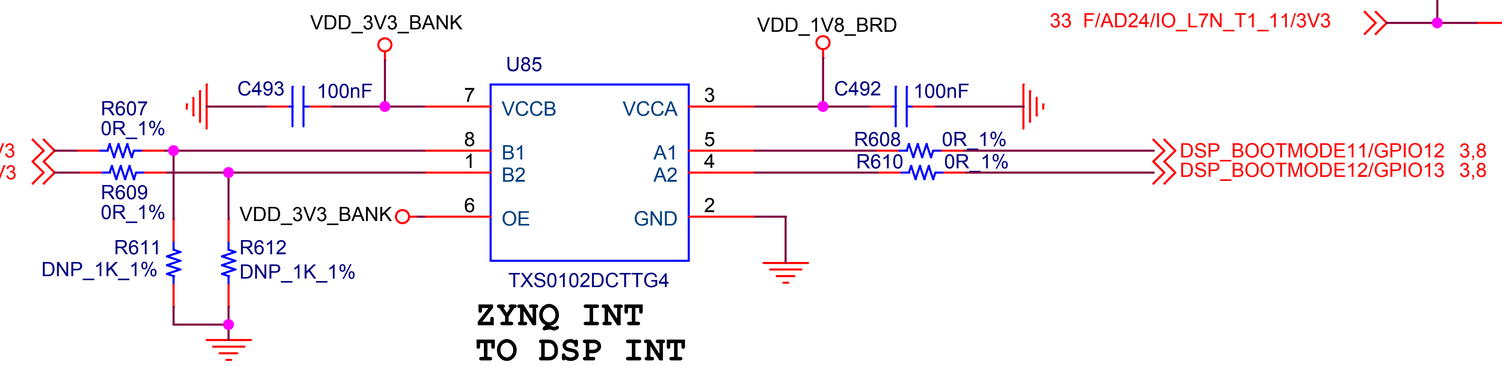




COMMUNICATE







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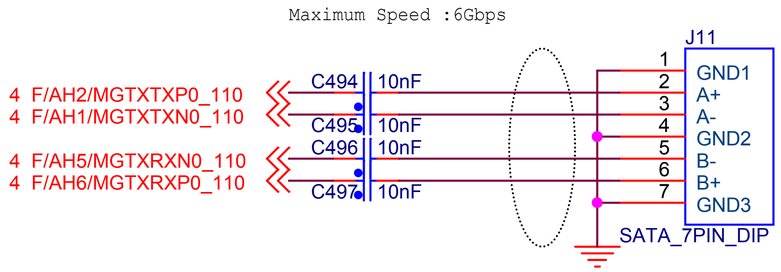

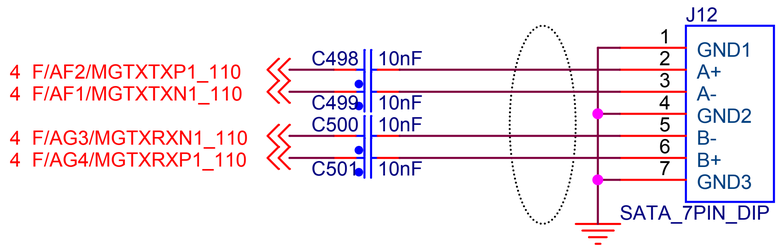

Data speed:6Gbps

Layout Note:

1.Signal ends +/- routing with 100ohm differential impedance,need to the same length with ±1mil;
2.AC coupling CAP should be placed close to connector

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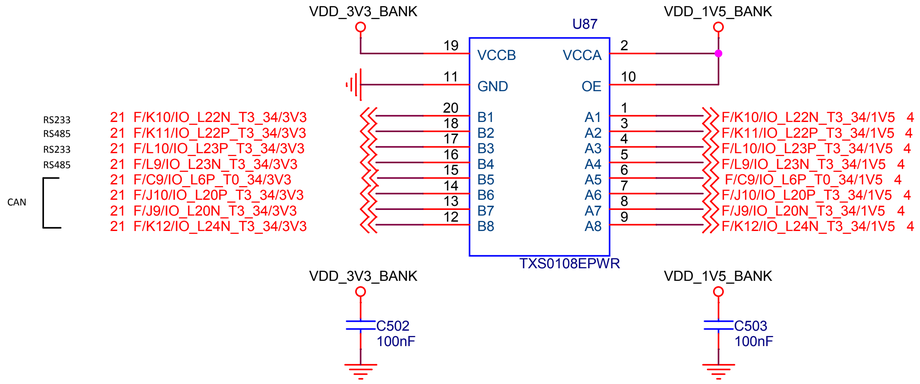
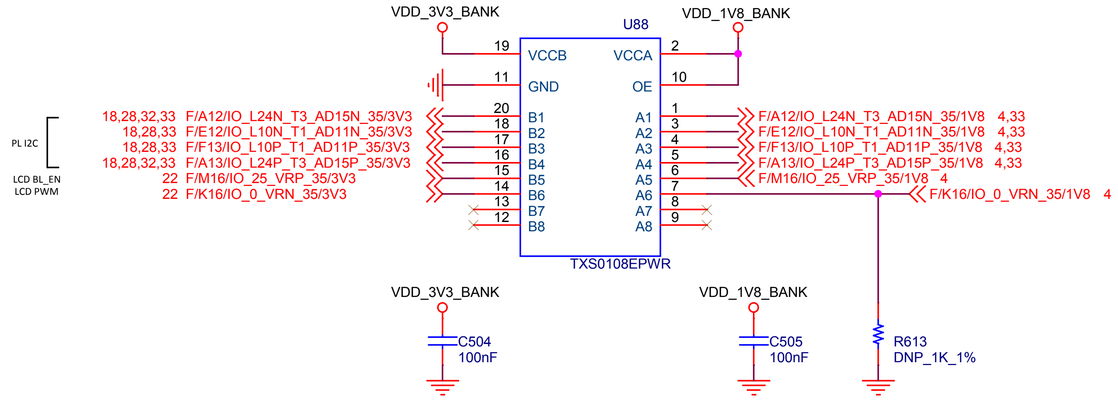
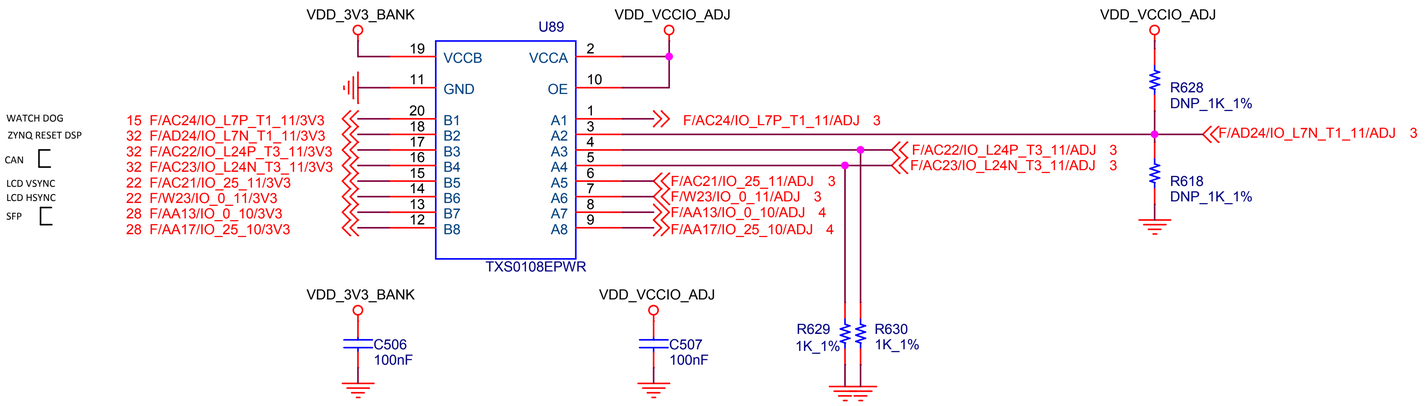
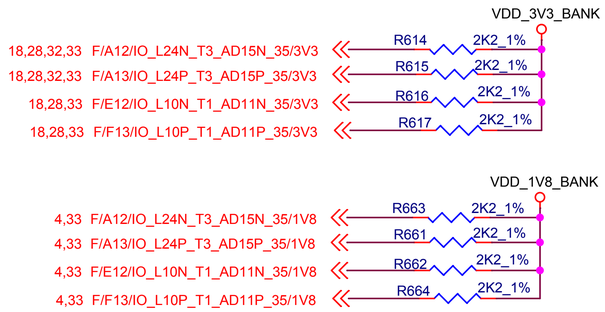
LEVEL SHIFTER









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