



University of California  
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Thursday, December 14, 2017.

8:00-11:00am

EE140/240A—Fall 2017: Final Exam

<b>NAME</b>	Last	First
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<b>GRAD/UNDERGRAD</b>	
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**Problem 1:** / 14

**Problem 2:** / 24 (28)

**Problem 3:** / 12

**Problem 4:** / 16

**Problem 5:** / 11 (17)

**Total:** / 77 (87)

### Problem 1 (14 pts)

You've landed your dream job as an analog design engineer at Keysight! Because of your design experience from EE140/240A, you are tasked with designing a low-power two-stage amplifier to drive a large capacitive load. However, you're working with short-channel devices that can't really be modeled with square-law I-V characteristics. After running some simulations, you find that the following short-channel device model gives a reasonable approximation of the I-V characteristics of the MOSFETs in your design kit:

$$I_D = k' \frac{W}{L} (|V_{GS}| - |V_{TH}|) V_{d,sat} (1 + \lambda V_{DS})$$

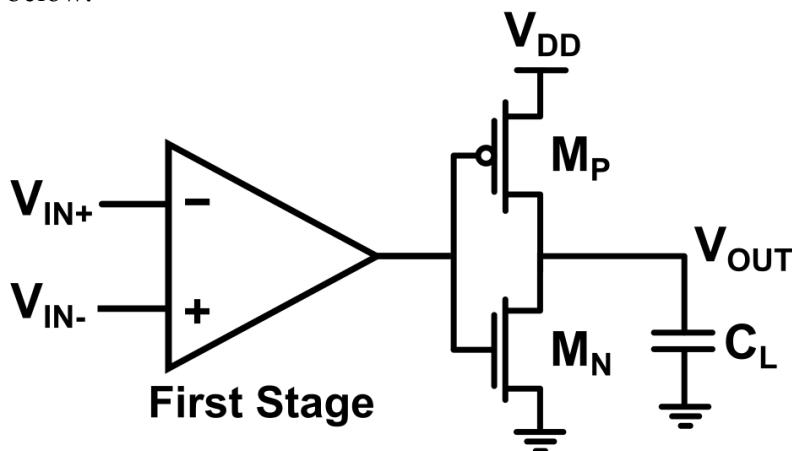
You have found that  $k'_N = 2k'_P$ ,  $|V_{TH,P}| = |V_{TH,N}|$ ,  $V_{d,satP} = V_{d,satN}$ , and  $\lambda_P = 2\lambda_N$ . Note that  $V_{d,sat}$  is a constant parameter. You may ignore any subthreshold effects for this problem unless told otherwise (e.g., assume that if  $|V_{GS}| < |V_{TH}|$ ,  $I_D = 0 A$ ).

- a) (2 points) What is the minimum current required to drive a load of  $C_L$  the full output swing of  $V_{sw,out}$  in  $t_{settle}$  seconds? Express your answer in terms of these parameters. You may assume the amplifier is slewing the entire time.

Because we know that  $I=C\Delta V/\Delta t$ :

$$I_{min} = C_L \left( \frac{V_{sw,out}}{t_{settle}} \right)$$

- b) (5 points) To improve your settling time, you initially try to use an inverter for the output stage, as illustrated below.



- i. (1 point) What is the ratio between  $W_N$  and  $W_P$  needed to guarantee that output stage has equal rising and falling edge drive current? Assume that the output of the first stage is biased around  $\frac{V_{DD}}{2}$  and that  $L_P = L_N = L$ .

To ensure that the rising and falling edge drive strength is equal,  $k'_P \frac{W_P}{L}$  must equal  $k'_N \frac{W_N}{L}$ . Since  $k'_N = 2k'_P$ , we know that  $W_P = 2W_N$ , so  $W_N/W_P = 0.5$ .

- ii. (4 points) Assuming  $W_N/W_P$  is chosen appropriately, what choice of  $W_P$  is needed to provide a peak drive current of  $I_{pk}$  if the peak output swing of the first stage is  $V_{SW}$  (so that the output of the first stage swings between  $\frac{V_{DD}}{2} + V_{SW}$  and  $\frac{V_{DD}}{2} - V_{SW}$ )? Express your answer in terms of device parameters,  $I_{pk}$ ,  $V_{sw}$ , and  $V_{DD}$ . You may assume that  $V_{sw} < \frac{V_{DD}}{2} - V_{TH}$  and that  $\frac{V_{DD}}{2} > V_{TH}$ .

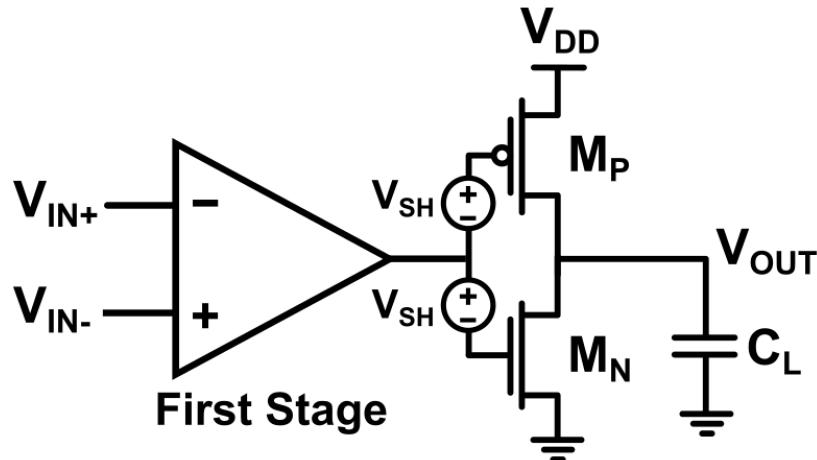
We can solve for the width that sets the peak drive current to  $I_{pk}$  (note:  $V_{S1}$  is the DC output voltage of the first stage):

$$\begin{aligned} I_{pk} &= I_P - I_N \\ I_{pk} &= k'_P \left( \frac{W_P}{L} \right) (V_{GS,P} - V_{TH,P}) V_{d,satP} - k'_N \left( \frac{W_N}{L} \right) (V_{GS,N} - V_{TH,N}) V_{d,satN} \\ I_{pk} &= k'_P \left( \frac{W_P}{L} \right) (V_{DD} - (V_{S1} - V_{sw}) - V_{TH,P}) V_{d,satP} - 2k'_P \left( \frac{\alpha W_P}{L} \right) (V_{S1} - V_{sw} - V_{TH,P}) V_{d,satP} \\ I_{pk} &= k'_P V_{d,satP} \frac{W_P}{L} \left( \left( \frac{V_{DD}}{2} + V_{sw} - V_{TH,P} \right) - 2\alpha \left( \frac{V_{DD}}{2} - V_{sw} - V_{TH,P} \right) \right) \end{aligned}$$

If the NMOS and PMOS drive strengths are equal,  $2\alpha = 1$  and the expression simplifies to:

$$\begin{aligned} I_{pk} &= k'_P V_{d,satP} \frac{W_P}{L} (2 V_{sw}) \\ W_P &= \frac{I_{pk} L}{k'_P V_{d,satP} (2 V_{sw})} \end{aligned}$$

- c) (3 points) To lower the quiescent current, you introduce the level shifters shown below.



- i. (1 point) What choice of  $V_{SH}$  will lower the nominal quiescent current to 0 A (still using the simplified short-channel I-V model)? Assume that one device should always be on if  $V_{sw} > 0 V$ .

In the model shown above,  $V_{SH}$  should be chosen to keep  $|V_{GS}| - |V_{TH}|$  at exactly 0 V. Because  $|V_{GS}| = \frac{V_{DD}}{2} - V_{SH}$ , this means that  $\frac{V_{DD}}{2} - V_{SH} = |V_{TH}|$  and  $V_{SH} = \frac{V_{DD}}{2} - V_{TH}$ .

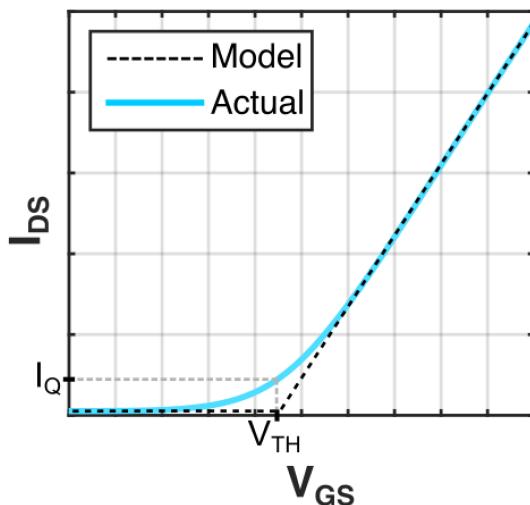
- ii. (2 points) Will introducing the level shifters cause  $W_P$  (and  $W_N$ ) to increase, stay the same, or decrease if  $I_{pk}$ ,  $V_{sw}$  and  $V_{DD}$  are fixed? Explain your answer. All assumptions described in part (b) apply to this problem.

**Circle one:**      Increase      Stay the same      Decrease

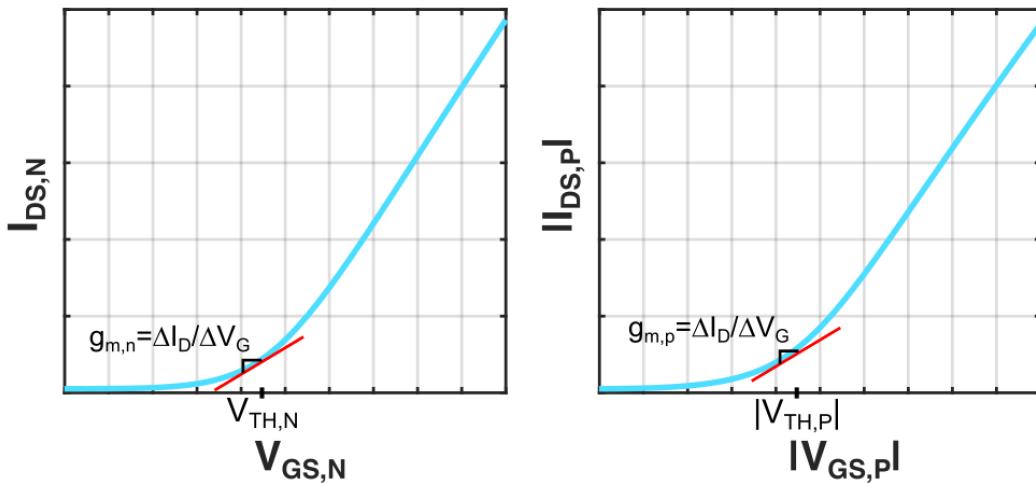
**Explanation:**

Because the overdrive voltage of both devices is smaller, the required device W/L ratio should increase to compensate.

- d) (4 points) Due to subthreshold operation, the actual  $I_{DS}$  vs.  $V_{GS}$  characteristic of the devices looks more like the following, so the level-shifted output stage actually draws some nonzero (but small) quiescent current  $I_Q$  that the simplified model presented at the beginning of the problem does not capture.

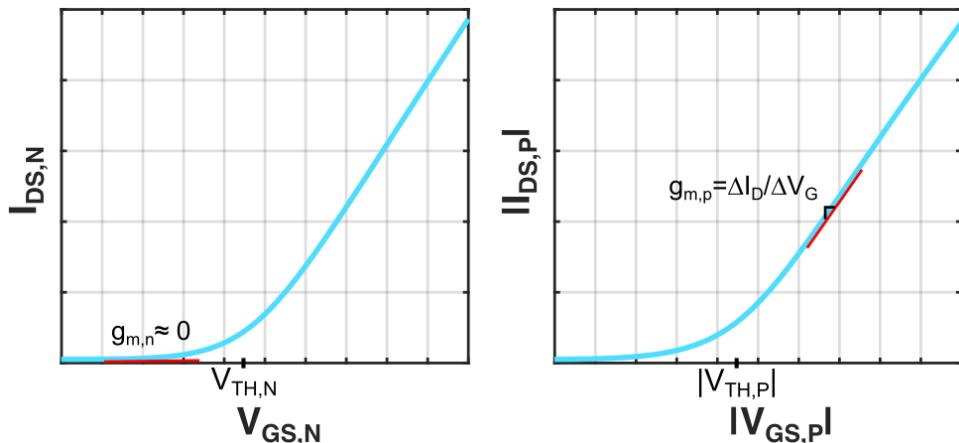


- i. (2 points) Using the provided plot of PMOS and NMOS  $|I_D|$  vs.  $|V_{GS}|$ , briefly explain how you would calculate the effective transconductance of the output stage in (c) when a very very small input step is applied. Feel free to sketch on the plots.



Because the output stage is biased around the threshold voltage of both devices, the overall transconductance will be the combination of the sum of the PMOS and NMOS transconductances calculated from the slopes marked above.

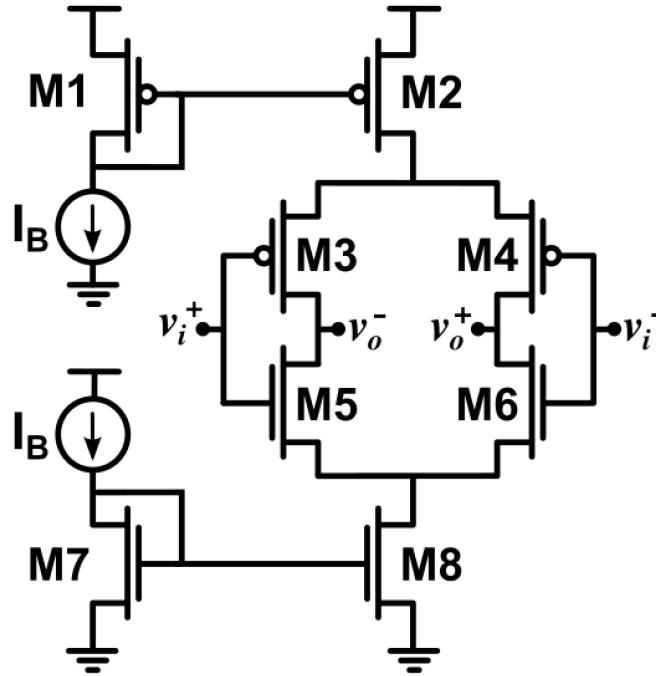
- ii. (2 points) Now explain how you would calculate the transconductance of the same circuit when a very large positive input step is applied to the input of the first stage ( $V_{IN+} > V_{IN-}$  in the diagrams from parts (b) and (c)). Again, feel free to sketch on the plots.



With a large positive input step, the input to the output stage will drop. This will make the PMOS  $V_{GS}$  large but the NMOS  $V_{GS}$  small. As a result, the overall transconductance in this case will be set by the  $g_m$  of this PMOS device (the NMOS device will not contribute). The PMOS  $g_m$  will be set by the linear slope of the I-V curve marked above.

**Problem 2 (24, 28 pts)**

You are taking EE 240B, and designing your final project with a partner, Anna Logue. As part of your project, you need to design a low-power 2-stage op-amp and Anna suggests the topology shown below.



Assume  $(W/L)_2 = 2(W/L)_1$ ;  $(W/L)_3 = (W/L)_4$ ;  $(W/L)_5 = (W/L)_6$ ;  $(W/L)_8 = 2(W/L)_7$ . You may assume all devices exhibit square-law behavior.

- a) (2 pts) Assume all devices are in saturation. Compute  $I_{D2}$  and  $I_{D3}$  in terms of  $I_B$ . Ignore  $V_{ds}$  mismatch between M1 and M2.

Because  $(W/L)_2 = 2(W/L)_1$ ,  $I_{D2}=2I_B$ .

Because  $(W/L)_3 = (W/L)_4$ , the bias current of  $2I_B$  splits evenly between M3 and M4, and  $I_{D3}=I_B$ .

- b) (2 pts) Compute  $\Delta V_3$  and  $\Delta V_2$  in terms of  $I_B$ , device sizes, and  $\Delta V_1$ . (note:  $\Delta V = V^* - v_{ov}$ )

Because the gate of M1 and M2 are connected,  $\Delta V_2=\Delta V_1$ .

In order for the drain current of M1 and M3 to be equal:

$$\begin{aligned} I_{D1} &= I_{D3} \\ \frac{1}{2} \mu C_{ox} \left( \frac{W}{L} \right)_1 \Delta V_1^2 &= \frac{1}{2} \mu C_{ox} \left( \frac{W}{L} \right)_3 \Delta V_3^2 \\ \left( \frac{W}{L} \right)_1 / \left( \frac{W}{L} \right)_3 &= \frac{\Delta V_3^2}{\Delta V_1^2} \\ \Delta V_3 &= \Delta V_1 \sqrt{\frac{\left( \frac{W}{L} \right)_1}{\left( \frac{W}{L} \right)_3}} \end{aligned}$$

- c) (4 pts) Compute the maximum and the minimum common-mode input voltage for normal operation of this circuit. Your answer should be in terms of  $V_{ThN}$ ,  $V_{ThP}$ , and  $\Delta V_M$  (where M=device number).

To remain in saturation,  $|V_{DS2}| \geq \Delta V_2$ . We rewrite this  $V_{DS}$ :

$$|V_{DS2}| = V_{S2} - V_{D2} = V_{DD} - (V_{CM} + |V_{GS3}|) = V_{DD} - (V_{CM} + \Delta V_{3/4} + V_{THP})$$

Rearranging for the case where  $|V_{DS2}| = \Delta V_2$ , we can find the maximum allowable  $V_{CM}$ :

$$\begin{aligned}\Delta V_2 &= V_{DD} - (V_{CM,max} + \Delta V_{3/4} + V_{THP}) \\ -(\Delta V_2 - V_{DD}) &= V_{CM,max} + \Delta V_{3/4} + V_{THP} \\ V_{DD} - \Delta V_2 - \Delta V_{3/4} - V_{THP} &= V_{CM,max}\end{aligned}$$

We can perform similar analysis to solve for  $V_{CM,min}$ :

$$V_{CM,min} = \Delta V_8 + \Delta V_{5/6} + V_{THN}$$

- d) (4 pts) Compute the maximum peak-to-peak differential output swing in terms of  $V_{CM}$ ,  $V_{ThN}$ ,  $V_{ThP}$ , and  $\Delta V_M$ .

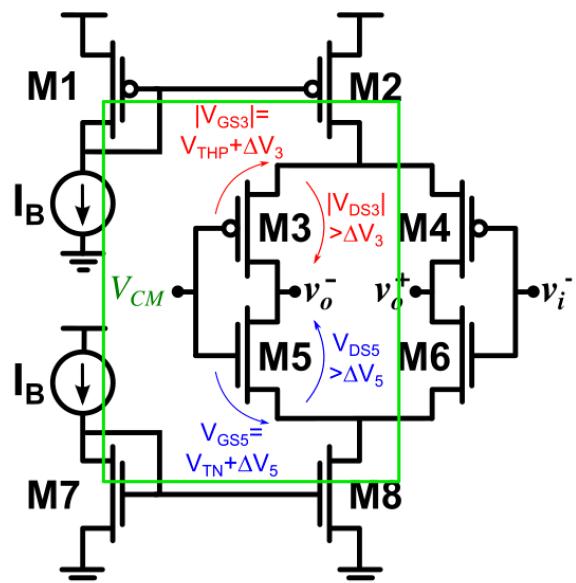
For a given  $V_{CM}$ , the maximum output voltage on a single side can be calculated by tracing the required  $V_{GS}$  and  $V_{DS}$  drops to keep the input devices in saturation. The maximum output is:

$$\begin{aligned}V_{o,max} &= V_{CM} + (V_{THP} + \Delta V_3) - \Delta V_3 \\ &= V_{CM} + V_{THP}\end{aligned}$$

The minimum output is:

$$\begin{aligned}V_{o,min} &= V_{CM} - (V_{THN} + \Delta V_5) + \Delta V_5 \\ &= V_{CM} - V_{THN}\end{aligned}$$

This makes the maximum single-ended swing  $V_{o,max} - V_{o,min} = V_{THP} + V_{THN}$ . To get the peak-to-peak differential swing, this has to be doubled, so the swing is  $2(V_{THP} + V_{THN})$ .



For the following parts (e-h) your answers should be in terms of small-signal device parameters, (e.g.  $g_{mnM}$ ,  $g_{mpM}$ ,  $r_{onM}$ ,  $r_{opM}$ ,  $g_{mbnM}$ ,  $g_{mbpM}$ , where M=device number.)

- e) (4 pts) Compute the differential short-circuit output transconductance of the circuit,  $G_m$ , and the differential circuit output resistance  $R_o$ .

The effective  $G_m$  is given by the sum of all input device transconductances divided by two to account for measuring the output signal differentially:

$$G_M = \frac{g_{mp3} + g_{mp4} + g_{mn5} + g_{mn6}}{2}$$

The effective  $R_o$  is given by the sum of the output resistances on each side of the amplifier:

$$R_o = (r_{op3} || r_{on5})$$

- f) (4 pts) Compute the gain from the power supply (positive rail) to the differential output of the amplifier,  $A_{V_{DD}-dm,out}$ . What is the corresponding power supply rejection ratio ( $PSRR = A_{dm,in-dm,out}/A_{V_{DD}-dm,out}$ ) of the circuit?

If there is no mismatch, the gain from  $V_{DD}$  to the differential output will be 0, since there is no differential component to the power supply signal.

**Because  $A_{V_{DD}-dm,out} = 0$ , the PSRR will be infinite.**

- g) (4 pts) Name one advantage and one disadvantage of this circuit over an ordinary differential pair with an active load. While there are many possible answers, try to pick the ones you think are the most important considerations for using this circuit as the first stage in a 2-stage op-amp design.

**Advantage:**

This topology improves the achievable  $G_m/I_D$  of the input stage, which enables the amplifier to operate faster (higher achievable unity-gain frequency) and improves the noise performance for the same amount of power dissipation.

**Disadvantage:**

This topology reduces the allowable input  $V_{CM}$  range. It also reduces the output swing of the stage. Furthermore, mismatches between the upper and lower current sources have significant effect on the bias voltages of the circuit; therefore common-mode feedback is typically required for these circuits.

- h) (4 pts) **EE240A only:** How does this topology impact input-referred noise compared to a diff pair with active load? Be quantitative in your answer.

*In a conventional NMOS-input differential pair, the total current noise generated will be proportional to the sum of the transconductance of the PMOS load and NMOS input devices:*

$$\overline{i_{n,tot}^2} \propto g_{mN} + g_{mP}$$

In calculating the input-referred noise,  $\overline{i_{n,tot}^2}$  would be divided by the  $g_m$  of the input devices:

$$\overline{v_{n,in}^2} \propto \frac{g_{mN} + g_{mP}}{g_{mN}^2}$$

The total noise of this amplifier topology would be the same, but the effective  $G_m$  used to calculate the input-referred noise will now be the sum of NMOS and PMOS transconductances:

$$\overline{v_{n,in,new}^2} \propto \frac{g_{mN} + g_{mP}}{(g_{mN} + g_{mP})^2}$$

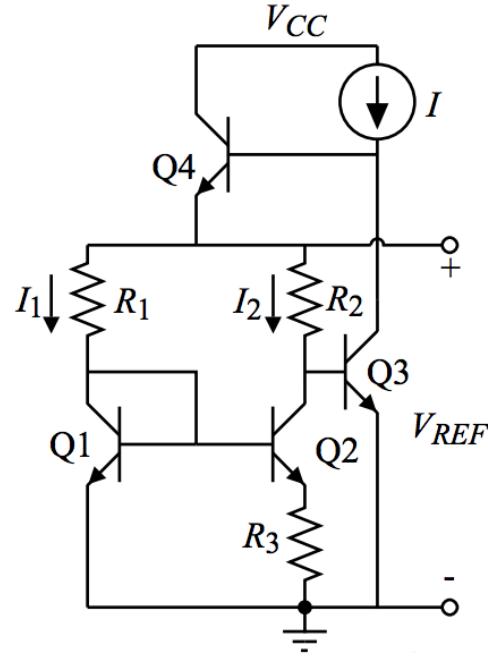
**Therefore, the reduction in noise will be given by:**

$$\frac{g_{mN}^2}{(g_{mN} + g_{mP})^2}$$

Generally, the improved  $G_m/I_d$  improves the noise performance.

**Problem 3 (12 pts)**

The circuit below is called a Widlar Bandgap Voltage Reference. Neglect the Early effect.



- a) (4 pts) Compute the voltage drop across  $R_3$  ( $V_{R3}$ ) in terms of BJT device parameters and the currents labeled in the circuit.

By KVL, we can see that  $V_{R3} = V_{BE1} - V_{BE2}$ . We can express the  $V_{BE}$  of a BJT in terms of its collector current and device parameters:

$$I_C = I_S e^{\frac{V_{BE}}{V_T}}$$

$$V_T \ln\left(\frac{I_C}{I_S}\right) = V_{BE}$$

Using this, we can rewrite the expression for  $V_{R3}$  in terms of device parameters and simplify:

$$V_{R3} = V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right) - V_T \ln\left(\frac{I_{C2}}{I_{S2}}\right)$$

$$V_{R3} = V_T \left( \ln\left(\frac{I_{C1}}{I_{S1}}\right) - \ln\left(\frac{I_{C2}}{I_{S2}}\right) \right)$$

$$V_{R3} = V_T \left( \ln\left(\frac{I_{C1} I_{S2}}{I_{S1} I_{C2}}\right) \right)$$

- b) (4 pts) What is the purpose of Q3?

Q3 ensures that the voltage drop across  $R_2$  is equal to the voltage drop across  $R_1$ , allowing the ratio  $I_1/I_2$  to be controlled via a ratio of resistances.

Q3 also provides the  $V_{BE}$  for  $V_{REF} = KV_t + V_{BE}$ , since  $V_{REF} = I_2 R_2 + V_{BE3}$ . This device sets the negative temperature coefficient for the circuit, making it temperature independent.

- c) (4 pts) The PTAT reference  $V_{REF} = KV_t + V_{BE}$ . Compute K in terms of device parameters and resistances in the circuit.

Assuming  $V_{BE1} \approx V_{BE3}$ , we can see that  $I_1 R_1 \approx I_2 R_2$  because the voltage drop across both resistors will be roughly equal. This means that  $I_1/I_2 \approx R_2/R_1$  and we can rewrite the result from (a) as:

$$V_{R3} = V_T \left( \ln \left( \frac{R_2}{R_1} \frac{I_{S2}}{I_{S1}} \right) \right)$$

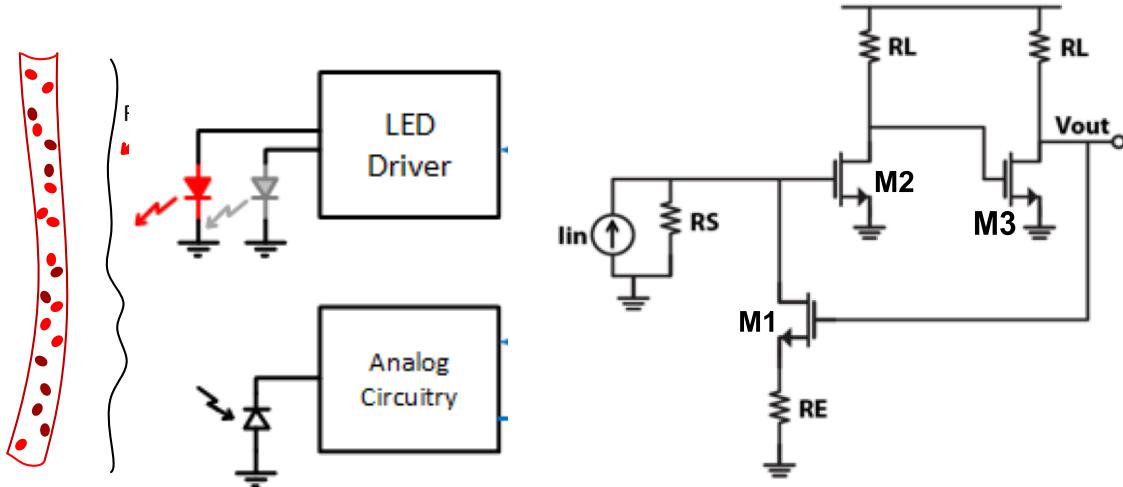
We can also see that  $V_{REF} = V_{BE3} + V_{R2} = V_{BE3} + I_2 R_2$ . Since we know (assuming  $\beta$  is large) that  $I_2 = V_{R3}/R_3$ , we can plug in the previous result to get:

$$V_{REF} = V_{BE3} + \frac{R_2}{R_3} V_T \left( \ln \left( \frac{R_2}{R_1} \frac{I_{S2}}{I_{S1}} \right) \right)$$

This is in the form we would like, with  $K = \frac{R_2}{R_3} \left( \ln \left( \frac{R_2}{R_1} \frac{I_{S2}}{I_{S1}} \right) \right)$ .

### Problem 4 (16 pts)

You are designing a readout circuit for a pulse oximeter (a non-invasive method to measure a person's oxygen saturation). The oximeter functions by shining two wavelengths of light through the body part (typically finger or earlobe) to a photodiode. The photodiode converts the unabsorbed light to a current, which can be amplified by a transimpedance amplifier (TIA). A simple TIA is shown in the figure below. A photodiode can be modeled by a current source and shunt impedance as shown below (*note: real photodiodes have significant shunt capacitance, which we are ignoring in this problem*).



The signal of interest ( $i_{in}$ ) is typically small compared to the DC value of the input current ( $I_{IN}$ ). For the problems below, do not ignore  $r_o$ , but you may ignore the body effect. Assume that  $g_m r_o$ ,  $g_m R_L$ , and  $g_m R_E$  are large,  $R_L \ll r_o$ , and  $R_S$  is very large. All transistors are identical.

- a) (2 pts) Identify the type of feedback.

Shunt-shunt feedback

- b) (4 pts) Calculate the mid-band input impedance exclusive of the source resistance  $R_S$ .

Apply Blackman's formula, cutting on M2.

$$R_{in0} = g_m r_{o1} R_E$$

$$RR_o = g_{m2} R_L g_{m3} R_L \left( \frac{g_m}{1 + g_m R_E} r_{o1} (1 + g_m R_E) \right) = (g_m R_L)^2 g_m r_o$$

$$RR_s = 0$$

$$R_{in} = \frac{g_m r_o R_E}{1 + (g_m R_L)^2 g_m r_o} \approx \frac{R_E}{(g_m R_L)^2}$$

$$R_{in} =$$

c) (4 pts) Calculate the output impedance. Do not neglect  $R_S$ .

Apply Blackman's formula, cutting on M2.

$$R_{out0} = R_L || r_{o1}$$

$$RR_o = g_{m2}R_Lg_{m3}R_L \left( \frac{g_m}{1 + g_m R_E} R_S || r_{o1}(1 + g_m R_E) \right)$$

$$RR_s = 0$$

$$R_{in} = \frac{R_L || r_{o1}}{1 + RR_o}$$

$$R_{out} =$$

d) (4 pts) Calculate the closed-loop gain  $V_{out}/I_{in}$ . You should include  $R_S$  in this calculation.

Since we already know the input impedance, we can say that:

$$V_{in} = (R_S || R_{in})I_{in}$$

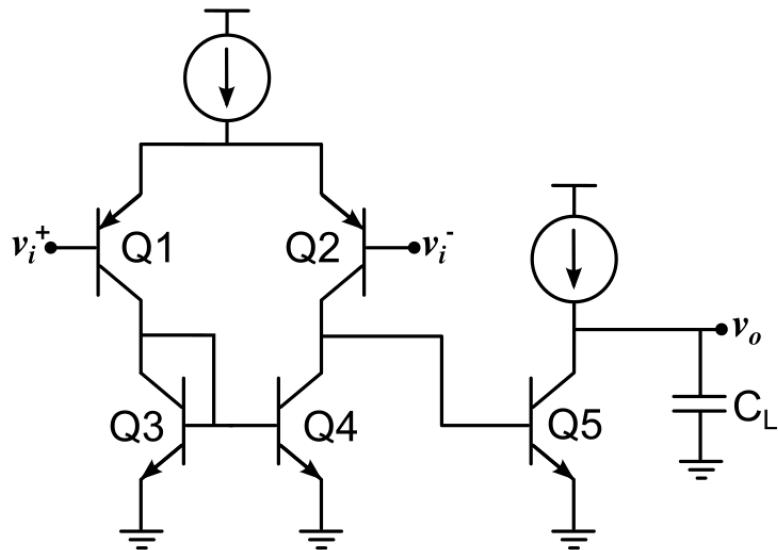
$$\frac{V_{out}}{I_{in}} = \frac{V_{out}}{V_{in}} \frac{V_{in}}{I_{in}} = (g_m R_L)^2 (R_S || R_{in})$$

$$V_{out}/V_{in} =$$

e) (2 pts) Why is this type of feedback advantageous in this application?

It provides low input impedance, suitable for amplifying a current input, and low output impedance suitable for providing a voltage-mode output.

**Problem 5 (11, 17 pts)**



The BJT op amp shown above is a simplified version of many early op amp designs which were done in a bipolar process. You may assume that all transistors are identical, with the same small signal parameters. You may also assume that differential transistors are perfectly matched.

Do not neglect  $r_\pi$ . Neglect all capacitors except for the device  $C_\pi$  and the load  $C_L$ . Assume that the input is driven by an ideal voltage source and that all devices are in forward active operation.

- a) (2pts) Calculate the DC open-loop gain of this circuit.

$$A_V = g_{m2} (r_{o2} || r_{o4} || r_{\pi5}) g_{m5} r_{o5}$$

Gain =

- b) (3 pts) There are three poles in this circuit. Find the three pole frequencies, expressing your answers in terms of the small signal parameters of the transistors and  $C_L$ .

$$\omega_{p1} = \frac{1}{(r_{o2} || r_{o4} || r_{\pi5}) C_{\pi5}}$$

$$\omega_{p2} = \frac{1}{r_{o5} C_L}$$

$$\omega_{p3} = \frac{g_{m3}}{2 C_{\pi3}}$$

$\omega_{p1} =$

$\omega_{p2} =$

$\omega_{p3} =$

c) (2 pts) There is one zero in the circuit as drawn, what is its frequency?

This comes from the mirror pole-zero pair, so we know that

$$\omega_z = 2\omega_{p3} = \frac{g_{m3}}{C_{\pi3}}$$

$$\omega_z =$$

- d) (4 pts) Place a capacitor and size it for dominant pole compensation to achieve phase margin of 45 degrees. Your goal is to minimize the size of  $C_C$ . Note: do not use the Miller effect (i.e., your capacitor should be connected to ground). Where is the best location for this capacitor? State your assumptions. You may assume that the second pole does not impact the location of the unity-gain frequency.

We place the compensation cap at the output since this is the highest-impedance node, and also probably CL is the largest capacitance in the circuit.

To size it for 45 degrees phase margin, we want unity-gain bandwidth equal to the second pole frequency:

$$\frac{A_{DC}}{r_{o5}(C_L + C_C)} = \frac{1}{(r_{o2}||r_{o4}||r_{\pi5})C_{\pi5}}$$

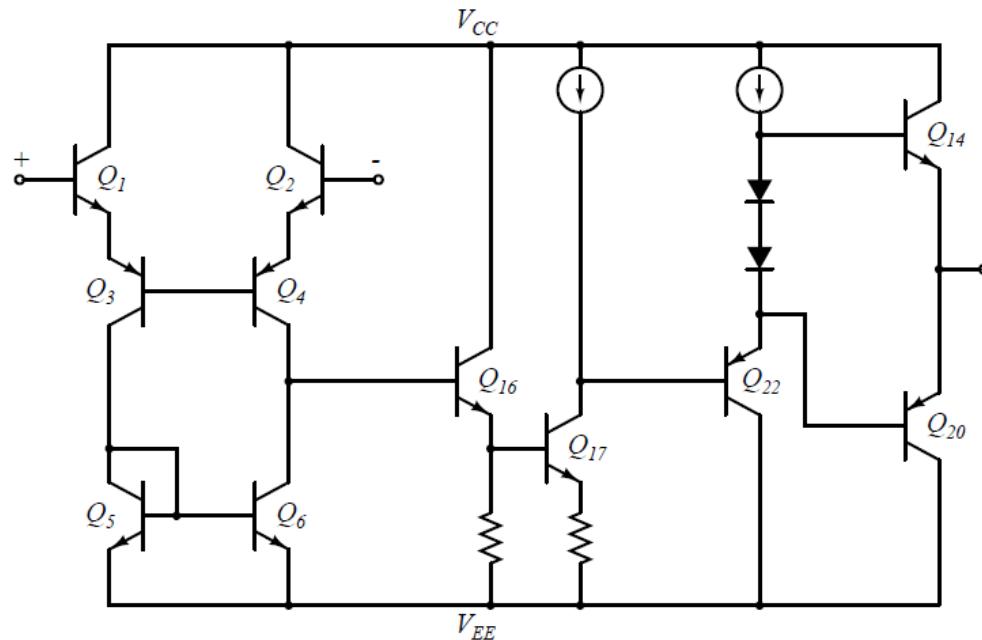
Solving for  $C_C$ :

$$C_C = A_{DC} \frac{(r_{o2}||r_{o4}||r_{\pi5})}{r_{o5}} C_{\pi5} - C_L$$

$$C_C =$$

$C_C$  should be placed between \_\_\_\_\_ and ground because:

e) (4 pts) EE240A only:



The above circuit represents a simplified schematic of the famous Fairchild uA741 op amp. For each of the legs containing transistors Q16, Q17, Q22, Q20, give a one sentence explanation explaining the function.

Q16 branch: Source follower to boost the input impedance of Q17.

Q17 branch: Second gain stage

Q22 branch: Bias branch for the class-AB output stage

Q20 branch: Class-AB output stage

f) (2 pts) EE240A only: Draw in the schematic the best location for a Miller compensation capacitor and justify your answer. Do you have to worry about the RHP zero? Why or why not?

Reason for Miller capacitor placement: From the base of Q16 to the collector of Q17. This is an inverting gain stage so it's suitable for Miller compensation

RHP zero explanation: Yes, you do need to worry about it, for the same reason as it appears in a MOS op amp.

**Extra page for work, clearly label problem number**

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**EE 140 / 240A Equation Sheet**  
**Prof. Rikky Muller, Fall 2017**

MOSFET Large Signal - Saturation

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

$$V_{TH} = V_{t0} - \gamma (\sqrt{2|\Phi_F| + V_{SB}} - \sqrt{2|\Phi_F|})$$

$$V_{OV} = \Delta V = V_{GS} - V_{TH}$$

MOSFET Small Signal - Saturation

$$g_m = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) = \sqrt{2\mu C_{ox} \frac{W}{L} I_D}$$

$$g_{mb} = \frac{\gamma g_m}{2\sqrt{2|\Phi_F| + V_{SB}}} ; \gamma = \frac{\sqrt{2\epsilon_s N_A}}{C_{ox}}$$

$$r_o = \frac{1}{\lambda I_D}$$

MOSFET Large Signal - Velocity Saturation

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{dsat,l} (1 + \lambda V_{DS})$$

$$V_{dsat,l} \approx \frac{(V_{GS} - V_{TH}) L E_{sat}}{(V_{GS} - V_{TH}) + L E_{sat}}$$

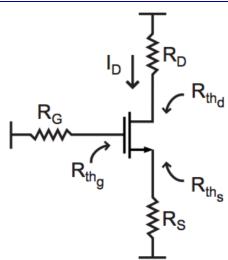
MOSFET Large Signal - Triode

$$I_D = \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS}$$

MOSFET Small Signal - Triode

$$r_{ds} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH} - V_{DS})}$$

Thevenin Resistances - Saturation



$$R_{thd} = r_o (1 + (g_m + g_{mb}) R_S) + R_S$$

$$R_{thg} = \infty$$

$$R_{ths} = \left(1 + \frac{R_D}{r_o}\right) (r_o || \frac{1}{g_m + g_{mb}})$$

MOSFET Capacitance

$$C_{ov} = C_{OL} = W L_D C_{ox} + W C_{fringe}$$

$$C_{gs} = \frac{2}{3} C_{ox} W (L + 2L_D) + C_{ov}$$

$$C_{gd} = C_{ov}$$

$$C_{jsb/jfdb} = \frac{C_j(0)WE + C_{jsw}(0)(W + 2E)}{\sqrt{1 + \frac{V_{SB\{DB\}}}{|\Phi_F|}}}$$

MOSFET G<sub>m</sub>, Source Degeneration

$$G_m = \frac{g_m}{1 + (g_m + g_{mb}) R_S}$$

BJT Large Signal - Forward Active

$$i_E = i_B + i_C$$

$$i_B = i_C / \beta$$

$$i_C = I_S e^{\frac{V_{BE}}{V_T}} \left( 1 + \frac{V_{CE}}{V_A} \right)$$

$$I_S = \frac{A_E q D_n n_i^2}{N_A W}$$

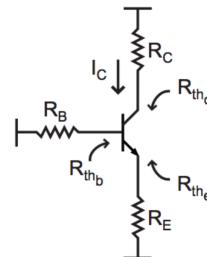
BJT Small Signal - Forward Active

$$g_m = \frac{I_C}{V_T}; V_T = \frac{kT}{q}$$

$$r_o = \frac{V_A + V_{CE}}{I_C} \approx \frac{V_A}{I_C}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{V_T}{I_B}$$

Thevenin Resistances - Forward Active



$$R_{thb} = (r_e + R_E)(\beta + 1) = r_\pi + (\beta + 1)R_E$$

$$R_{thc} = \frac{r_\pi + R_B}{\beta + 1} \cong \frac{1}{g_m} + \frac{R_B}{\beta + 1}$$

$$R_{the} = r_o + R_E \parallel (r_\pi + R_B) + g_m r_o \frac{R_E}{1 + \frac{R_E + R_B}{r_\pi}}$$

BJT Gains - Forward Active

$$\frac{v_c}{v_b} = -G_M R_C; g_m = \frac{g_m}{1 + g_m R_E}$$

$$\frac{v_c}{v_e} = -G_m R_C; G_m = \frac{g_m}{1 + g_m R_E}$$

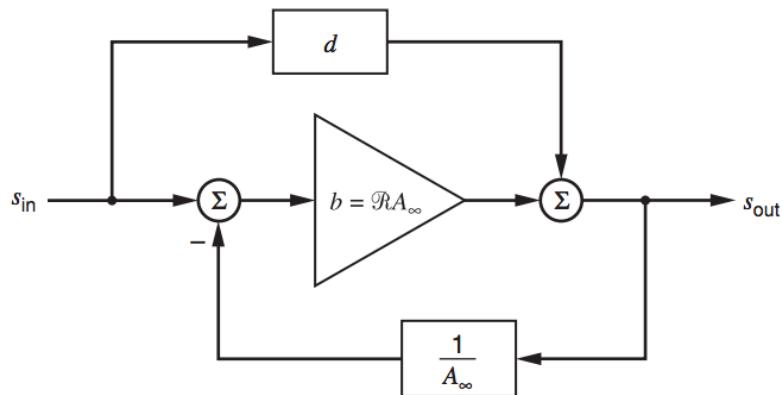
$$\frac{v_e}{v_b} = \frac{R_E || r_o}{R_E || r_o + r_e}$$

BJT Capacitance - Forward Active

$$C_\pi = \tau_p g_m + \frac{C_{je0}}{\left(1 + \frac{V_{EB}}{\psi_0}\right)^m}$$

$$C_\mu = \frac{C_{\mu 0}}{\left(1 + \frac{V_{CB}}{\phi_j}\right)^m}$$

## Return Ratio Analysis



To find the return ratio:

1. Set all independent sources to zero
2. Disconnect the dependent source from the rest of the circuit, which introduces a break in the FB loop
3. On the side of the break that is not connected to the dependent source, connect an independent test source  $s_t$
4. Find the return signal  $s_r$  generated by the dependent source.
5.  $RR = -s_r/s_t$
6.  $d$  is found by setting the dependent source of the amplifier = 0

7.  $A_\infty$  is determined by the passive feedback network =  $1/f$

$$\frac{s_{out}}{s_{in}} = \frac{A_\infty RR}{1+RR} + \frac{d}{1+RR}$$

$$Z_{CL} = Z_{OL} \frac{(1+RR_{short})}{1+RR_{open}}$$

### Noise

Resistor noise:

$$\begin{aligned}\overline{v_n^2} &= 4kTRB \\ \overline{i_n^2} &= \frac{4kTB}{R}\end{aligned}$$

MOSFET noise:

$$\overline{v_n^2} = \frac{4kT \left(\frac{\gamma}{\alpha}\right) B}{g_m}$$

$$\overline{i_n^2} = 4kT \left(\frac{\gamma}{\alpha}\right) g_m B$$

### Mismatch

$$\begin{aligned}\sigma_{\Delta V_{TH}} &\approx \frac{A_{V_{TH}}}{\sqrt{WL}} \\ \sigma_{\Delta W/L} &\approx \frac{A_K}{\sqrt{WL}}\end{aligned}$$

### Bandgaps

$$\begin{aligned}V_{OUT} &= V_{BE} + K\Delta V_{BE} \\ \frac{dV_{BE}}{dT} &= -2 \frac{mV}{^\circ C} \\ \frac{dV_T}{dT} &= 0.18 \frac{mV}{^\circ C}\end{aligned}$$