University of California
College of Engineering
Department of Electrical Engineering
and Computer Sciences

Rikky Muller **Friday, December 18, 2020.**
11:30-14:30

EE140/240A—Fall 2020: Final Exam

NAME	Last First

GRAD/UNDERGRAD	

Problem 1: **/ 12 (14)**

Problem 2: **/ 17 (17)**

Problem 3: **/ 20 (20)**

Problem 4: **/ 15 (17)**

Problem 5: **/ 13 (17)**

Problem 6: **/ 12 (15)**

Total: **/ 89 (100)**

EE 140 / 240A Equation Sheet
Prof. Rikky Muller, Fall 2020

MOSFET Large Signal - Saturation

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

$$V_{TH} = V_{t0} + \gamma(\sqrt{2|\Phi_F|+V_{SB}} - \sqrt{2|\Phi_F|})$$

$$V_{OV} = \Delta V = V_{GS} - V_{TH}$$

MOSFET Small Signal - Saturation

$$g_m = \mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH}) = \sqrt{2\mu C_{ox}\frac{W}{L}I_D}$$

$$g_{mb} = \frac{\gamma g_m}{2\sqrt{2|\Phi_F|+V_{SB}}}$$

$$\gamma = \frac{\sqrt{2q\epsilon_s N_A}}{C_{ox}}$$

$$r_o = \frac{1}{\lambda I_D}$$

MOSFET G_m, Source Degeneration

$$G_m = \frac{g_m}{1+(g_m+g_{mb})R_S}$$

MOSFET Large Signal – Velocity Saturation

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH})V_{dsat,l}(1+\lambda V_{DS})$$

$$V_{dsat,l} \approx \frac{(V_{GS}-V_{TH})LE_{sat}}{(V_{GS}-V_{TH})+LE_{sat}}$$

MOSFET Large Signal – Triode

$$I_D = \mu C_{ox}\frac{W}{L}\left(V_{GS}-V_{TH}-\frac{V_{DS}}{2}\right)V_{DS}$$

MOSFET Small Signal – Triode

$$r_{ds} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH}-V_{DS})}$$

MOSFET Capacitance

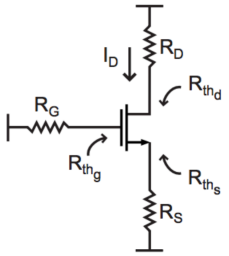
$$C_{OV} = C_{OL} = WL_D C_{ox} + WC_{fringe}$$

$$C_{gs} = \frac{2}{3}C_{ox}W(L-2L_D) + C_{ov}$$

$$C_{gd} = C_{OV}$$

$$C_{jsb\{jsdb\}} = \frac{C_j(0)WE}{\sqrt{1+V_{SB\{DB\}}/|\Phi_B|}} + \frac{C_{jsw}(0)(W+2E)}{\sqrt{1+V_{SB\{DB\}}/|\Phi_B|}}$$

Thevenin Resistances - Saturation



$$R_{thd} = r_o(1+(g_m+g_{mb})R_S)+R_S$$

$$R_{thg} = \infty$$

$$R_{ths} = (1+\frac{R_D}{r_o})(r_o \| \frac{1}{g_m+g_{mb}})$$

Diode Equations

$$\psi_0 = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right)$$

$$W_A = \left[\frac{2\epsilon(\psi_0+V_R)}{q\,N_A\left(1+\frac{N_A}{N_D}\right)}\right]^{\frac{1}{2}}$$

$$C_j = A\left[\frac{q\epsilon N_A N_D}{2(N_A+N_D)}\right]^{\frac{1}{2}}\frac{1}{\sqrt{\psi_0 - V_D}}$$

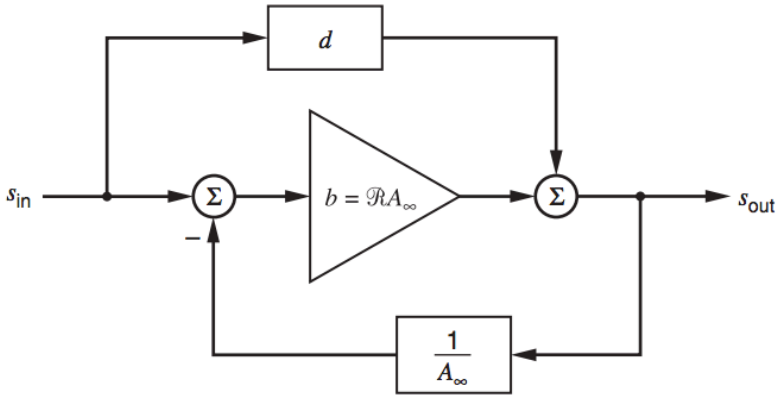
$$I_D = I_s\left(e^{\frac{V_D}{\eta V_T}}-1\right)$$

Mismatch

$$\sigma_{\Delta V_{TH}} \approx \frac{A_{V_{TH}}}{\sqrt{WL}}$$

$$\sigma_{\Delta W/L} \approx \frac{A_K}{\sqrt{WL}}$$

Return Ratio Analysis



To find the return ratio:
1. Set all independent sources to zero
2. Disconnect the dependent source from the rest of the circuit, which introduces a break in the FB loop
3. On the side of the break that is not connected to the dependent source, connect an independent test source s_t
4. Find the return signal s_r generated by the dependent source.
5. RR = $-s_r/s_t$
6. d is found by setting the dependent source of the amplifier = 0
7. A_∞ is determined by the passive feedback network = 1/f

$$\frac{s_{out}}{s_{in}} = \frac{A_\infty RR}{1+RR} + \frac{d}{1+RR} \qquad Z_{CL} = Z_{OL}\frac{(1+RR_{short})}{1+RR_{open}}$$

Problem 1. [14 points] MOS Models

Consider two well-designed n-channel MOSFETs, M_A and M_B, that are identical in structure and dimension except that the gate length, L, of M_A is twice that of M_B. How do the following parameters compare? Explain your answers - no credit will be given without an explanation.

a. (2 pts) The drain current at the bias voltages $V_{GS} = 1\ V > V_{ThN}$, and $V_{DS} = 5\ V$:
   - ☐ A greater than B
   - ☐ A less than B
   - ☐ A similar to B

   Because:

b. (2 pts) The threshold voltage, V_{ThN}:
   - ☐ A greater than B
   - ☐ A less than B
   - ☐ A similar to B

   Because:

c. (2 pts) The gate-to-source bias voltage, V_{GS}, at the bias point $I_D = 0.5\ mA$, $V_{DS} = 5\ V$:
   - ☐ A greater than B
   - ☐ A less than B
   - ☐ A similar to B

   Because:

d. (2 pts) The small-signal model output conductance, g_{ds}, at the bias $I_D = 0.5\ mA$, $V_{DS} = 5\ V$:
   - ☐ A greater than B
   - ☐ A less than B
   - ☐ A similar to B

   Because:

e. (2 pts) The small-signal model gate-to-source capacitance, C_{gs}, at the bias $I_D = 0.5$ mA, $V_{DS} = 5$ V:
☐ A greater than B
☐ A less than B
☐ A similar to B

Because:

f. (2 pts) The small-signal model gate-to-drain capacitance, C_{gd}, at the bias $I_D = 0.5$ mA, $V_{DS} = 5$ V:
☐ A greater than B
☐ A less than B
☐ A similar to B

Because:

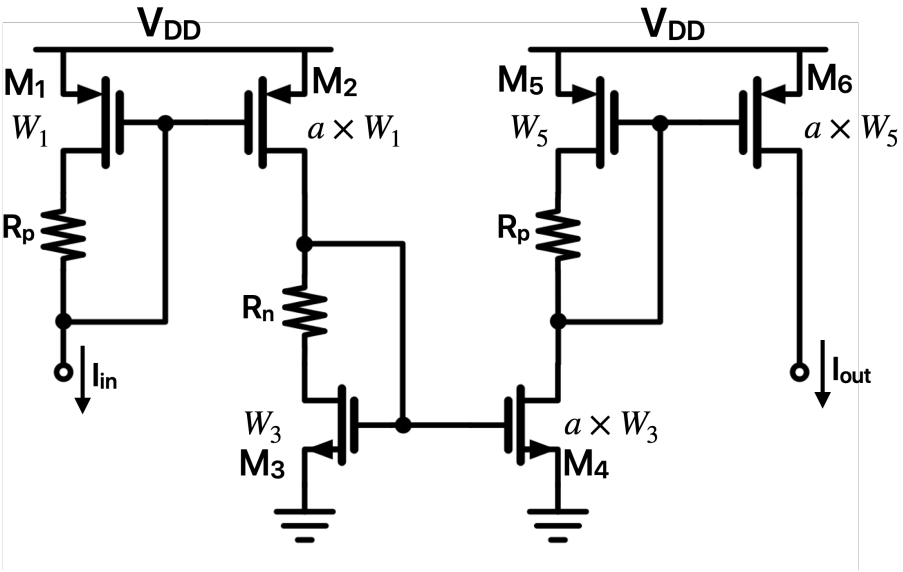
g. (2 pts) **EE240A only:** Percent of I_D error resulting from one standard deviation of area mismatch, $+\sigma_{W/L}$ at the bias voltages $V_{GS} = 1$ V > V_{ThN}, and $V_{DS} = 5$ V. Matching is measured between two identical devices M_A to M_A, and M_B to M_B. You may ignore threshold voltage mismatch.
☐ A greater than B
☐ A less than B
☐ A similar to B

Because:

Problem 2. [17 points] Multi-stage Current Amplifier

In the midterm exam, we reviewed a single stage current amplifier. Shown below is a three-stage current amplifier that is formed by cascading single gain stages. The design is done such that all devices have the **same length, g_m/I_D, and g_m/C_{GS}** parameters. You may neglect all capacitances except for C_{GS} of the devices and assume that ω_T can be approximated as $\omega_T \approx \frac{g_m}{C_{GS}}$. Other parameters are listed here.

$$\lambda = 0, \qquad \gamma = 0, \qquad W_6 = a\,.W_5, \qquad W_4 = a\,.W_3, \qquad W_2 = a\,.W_1$$



a. [2 points] What is the small signal DC gain of this amplifier, $\frac{i_{out}}{i_{in}}$?

$$\frac{i_{out}}{i_{in}} =$$

b. [6 points] Find the pole frequencies associated with each mirror node, and then use your answer from part (a) to derive the frequency dependent transfer function of the amplifier, $H(s) = \frac{i_{out}}{i_{in}}(s)$. You may use transistor specific small signal parameters in your derivation but simplify your result and find the answer in terms of "s", "a", and "ω_{T_1}" which is the ω_T of M_1.

$H(s) = \frac{i_{out}}{i_{in}}(s) =$

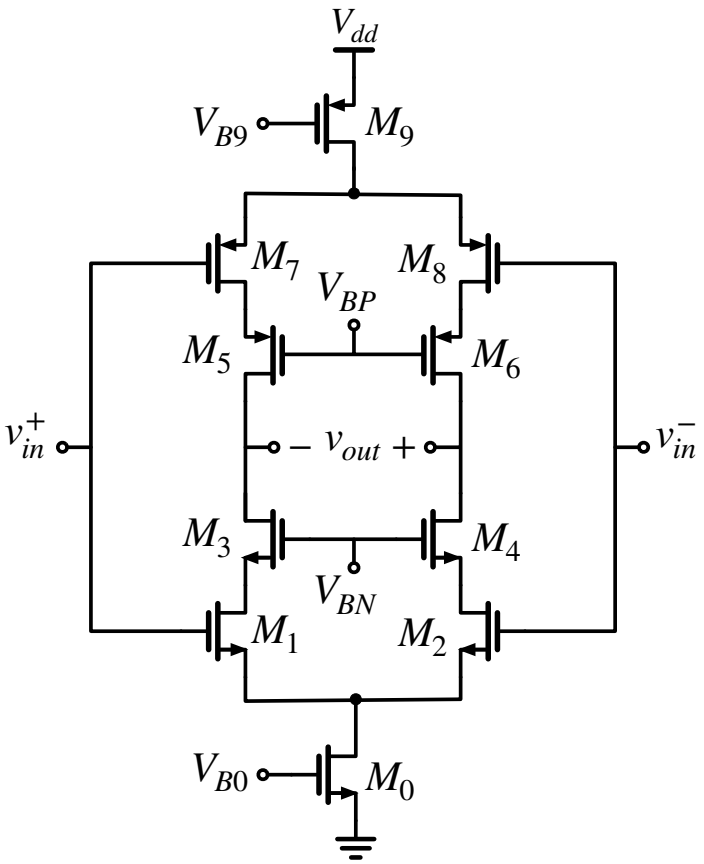
c. [6 points] Draw the bode magnitude plot for the above amplifier. Assuming $a > 1$, approximate the unity-gain bandwidth frequency (ω_u)?

$\omega_u =$

d. [3 points] Current mirrors are widely used in the design of analog circuits and are commonly cascaded to distribute current throughout the chip. This cascade forms current amplifiers like the one in this problem. A major issue with these mirrors is that interference can couple in, propagate and amplify. To mitigate this issue, you can add one capacitor to this circuit - what is the best location to add the capacitor and why? Assume the interference is only coupling at the input.

Problem 3. [20 points] Complementary Amplifier

You are designing a power efficient gain stage for your final project in EE140/240A. You read some papers and came across an interesting amplifier with complementary inputs as shown below. You decide to analyze whether this is a good choice for your project. For simplicity, assume $\mu_n = \mu_p$ and all the transistors have the same length, oxide thickness, overdrive voltage ΔV $(or\ v_{ov})$ and threshold voltage $(V_{Th} > \Delta V)$. Ignore the body effect.



a. [3 points] Determine the **<u>minimum</u>** power supply voltage $V_{dd,min}$ such that all the devices are biased in saturation. Express your answer in terms of ΔV $(or\ v_{ov})$ and V_{Th} of the transistors.

$V_{dd,min}=$

b. [3 points] Determine the maximum differential peak-to-peak swing of v_{out} when $V_{dd,min}$ is used. Express you answer in terms of ΔV and V_{Th} (and V_{dd} in case you did not answer part (a)).

$V_{out,pp}=$

c. [4 points] Draw the differential-mode half-circuit and determine the differential-mode gain $A_{DM} = \frac{v_{out}}{v_{in}^{+} - v_{in}^{-}}$ of this amplifier. Express your answer in terms of g_m and r_o of M_0 (Hint: recall the scaling of g_m and r_o with drain current). Assume $g_m r_o \gg 1$.

$$A_{DM} = \frac{v_{out}}{v_{in}^{+} - v_{in}^{-}} =$$

d. [4 points] Draw the common-mode half-circuit and determine the common-mode gain $A_{CM} = V_{out,CM}/v_{in,CM}$ of this amplifier. Assume $g_m r_o \gg 1$.

$A_{CM} =$

e. [6 points] Determine the power supply gain from the positive supply rail V_{dd} to the single-ended output v_{out^+} ($A_{vdd,S} = v_{out^+}/V_{dd}$) and to the differential output ($A_{vdd,D} = v_{out}/V_{dd}$). Assume $g_m r_o \gg 1$.

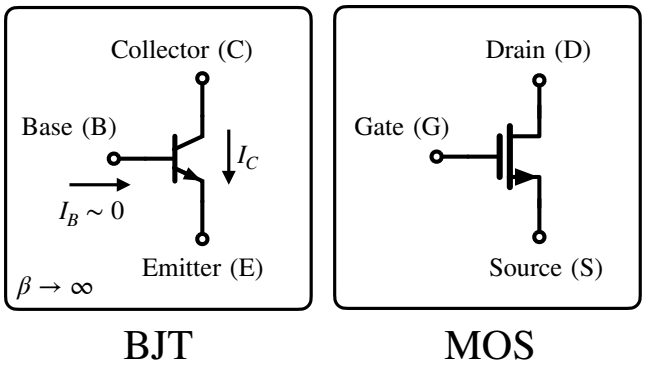
$A_{vdd,S} =$

$A_{vdd,D} =$

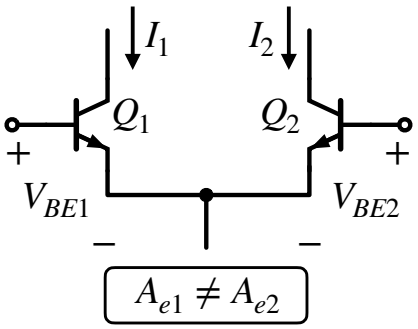
Problem 4. [17 points] Biasing

In this problem we will use Bipolar Junction Transistors (BJTs) to build an amplifier. BJTs are 3-terminal transistors with an exponential relationship between V_{BE} (equivalent to V_{GS} in a MOS device) and I_C (equivalent to I_D in a MOS device).

You may ignore the channel length modulation and assume that there is no current flowing into the base (equivalent to the gate in a MOS device) for simplicity. The small-signal equivalent circuit model of a BJT under these conditions is the same as that of a MOS, that is a voltage-controlled current source with v_{be} being the controlling signal and i_c being the output current.

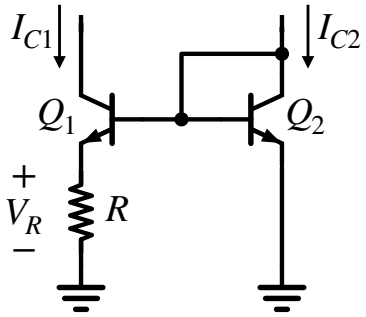


a. [3 points] The collector current of a BJT biased in the forward active region is expressed by $I_C = I_s A_e e^{V_{be}/V_T}$, where $V_T = \frac{kT}{q}$ and $I_s A_e$ is the reverse saturation current (A_e is the emitter area of the BJT). In the following circuit, derive and expression for $\Delta V_{BE} = V_{BE1} - V_{BE2}$ in terms of the emitter areas and collector currents of the transistors.



ΔV_{BE}=

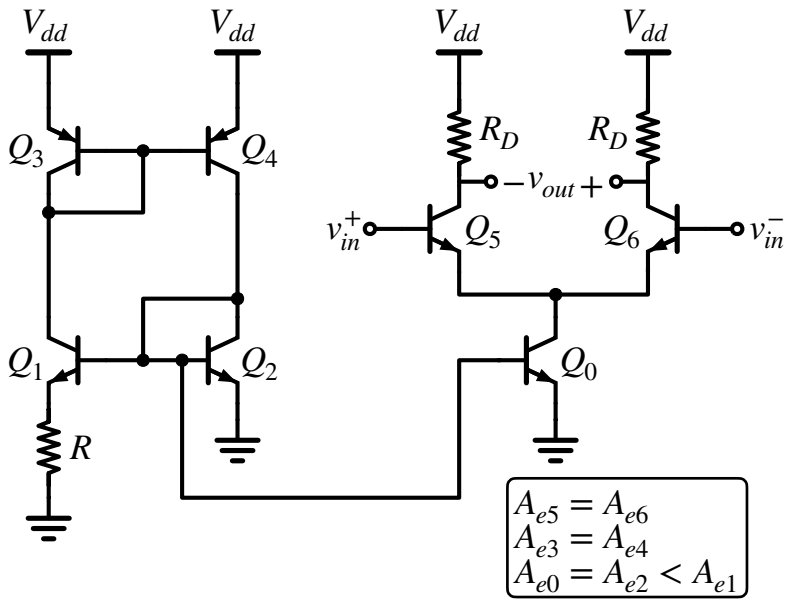
b. [3 points] Based on the observation from part (a) you are going to build and analyze a commonly used biasing technique called constant-gm. In the following circuit, assuming $I_{C1} = I_{C2}$, find the voltage drop across the resistor V_R in terms of the emitter areas of the devices.



$A_{e1} > A_{e2}$

$V_R =$

c. [6 points] Now, let's bias the tail current source of a resistively loaded differential amplifier using the V_{BE} of Q_2 as shown below. What is the differential-mode gain of this circuit. Given for a BJT $g_m = I_C/V_T$, express your answer in terms of the emitter areas of the transistors.



$$A_{DM} = \frac{v_{out}}{v_{in}^+ - v_{in}^-} =$$

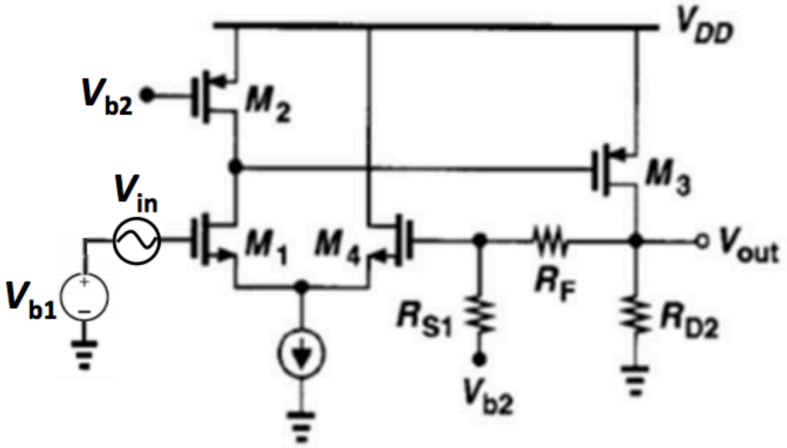
d. [3 points] In the design rule manual of this process, it says all the resistors in this process have a global process variation of up to 20%. What is the maximum gain deviation (in percent) that you would expect from this amplifier?

e. [2 points] **EE240A Only:** What is the sensitivity of the gain of this amplifier to temperature variations.

Problem 5. [17 points] Feedback Analysis

The two stage CMOS amplifier circuit shown below is being used to provide modest gain for an input sensor at V_{in} with very low supply voltage and power consumption. Let's analyze the performance of this circuit in feedback using return ratio. You may assume the following:

$$g_m r_o \gg 1,$$
$$r_{o1} = r_{o2} = r_{o4},$$
$$g_{m1} = g_{m4},$$
$$r_o \gg R_{D2}, r_o \gg R_F, r_o \gg R_{S1}$$



a. [2 points] What type of feedback is being utilized in this circuit?

Feedback Type:

b. [3 points] What is the loop gain or return ratio (RR) for this circuit?

RR=

Now calculate the closed-loop voltage gain ($A_{CL} = v_{out}/v_{in}$) and output impedance, Z_{out}, using return ratio.

c. [2 points] Find the ideal closed loop gain, A_∞. Leave your answers in terms of device specific small signal parameters.

A_∞=

d. [2 points] Next, let's find the feed forward co-efficient, d. Leave your answers in terms of device specific small signal parameters.

d=

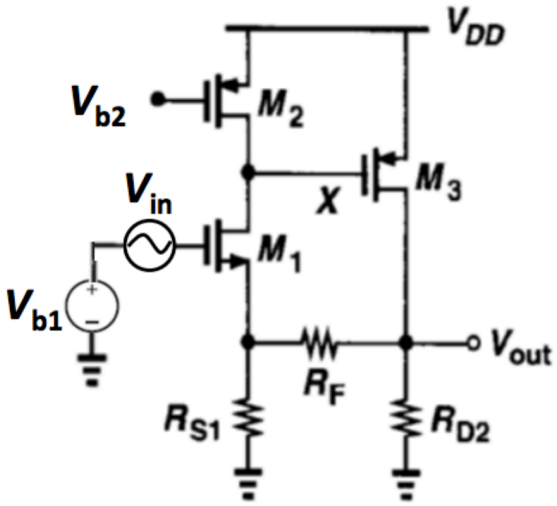
e. [1 point] Putting it together, write the expression for the closed-loop gain, A_{CL}. Express your answer in terms of RR and other circuit parameters.

A_{CL}=

f. [3 points] Find the closed-loop output impedance for the circuit, Z_{out}. Write your answer in terms of device specific small signal parameters.

$Z_{out} =$

g. **[EE240]** [4 points] In an attempt to save power you modify the circuit as shown below, feeding the output directly back into the source of M1. Find the new loop gain (RR) for this circuit and comment on whether it is greater or less than before. Assume that g_{m1} in this new circuit is the same as g_{m1} from the previous circuit.



RR_{new} =

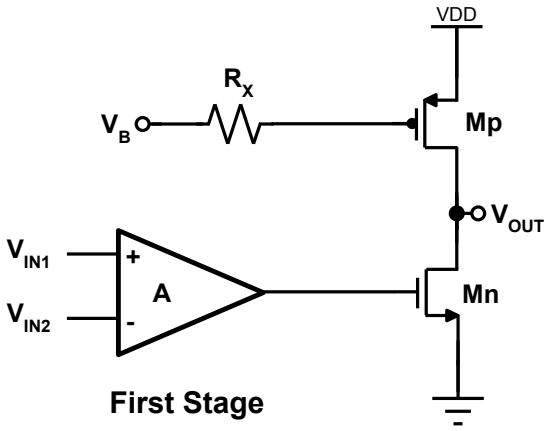
The new RR is: Larger or Smaller

Problem 6. [15 points] Output Stages

You are tasked with designing a low-power two-stage amplifier to drive a large capacitive load. After running some device level simulations, you find that your technology node has the following features:

$$k_N = 2k_P = 2.5mA/V^2,$$
$$|V_{THP}| = V_{THN}, \text{ and}$$
$$\lambda_P \neq \lambda_N.$$

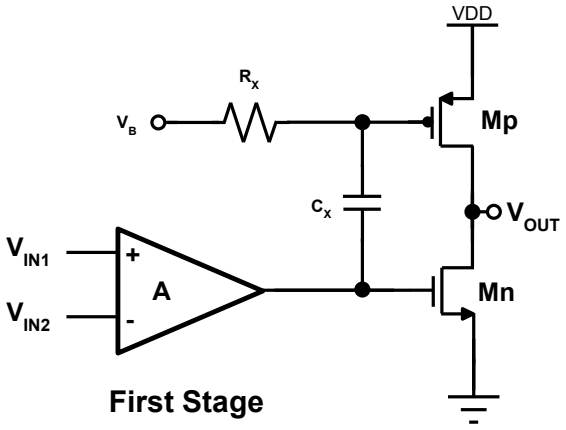
You begin your design with a standard class A common source amplifier shown below.



a. [2 points] What is the minimum bias current required for this output stage to drive a 20 MHz, 1 Vpp sine wave into a load capacitance of 0.1nF without slewing?

$I_{BIAS} =$

To avoid burning all this current in your output stage, you decide to convert your class A output stage into an inverter-based class AB output stage using this simple circuit modification below.



b. [3 points] Size the PMOS and NMOS devices so as to guarantee that the output stage has equal rising and falling edge drive current and the combined NMOS and PMOS G_m for this stage is $5\ mS$. Assume that $L_P = L_N = 200\text{nm}$ and ΔV equal 0.1V for both devices.

W_N=
W_P=

c. [4 points] Find the voltage gain, $A_v = v_{out}/(v_{in1} - v_{in2})$, for this 2-stage amplifier as a function of frequency, considering only the caps explicitly drawn in the circuit. Leave your answer in terms of G_m and device specific small signal parameters.

A_v=

d. [3 points] Find the gain error at DC, ϵ_{DC}, and at high frequency, ϵ_{AC}, (i.e. above any poles and or zeros in the loop gain) for this two stage amplifier, assuming unity gain feedback.

$\epsilon_{DC}=$
$\epsilon_{AC}=$

e. **[EE240A Only]** [3 points] You decide to improve the static error by resizing the AC coupling cap. Compute the minimum cap value to guarantee the gain error at 10 MHz and 20 MHz are both equal and both are minimized. The value of Rx is fixed at 1 kΩ.

$C_X>$

Extra work space, please label the number and part of each question
Final answers must be given in the answer boxes of the exam

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Final answers must be given in the answer boxes of the exam