

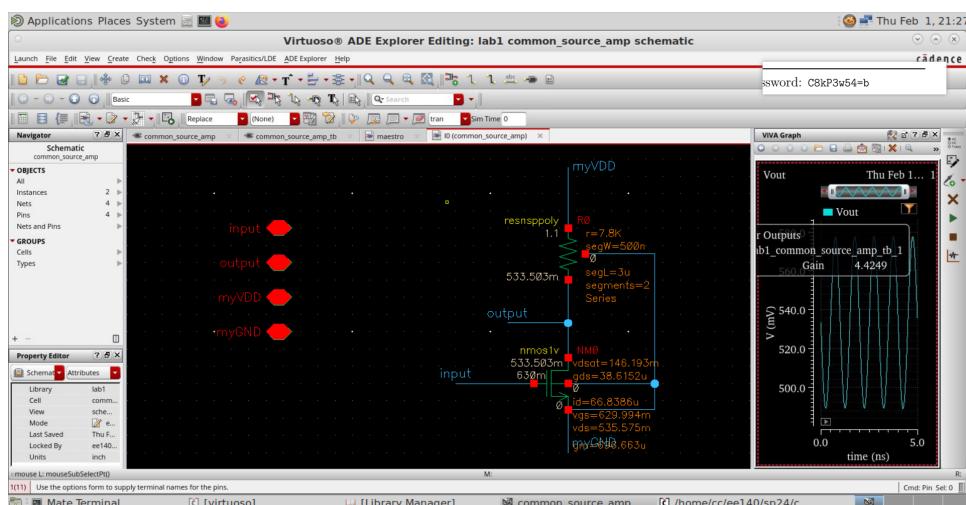
# EE140 Lab 1: Introduction to Cadence

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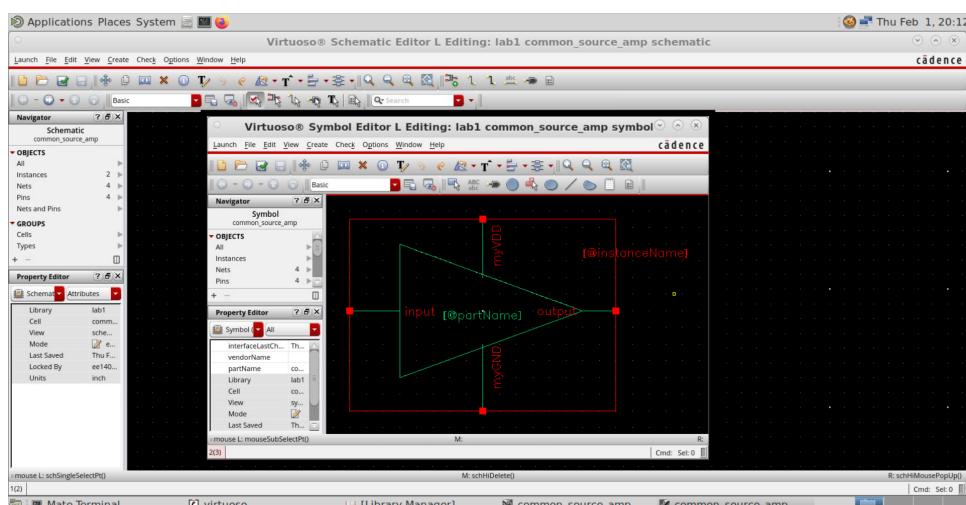
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## Lab1 Report

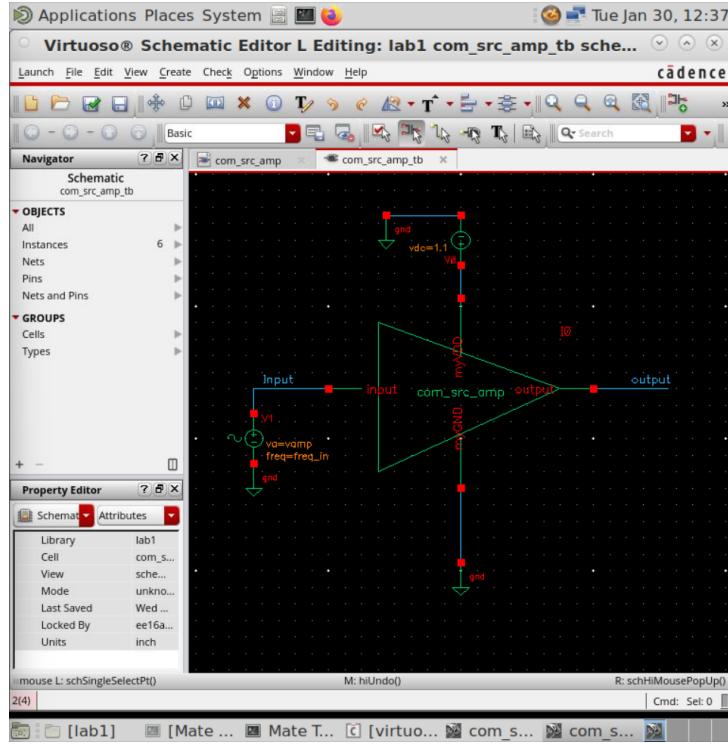
1. An image of the circuit schematic with the DC operating points.



2. An image of the circuit symbol.



3. An image of the testbench.



4. The voltage gain ( $A_v$ ) in a common-source amplifier configuration, is determined by ( $g_m$ ) and the output resistance ( $r_{out}$ ), represented as:

$$A_v = -g_m \cdot r_{out}$$

Where the negative sign signifies a phase inversion. The transconductance ( $g_m$ ), defining the sensitivity of the drain current ( $I_D$ ) to the gate-source voltage ( $V_{GS}$ ) changes, is given by:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \approx \frac{2I_D}{V_{GS} - V_{th}}$$

The output resistance ( $r_{out}$ ), equivalent to the resistance seen looking into the drain, for a long-channel MOSFET, is approximated by:

$$r_{out} = \frac{1}{\lambda I_D}$$

So

$$A_v = - \left( \frac{2I_D}{V_{GS} - V_{th}} \right) \cdot \left( \frac{1}{\lambda I_D} \right) = - \frac{2}{\lambda(V_{GS} - V_{th})}$$

Reason for the gain of a biasing transistor in saturation:

**Control over  $I_D$ :** In saturation,  $I_D$  is primarily controlled by  $V_{GS}$  and not significantly affected by  $V_{DS}$ . This allows a small change in  $V_{GS}$  (input voltage) to produce a relatively large change in  $I_D$  (output current), creating the potential for voltage gain when the current passes through a load resistance in the circuit.

**High Output Impedance:** Saturation mode provides high output impedance ( $r_{out}$ ), which is beneficial for achieving high voltage gain. The gain of a common-source amplifier is given by  $A_v = -g_m r_{out}$ , where  $g_m$  is the transconductance (change in  $I_D$  per change in  $V_{GS}$ ). A high  $r_{out}$

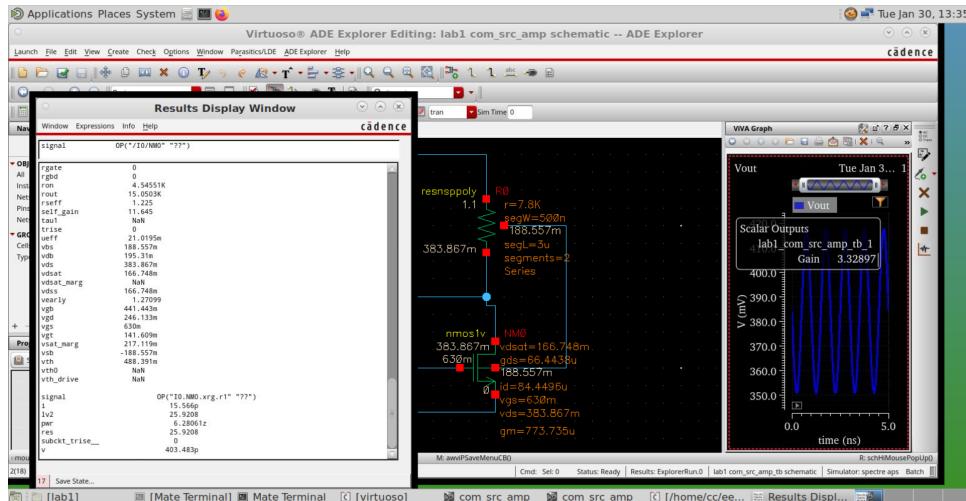
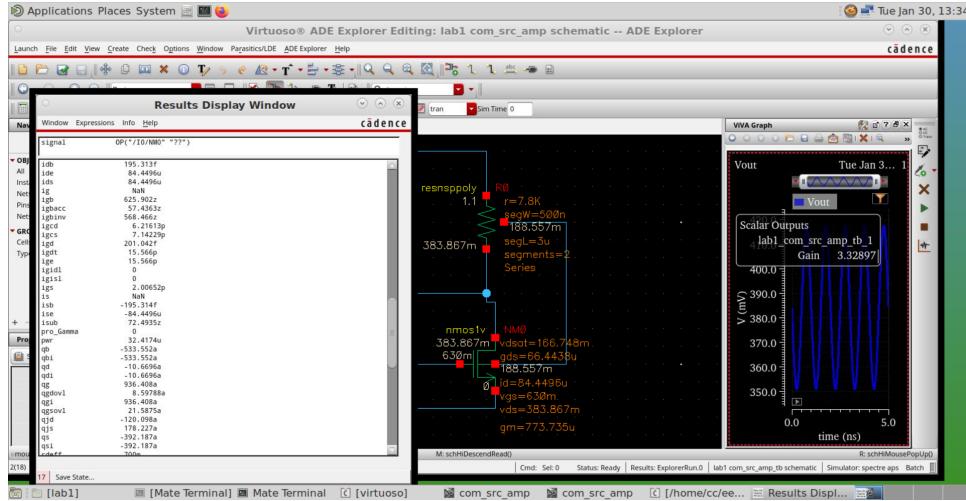
in saturation mode maximizes the voltage gain since  $r_{out}$  effectively acts as the load resistance through which the drain current flows.

In summary, in saturation the transistor facilitates the conversion of small input voltage variations into significant output voltage changes, achieving amplification, characterized by  $g_m$  and  $r_{out}$ .

- From the formula derived from the previous question we can get  $g_m$ . A table comparing the theoretical gain and the simulated gain, and an explanation of any discrepancies between the two.

Parameter	Theoretical Value	Simulated Value
Transconductance $g_m$ (m)	830.010	696.663
Output resistance $r_{out}$ (ohms)	7800	6351.56
Gain $A_v$	6.4740	4.4249

Table 1: Theoretical and simulated gain values with relevant parameters



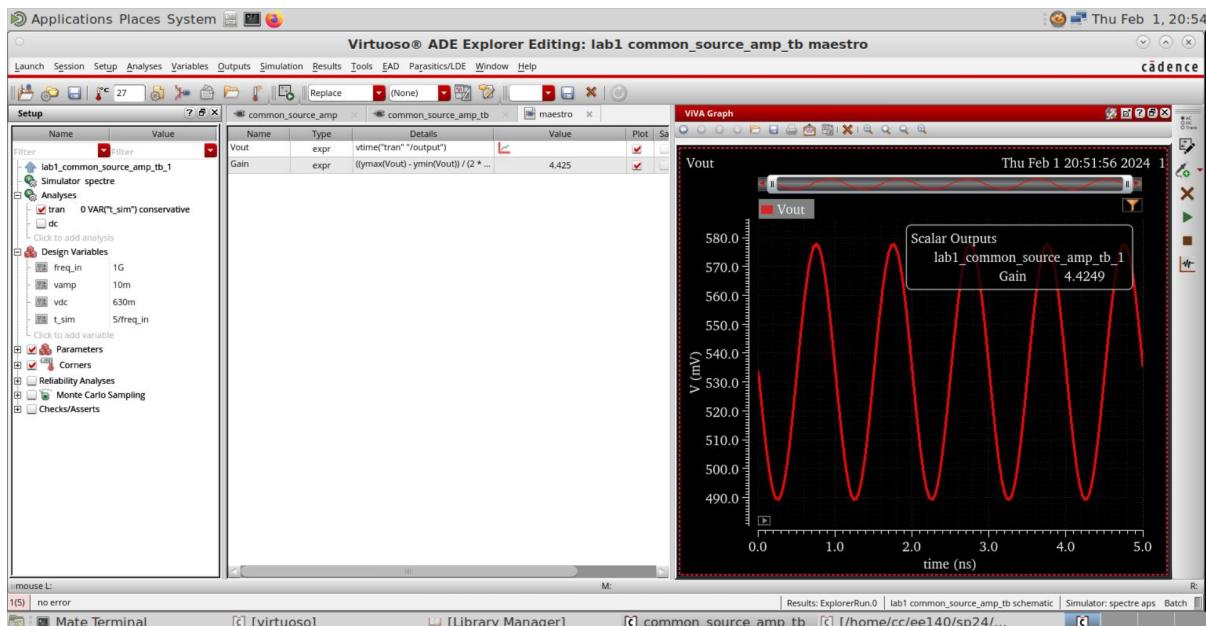
Theoretical models of electronic circuits often make ideal assumptions that lead to discrepancies when compared to simulated or practical results. Such discrepancies can be attributed to several factors:

- Ideal Assumptions:** Theoretical calculations assume ideal components without parasitic elements, which is rarely the case in real-world scenarios.

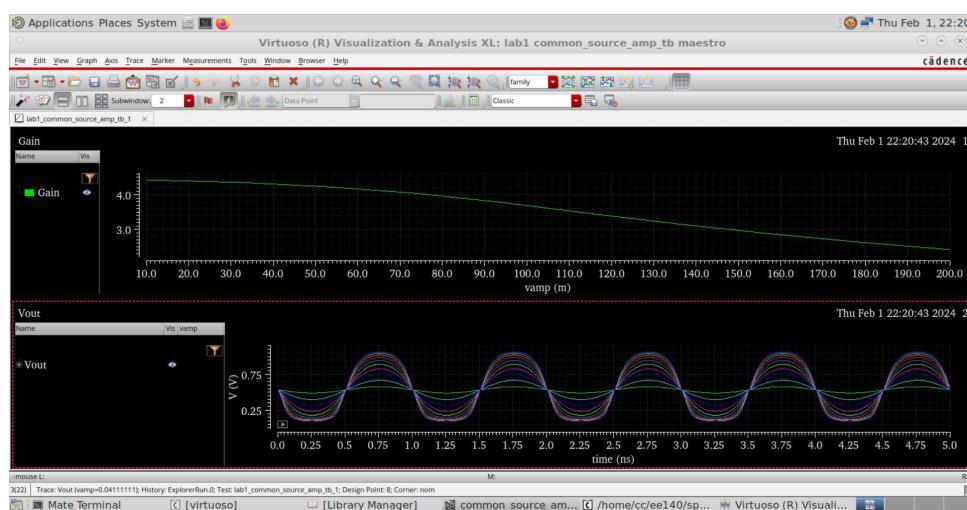
- **Parasitic Effects:** Simulations take into account parasitic capacitances and resistances, which can affect the circuit's behavior, especially at high frequencies.
- **Channel Length Modulation:** The output resistance  $r_{out}$  in simulations may include channel length modulation, which affects the transistor's output characteristics and is not always considered in theoretical models.
- **Complex Models:** Simulation tools use complex models for devices that include effects like temperature, carrier mobility variations, and sub-threshold conduction, which are not included in basic theoretical models.

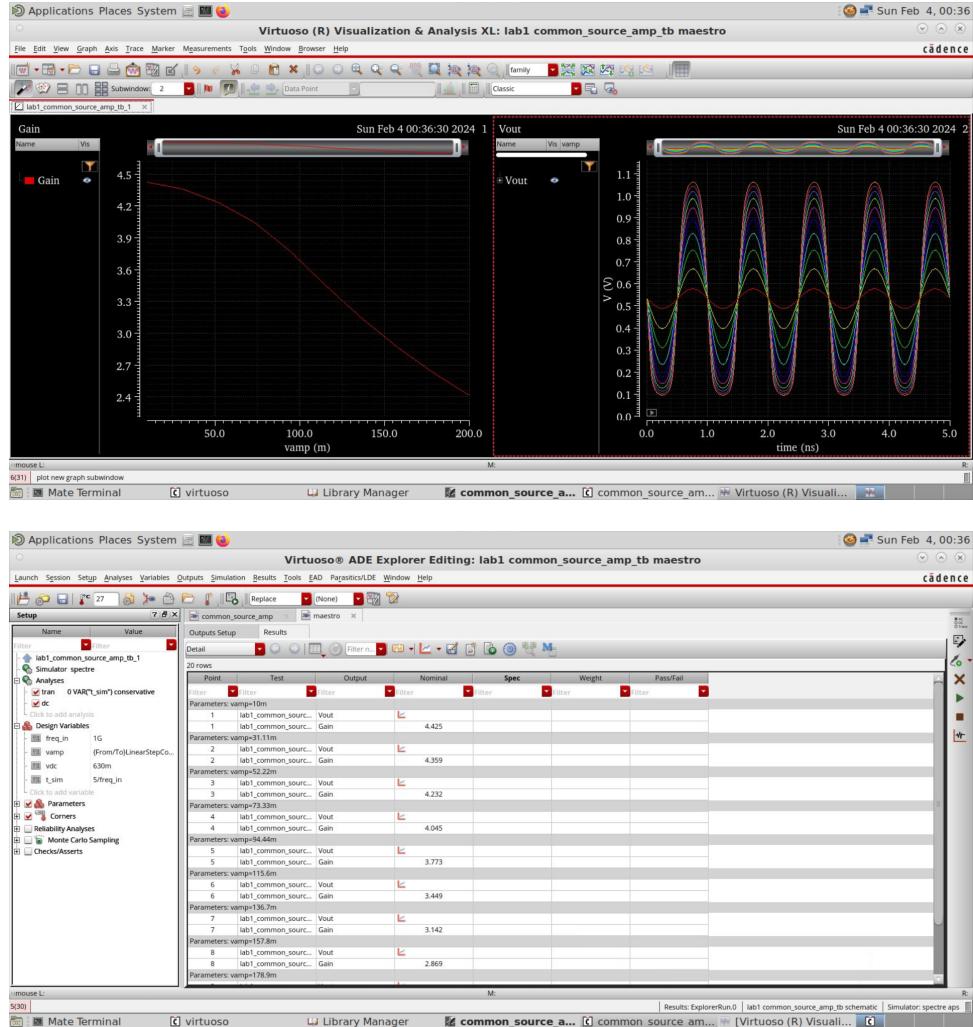
The gain of an amplifier, given by  $A_v = -g_m \cdot r_{out}$ , is thus affected by these factors, leading to the observed differences between theory and simulation.

6. Image of transient waveform of the small-signal input ( $v_{amp} = 10m$ ).



7. When a common-source amplifier is driven with an input voltage ( $v_{amp}$ ) that is too large, the output waveform can exhibit clipping. This distortion occurs because the input signal pushes the transistor's operation beyond its linear amplifying region, either into cutoff or saturation, where it can no longer linearly amplify the input signal.





Comparing the transient response at  $v_{amp} = 10m$  to the distorted waveform, the ideal undistorted output should resemble a sine wave, scaled by the amplifier's gain. However, as  $v_{amp}$  increases, the peaks of the output waveform begin to flatten, indicating that the transistor is entering saturation too early during each cycle and is cut off too late.

The specific  $v_{amp}$  value(s) chosen to show this distortion. Associated gain(s) with these  $v_{amp}$  value(s) will be significantly different from the expected linear gain, reflecting the non-linear behavior at these high input levels.