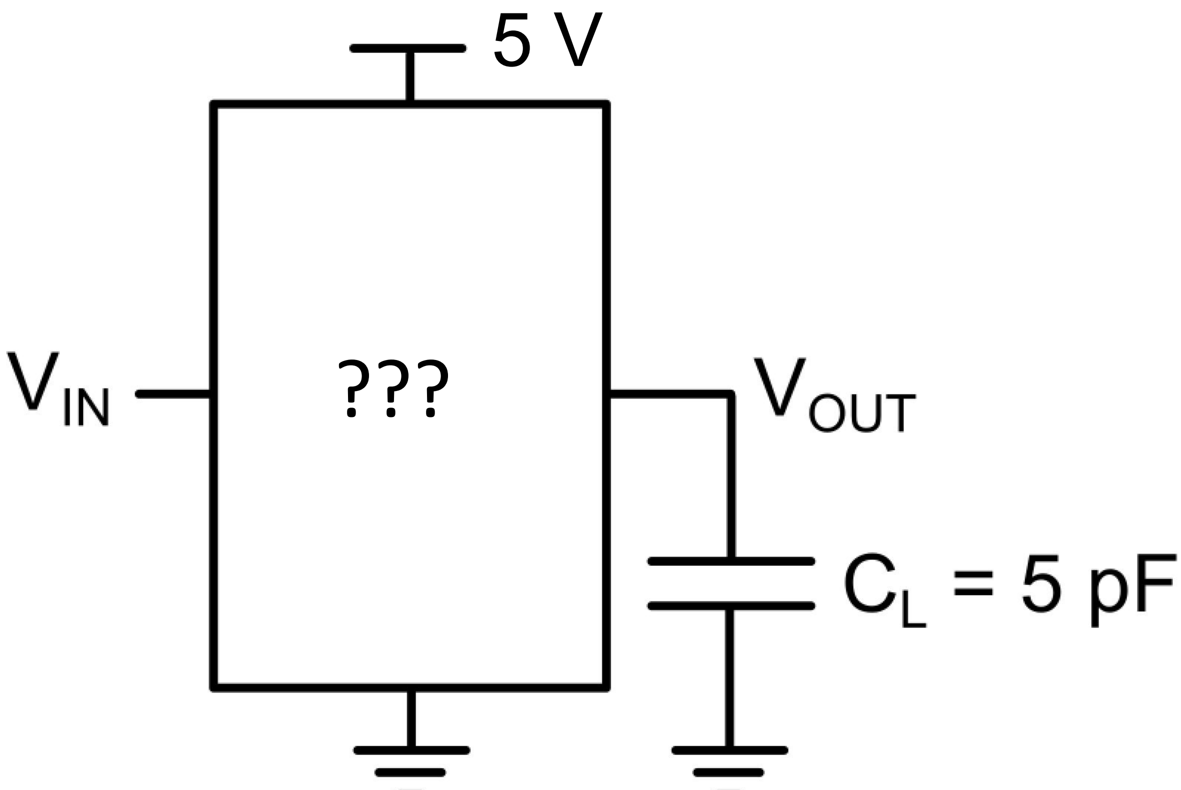
“Design Procedure:” Example

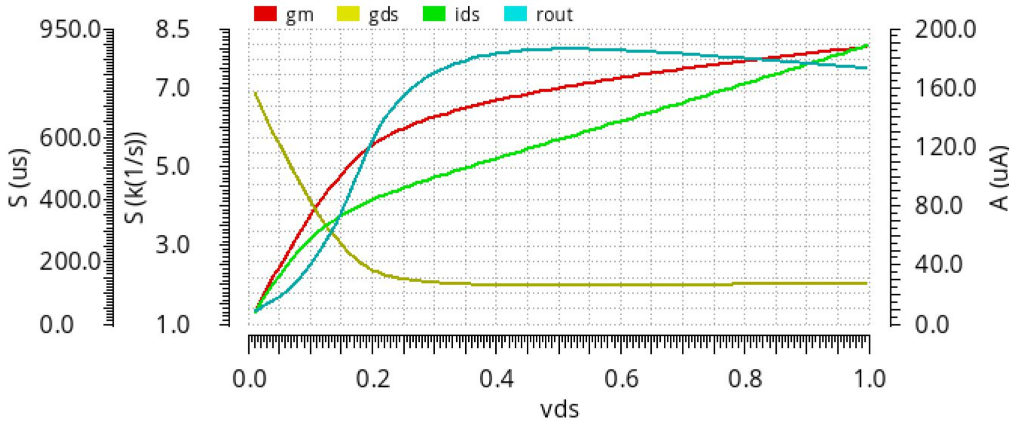
- **Goal:** Design an amplifier to drive a 5 pF load that provides gain > 10, bandwidth > 1 MHz, with an output swing within 500 mV of +5 V / 0 V supply rails



Step 0: What can this process technology do?

Characterize the small-signal parameters of devices in the technology you are using.

- Short-channel devices (example):



Use simulator to characterize small-signal parameters vs. bias point

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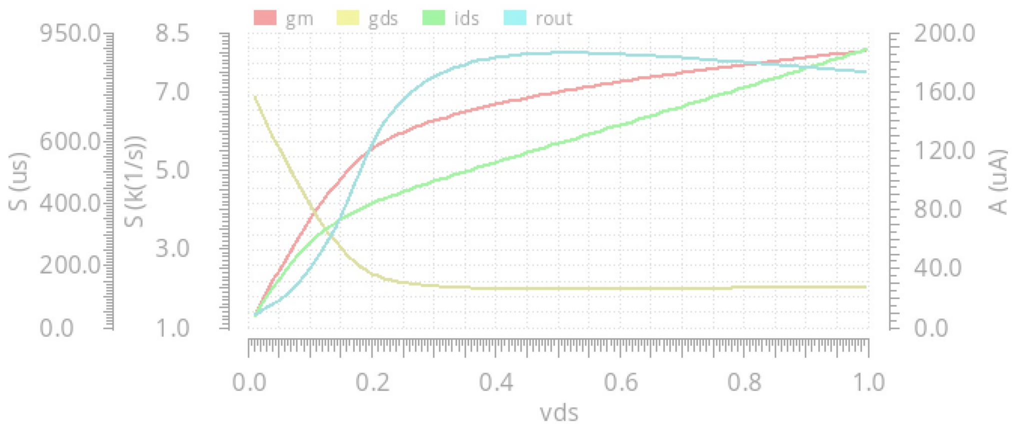

Use simulator to characterize small-signal parameters vs. bias point

- Long-channel devices (square-law model holds):

Hand calculations suffice for most parameters:

$$\boldsymbol{I_{DS}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$$\boldsymbol{g_m} \approx \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH}) \approx \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}$$

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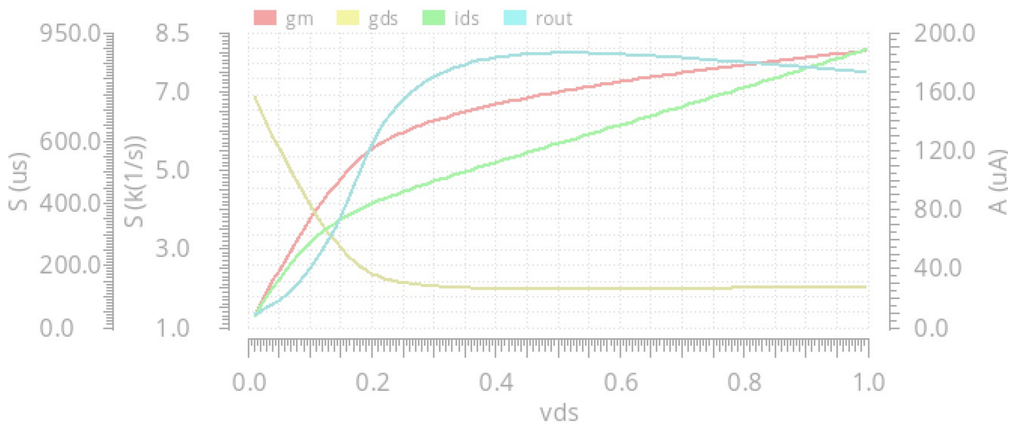

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This process technology:

Parameter	NMOS	PMOS
VTO	0.8 V	-0.8 V
KP	90 μA/V^2	30 μA/V^2
LAMBDA	0.01 V^{-1}	0.02 V^{-1}

Step 0: What can this process technology do?

Characterize the small-signal parameters of devices in the technology you are using.

- Full process parameter list

Parameter	NMOS	PMOS	
Model Level	3 (in HSPICE)	3 (in HSPICE)	
VTO	0.8 V	-0.8 V	Threshold voltage
KP	90 μA/V^2	30 μA/V^2	Transconductance
GAMMA	0.8 $\sqrt{V}$	0.4 $\sqrt{V}$	Bulk threshold parameter
LAMBDA	0.01 V^{-1}	0.02 V^{-1}	Channel length modulation
TOX	200 Å	200 Å	Gate oxide thickness
XJ	0.5 μm	0.5 μm	Junction depth
LD	0.3 μm	0.3 μm	Lateral diffusion length
PHI	0.7 V	0.6 V	Surface potential
NSUB	3.33 x 10^{16} cm^{-3}	3.33 x 10^{15} cm^{-3}	Substrate doping density
RSH	0 Ω	0 Ω	Drain/source siddution sheet resistance
CGSO	500 pF/m	500 pF/m	Gate-source overlap capacitance
CGDO	500 pF/m	500 pF/m	Gate-drain overlap capacitance
CGBO	0 F/m	0 F/m	Gate-bulk overlap capacitance
CJ	300 μF/m^2	300 μF/m^2	Bulk junction cap, 0V, bottom
MJ	0.5	0.5	Bulk junction grading coeff., bottom
CJSW	0 F/m	0 F/m	Bulk junction cap, 0V, sidewall
MJSW	0.33	0.33	Bulk junction grading coeff., sidewall

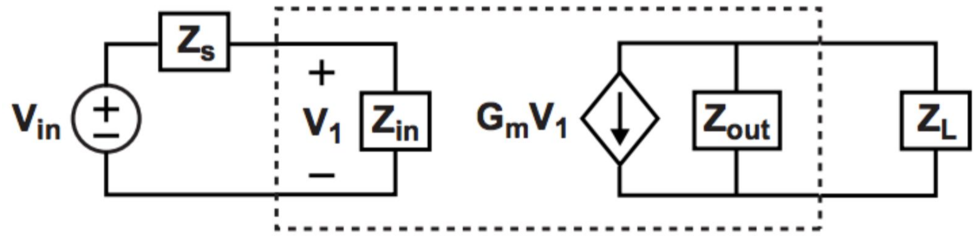
Process / SPICE parameters for NMOS / PMOS transistors.

Step 1: What topology should you use?

Find out how target specs impact specific parameters, and choose topology accordingly.

- Topology choice sets achievable G_m and R_{out}

From lecture:



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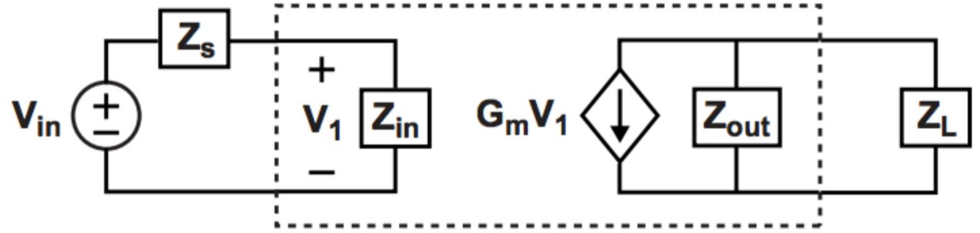

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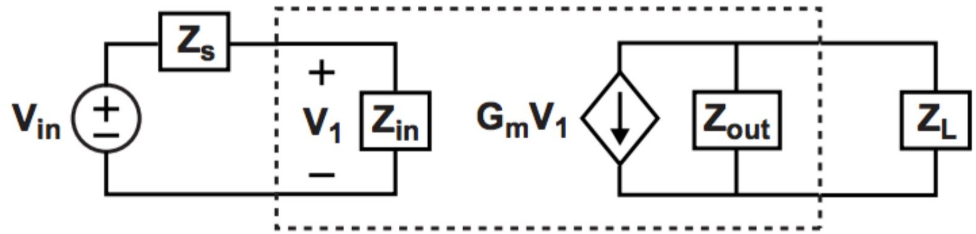

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Single device performance

Swing constraint: $V_{DS} > V_{GS} - V_T$

	V_{GS}=1V, W/L=5		V_{GS}=1.3 V, W/L=20	
	NMOS	PMOS	NMOS	PMOS
	9 µA	3 µA	0.2 mA	75 µA
	90 µS	30 µS	0.9 mS	0.3 mS
	11 MΩ	17 MΩ	0.4 MΩ	0.7 MΩ

g_m in the 100s of µS, r_o in the 100s of kΩ

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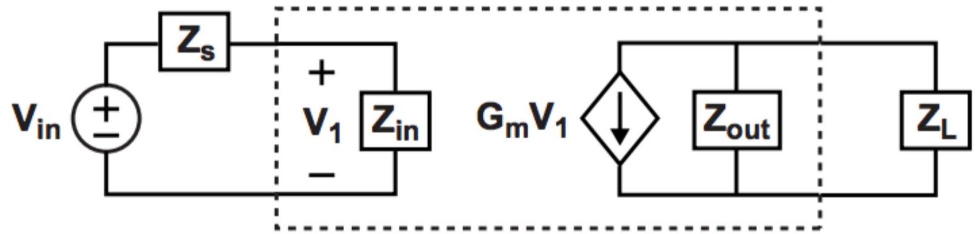

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Requirements

Bandwidth constraint:

$$f_{BW} \approx \frac{1}{2\pi R_{out} C_L} \geq 1\ MHz$$

$$R_{out} \leq \frac{1}{2\pi \cdot 1MHz \cdot 5\ pF} = 32\ k\Omega$$

Gain constraint:

$$A_V = G_m R_{out} \geq 10 \rightarrow G_m \geq \frac{10}{R_{out}} = 0.31\ mS$$

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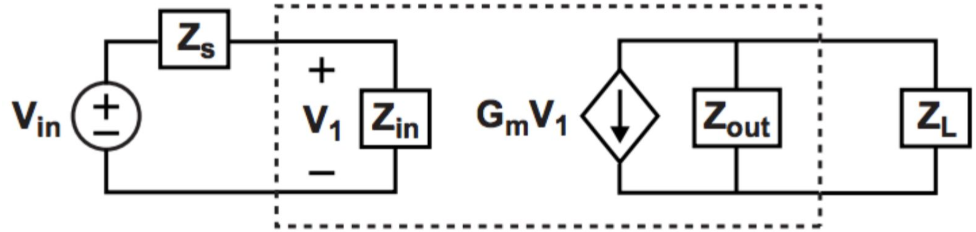

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g_m about right, r_o needs to be smaller

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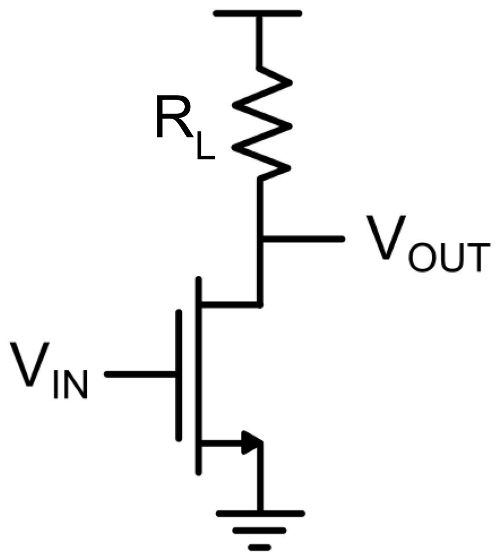
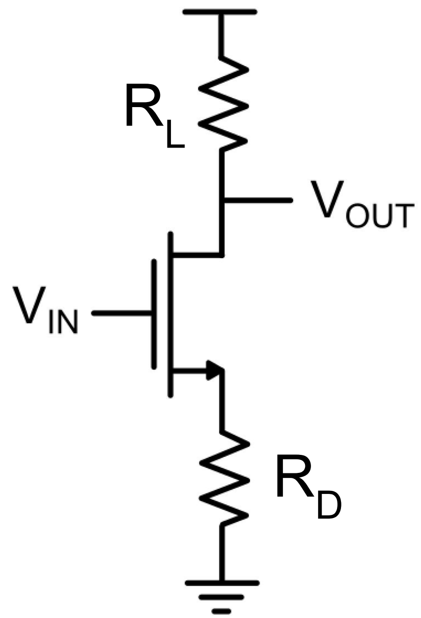
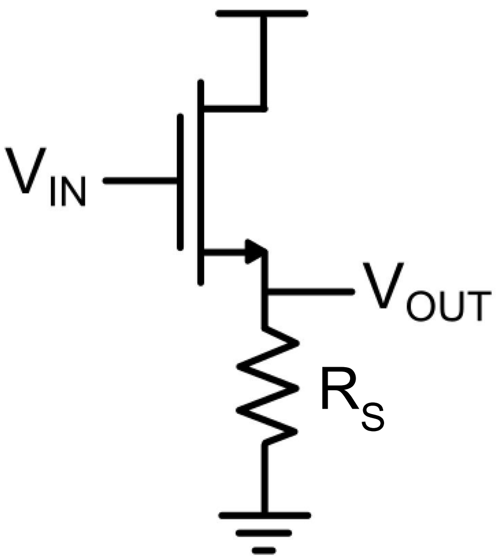
Common Source Amplifier



Common Source Amplifier w/ Degeneration



Source Follower



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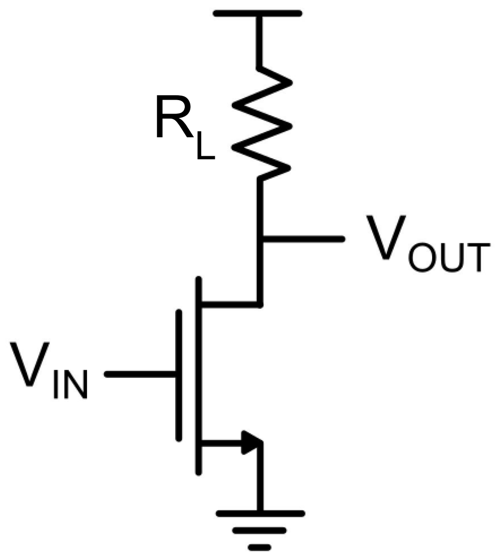

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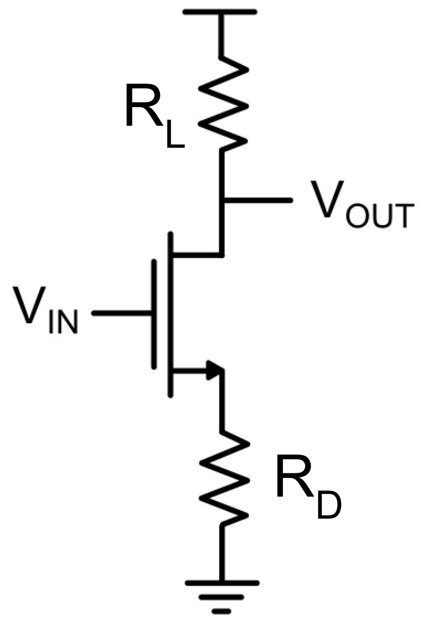

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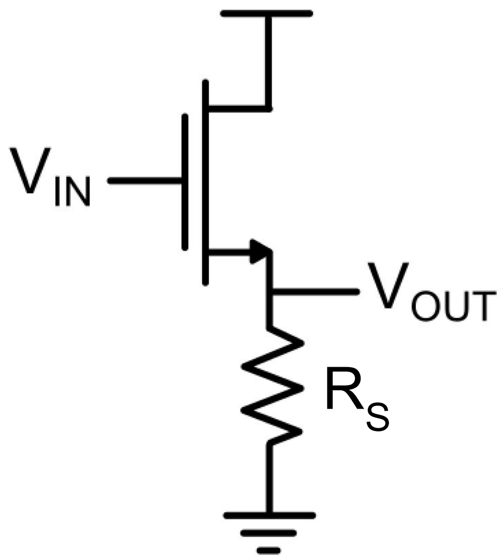

	Equation	Effect
G_m	g_m	Same
R_{out}	$r_o \| \| R_L$	⬇️

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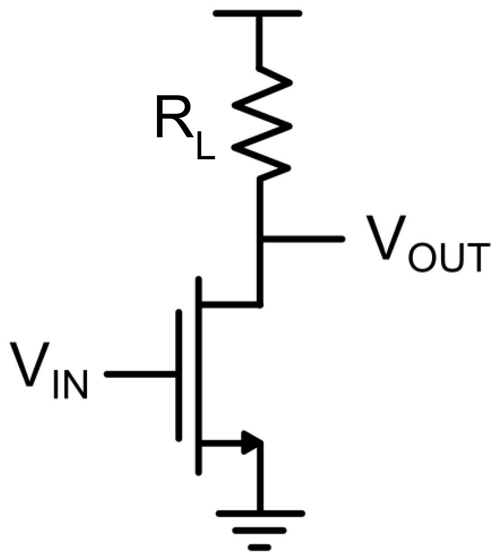

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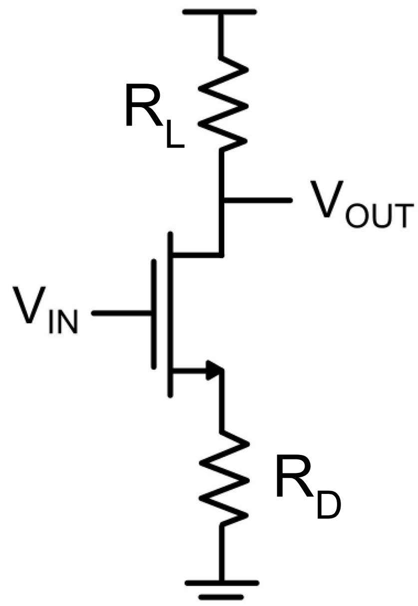

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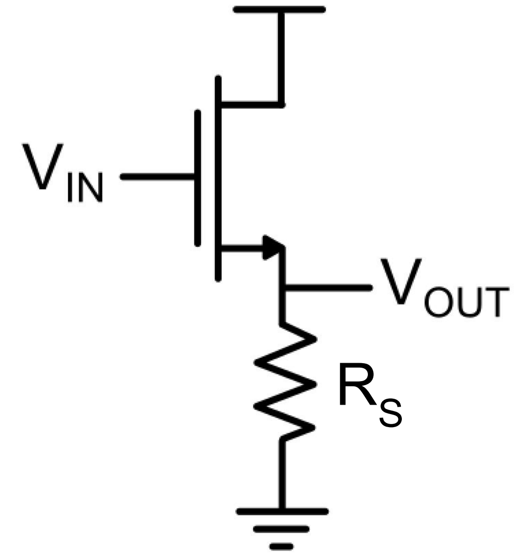

	Equation	Effect	Equation	Effect
G_m	g_m	Same	$g_m/(1+g_m R_D)$	⬇️
R_{out}	$r_o \| \| R_L$	⬇️	$(r_o(1+g_m R_D)) \| \| R_L$	Varies

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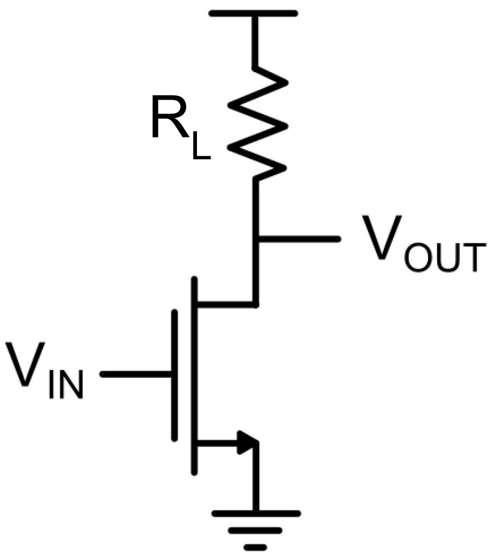

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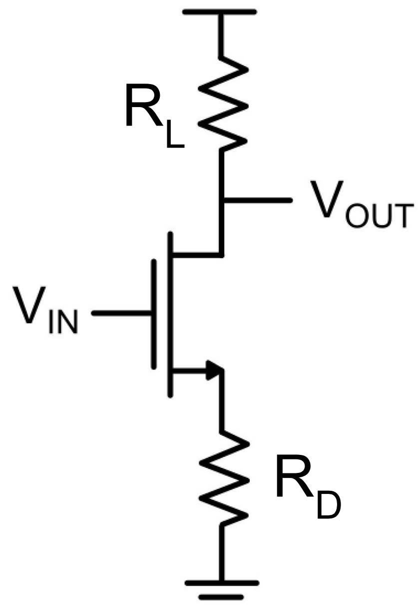

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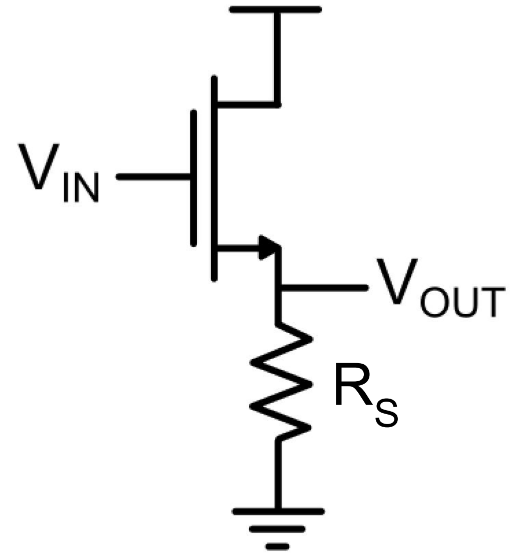

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G_m	g_m	Same	$g_m/(1+g_m R_D)$	⬇️	g_m	Same
R_{out}	$r_o \| \| R_L$	⬇️	$(r_o(1+g_m R_D)) \| \| R_L$	Varies	$R_s \| \| (1/g_m)$	⬇️⬇️

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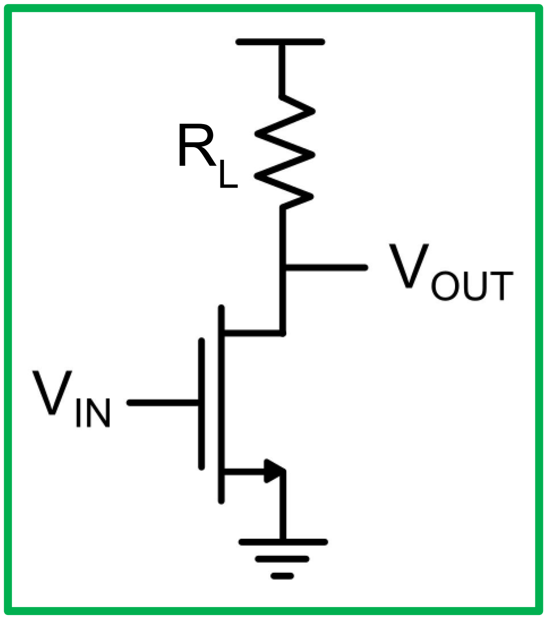

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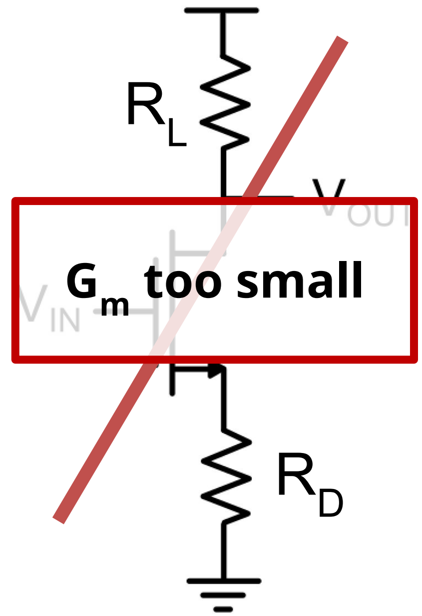

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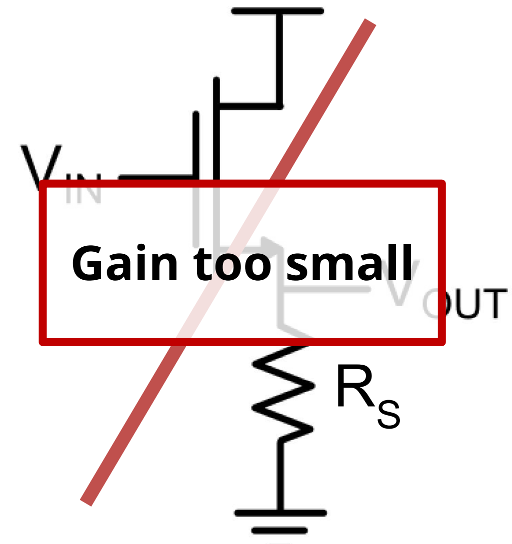

	Equation	Effect	Equation	Effect	Equation	Effect
G_m	g_m	Same	$g_m/(1+g_m R_D)$	⬇️	g_m	Same
R_{out}	$r_o \| \| R_L$	⬇️	$(r_o(1+g_m R_D)) \| \| R_L$	Varies	$R_s \| \| (1/g_m)$	⬇️⬇️

Step 2: What parameters and constraints exist?

Make a list of relevant equations and sort out how many "free" variables you really have.

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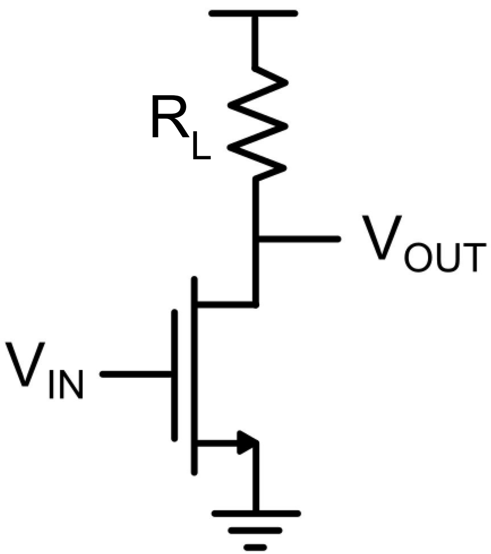

Design constraints	Relevant equations
Gain > 10	$A_V = G_m R_{out} = g_m(r_o\|\|R_L)$
BW > 1 MHz	$f_{BW} \approx 1/(2\pi(r_o\|\|R_L)C_L)$
Output swing within 500 mV of supply rails	$V_{OUT} > V_{GS}-V_T$ $V_{min} = V_{GS}-V_T$

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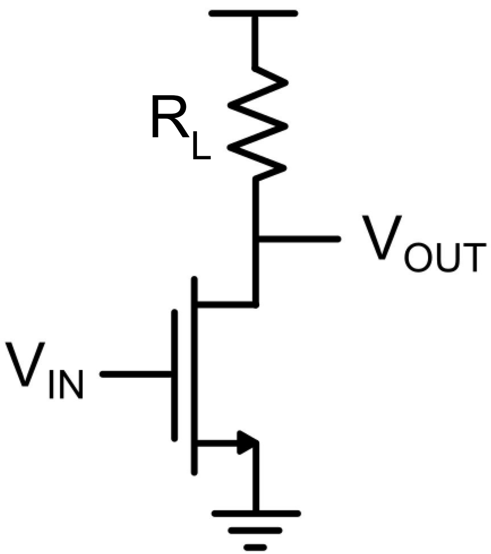

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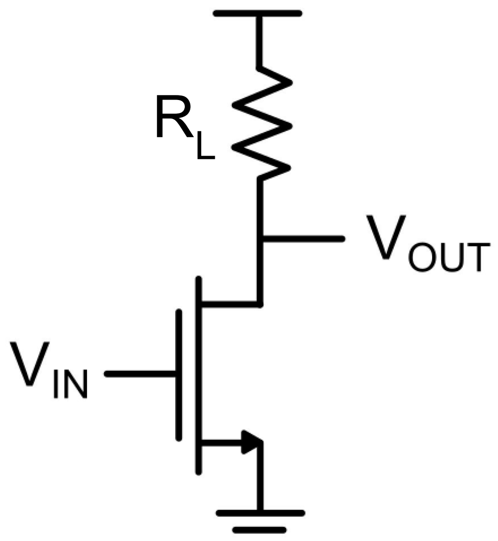

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$$\boxed{R_L = \frac{V_{DD} - V_{OUT}}{I_{DS}}}$$

Full equations for R_{out} and G_m:

$$R_{out} = r_o || R_L = \frac{1}{I_{DS}} \frac{V_{DD} - V_{OUT}}{(1 + \lambda(V_{DD} - V_{OUT}))} \approx \frac{2(V_{DD} - \boldsymbol{V_{OUT}})}{k' \boldsymbol{\frac{W}{L}} (\boldsymbol{V_{GS}} - V_{TH})^2}$$

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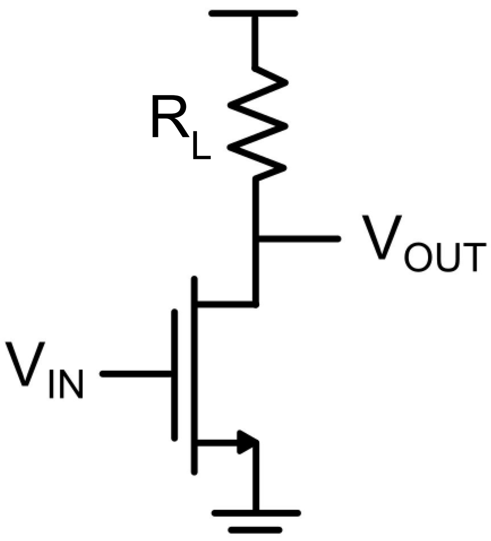

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Step 3: How do constraints impact parameters?

Solve equations to find acceptable design parameter ranges.

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1) Swing constraint: $V_{min} \leq 500$ mV

$$V_{min} = V_{GS} - V_T \quad \Rightarrow \quad V_{GS} - V_T \leq 500\ mV$$

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$$G_m R_{out} = k'\frac{W}{L}(V_{GS} - V_{TH})\frac{2}{k'\frac{W}{L}(V_{GS} - V_{TH})^2}\frac{V_{DD} - V_{OUT}}{(1 + \lambda(V_{DD} - V_{OUT}))}$$

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Bandwidth: $R_{out} \le 32\ k\Omega$

$$G_m R_{out} = \cancel{k'\frac{W}{L}(V_{GS} - V_{TH})}\frac{2}{\cancel{k'\frac{W}{L}}(V_{GS} - V_{TH})^{\cancel{2}}}\frac{V_{DD} - V_{OUT}}{(1 + \lambda(V_{DD} - V_{OUT}))}$$

$$= \frac{2}{(V_{GS} - V_{TH})}\frac{V_{DD} - V_{OUT}}{(1 + \lambda(V_{DD} - V_{OUT}))}$$

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$$10 \leq \frac{2}{(V_{GS} - V_{TH})}\frac{V_{DD} - V_{OUT}}{(1 + \lambda(V_{DD} - V_{OUT}))}$$

$$V_{GS} - V_{TH} \leq \frac{2}{10}\frac{5V - 2.5V}{(1 + 0.01\ V^{-1}(5V - 2.5V))} \approx 500\ mV$$

Step 3: How do constraints impact parameters?

Solve equations to find acceptable design parameter ranges.

$$G_m = g_m = k'\frac{\boldsymbol{W}}{\boldsymbol{L}}(\boldsymbol{V_{GS}} - V_{TH})$$

$$R_{out} = \frac{2(V_{DD} - \boldsymbol{V_{OUT}})}{k'\frac{\boldsymbol{W}}{\boldsymbol{L}}(\boldsymbol{V_{GS}} - V_{TH})^2}$$

1) Swing constraint: V_{min} ≤ 500 mV

$$V_{min} = V_{GS} - V_T \rightarrow V_{GS} - V_T \leq 500\ mV$$

2) Bandwidth & gain constraints:

Gain: $G_m R_{out} \geq 10$

Bandwidth: $\boldsymbol{R_{out} \leq 32\ k\Omega}$

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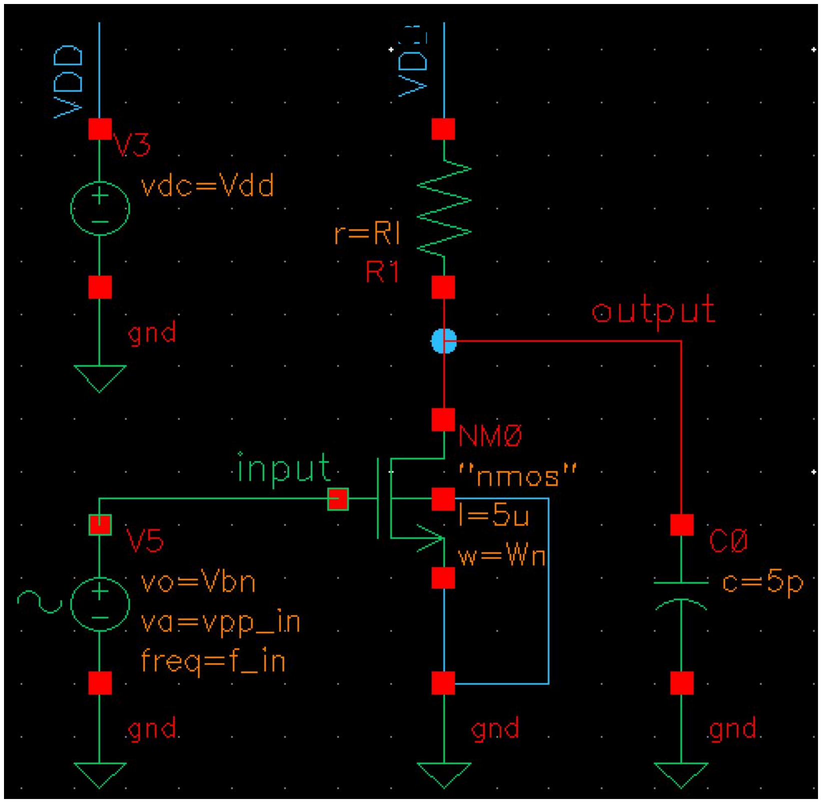
Parameter	Value
W/L	7
V_{GS}	0.5 V + V_{TH} = 1.3 V
I_{DS}	78 µA
R_L	$(V_{DD}-V_{OUT})/I_{DS}$ = 32 kΩ

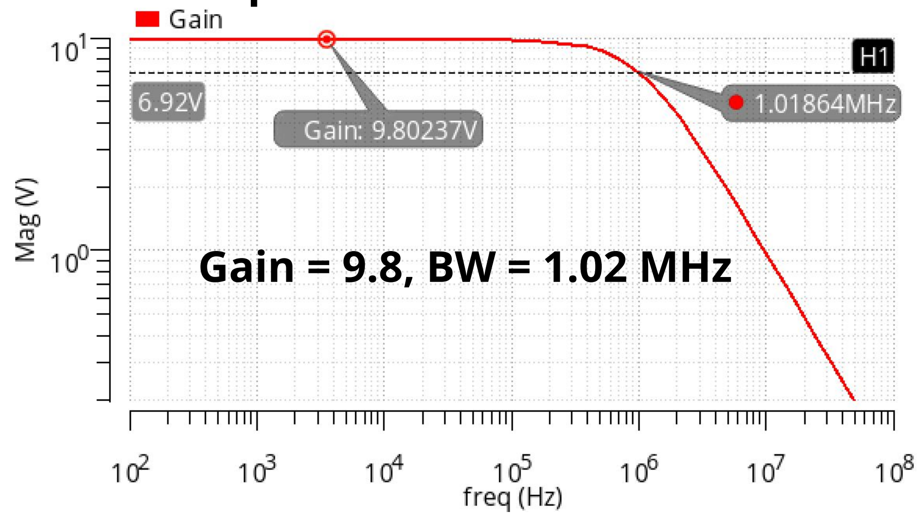
Step 4: Does this actually work?

Verify your design performance in a circuit simulator.

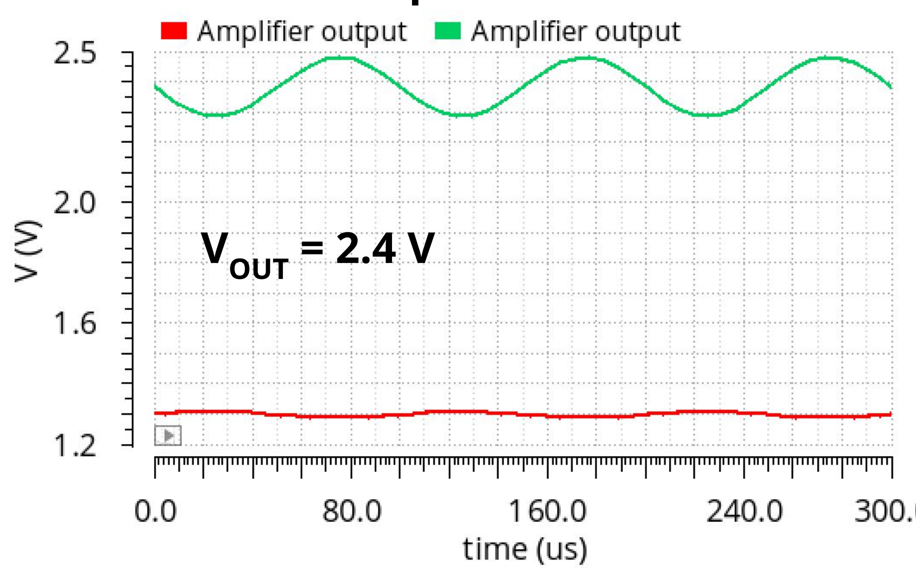
Simulation



AC Response:



Transient Response:



Pretty close! Gain is a little short, so let's increase W/L to boost g_m since R_L dominates R_{OUT}.

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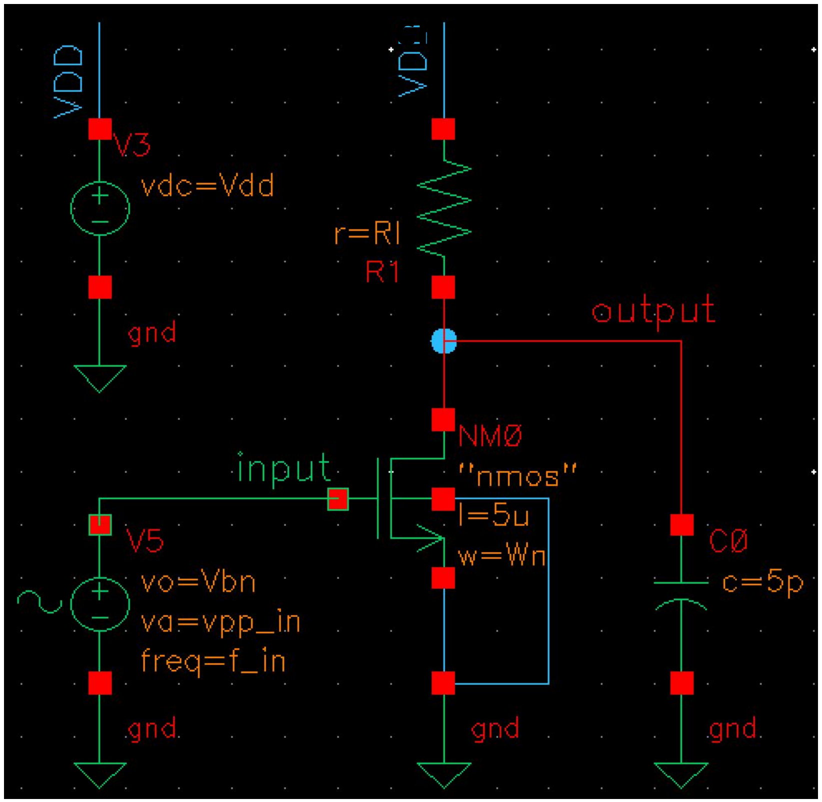

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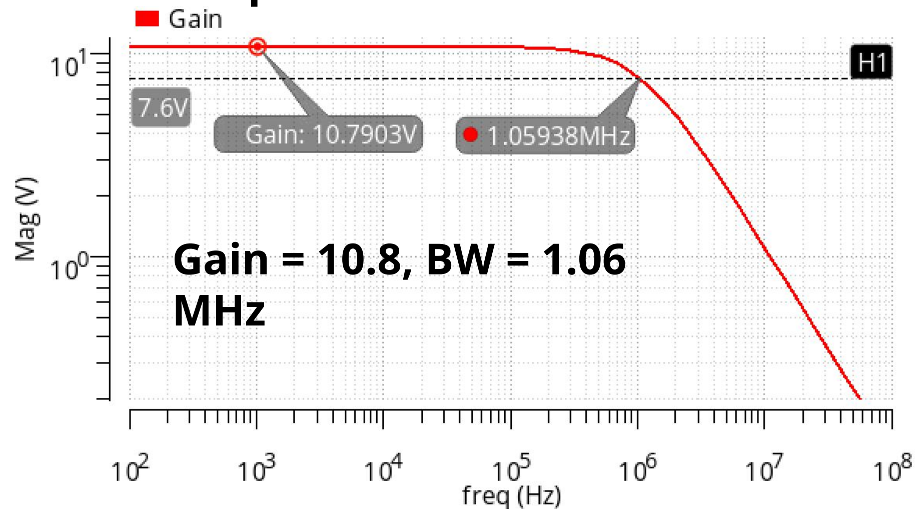

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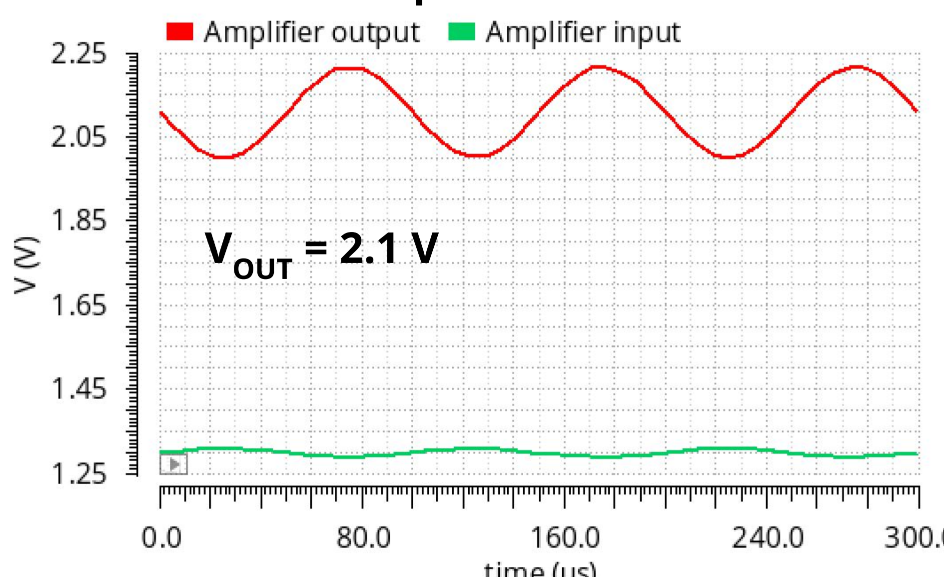

Looks like this will do the job!

Final Note

- Design goals usually involve some sort of optimization:
  - Smallest area
  - Lowest power
  - Highest bandwidth
  - Highest gain
  - Lowest noise
  - “Best” figure of merit (combination of parameters)
- Mathematical solution:
  - Find where derivative of performance metric with respect to design parameters is 0
- Practically:
  - Choose topology carefully for target specifications
  - Identify *key* design parameters