EE 140/240A Lab

About Me

Matthew Dharmawan

- 3rd Year Undergraduate Student
- OH: Every Monday from 5-6pm at Cory 400

  Come ask anything about the class (homework, lecture, labs, project, exams) (also Homework are due Monday, so you can get your last minute questions answered here)

- I run both the labs
  - Tues: 11am-2pm, 2pm-5pm

Lab Logistics

- Come to any of the two lab times, but you must attend lab every week, unless you are done with the lab assignment.

- There will be no prelabs for this class, but a lab report will be turned in at the due date. Please email me for any extenuating circumstances.

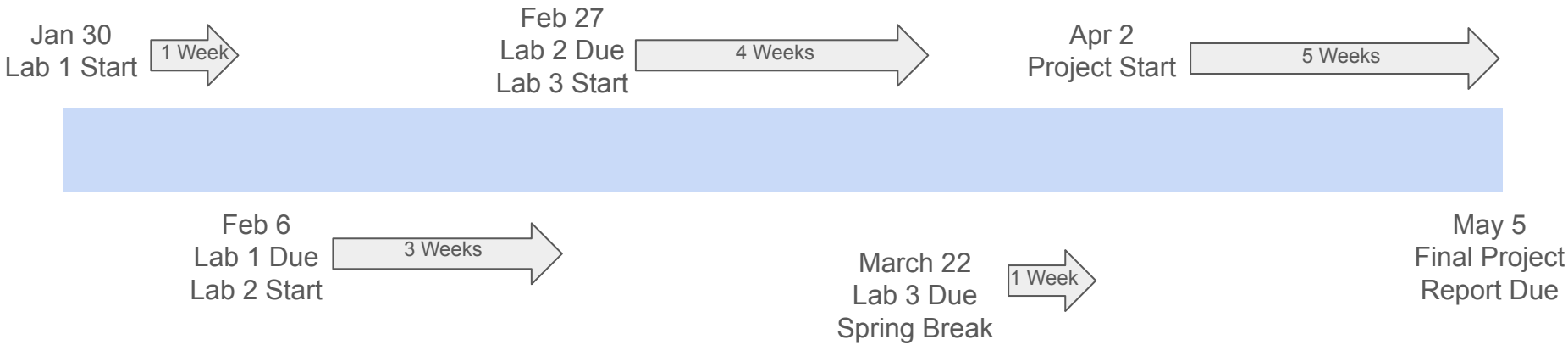
- Some labs will have a checkoff component as well (Lab 1 has a checkoff **and** a report). Think of the checkoff like a checkpoint to ensure you are on track.

- From the syllabus, Lab makes up 25% of your grade. This includes the 3 lab assignments and the project.

Lab Timeline

EE140/240A is all about Amplifier Design

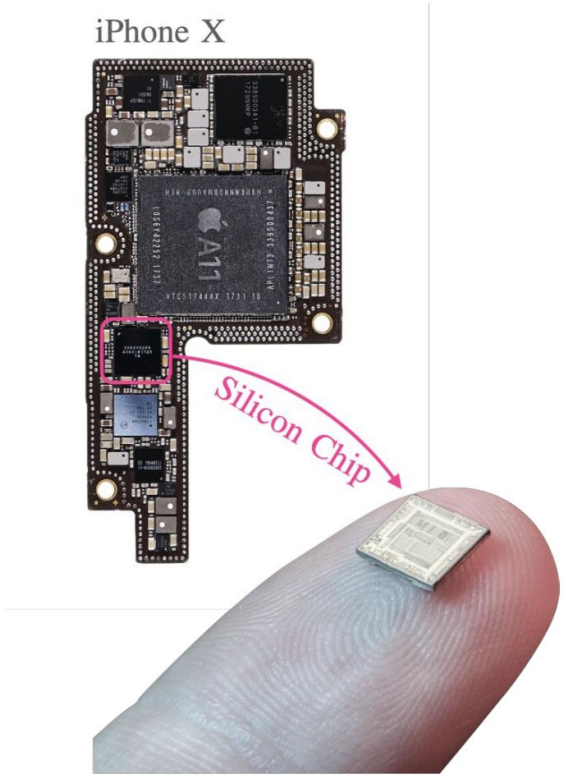
- Lab 1: Introduction to Cadence
- Lab 2: Designing Amplifiers via Hand Calculations
- Lab 3: Designing Amplifiers via Python/Matlab Scripts
- Project: Amplifier Design for an Application



Lab 1

Introduction to Cadence

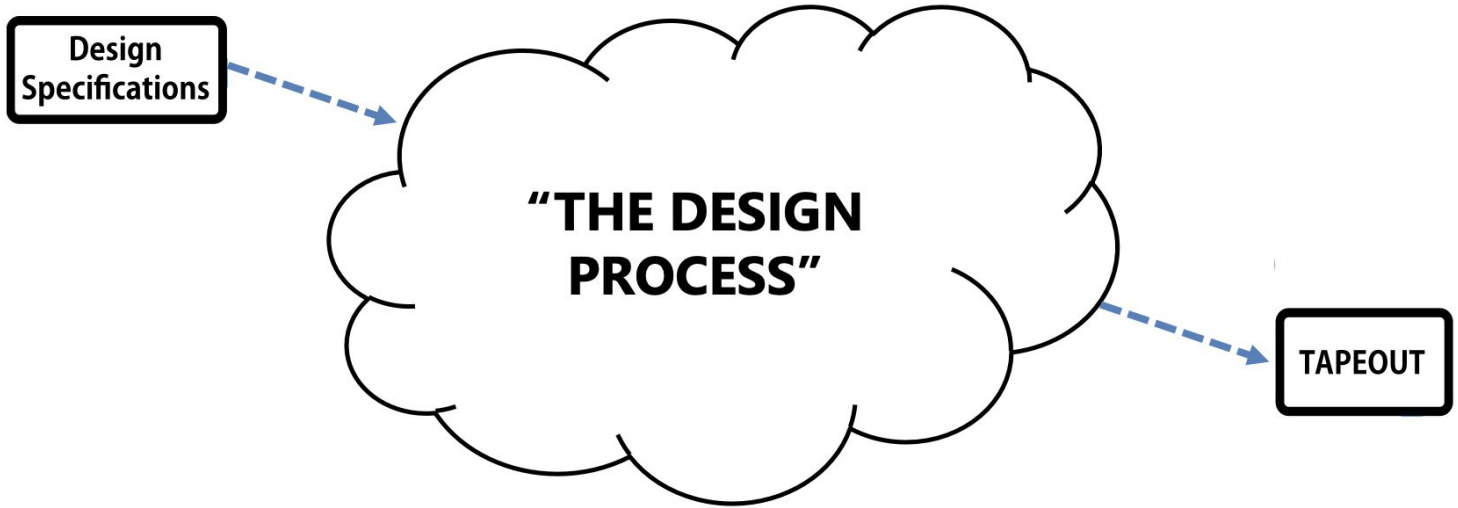
Introduction to **analog IC design flow** and cadence



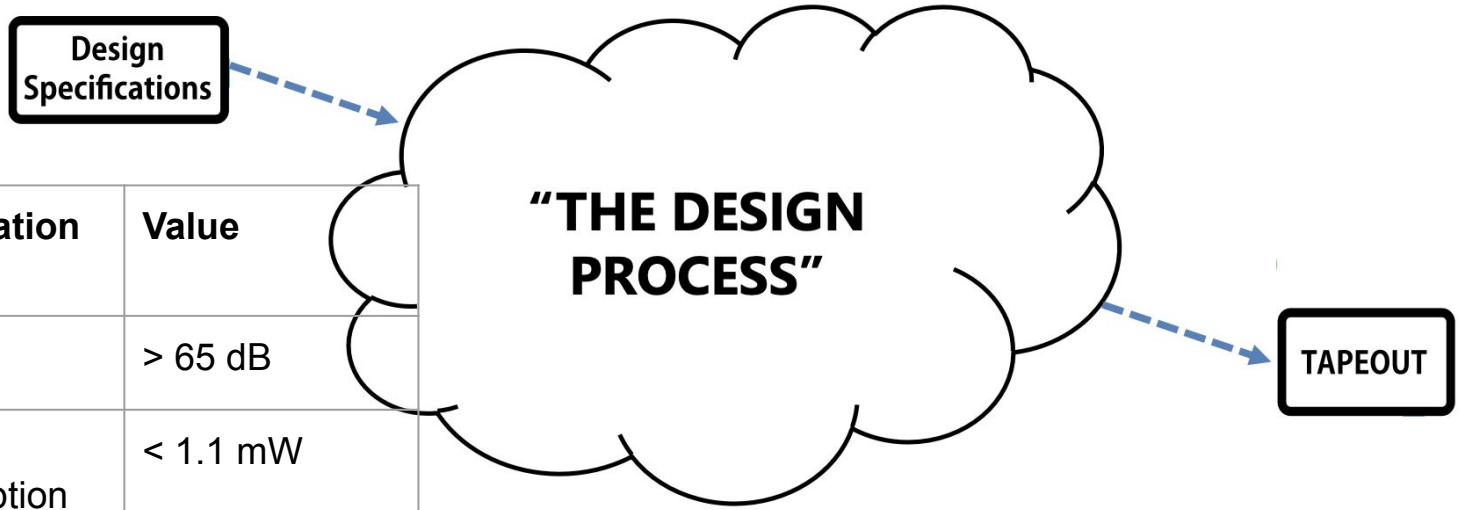
Introduction to **analog IC design flow** and cadence

Specification	**Value**
Gain	> 65 dB
Power Consumption	< 1.1 mW
Bandwidth	> 100 MHz
Setting Time	200 ns

Introduction to **analog IC design flow** and cadence



Introduction to **analog IC design flow** and cadence



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Power Consumption	< 1.1 mW
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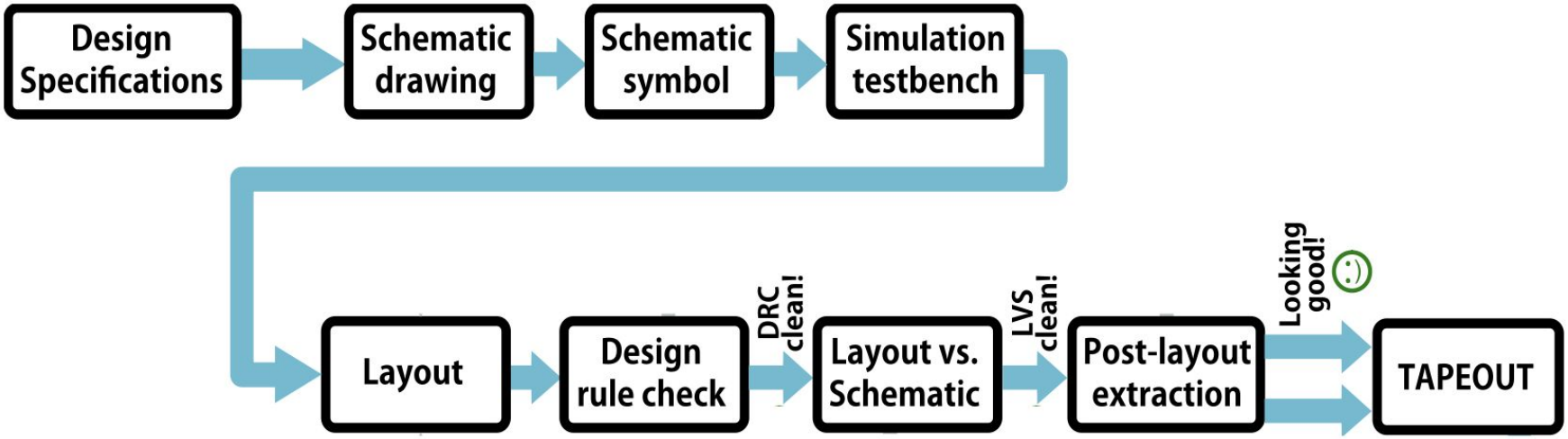
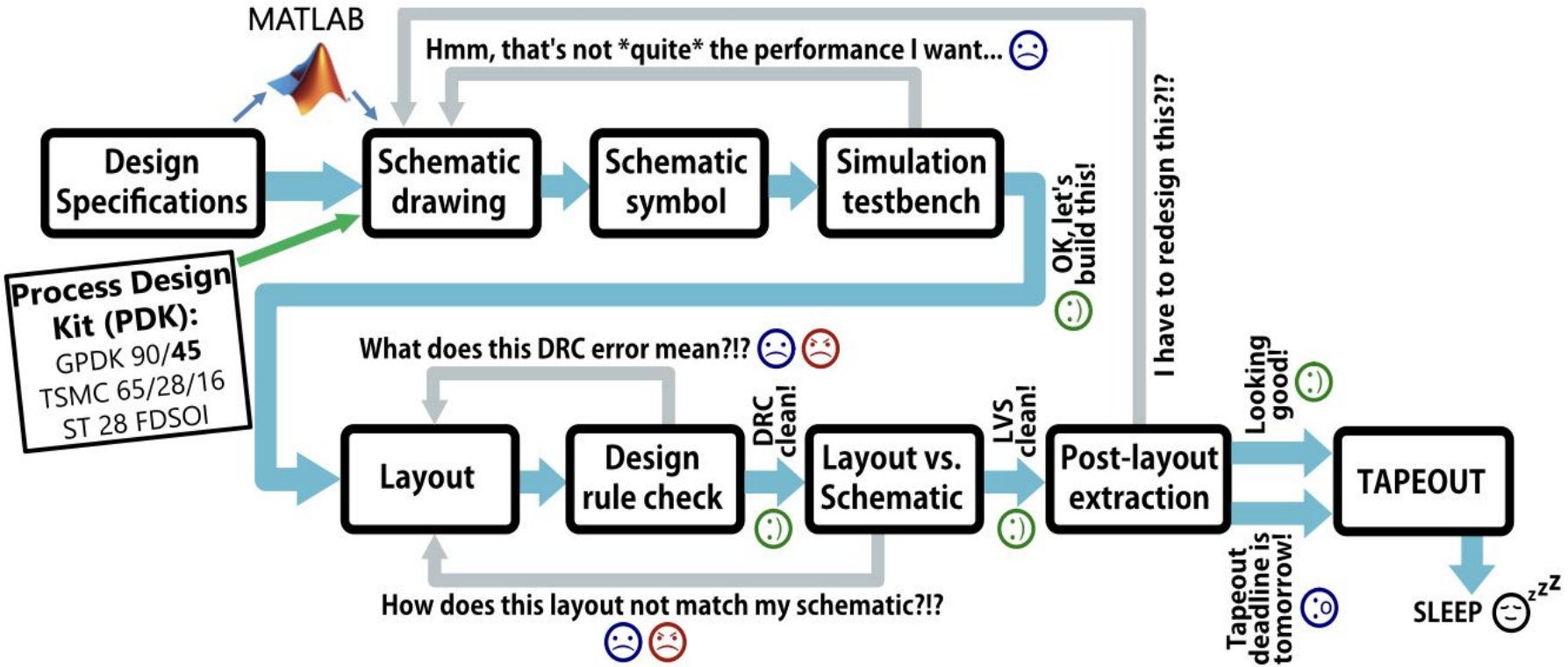
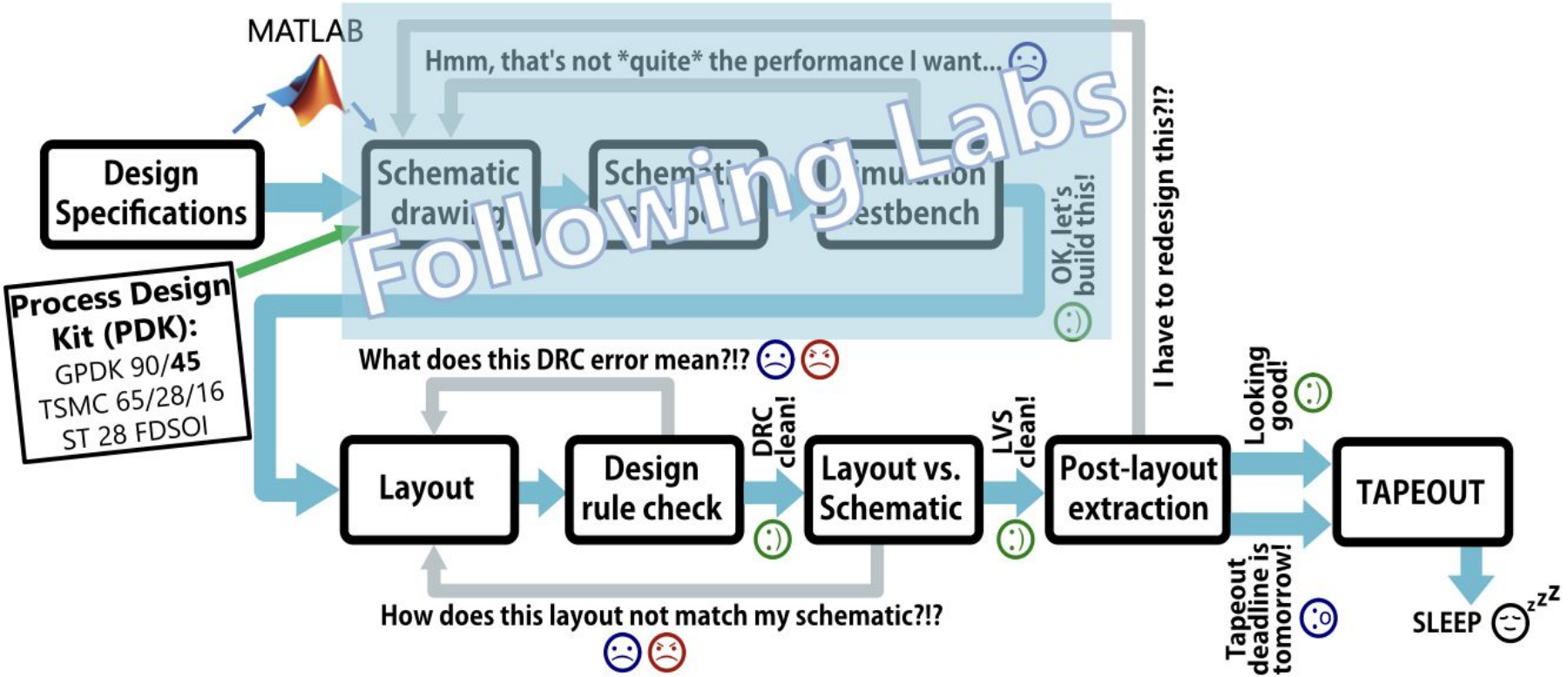
Steps along the Design Process

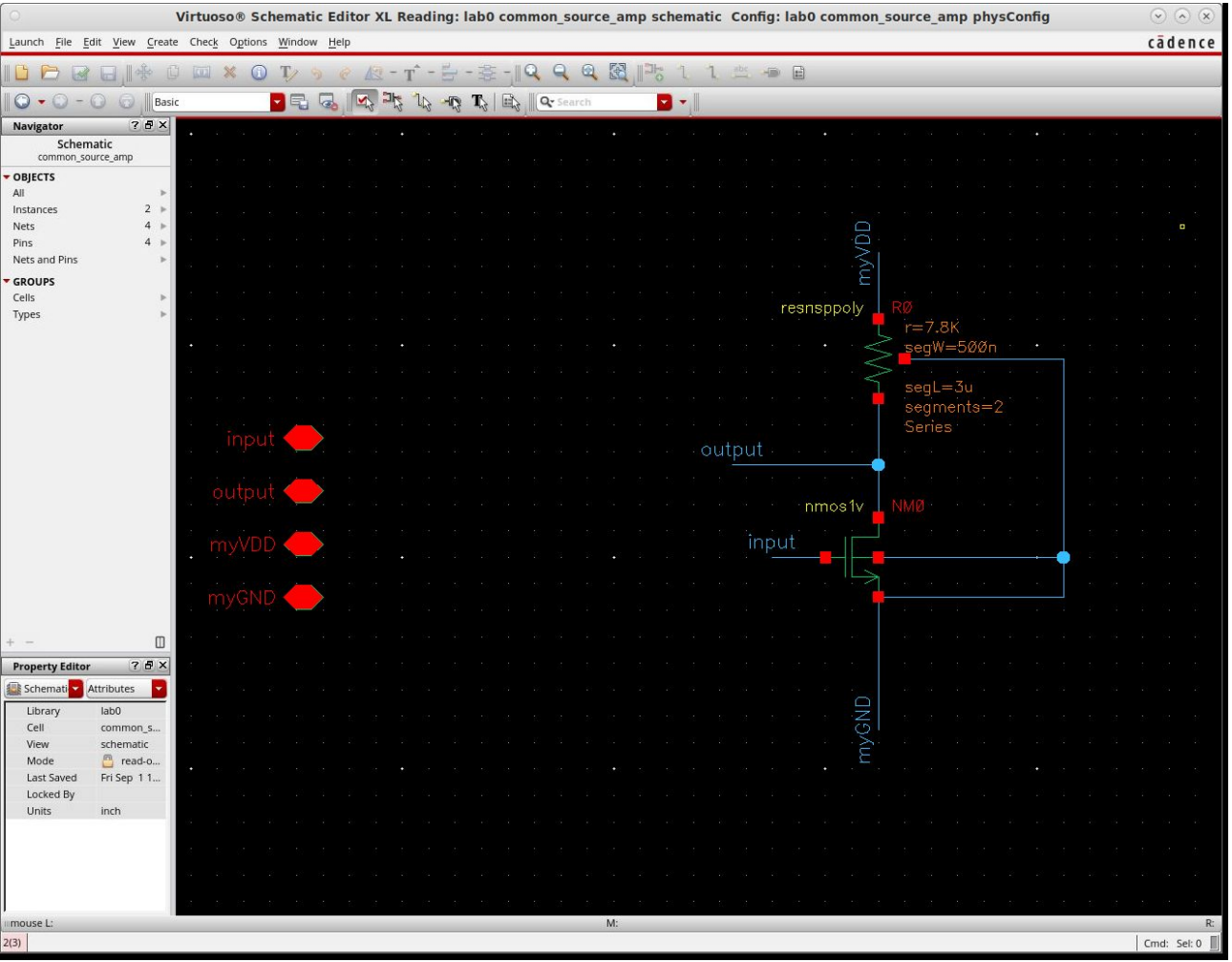


More Realistic Process…

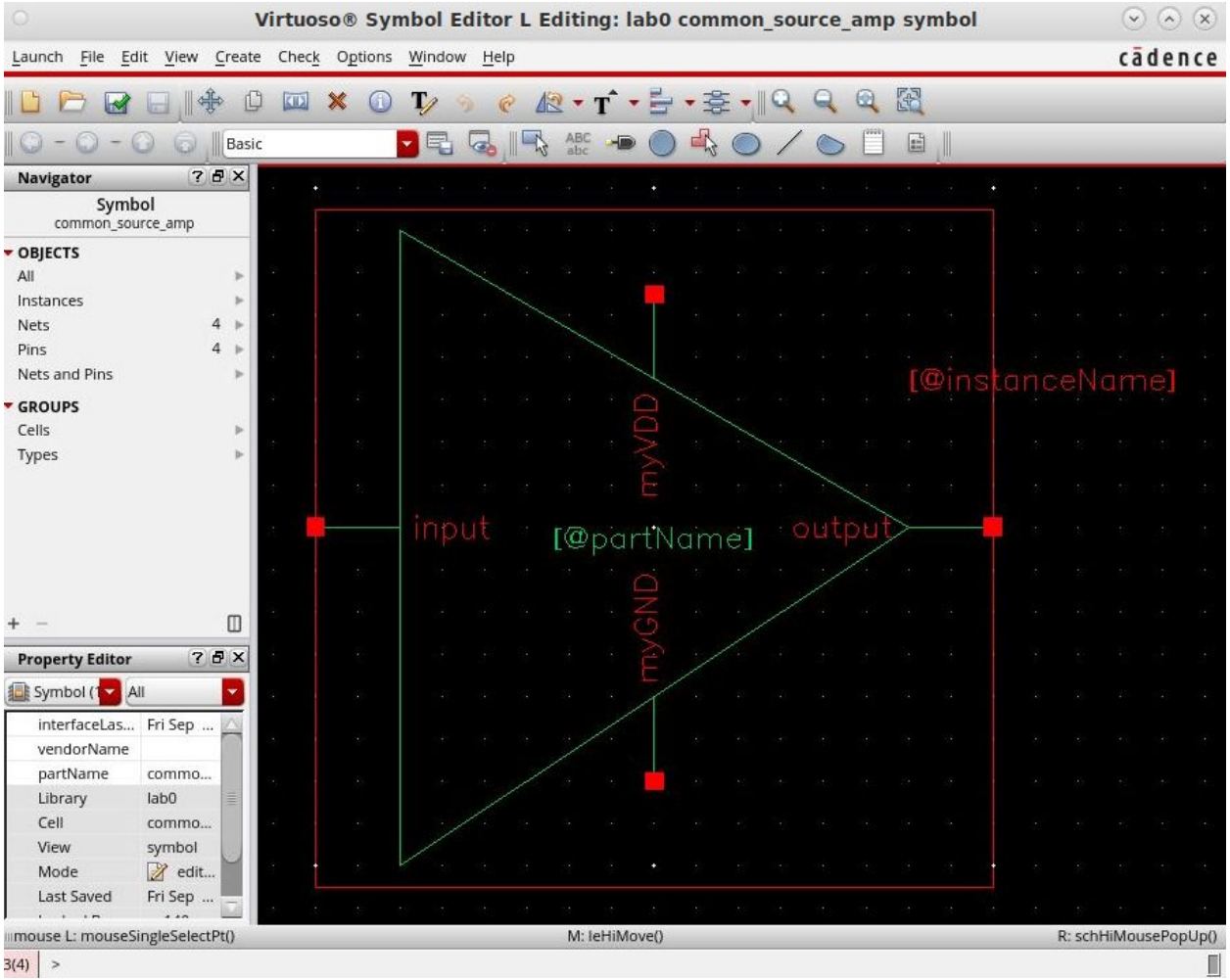


More Realistic Process…

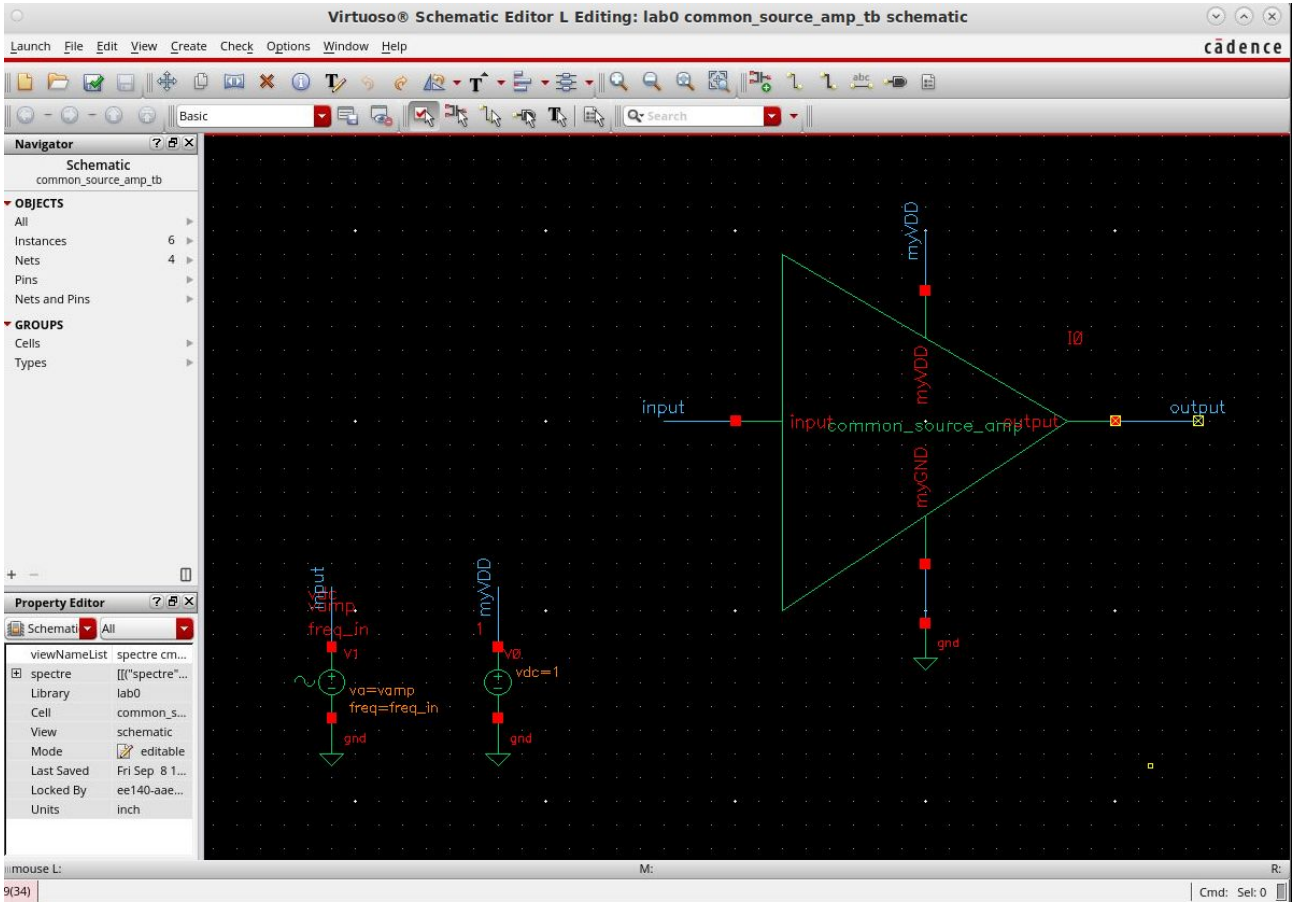




1. Schematic Drawing



2. Schematic Symbol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Launch File Edit View Create Check Options Window Help
cadence
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common_source_amp_tb
OBJECTS
All
Instances 6
Nets 4
Pins
Nets and Pins
GROUPS
Cells
Types
Property Editor
viewNameList spectre cm...
spectre [[("spectre"...
Library lab0
Cell common_s...
View schematic
Mode editable
Last Saved Fri Sep 8 1...
Locked By ee140-aae...
Units inch
myVDD
input
input
common_source_amp
output
output
myGND
gnd
vamp
freq_in
V1
va=vamp
freq=freq_in
gnd
myVDD
1
V0
vdc=1
gnd
mouse L:
M:
R:
Cmd: Sel: 0

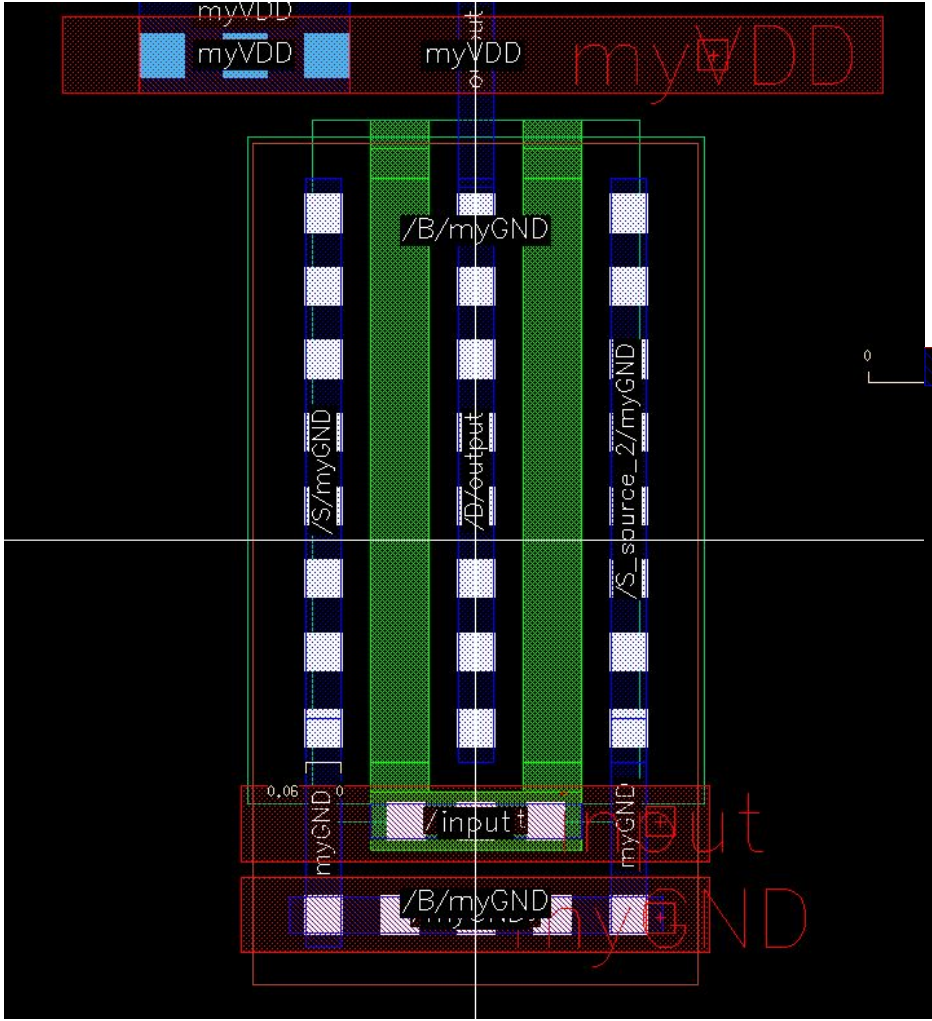
3. Testbench

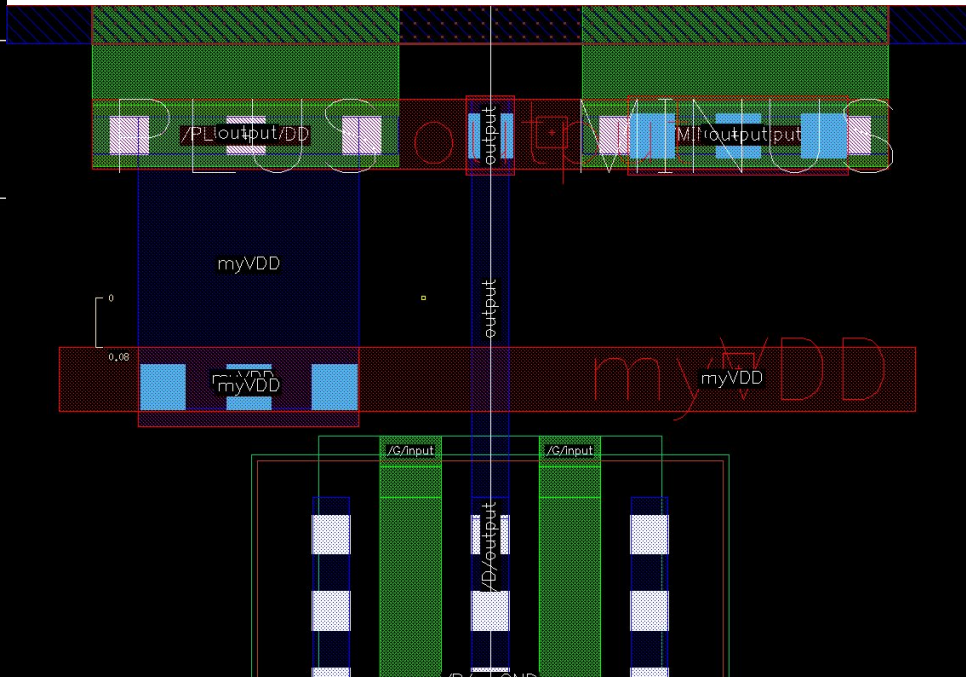
Then there is Layout, DRC, LVS, and Post-Layout Extraction…

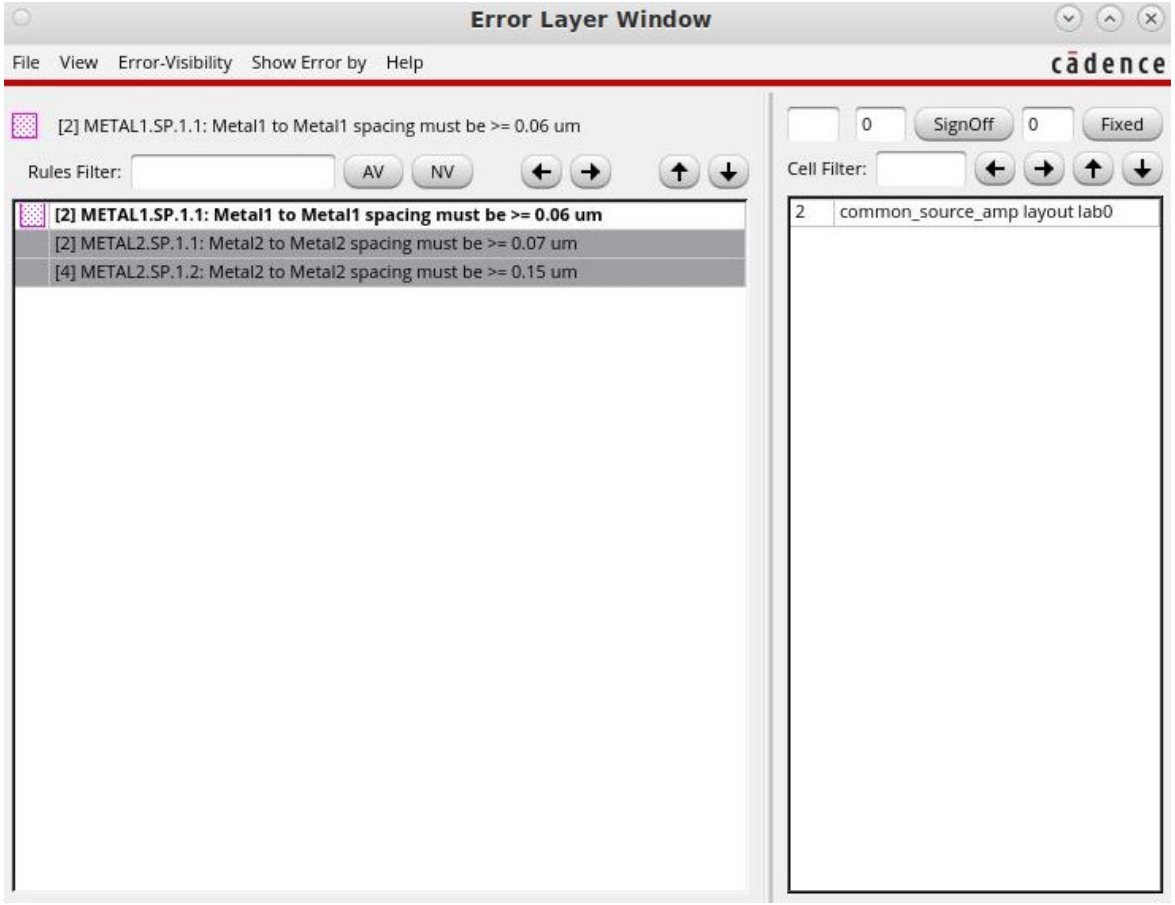
(you won’t do this in this class, but it is likely you would do this in industry or research!)

Here is a quick overview of these steps:

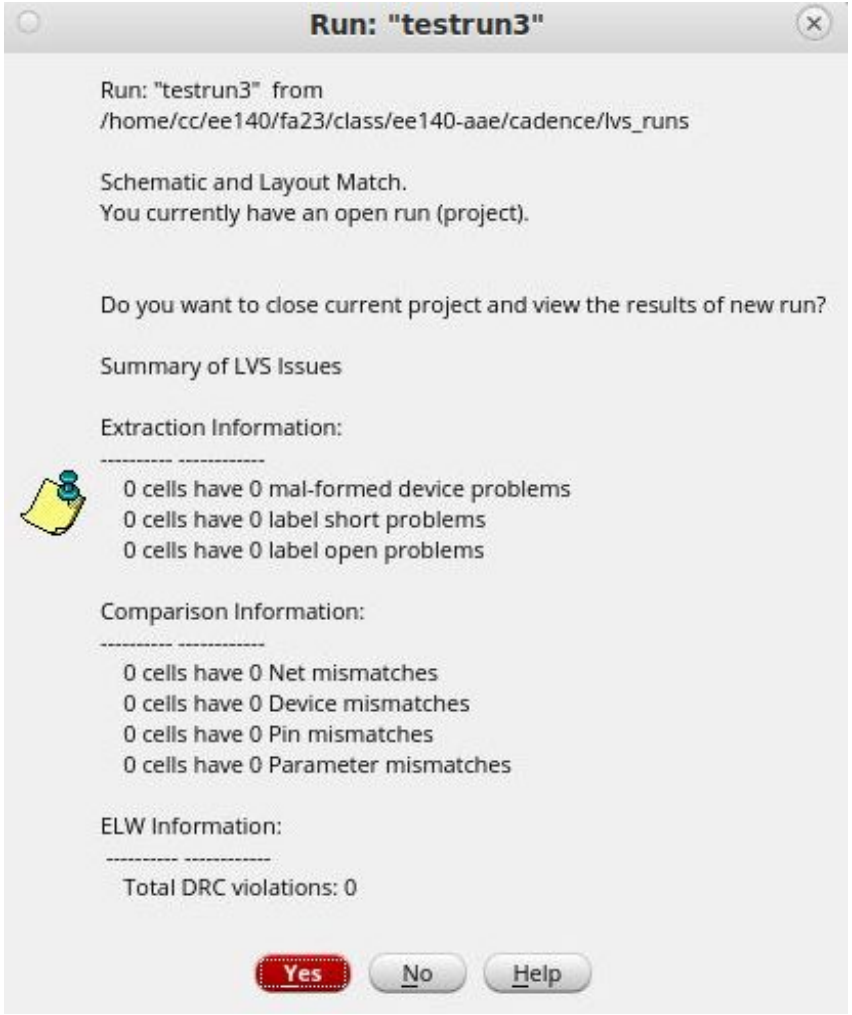
4. Layout


myVDD
myVDD
myVDD
/B/myGND
/S/myGND
/D/output
/S_source_2/myGND
0.06
myGND
/input
myGND
/B/myGND

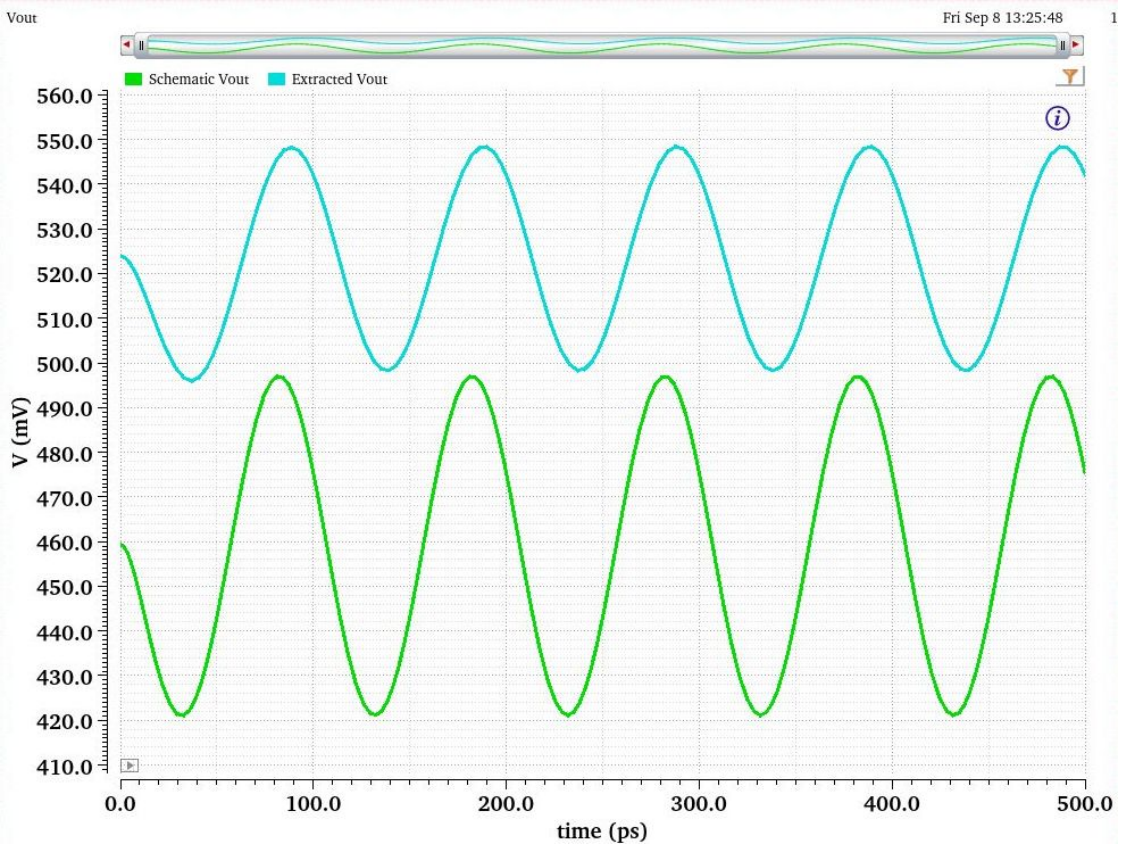

/PL/output/DD
output
myVDD
0.08
myVDD
myVDD
/G/input
/G/input



5. DRC (Design Rule Checking)



6. LVS (Layout vs. Schematic)



7. Post-Layout Extraction

Instructional Machines

- Can ssh to eda-X.eecs.berkeley.edu, where X = 1-11
- Can use remote login via X2Go (X2Go lets you return to your session later
- But in my experience, the lab computers are much, much faster.
- Use instructional account credentials to log on (get account at https://acropolis.cs.berkeley.edu/~account/webacct/)
- Don’t forget to save your work frequently and log out of machines when you are finished

Deliverables

- See the lab handout for the required plots / screenshots / explanations.
- There is a checkoff component and a lab report submission.
- Let me know if you have trouble with accounts, etc.
- Make sure your plots are legible!
- **Lab is Due February 6th at 11:59 pm.**
  - Checkoff in-person with Matthew
  - Report submitted to Gradescope