

Problem 1: MOS Models

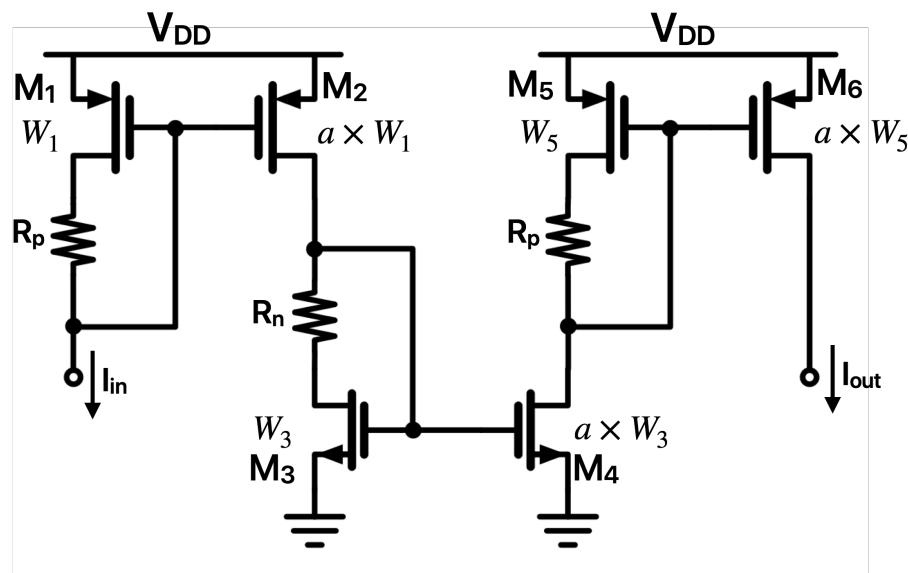
Answers:

- a) A less than B, because I_D varies inversely with L in saturation.
- b) A similar to B, because the threshold voltage does not depend on L.
- c) A greater than B, because A has a smaller K and thus must be biased stronger, or because V_{gs} is proportional to \sqrt{L} .
- d) A less than B, because r_o is bigger for the longer device, and thus g_{ds} is smaller.
- e) A greater than B, because the area of the gate ($W \times L$) is larger.
- f) A similar to B, because C_{gd} is proportional to the device width and that is the same in both devices.
- g) A greater than B, because the area of A is 2x larger, therefore $\sigma_{W/L}$ is $\sqrt{2}$ smaller, but I_D is 2x smaller. As a percent, the error is $\sqrt{2}$ higher.

2. Multi-stage Current Amplifier

In the midterm exam, we reviewed a single stage current amplifier. Shown below is a three-stage current amplifier that is formed by cascading single gain stages. The design is done such that all devices have the **same length, g_m/I_D , and g_m/C_{GS}** parameters. You may neglect all capacitances except for C_{GS} of the devices and assume that ω_T can be approximated as $\omega_T \approx \frac{g_m}{C_{GS}}$. Other parameters are listed here.

$$\lambda = 0, \quad \gamma = 0, \quad W_6 = a \cdot W_5, \quad W_4 = a \cdot W_3, \quad W_2 = a \cdot W_1$$



- a) What is the small signal DC gain of this amplifier, $\frac{i_{out}}{i_{in}}$?

Each current mirror has a DC gain of a as it is the mirror ratio. Thus, the overall gain of the amplifier is:

$$\frac{i_{out}}{i_{in}} = a \times a \times a = a^3$$

$$\frac{i_{out}}{i_{in}} = a^3$$

- b) Find the pole associated with each mirror node, and then use your answer from part (a) to derive the frequency dependent transfer function of the amplifier, $H(s) = \frac{i_{out}}{i_{in}}(s)$.

You may use transistor specific small signal parameters in your derivation but simplify your result and find the answer in terms of “ s ”, “ a ”, and “ ω_{T_1} ” which is the ω_T of M_1 .

Since all devices have the same $\frac{g_m}{C_{GS}}$, the ω_T is the same for all devices.

Each mirror node adds a pole of $p = \frac{g_m}{(1+a) C_{GS}}$ to the transfer function. We can write:

$$p_1 = \frac{g_{m1}}{(1+a) C_{GS_1}} = \frac{\omega_{T_1}}{(1+a)}$$

$$p_2 = \frac{g_{m3}}{(1+a) C_{GS_3}} = \frac{\omega_{T_3}}{(1+a)} \xrightarrow{f_T \text{ is the same for all devices}} p_2 = \frac{\omega_{T_1}}{(1+a)}$$

$$\text{Similarly, } p_3 = \frac{g_{m5}}{(1+a) C_{GS_5}} = \frac{\omega_{T_1}}{(1+a)}$$

As a result, there are three poles all at the same frequency.

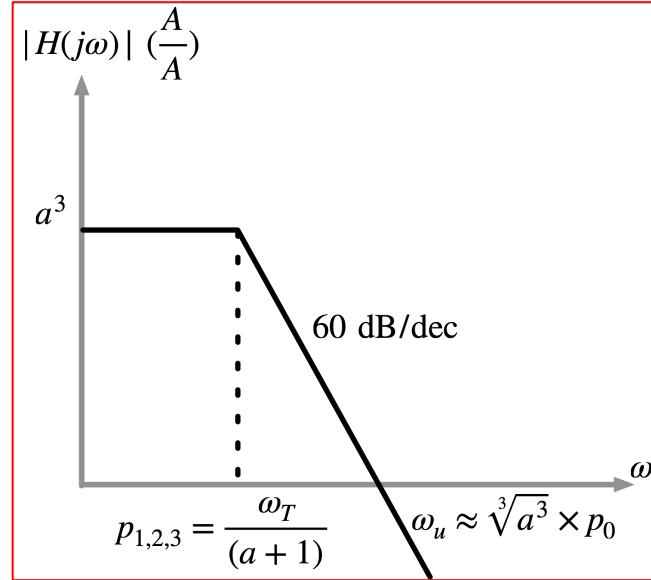
Therefore, the overall transfer function looks as follows:

$$H(s) = \frac{i_{out}}{i_{in}}(s) = \frac{a^3}{\left(1 + \frac{(a+1)s}{\omega_{T_1}}\right)^3}$$

$$H(s) = \frac{i_{out}}{i_{in}}(s) =$$

$$H(s) = \frac{a^3}{\left(1 + \frac{(a+1)s}{\omega_{T_1}}\right)^3}$$

- c) Draw the bode magnitude plot for the above amplifier. Assuming $a > 1$, can you approximate the unity-gain bandwidth frequency (ω_u)?



Since $a \gg 1$, the unity-gain bandwidth frequency can be approximated as:

$$\omega_u \approx \sqrt[3]{a^3} \times p_1 = a \times p_1 = \frac{a}{1+a} \omega_{T_1}$$

$$\omega_u \approx \frac{a}{a+1} \cdot \omega_{T_1}$$

More accurate answer:

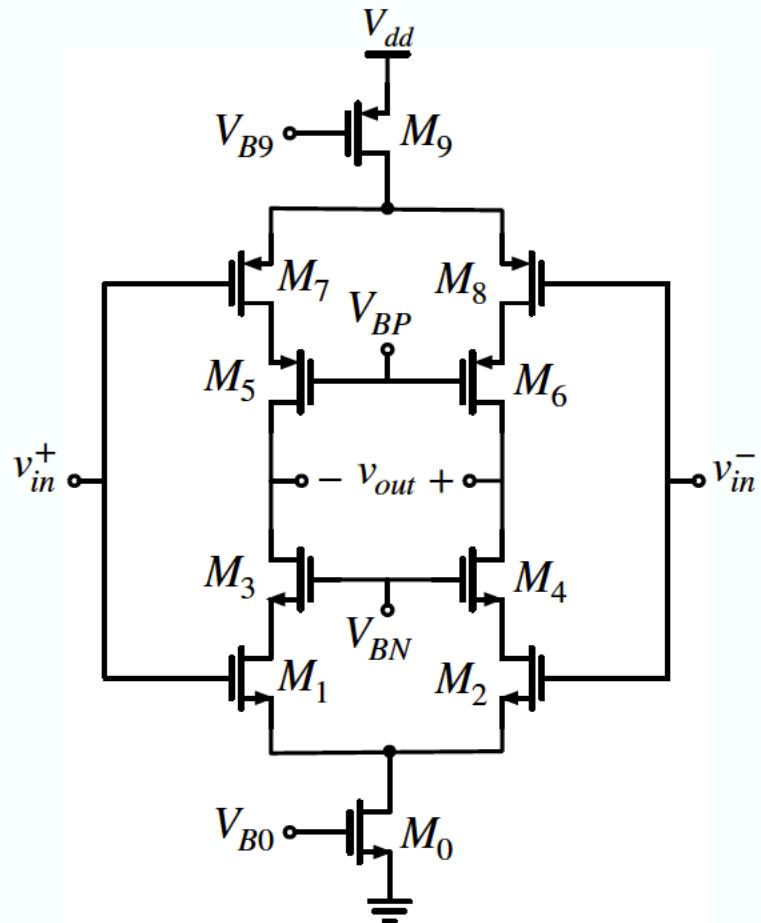
$$\omega_u = \frac{\sqrt{a^2 - 1}}{a + 1} \cdot \omega_{T_1}$$

- d) Current mirrors are widely used in the design of analog circuits to serve as active loads, biasing current sources, etc. and a lot of times are inevitably cascaded when a certain current travels from one subblock to the next, forming current amplifiers like the one above. Interference at the input (e.g. noise of the reference current, or any coupled interference) can propagate and get boosted throughout the path. To prevent this, a bypass capacitance (with one end to AC ground) can be added to limit the bandwidth of this amplifier. To minimize the additional needed capacitance, what is the best location to add one capacitor and why?

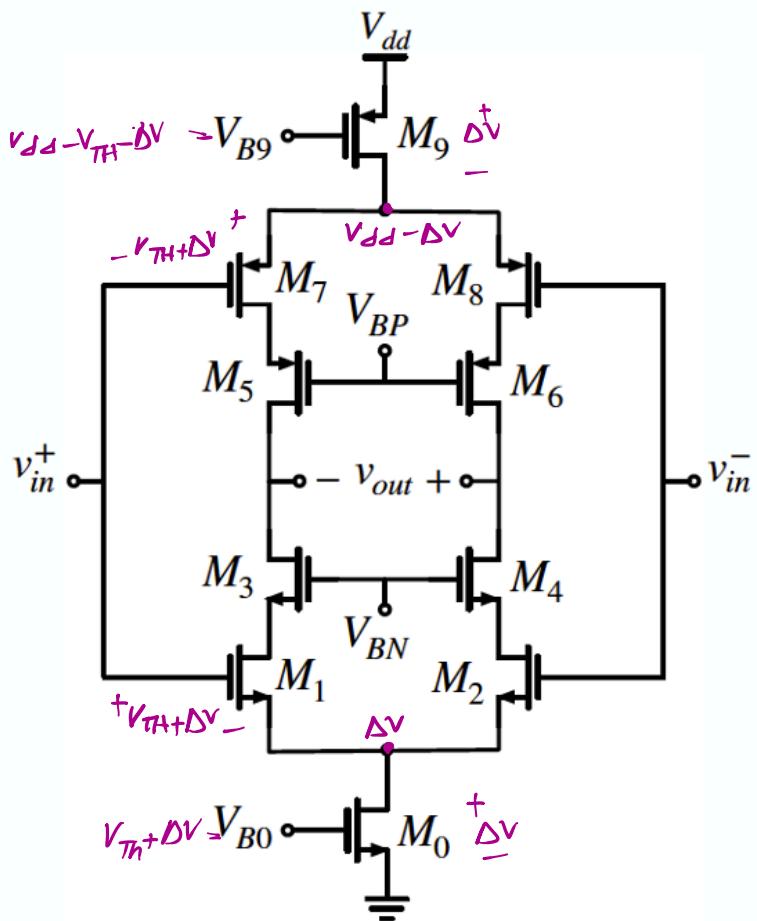
The capacitor should be added at the gate of M_1 and M_2 since that node has the largest resistance to AC ground. This is because the DC current of M_1 is the lowest among all and since all transistors have the same g_m/I_D , g_{m1} would be the smallest giving the largest mirror resistance. This way, with a smaller cap we can limit the bandwidth of the amplifier.

Problem 3. [20 points] Complementary Amplifier

You are designing a power efficient gain stage for your final project in EE140/240A. You read some papers and came across an interesting amplifier with complementary inputs as shown below. You decide to analyze whether this is a good choice for your project. For simplicity, assume $\mu_n = \mu_p$ and all the transistors have the same length, oxide thickness, overdrive voltage ΔV (or v_{ov}) and threshold voltage ($V_{Th} > \Delta V$). Ignore the body effect.



- a. [3 points] Determine the **minimum** power supply voltage $V_{dd,min}$ such that all the devices are biased in saturation. Express your answer in terms of ΔV (or v_{ov}) and V_{Th} of the transistors.

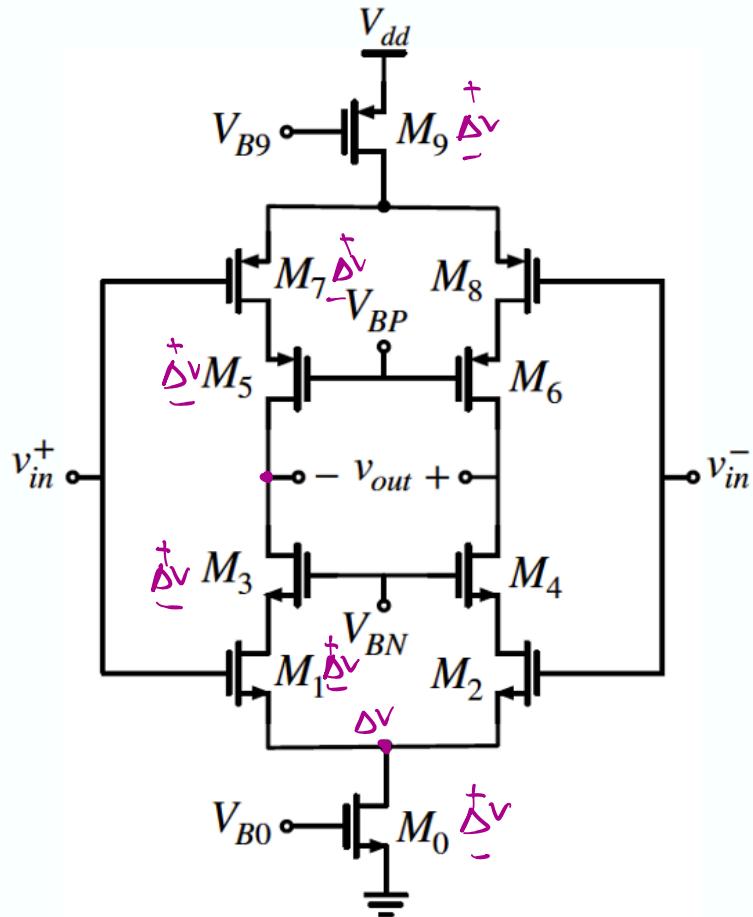


$$\left. \begin{array}{l} M_0 \& M_1: \quad V_{io} \geq V_{Th} + 2\Delta V \\ M_9 \& M_7: \quad V_i \leq V_{dd} - |V_{Th}| - 2\Delta V \end{array} \right\} \text{Therefore: } V_{Th} + 2\Delta V \leq V_{dd} - V_{Th} - 2\Delta V$$

$$V_{dd} \geq 2V_{Th} + 4\Delta V$$

$$V_{dd,min} = 2V_{Th} + 4\Delta V$$

- b. [3 points] Determine the maximum differential peak-to-peak swing of v_{out} when $V_{dd,min}$ is used. Express your answer in terms of ΔV and V_{Th} (and V_{dd} in case you did not answer part (a)).



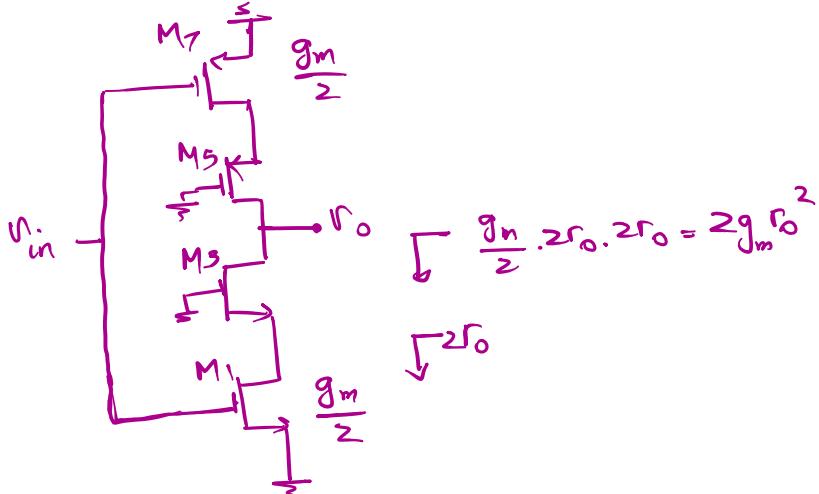
$$3\Delta V \leq v_o^- \leq V_{dd} - 3\Delta V \rightarrow \text{single-ended pp swing} = V_{dd} - 3\Delta V - 3\Delta V \\ = V_{dd} - 6\Delta V \\ V_{dd} = V_{dd,min} = 2V_{Th} + 4\Delta V \\ = 2V_{Th} - 2\Delta V$$

$$\text{differential swing} = 2 \times (2V_{Th} - 2\Delta V) = 4(V_{Th} - \Delta V)$$

$$V_{out,pp} = 4(V_{Th} - \Delta V)$$

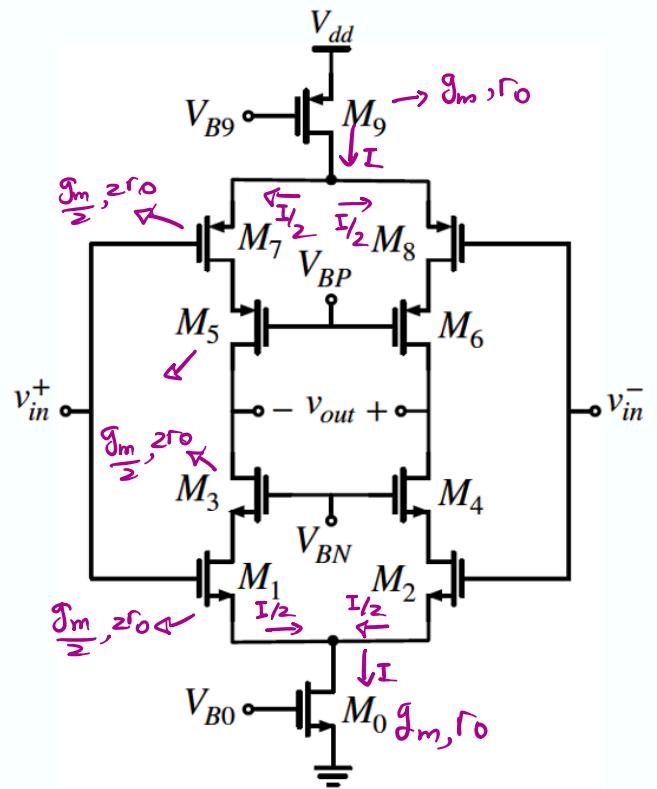
- c. [4 points] Draw the differential-mode half-circuit and determine the differential-mode gain $A_{DM} = \frac{v_{out}}{v_{in}^+ - v_{in}^-}$ of this amplifier. Express your answer in terms of g_m and r_o of M_0 (Hint: recall the scaling of g_m and r_o with drain current). Assume $g_m r_o \gg 1$.

DM half circuit:



$$G_m = g_m$$

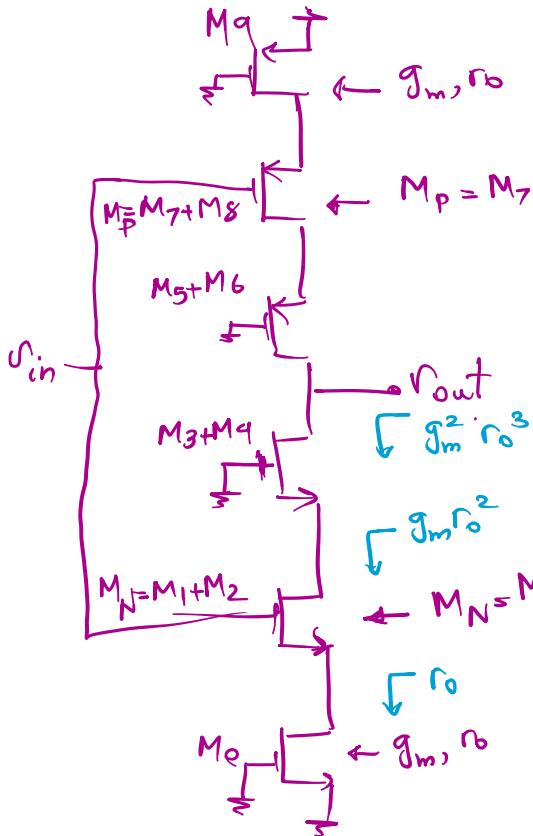
$$R_{out} = \frac{1}{2} (2 g_m r_o^2) = g_m^2 r_o^2 \quad \left. \right\} A_{DM} = g_m^2 r_o^2$$



$$A_{DM} = \frac{v_{out}}{v_{in}^+ - v_{in}^-} =$$

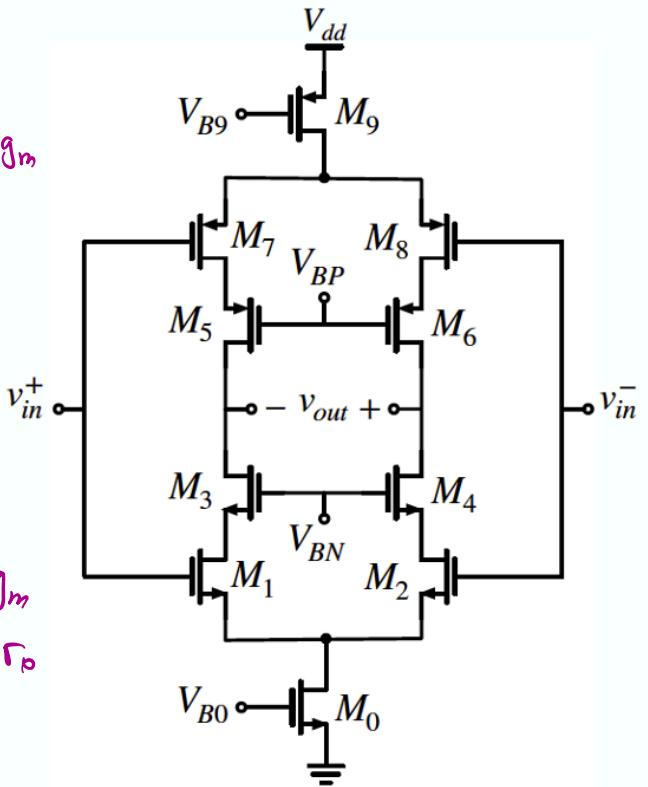
$$(g_m r_o)^2$$

- d. [4 points] Draw the common-mode half-circuit and determine the common-mode gain $A_{CM} = V_{out,CM}/v_{in,CM}$ of this amplifier. Assume $g_m r_o \gg 1$.



$$M_P = M_7 \parallel M_8 \left\{ \begin{array}{l} g_{mP} = \frac{i}{2} g_m + \frac{1}{2} g_m = g_m \\ r_{oP} = 2r_o \parallel 2r_o = r_o \end{array} \right.$$

$$M_N = M_1 \parallel M_2 \left\{ \begin{array}{l} g_{mN} = \frac{1}{2} g_m + \frac{1}{2} g_m = g_m \\ r_{oN} = 2r_o \parallel 2r_o = r_o \end{array} \right.$$



$$\left. \begin{aligned} G_m &\leq g_{mN} + g_{mP} = \frac{1}{r_o} + \frac{1}{r_o} = \frac{2}{r_o} \\ R_{out} &= \frac{1}{2} g_m^2 r_o^3 \end{aligned} \right\} A_{CM} = -g_m^2 r_o^2$$

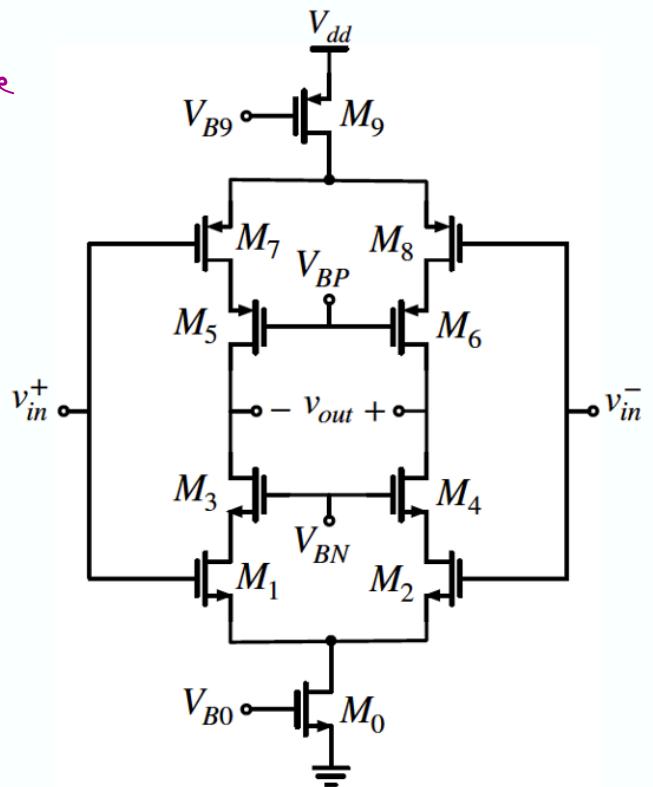
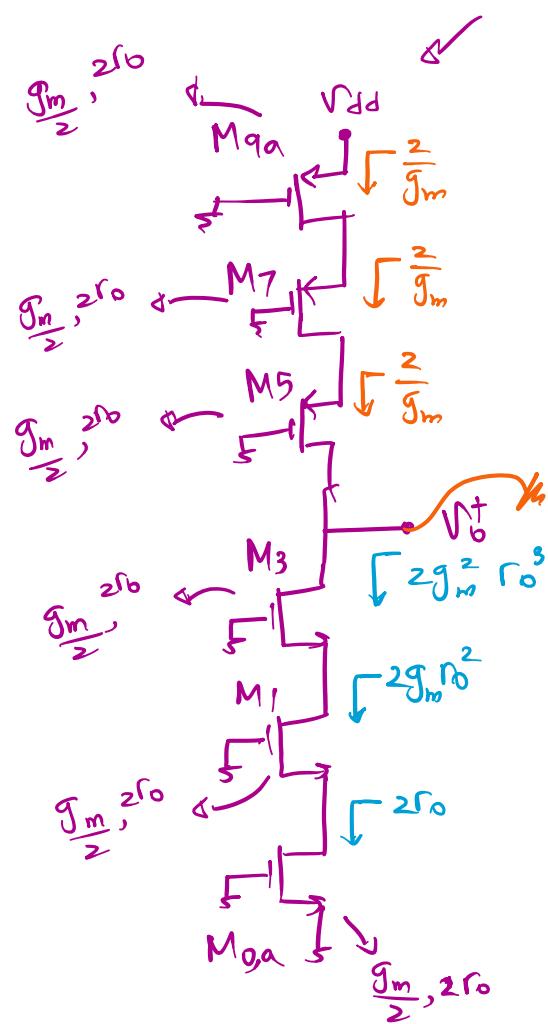
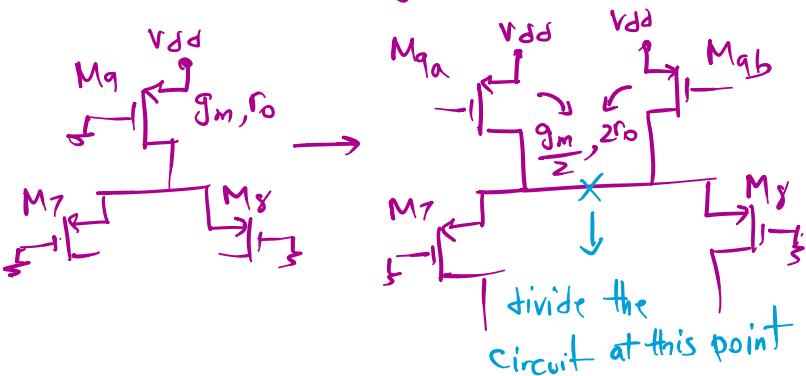
$$CMRR = 1$$

$$A_{CM} = -(g_m r_o)^2$$

- e. [6 points] Determine the power supply gain from the positive supply rail V_{dd} to the single-ended output v_{out+} ($A_{vdd,S} = v_{out+}/V_{dd}$) and to the differential output ($A_{vdd,D} = v_{out}/V_{dd}$). Assume $g_m r_o \gg 1$.

$A_{vdd,D} = 0 \rightarrow V_{dd}$ to v_{out+} & v_{out-} has the same gain.

for simplicity let's divide M_9 & M_0 :



$$\left\{ \begin{array}{l} R_{out} = \frac{1}{2} \left(2 g_m r_o^3 \right) = g_m^2 r_o^3 \\ G_m = \frac{g_m}{2} \end{array} \right.$$

$$A_{vdd,S} = \frac{1}{2} g_m^3 r_o^3$$

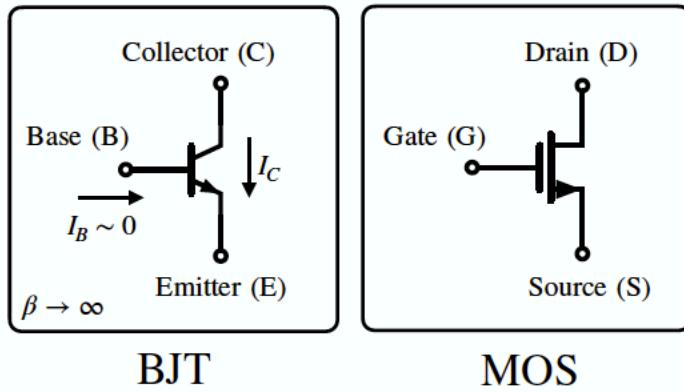
$$A_{vdd,S} = \frac{1}{2} (g_m r_o)^3$$

$$A_{vdd,D} = 0$$

Problem 4. [17 points] Biasing

In this problem we will use Bipolar Junction Transistors (BJTs) to build an amplifier. BJTs are 3-terminal transistors with an exponential relationship between V_{BE} (equivalent to V_{GS} in a MOS device) and I_C (equivalent to I_D in a MOS device).

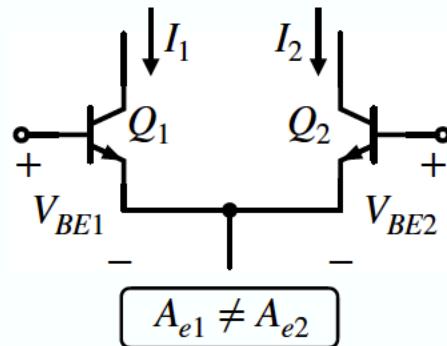
You may ignore the channel length modulation and assume that there is no current flowing into the base (equivalent to the gate in a MOS device) for simplicity. The small-signal equivalent circuit model of a BJT under these conditions is the same as that of a MOS, that is a voltage-controlled current source with v_{be} being the controlling signal and i_c being the output current.



a. [3 points] The collector current of a BJT biased in the forward active region is expressed by

$$I_C = I_s A_e e^{V_{be}/V_T}, \text{ where } V_T = \frac{kT}{q} \text{ and } I_s A_e \text{ is the reverse saturation current (} A_e \text{ is the emitter area of the BJT).}$$

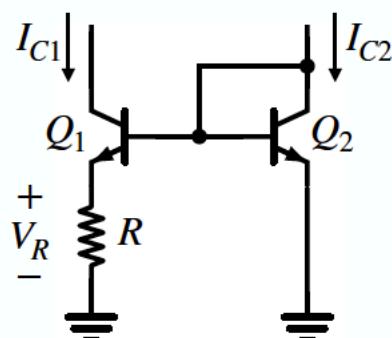
In the following circuit, derive an expression for $\Delta V_{BE} = V_{BE1} - V_{BE2}$ in terms of the emitter areas and collector currents of the transistors.



$$V_{BE1} - V_{BE2} = V_T \ln \frac{I_1}{I_s A_{e1}} - V_T \ln \frac{I_2}{I_s A_{e2}} = V_T \ln \left(\frac{I_1}{I_2} \cdot \frac{A_{e2}}{A_{e1}} \right)$$

$$\Delta V_{BE} = V_T \ln \left(\frac{I_1}{I_2} \cdot \frac{A_{e2}}{A_{e1}} \right)$$

- b. [3 points] Based on the observation from part (a) you are going to build and analyze a commonly used biasing technique called constant-gm. In the following circuit, assuming $I_{C1} = I_{C2}$, find the voltage drop across the resistor V_R in terms of the emitter areas of the devices.

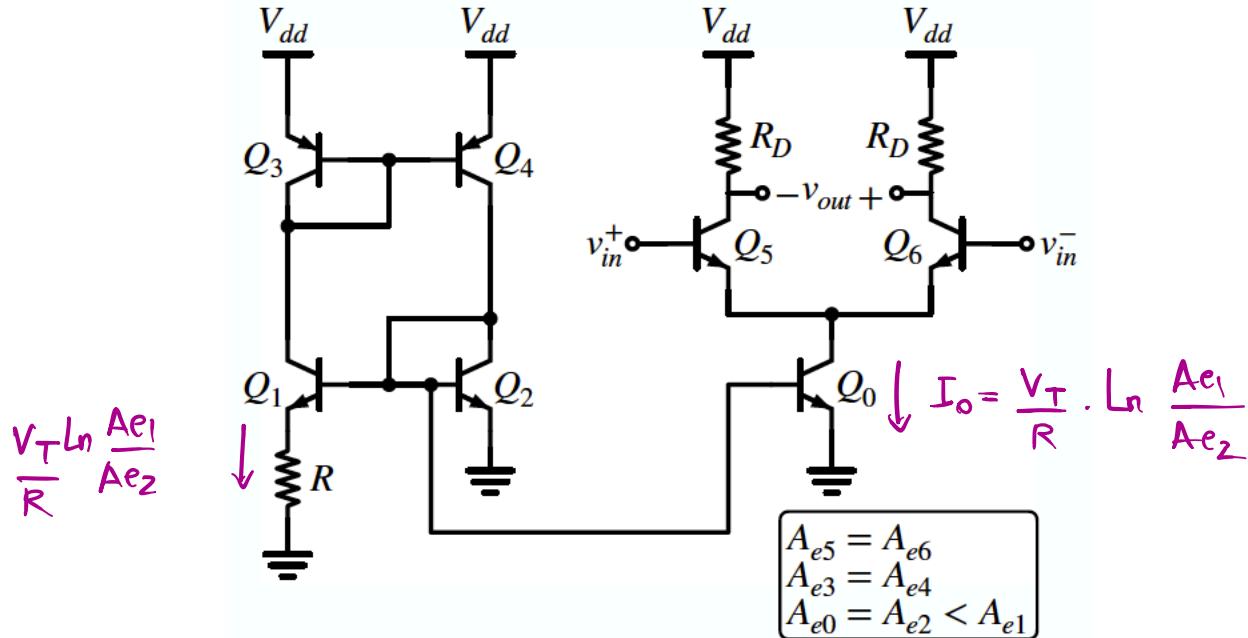


$$A_{e1} > A_{e2}$$

$$V_R = -\Delta V_{BE} \Big|_{I_{C1}=I_{C2}} = V_T \ln \frac{A_{e1}}{A_{e2}}$$

$$V_R = V_T \ln \frac{A_{e1}}{A_{e2}}$$

- c. [6 points] Now, let's bias the tail current source of a resistively loaded differential amplifier using the V_{BE} of Q_2 as shown below. What is the differential-mode gain of this circuit. Given for a BJT $g_m = I_C/V_T$, express your answer in terms of the emitter areas of the transistors.



$$A = g_{m5} \cdot R_D = \frac{I_5}{V_T} \cdot R_D = \frac{I_o}{2V_T} \cdot R_D = \frac{R_D}{2R} \cdot \ln \frac{A_{e1}}{A_{e2}}$$

$$A_{DM} = \frac{v_{out}}{v_{in}^+ - v_{in}^-} = \frac{R_D}{2R} \cdot \ln \frac{A_{e1}}{A_{e2}}$$

- d. [3 points] In the design rule manual of this process, it says all the resistors in this process have a global process variation of up to 20%. What is the maximum gain deviation (in percent) that you would expect from this amplifier?

$$A \propto \frac{R_D}{R} \xrightarrow{(1 \pm 20\%)} \text{gain deviation} = 0$$

$(1 \pm 20\%)$

Global variation affects both R & R_D by the same factor, that is both increase/decrease together & therefore the gain is insensitive to global variations of R & R_D !

- e. [2 points] **EE240A Only:** What is the sensitivity of the gain of this amplifier to temperature variations.

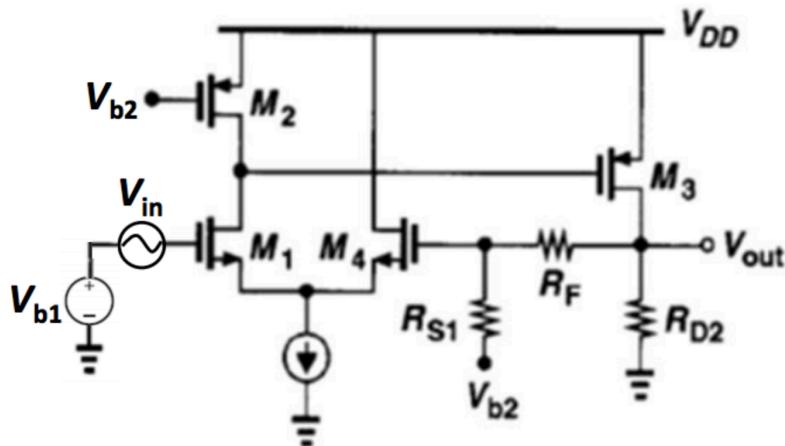
$$A \propto \frac{R_D}{R} \xrightarrow{\left. \begin{array}{l} R_D = R_o(1 + \alpha \Delta T) \\ R = R_o(1 + \alpha \Delta T) \end{array} \right\}} A \propto \frac{R_{D0}}{R_o} \neq f(\Delta T)$$

Not sensitive at all

Problem 5. [17 points] Feedback Analysis

The two stage CMOS amplifier circuit shown below is being used to provide modest gain for an input sensor at V_{in} with very low supply voltage and power consumption. Let's analyze the performance of this circuit in feedback using return ratio. You may assume the following:

$$\begin{aligned} g_m r_o &\gg 1, \\ r_{o1} = r_{o2} &= r_{o4}, \\ g_{m1} &= g_{m4}, \\ r_o &\gg R_{D2}, r_o \gg R_F, r_o \gg R_{S1} \end{aligned}$$



- a. [2 points] What type of feedback is being utilized in this circuit?

Feedback Type:

Series-Shunt or Voltage-Voltage

- b. [3 points] What is the loop gain or return ratio (RR) for this circuit?

Breaking the loop at the gate of M4 and injecting a test signal (v_t), we can find the return signal (v_r), taking care to note that M1, M2, M4 form a single-ended output diff pair.

$$RR = \frac{g_{m1,4}}{2} (2r_{o1}||r_{o2}) \times g_{m3}(R_{D2}||(R_F + R_{S1})) \left(\frac{R_{S1}}{R_{S1} + R_F} \right)$$

$$RR = \frac{g_{m1,4}}{2} (2r_{o1}||r_{o2}) \times g_{m3}(R_{D2}||(R_F + R_{S1})) \left(\frac{R_{S1}}{R_{S1} + R_F} \right)$$

Now calculate the closed-loop voltage gain ($A_{CL} = v_{out}/v_{in}$) and output impedance, Z_{out} , using return ratio.

- c. [2 points] Find the ideal closed loop gain, A_∞ . Leave your answers in terms of device specific small signal parameters.

Setting the gain of the differential stage to infinity, $g_{m1,2} = \infty$, for a finite output, $v_{gs1,2}$ must be zero. Therefore, $v_{g1} = v_{s1} = v_{in} = v_{s4} = v_{g4}$. With $v_{g4} = v_{in}$ and V_{b1} a small signal ground.

$$A_\infty = 1 + \frac{R_F}{R_{S1}}$$

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- d. [2 points] Next, let's find the feed forward co-efficient, d . Leave your answers in terms of device specific small signal parameters.

Setting the gain of the differential stage to infinity, $g_{m1,2} = 0$, we can see that no output signal is generated for a given input. So:

$$d = 0$$

$$d =$$

- e. [1 point] Putting it together, write the expression for the closed-loop gain, A_{CL} . Express your answer in terms of RR and other circuit parameters.

$$A_{CL} = A_\infty \frac{RR}{1 + RR} + \frac{d}{1 + RR}$$

$$A_{CL} = \left(1 + \frac{R_F}{R_{S1}}\right) \frac{RR}{1 + RR}$$

$$A_{CL} = \left(1 + \frac{R_F}{R_{S1}}\right) \frac{RR}{1 + RR}$$

- f. [3 points] Find the closed-loop output impedance for the circuit, Z_{out} . Write your answer in terms of device specific small signal parameters.

Here, we use Blackman's Impedance formula:

$$Z_{out} = Z_{out}(gain \rightarrow 0) \frac{1 + RR_{short}}{1 + RR_{open}}$$

We find RR_{short} by shorting the output port and recomputing the return ratio. RR_{short} is zero in this circuit since no signal can return with the output shorted.

$$RR_{short} = 0$$

We find RR_{open} by opening the output port and recomputing the return ratio. RR_{open} here is identical to the RR from part (b).

$$RR_{open} = \frac{1}{2} g_{m1,2}(r_{o1} || r_{o2}) \times g_{m3}(R_{D2} || (R_F + R_{S1}))$$

Finally, we find $Z_{out}(gain = 0)$ by setting $g_{m1,2} = 0$.

$$Z_{out}(gain \rightarrow 0) = R_{D2} || (R_F + R_{S1})$$

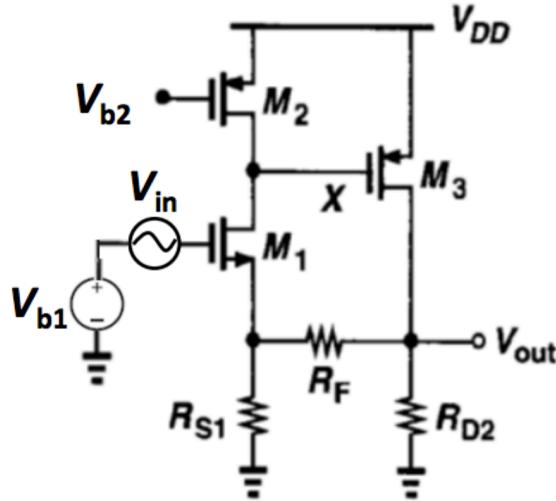
Putting it together,

$$Z_{out} = \frac{R_{D2} || (R_F + R_{S1})}{1 + \frac{g_{m1,4}}{2} (2r_{o1} || r_{o2}) \times g_{m3}(R_{D2} || (R_F + R_{S1})) \left(\frac{R_{S1}}{R_{S1} + R_F} \right)}$$

$$Z_{out} \approx \frac{2}{g_{m1,4}(2r_{o1} || r_{o2}) \times g_{m3}} \left(\frac{R_{S1} + R_F}{R_{S1}} \right)$$

$$Z_{out} = \frac{2}{g_{m1,4}(2r_{o1} || r_{o2}) \times g_{m3}} \left(\frac{R_{S1} + R_F}{R_{S1}} \right)$$

- g. [EE240] [4 points] In an attempt to save power you modify the circuit as shown below, feeding the output directly back into the source of M1. Find the new loop gain (RR) for this circuit and comment on whether it is greater or less than before. Assume that g_{m1} in this new circuit is the same as g_{m1} from the previous circuit.



Breaking the loop at the gate of M4 (node X) and injecting a test signal (v_t), we can find the return signal (v_r) by using inspection or KCL/KVL. We find the new return ratio:

$$RR_{new} = g_{m1}(r_{o1}||r_{o2}) \times g_{m3} \left(R_{D2} \parallel \left(R_F + \frac{2}{g_{m1}} || R_{S1} \right) \right) \left(\frac{\frac{2}{g_{m1}} || R_{S1}}{\frac{2}{g_{m1}} || R_{S1} + R_F} \right)$$

$$RR_{new} = \frac{g_{m1}(r_{o1}||r_{o2})}{1 + \frac{g_{m1}}{2}(R_{S1}||R_F)} \times g_{m3} \left(R_{D2} \parallel \left(R_F + \frac{2}{g_{m1}} || R_{S1} \right) \right) \left(\frac{R_{S1}}{R_{S1} + R_F} \right)$$

The new RR is: Larger OR Smaller

$$RR_{new} = \frac{g_{m1}(r_{o1}||r_{o2})}{1 + \frac{g_{m1}}{2}(R_{S1}||R_F)} \times g_{m3} \left(R_{D2} \parallel \left(R_F + \frac{2}{g_{m1}} || R_{S1} \right) \right) \left(\frac{R_{S1}}{R_{S1} + R_F} \right)$$

$$RR_{old} = \frac{g_{m1,4}}{2} (2r_{o1}||r_{o2}) \times g_{m3}(R_{D2}||(R_F + R_{S1})) \left(\frac{R_{S1}}{R_{S1} + R_F} \right)$$

Comparing the new and old return ratio, we see that it has been reduced. The cost of saving power here is lower RR and therefore less accurate gain and higher output impedance.

$$RR_{new} = \frac{g_{m1}(r_{o1}||r_{o2})}{1 + \frac{g_{m1}}{2}(R_{S1}||R_F)} \times g_{m3} \left(R_{D2} \parallel \left(R_F + \frac{2}{g_{m1}} || R_{S1} \right) \right) \left(\frac{R_{S1}}{R_{S1} + R_F} \right)$$

The new RR is: Larger or Smaller

Problem 6. [15 points] Output Stages

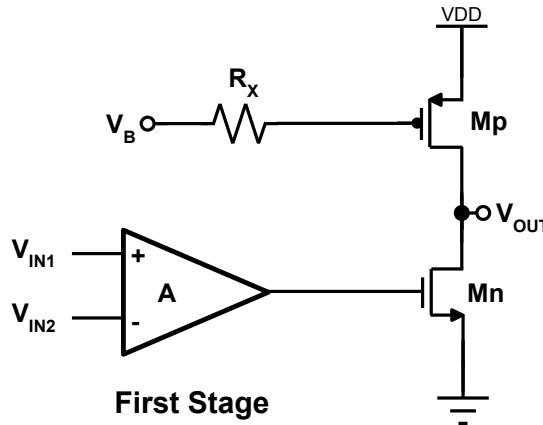
You are tasked with designing a low-power two-stage amplifier to drive a large capacitive load. After running some device level simulations, you find that your technology node has the following features:

$$k_N = 2k_P = 2.5mA/V^2,$$

$$|V_{THP}| = V_{THN}, \text{ and}$$

$$\lambda_P \neq \lambda_N.$$

You begin your design with a standard class A common source amplifier shown below.



- a. [2 points] What is the minimum bias current required for this output stage to drive a 20 MHz, 1 Vpp sine wave into a load capacitance of 0.1nF without slewing?

Maximum output current is determined by maximum slew rate. The slew rate here is the rate of change with respect to time of the output voltage (20MHz, 1Vpp sine wave)

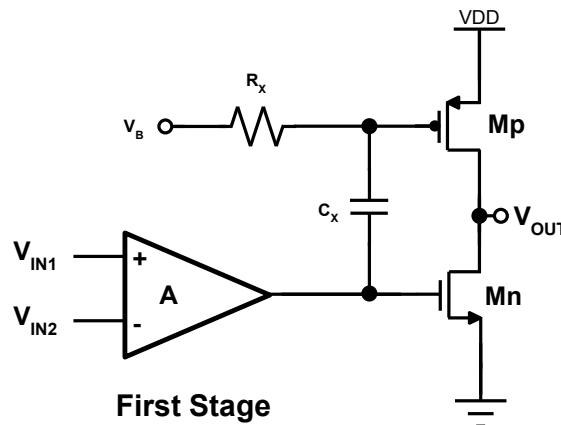
$$\max\{i_{bias}\} = C_L \max\left\{\frac{dv_{out}}{dt}\right\} = C_L \max\left\{\frac{d}{dt}(0.5 \sin(2\pi \times 20MHz \times t))\right\}$$

$$\max\{i_{bias}\} = C_L \max\{(0.5 \times 2\pi \times 20MHz \times \cos(2\pi \times 20MHz \times t))\}$$

$$\max\{i_{bias}\} = C_L \times 0.5 \times 2\pi \times 20MHz \approx 6.28mA$$

$I_{BIAS} = 6.28mA$

To avoid burning all this current in your output stage, you decide to convert your class A output stage into an inverter-based class AB output stage using this simple circuit modification below.



- b. [3 points] Size the PMOS and NMOS devices so as to guarantee that the output stage has equal rising and falling edge drive current and the combined NMOS and PMOS G_m for this stage is 5 mS . Assume that $L_p = L_n = 200\text{nm}$ and $\Delta V_{\text{equal}} = 0.1\text{V}$ for both devices.

Same current drive for rising and falling edge means $g_{mn} = g_{mp}$

Total $G_m = 5\text{mS}$ means $G_m = g_{mn} + g_{mp}$

So $g_{mn} = g_{mp} = G_m/2 = 2.5\text{mS}$

$$\therefore g_m = k \frac{W}{L} \Delta V$$

$$W = \frac{g_m L}{k \Delta V}$$

$$W_n = \frac{g_{mn} L}{k_n \Delta V} = \frac{(G_m/2)L}{k_n \Delta V} = 2\text{um}$$

$$W_p = \frac{g_{mp} L}{k_p \Delta V} = \frac{(G_m/2)L}{k_p \Delta V} = 4\text{um}$$

- c. [4 points] Find the voltage gain, $A_v = v_{out}/(v_{in1} - v_{in2})$, for this 2-stage amplifier as a function of frequency, considering only the caps explicitly drawn in the circuit. Leave your answer in terms of G_m and device specific small signal parameters.

Considering the gain from the NMOS and PMOS separately...

Gain due to MN:

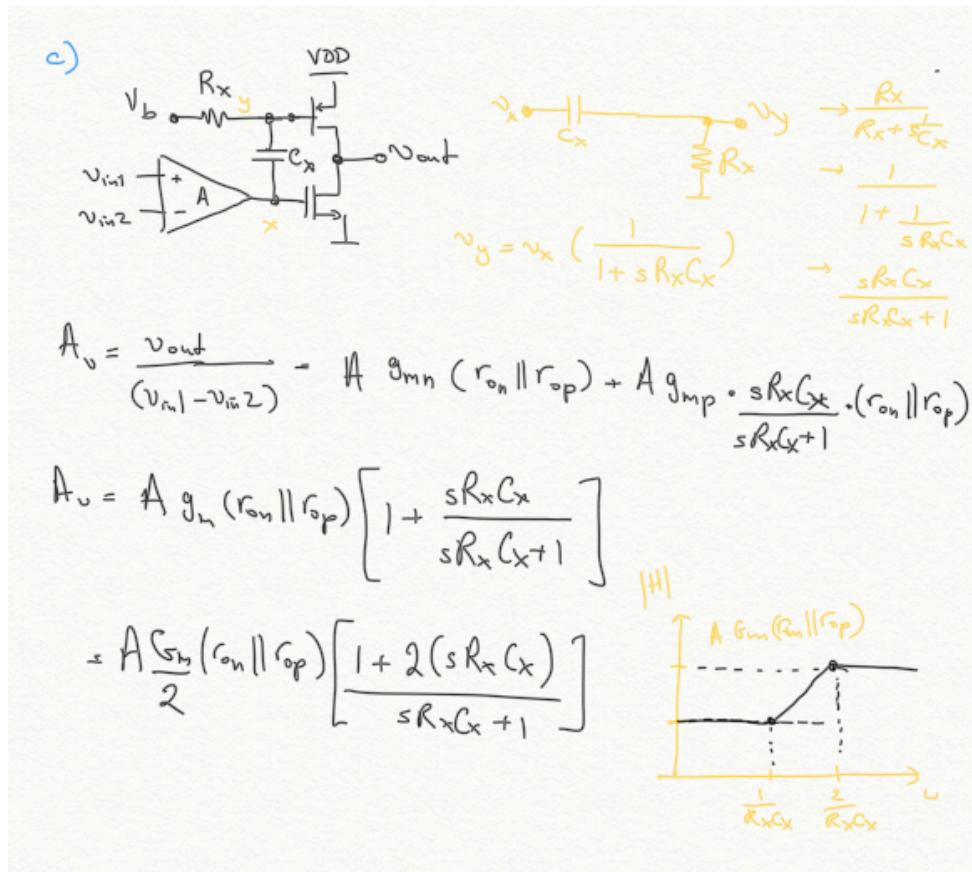
$$A_v = A g_{mn} (r_{op} \parallel r_{on}) = A_v = A \frac{G_m}{2} (r_{op} \parallel r_{on})$$

Gain due to MP (note that R_X and C_X form a high pass filter which attenuates the effective gm):

$$A_v = A g_{mp} \left[\frac{s R_X C_X}{s R_X C_X + 1} \right] (r_{op} \parallel r_{on}) = A_v = A \frac{G_m}{2} \left[\frac{s R_X C_X}{s R_X C_X + 1} \right] (r_{op} \parallel r_{on})$$

Summing these together:

$$A_v = A \frac{G_m}{2} (r_{op} \parallel r_{on}) \left[1 + \frac{s R_X C_X}{s R_X C_X + 1} \right] = A \frac{G_m}{2} (r_{op} \parallel r_{on}) \left[\frac{1 + 2 s R_X C_X}{1 + s R_X C_X} \right]$$



$$A_v = A \frac{G_m}{2} (r_{op} \parallel r_{on}) \left[\frac{1 + 2 s R_X C_X}{1 + s R_X C_X} \right]$$

- d. [3 points] Find the gain error at DC, ϵ_{DC} , and at high frequency, ϵ_{AC} , (i.e. above any poles and or zeros in the loop gain) for this two stage amplifier, assuming unity gain feedback.

$$\text{Gain Error} = \frac{1}{1 + RR} = \frac{1}{1 + \frac{G_m}{2}(r_{op}||r_{on}) \left[\frac{1 + 2sR_XC_X}{1 + sR_XC_X} \right]}$$

@ DC ($s \rightarrow 0$)

$$\text{Gain Error} = \frac{1}{1 + \frac{G_m}{2}(r_{op}||r_{on})}$$

@ High Frequency ($s \rightarrow \infty$)

$$\text{Gain Error} = \frac{1}{1 + G_m(r_{op}||r_{on})}$$

This problem can also be solved by inspection. Noting that at DC, C_X is an open circuit, so the PMOS' g_m doesn't contribute to the output, reducing the output G_m by a factor of 2. While at high frequency, C_X is an open circuit, so the PMOS' g_m contributes fully to the output.

$$\epsilon_{DC} = \frac{1}{1 + \frac{G_m}{2}(r_{op}||r_{on})}$$

$$\epsilon_{AC} = \frac{1}{1 + G_m(r_{op}||r_{on})}$$

- e. [EE240A Only] [3 points] You decide to improve the static error by resizing the AC coupling cap. Compute the minimum cap value to guarantee the gain error at 10 MHz and 20 MHz are both equal and both are minimized. The value of Rx is fixed at 1 kΩ.

To minimize error we want $|RR(jw)|$ to be maximized at both 10 MHz and 20 MHz. Therefore, both frequencies of interest must be above the pole in the transfer function since this is where A_v is maximized.

$$\frac{1}{R_X C_X} < \min\{2\pi 10\text{MHz}, 2\pi 20\text{MHz}\} = 2\pi 10\text{MHz}$$

$$C_X > \frac{1}{R_X 2\pi 10\text{MHz}} = 15.92\text{pF}$$