Project: LCD Driver Design Guide

EE140/240A – Linear Integrated Circuits

Spring 2024

This document serves to help you design your amplifier. Although none of this is fully required, this document gives you very important design considerations to take when designing your amplifier, and you are recommended to try and answer these questions below for your understanding of the project. **Check Section 4 on the requirements for the Checkoff.**

1. Concept: 2-Stage Operational Amplifiers

Reviewing the lecture on two-stage opamps will be helpful in designing your amplifier. In addition, Razavi has great information on 2-stage opamps as well

- Chapter 8 on Feedback: Good for reviewing open-loop, closed-loop, and loop gain. Example 8.5 resembles the feedback network of this project.
- Chapter 9 discusses Op Amps: You might find interesting architectures to implement your design for this project. Pay attention especially figure 9.8, and 9.15 for examples of telescopic and folded-cascode topologies as well as the analysis that follows from them. Figure 9.21 shows two telescopic cascodes with different properties. Section 9.6 discusses various tradeoffs of op amp topologies. Note that a two-stage opamp is essentially required, but the first and second stage can be what you choose. Slew rate is discussed in section 9.9, and 9.10 discusses 1-stage opamps with high-slew rate. An intro to power supply rejection is found in section 9.11
- Chapter 10 is on Stability and Compensation: when tying your opamp in feedback, stability issues can arise. This section analyzes the transient response of amplifiers in multipole systems. There is also a compensation technique you have seen in lecture, and this chapter reviews it.

Grey and Meyer also has topics that are important and worth reviewing for the project. Keep in mind that this textbook also analyzes BJT circuits, but there should be treatment of both MOS and BJT circuits in each section.

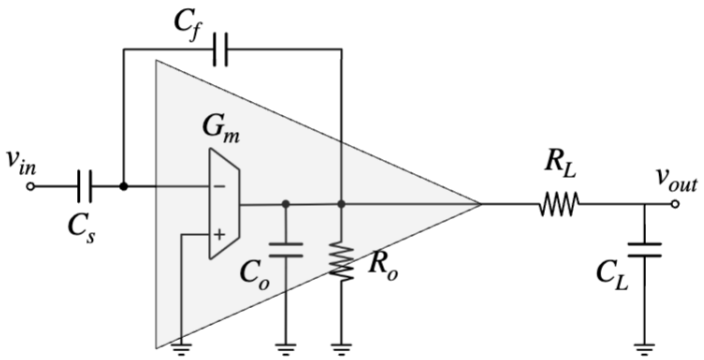
- Chapter 4 talks about current mirrors and biasing. Some of the topologies that you might choose require a biasing circuit. You cannot use ideal voltage sources in the project, and you will need to bias your circuit using current mirrors. You might have seen in Lab 3 that a single current mirror might not give the required current through the tail (current is not mirrored 1-to-1). This is because of finite impedance compared to the infinite impedance from an ideal current source.
- Chapter 5 is on output stages. In addition, feel free to lookup online more information on MOS output stages since this book opts to show more BJT output stage design.
- Chapter 6 is on Op amps. There are schematics of folded and telescopic cascodes here, and it is another good source to see this analysis too in addition to Razavi's
- Chapter 7 discusses multistage amplifier frequency responses (Section 7.3), and Chapter 8 is on feedback. Both this and Razavi's textbook talk about similar topics, so feel free to just look at one or the other.
- Chapter 9 is on stability. It is good to look at both Razavi and Grey/Meyer on this topic to understand how to achieve phase margin, and how it might affect your transient results.

2. System-Level Analysis

1. Carefully read the project description while paying special attention to the design specifications listed.

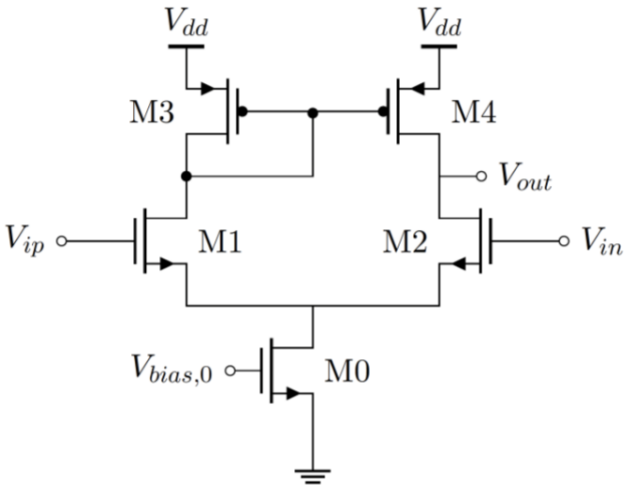
2. Analyze the LDC driver:

- For the switched capacitor amplifier used in this display driver, what sets the bias point of the input? What sets the bias point of the output?
- Using the ideal model of a single-stage amplifier shown below, find the loop gain, $T(s) = \beta H(s)$.
- Based on your loop-gain expression, formulate expressions for the static (ϵ_s) and dynamic (ϵ_d) settling errors of the driver in terms of C_L, R_L, C_s, C_f, G_m, and R_o of the amplifier. These are your main design equations using which you should be able to find G_m and R_o to achieve the required settling time for your amplifier.



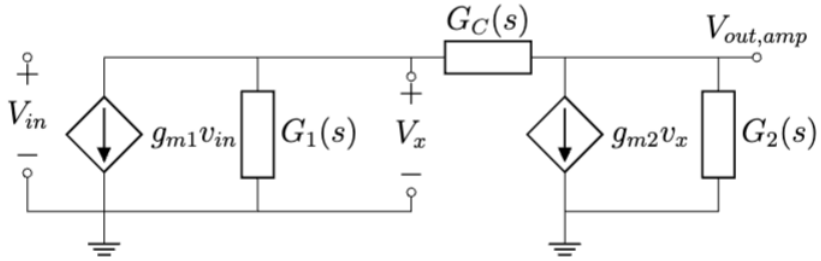
3. Get familiar with the testbenches provided for you in Cadence using a single-stage 5T Workhorse Amplifier. Use the amplifer you design in Exercise 6 of Lab 3. (Don't worry, you don't have to meet the specifications now, you will need to modify the topology anyways).

- Connect your amplifier into the symbol provided along with the lab testbenches.
- Run a transient analysis using the single-stage amplifier you created in Lab 3. Be sure to set the correct input and output common mode.
- Determine the settling error of the amplifier vs. time. You will need to create a new expression. Annotate the time when the settling error reaches your target.
- Open the AC simulation testbench and understand how the amplifier is configured for each test. Understand how the output expressions are defined. Run the AC testbench on your amplifier.
- Do you think this single-stage amplifier (given the ranges of G_m and R_o you found for the required settling time) can achieve the required settling error?


V_{dd}
V_{dd}
M3
M4
V_{out}
V_{ip}
M1
M2
V_{in}
$V_{bias,0}$
M0

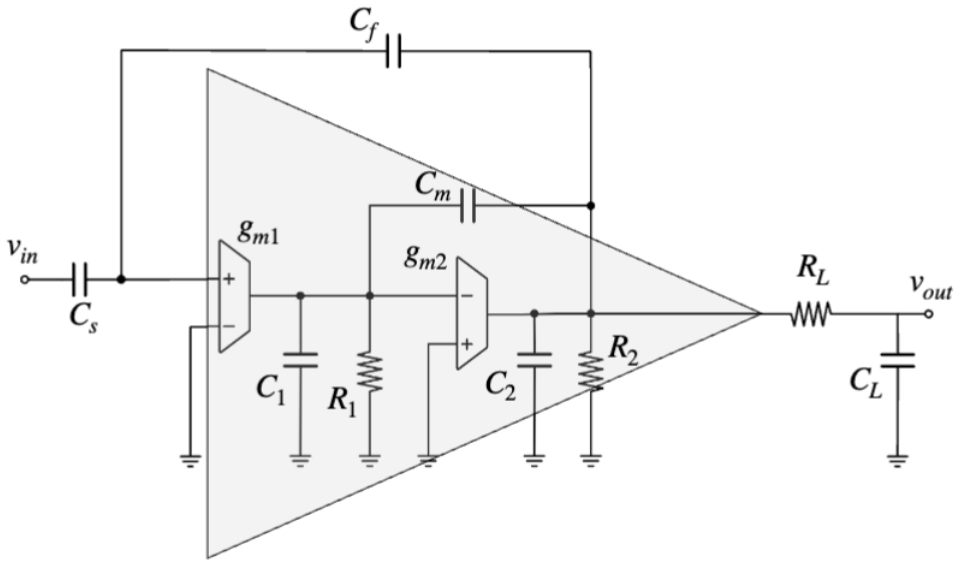
3. Ideal Behavioral Simulation and Checkoff

Because of the static error requirement, it will be difficult to design a single stage amplifier that can achieve the required specifications. Let's now explore a two stage topology. Below is a system with a model of a two stage amplifier. Our goal is to have a script we can use to understand how to size the various parameters of this two stage amplifier (g_{m1}, g_{m2}, etc.). Our script should take as an input selected values of the amplifier model and output the expected step response. We then can sweep over values of various parameters to see what step responses are possible. Additionally, we must be careful to make sure the system remains stable, thus our script should also calculate the phase margin of the loop gain.



1. Let's find some initial sizing for all the opamp parameters. Assume that $g_m r_o = 100$, $f_T = 10GHz$, and $C_{dd} = C_{gg}/10$. Additionally, assume $C_c = 1pF$ and $R_L = 0$. Find all the remaining opamp parameters assuming the opamp has 45 degrees of phase margin and a unity gain bandwidth of $100MHz$. That is, find $g_{m1}, R_1, C_1, g_{m2}, R_2$, and C_2. Use the results we've obtained from lecture and ignore the right half plane zero for now.

2. To check our initial values of opamp parameters, we need to first find the loop gain of the two stage amplifier. The design in below has too many variables inside of it to solve by hand. We can use a symbolic library in Python to help us find the loop gain. To make our job easier, let's first simplify the above model of a two stage amplifier into the following model you've seen in lecture. Find the transfer function for the above from V_{in} to $V_{out,amp}$ in terms of g_{m1}, g_{m2}, G_1, G_2, G_c. Note that G_1, G_2, and G_c are all frequency dependent conductances that represent the components of the model.



3. Our above model lumps together many individual components that are connected in series and in parallel, Find $G_1(s) = \frac{1}{Z_1(s)}$ in terms of R_1 and C_1.

4. Find $G_2(s)$ in terms of R_2, C_2, C_S, C_F, R_L, and C_L.

5. Finally, find $G_C(s)$ in terms of C_C.

6. In this amplifier, the output is not taken at the output of the amplifier but rather after the load resistance R_L. Assuming the opamp was ideal (infinite DC gain, infinite bandwidth), find the transfer function from V_{in} to V_{out} for the system. This is A_∞ for this system.

7. Now that you have calculated A_∞, and the return ratio, RR, we can find the closed loop gain: $\frac{A_\infty RR}{1+RR}$. Use your previous expressions to complete the code found in the project folder on bCourses to find the loop gain and the closed loop gain. Note, you might have to install these libraries if you have not yet.

8. Let's sanity check our above calculations. Plot the Bode plot of the Loop gain assuming $R_L = 0$, and $C_c = 0$. Is this system stable?

9. Now plot the Bode plot of the loop gain with $C_c = 1pF$ but with $R_L = 0$. Is this system stable? Plot the step response of this system.

10. Finally, let's add in the real R_L. Plot the Bode plot of the Loop gain. Is this system stable? Plot the step response. What was the impact of R_L on the loop gain? What was the impact of the R_L of the step response?

11. Using the ideal behavioral script, find sizes for the opamp parameters such that you meet the required specifications. Note, you can break our initial assumptions in question 1 of this section.

4. Checkoff

Show me the following:

1. Show me your Lab 3 Exercise 6 when input into the AC and Transient Simulations. Show me the CMRR, PSRR, settling time for the rising and falling case. Show me the loop gain and the phase margin. Take screenshots of these.

2. Explain to me why the compensation capacitor is helpful, and why a compensation resistor might be useful methods to handle the RHP zero.

3. Explain to me the relationship between the phase margin and the settling time. How does R_L at the load help you in the design? Hint: going through the coding found in the previous section will be helpful in describing this relationship.

5. Transistor-Level Analysis

At this point, your design does not have to meet all the specifications. however, you should have a design that could meet the specifications with more size optimizations. As a baseline, you may follow the instructions below.

1. You should have order of magnitude estimates for g_m's and r_o's of each stage, and you likely know where your poles lie. Depending on your topology, write out relevant equations that determine unity gain bandwidth and loop gain. Consider the effects of the dominant pole when a compensation capacitor is placed. Write expressions for that as well.

2. Using the g_m/I_D systematic design methodology you learned in Lab 3, design a two-stage amplifier based on the design parameters you obtained in the previous section. You can either use your previous scripts from Exercise 5 and 6 to help design your amplifier, or you can create your own from scratch. Try and understand how stage 1 might affect stage 2 design, and vice versa.

3. Combine the two stages, then compensate the two-stage amplifier and verify its stability and other performance metrics in Cadence.

4. The Ideal-Behavior Scripts and the scripts you use for designing both of your stages will all be used iteratively together to improve your design. Move on to Cadence once you have results that seem to give you good results. If the Cadence sims give you bad results, use that information to help make improvements to your scripts.

6. Debugging Tools

Check Ed for any helpful tools with debugging as well.

1. When your schematic design is complete, run a dc analysis to make sure all of the device operating points are as expected. A dc simulation can be run together with your main ac/transient simulations.

- Annotate the DC voltages to make sure the power supplies are connected to your amplifier correctly.
- Annotate or print the dc operating points to make sure the devices are not in cut-off or triode regions of operation.

2. Always check the polarity of the feedback to avoid generating a positive feedback loop accidentally.