EE 140/240A — Analog Integrated Circuits

Prof. Rikky Muller — Final Exam

INSTRUCTIONS

- Please do not open this exam until instructed to do so.
- Write final answers in the boxes provided. Justification and supporting work for all problems should be shown outside the answer box.
- If your answers do not fit in the boxes provided, you may write them elsewhere, but you should clearly box/circle them.
- Clearly label any scratch paper with the problem you are working on.
- The equation sheet is the last page of this packet. You may tear it off if desired.
- Please fill in the table below before the exam starts.

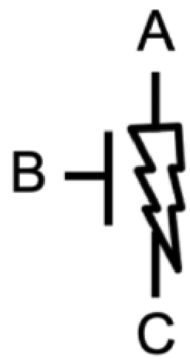
First Name	
Last Name	
Student ID	
Email Address	
Course	Circle one: EE140 EE240A

SCORING

Problem	**EE140**	**EE240A**
Problem 1	/8	/8
Problem 2	/11	/11
Problem 3	/9	/9
Problem 4	/13	/13
Problem 5	/13	/16
Problem 6	/13	/19
Total	/67	/76

1 Non-MOS Devices

Congratulations, you've invented a new type of transistor! You are proud to contribute to the tradition of important semiconductor inventions at UC Berkeley. You are particularly excited about your device because it has a threshold of 0V - it's a terrible switch, but a great amplifier! The device is shown below and exhibits the following I-V characteristic:



$$I_{AC} = \kappa V_{BC}^3 (1 + \gamma V_{AC})$$

κ and γ are constants. You may assume your device has the same basic small signal model as a MOSFET.

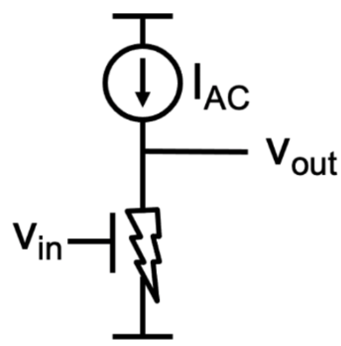
(a) (2 points) Calculate g_m as a function of I_{AC}.

$g_m =$

(b) (2 points) Calculate r_o as a function of I_{AC}.

$r_o =$

(c) (2 points) You use this device as an amplifier with an ideal current source load as shown below. Calculate the gain $A_v = V_{out}/V_{in}$.

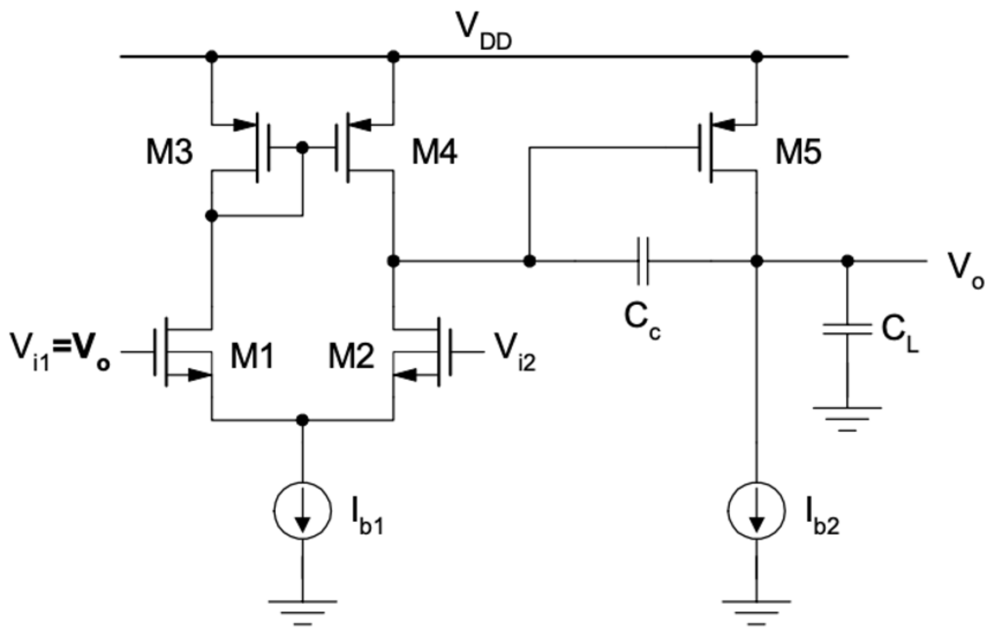


$A_v =$

(d) (2 points) Assuming I_{AC} is fixed, how would you bias the device in the circuit from the previous part to maximize gain?

2 Two-Stage Amplifier

(a) (9 points) Fill in the table below. The two-stage amplifier shown below is used in unity gain feedback. The first column lists amplifier parameters. In each empty cell, indicate how the amplifier characteristics change when the parameter listed in the first column is **increased**. Use the following code: (↑) for increase, (↓) for decrease, (=) for no significant change and (?) if it is impossible to answer the question with the information given. Ignore all capacitors except those explicitly shown.



Parameter	DC Gain	-3dB Bandwidth	Phase Margin
I_{b1}			
I_{b2}			
C_c			
C_L			

Extra workspace for part (a)

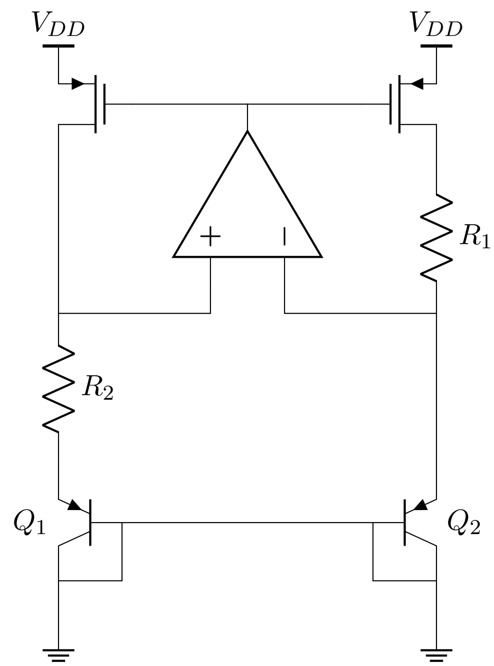
(b) (2 points) Assume this amplifier is designed such that it has zero systematic offset, meaning $I_{b1} = 2I_{b2}$ and $\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_5$. What would be the polarity (positive or negative?) of the output referred offset if due to some fabrication error L_5 increases by 10%. Briefly justify your answer.

Output offset voltage is:

Positive Negative

3 Bandgap References

Consider the bandgap circuit shown below, which uses PNP BJTs available in a CMOS process.



The emitter area of Q_1 is N times larger than that of Q_2, and the dimensions of the PMOS devices are equal. Assume that the amplifier is ideal and the base current of the BJTs is zero.

(a) (2 points) What is the ratio of the currents through the right and left branches of the circuit I_{Q1}/I_{Q2}?

$\frac{I_{Q1}}{I_{Q2}} =$

(b) (2 points) This circuit generates a PTAT current. Find an expression for the current flowing through R_1.

$I_{R1} =$

(c) (3 points) With a correct choice of R_1 and R_2, this circuit can also generate a temperature independent bandgap voltage at one of its nodes. Identify and mark this node on the schematic on the previous page. Then write an expression for V_{bg}.

$V_{bg} =$

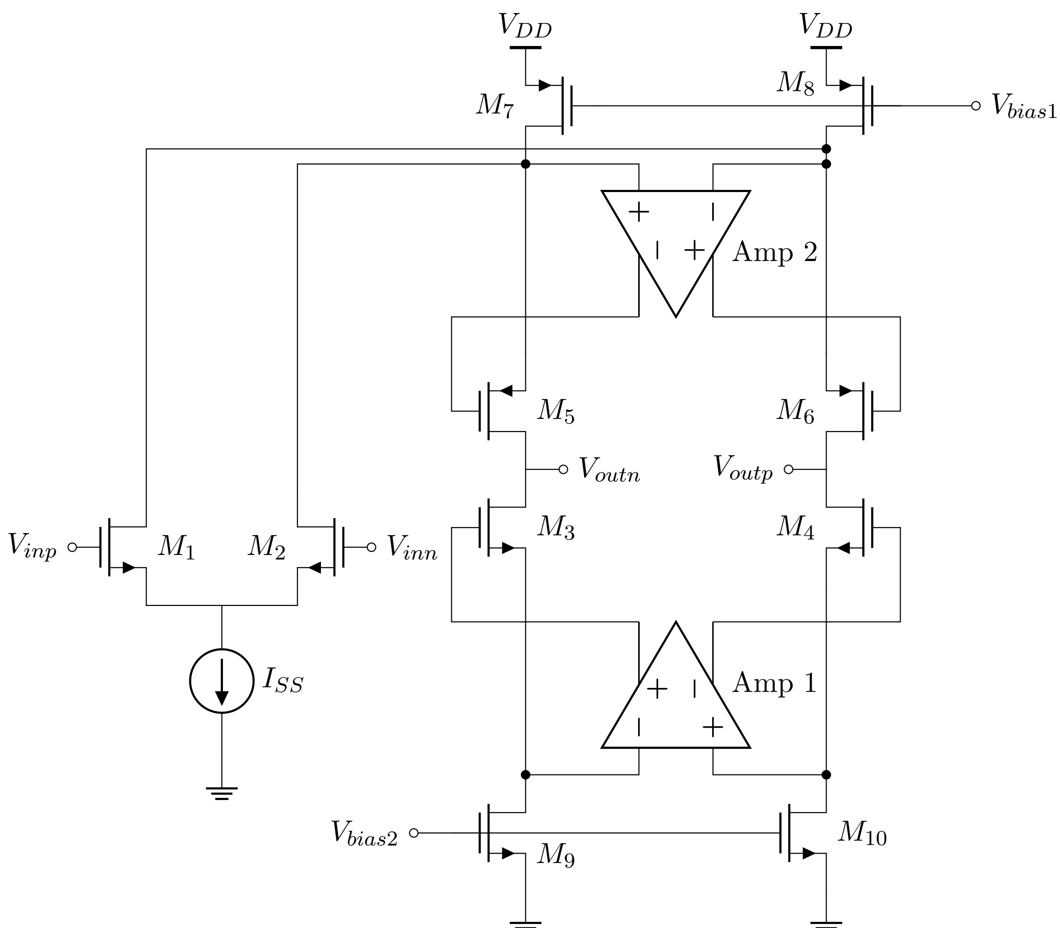
(d) (2 points) Now, determine the ratio of R_1/R_2 such that the node identified in part (c) becomes a bandgap reference voltage.

$\frac{R_1}{R_2} =$

4 Gain-Boosted Folded Cascode

You are asked to design an amplifier for a high-precision sensing device to minimize the static error. You propose the gain-boosted folded cascode topology shown below.

Assume all of the devices have the same overdrive voltage (ΔV) and $I_{M1} = I_{M5} = \frac{I_{SS}}{2}$.
Express your answers in terms of g_m and r_o if needed, where $g_m = \frac{I_{SS}}{\Delta V}$ and $r_o = \frac{1}{\lambda \frac{I_{SS}}{2}}$ and $g_m r_o \gg 1$.
All of the devices have the same channel length L and the current source is ideal and $V_{th} > \Delta V$.

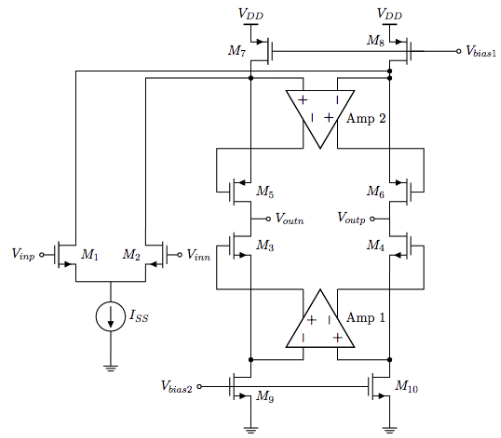


(a) (3 points) If Amp 1 and Amp 2 are implemented with single stage differential amplifiers, what is the best choice for the input transistors of each amplifier (NMOS or PMOS) to maximize swing? Explain your answer.

Amp 1:
Amp 2:

(b) (4 points) Compute R_{out} of the amplifier assuming that the differential gain of the amplifiers Amp 1 and Amp 2 is A ($A \gg 1$).

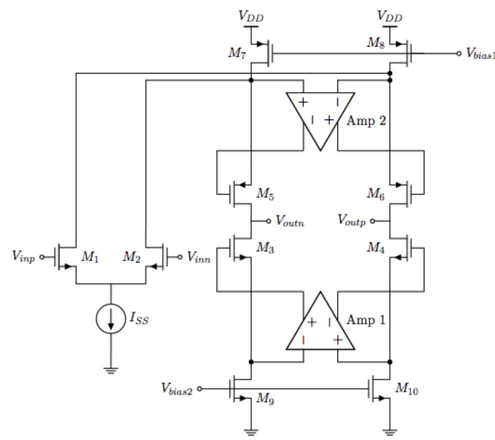
Hint: draw the differential half circuit and compute $R_{thd,n}$ and $R_{thd,p}$.



$R_{out} =$

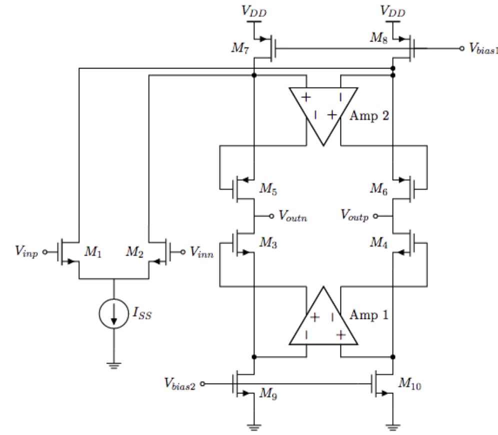
(c) (3 points) Using R_{out} from part (b), calculate the differential gain of the amplifier

$$A_{vd} = \frac{V_{outp} - V_{outn}}{V_{inp} - V_{inn}}.$$



$A_{vd} =$

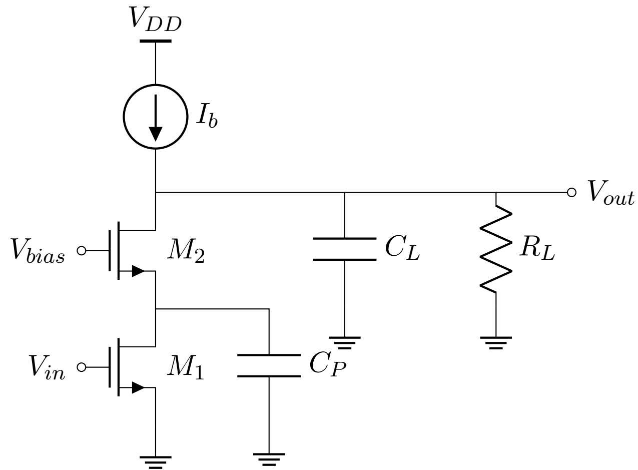
(d) (3 points) Determine the power supply gain from V_{DD} to the single-ended output.



$A_{V_{DD}} =$

5 Settling Time

Consider the cascode amplifier shown below:



Assume $\lambda = 0$ for all transistors, $C_L \gg C_P$, and $g_m R_L > 1$. Consider only the capacitances explicitly drawn.

(a) (3 points) Design a circuit that generates the bias voltage V_{bias} necessary for maximum output swing. You are given one ideal current source of value $I_b/2$, which must have one end connected to V_{DD} or ground.

Specify the sizing of all devices in terms of $(W/L)_1 = (W/L)_2 = W/L$.

Neglect the body effect and channel length modulation.

(b) (2 points) Estimate the DC gain H_0 and the poles of the transfer function $H(s) = V_{out}(s)/V_{in}(s)$. Identify which pole is the dominant pole.

Answer in terms of g_{m1}, g_{m2}, C_L, C_P, and R_L.

$H_0 =$

Poles (circle dominant one):

(c) (4 points) Regardless of your answer to the previous part, assume that

$$H(s) = \frac{H_0}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})}.$$

Our goal in this problem is to calculate the settling time of the amplifier above in response to a step input. To do this, we will take the inverse Laplace transform of $V_{out}(s)$. Calculate the partial fraction decomposition of $V_{out}(s)$ by finding the values of A, B, and C in the equation below.

$$V_{out}(s) = \frac{1}{s}H(s) = \frac{H_0}{s\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} = \frac{A}{s} + \frac{B}{s + \omega_{p1}} + \frac{C}{s + \omega_{p2}}$$

Leave your answers in terms of H_0, ω_{p1}, and ω_{p2}.

$A =$

$B =$

$C =$

(d) (3 points) At time $t = 0$, a unit step input is applied to V_{in}. At time T, the amplifier output is sampled. Calculate the settling error of the amplifier at the time it is sampled.

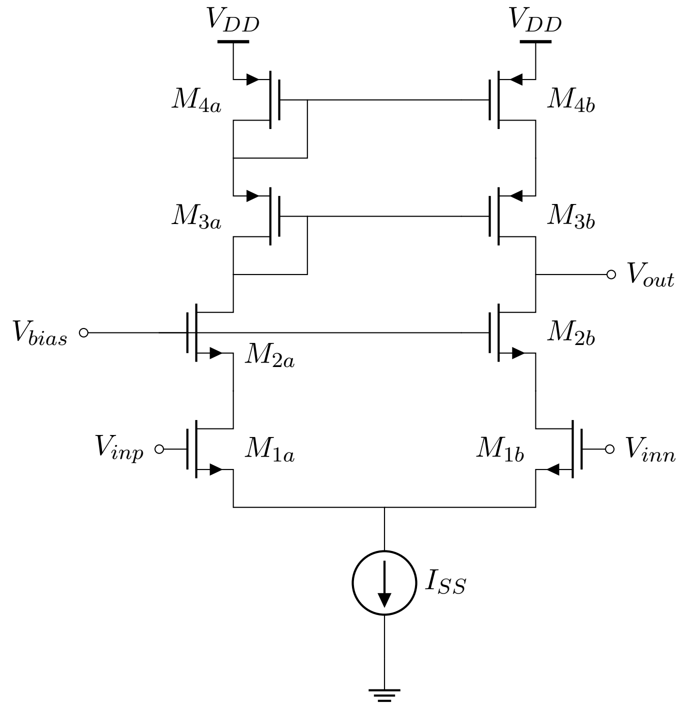
We define settling error as

$$\epsilon = \left| \frac{V_{out}(t = \infty) - V_{out}(t = T)}{V_{out}(t = \infty)} \right|$$

Express your answer in terms of $\omega_{p1}, \omega_{p2}, T$, and H_0 (your answer need not involve all these variables). If you did not solve the previous part, you may leave the constants A, B, and C in your answer.

$\epsilon =$

(e) (1 point) You now build a telescopic cascode differential amplifier, as shown below.



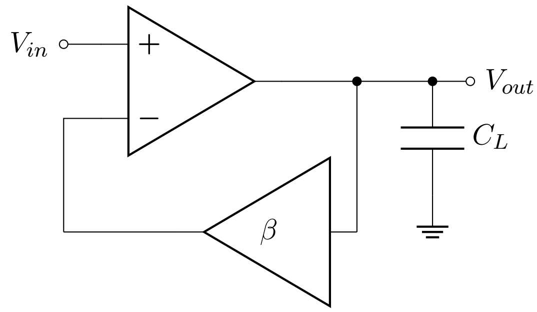
Assume that the current mirror formed by M_{3a}, M_{3b}, M_{4a}, and M_{4b} is an ideal 1:1 current mirror. What is the maximum current $I_{out,p}$ that can be delivered **to** a load connected to the output? What is the maximum current $I_{out,n}$ that can be drawn **from** the load connected to the output?

Don't worry about the sign of your answer.

$I_{out,p} =$

$I_{out,n} =$

(f) **(EE240A ONLY)** (3 points) The input devices are biased with overdrive voltage ΔV. The telescopic cascode amplifier from the previous part is connected in feedback with feedback factor β, as follows:



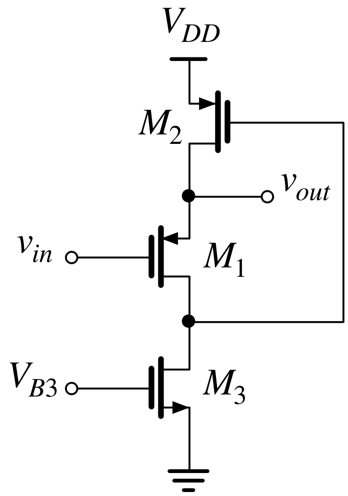
Assume that the feedback network does not load the amplifier. We will consider the amplifier to be slew-rate limited when $|V_{inp} - V_{inn}| \geq \Delta V$, and assume that in this regime, one of the input devices is completely off (ie. no current flows through it). If we apply an input step to V_{in} with amplitude $V_A > \Delta V$ at $t = 0$, estimate the duration T_{slew} for which the amplifier will be slew-rate limited.

Answer in terms of $C_L, I_{SS}, V_A, \Delta V$, and β.

$T_{slew} =$

6 Flipped Voltage Follower

In this problem, we analyze a circuit known as the flipped voltage follower (FVF) which is often found as a building block in low-power analog circuits.



For simplicity, assume $\lambda_1 = \lambda_2 = 0$ and $\lambda_3 \neq 0$. Ignore the body effect.

(a) (1 point) Find the small-signal transconductance G_m of the FVF.

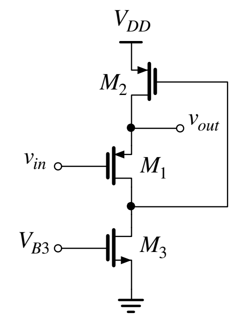
$G_m =$

(b) (3 points) Note that the FVF is essentially a feedback circuit. Use the Blackman's impedance formula to find the resistance seen into the output terminal v_{out}.

The Blackman's impedance formula is:

$$R_{out} = R_{(out,k=0)} \frac{1+\mathfrak{R}_{\text{port,shorted}}}{1+\mathfrak{R}_{\text{port,open}}}$$

Express your answer in terms of the circuit parameters ($g_{m1}, g_{m2},\ r_{o3}, \ldots$).



$R_{out} =$

(c) (1 point) Now, find the small-signal gain of the FVF using your findings in (a) and (b).

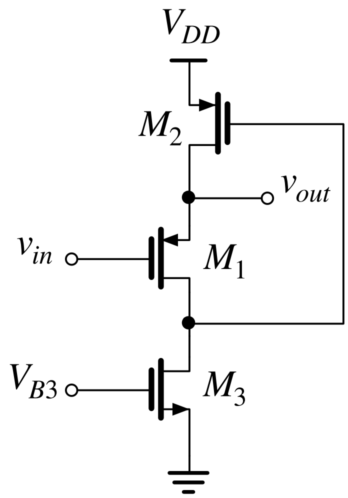
$A_v =$

(d) (3 points) The FVF loop gain transfer function has two poles and therefore needs to be properly analyzed for stability. Derive the loop gain transfer function by only considering the c_{gs} of the devices. In particular, find the DC value of the loop gain, and the locations of the two poles. Express your answer in terms of the circuit parameters $(g_{m1}, g_{m2},\ r_{o3}, c_{gs1}, c_{gs2} \ldots)$.

$LG(s) =$

(e) (5 points) Plot the bode diagram (magnitude and phase) of the loop gain transfer function, and clearly annotate critical points of the bode diagram (e.g., ω_u) in terms of the circuit parameters ($g_{m1}, g_{m2},\ r_{o3}, c_{gs1}, c_{gs2} \ldots$).

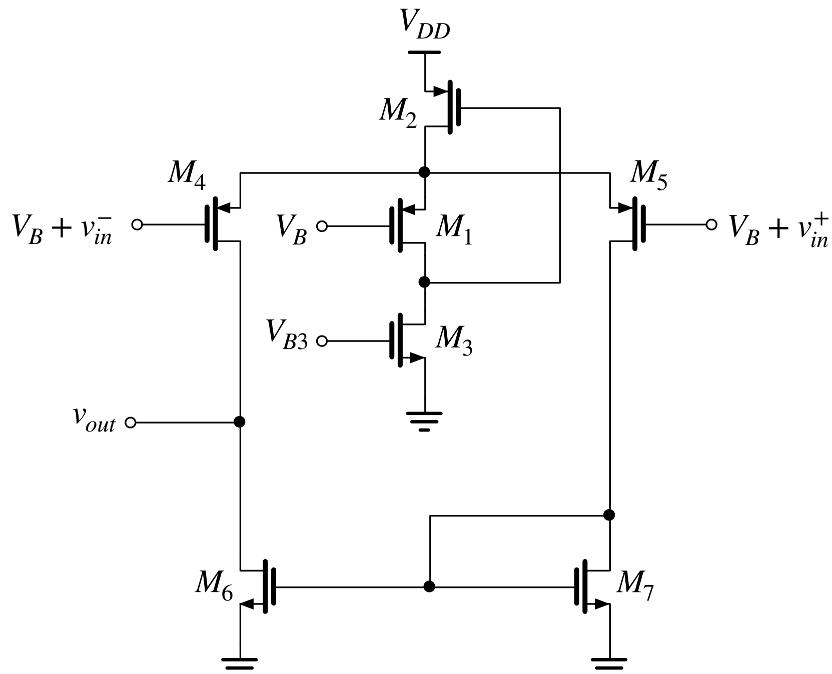
(f) **[EE240A ONLY]** (3 points) Assuming $L_1 = 2L_2$, find W_2/W_1 in order to achieve a phase margin of 45°. Assume M_{1-3} are long channel devices.



$\frac{W_2}{W_1} =$

(g) **[EE240A ONLY]** (3 points) Now, let's use the FVF as an adaptive tail current source of a differential pair as shown below. Assuming that $W_1 = W_4 = W_5$, and $L_1 = L_4 = L_5 = 2L_2$, redesign W_2/W_1 so that the FVF feedback loop has a phase margin of 45°. Assume $\lambda_1 = \lambda_2 = \lambda_4 = \lambda_5 = 0$ and $\lambda_3 \neq 0$.

Hint: the FVF loop gain transfer function is now impacted by M_{4-5}.



$\frac{W_2}{W_1} =$

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EE 140 / 240A Equation Sheet
Prof. Rikky Muller, Fall 2021

MOSFET Large Signal - Saturation

$$I_D=\frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$
$$V_{TH}=V_{t0}+\gamma(\sqrt{2|\Phi_F|+V_{SB}}-\sqrt{2|\Phi_F|})$$
$$V_{OV}=\Delta V=V_{GS}-V_{TH}$$

MOSFET Small Signal - Saturation

$$g_m=\mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH})=\sqrt{2\mu C_{ox}\frac{W}{L}I_D}$$
$$g_{mb}=\frac{\gamma g_m}{2\sqrt{2|\Phi_F|+V_{SB}}}$$
$$\gamma=\frac{\sqrt{2q\epsilon_s N_A}}{C_{ox}}$$
$$r_o=\frac{1}{\lambda I_D}$$

MOSFET G_m, Source Degeneration

$$G_m=\frac{g_m}{1+(g_m+g_{mb})R_S}$$

MOSFET Large Signal – Velocity Saturation

$$I_D=\frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH})V_{dsat,l}(1+\lambda V_{DS})$$
$$V_{dsat,l}\approx\frac{(V_{GS}-V_{TH})LE_{sat}}{(V_{GS}-V_{TH})+LE_{sat}}$$

MOSFET Large Signal – Triode

$$I_D=\mu C_{ox}\frac{W}{L}\left(V_{GS}-V_{TH}-\frac{V_{DS}}{2}\right)V_{DS}$$

MOSFET Small Signal – Triode

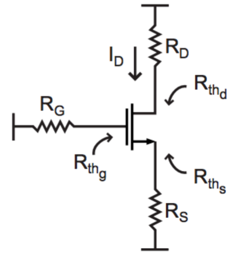
$$r_{ds}=\frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH}-V_{DS})}$$

MOSFET Capacitance

$$C_{OV}=C_{OL}=WL_DC_{ox}+WC_{fringe}$$
$$C_{gs}=\frac{2}{3}C_{ox}W(L-2L_D)+C_{ov}$$
$$C_{gd}=C_{OV}$$

$$C_{jsb\{jsdb\}}=\frac{C_j(0)WE}{\sqrt{1+V_{SB\{DB\}}/|\Phi_B|}}+\frac{C_{jsw}(0)(W+2E)}{\sqrt{1+V_{SB\{DB\}}/|\Phi_B|}}$$

Thevenin Resistances - Saturation



$$R_{thd}=r_o(1+(g_m+g_{mb})R_S)+R_S$$
$$R_{thg}=\infty$$
$$R_{ths}=(1+\frac{R_D}{r_o})(r_o||\frac{1}{g_m+g_{mb}})$$

Diode Equations

$$\psi_0=\frac{kT}{q}ln\left(\frac{N_A\,N_D}{n_i^2}\right)$$
$$W_A=\left[\frac{2\epsilon(\psi_0+V_R)}{qN_A\left(1+\frac{N_A}{N_D}\right)}\right]^{\frac{1}{2}}$$
$$C_j=A\left[\frac{q\epsilon N_AN_D}{2(N_A+N_D)}\right]^{\frac{1}{2}}\frac{1}{\sqrt{\psi_0-V_D}}$$
$$I_D=I_s\left(e^{\frac{V_D}{\eta V_T}}-1\right)$$

Mismatch

$$\sigma_{\Delta V_{TH}}\approx\frac{A_{V_{TH}}}{\sqrt{WL}}$$
$$\sigma_{\Delta W/L}\approx\frac{A_K}{\sqrt{WL}}$$

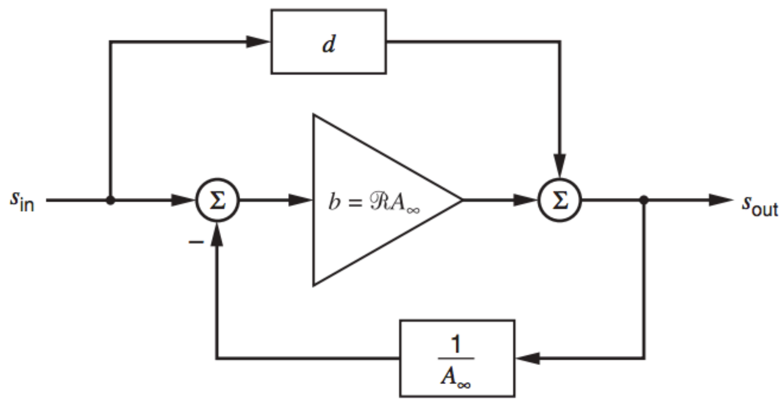
BJT Large Signal – Forward Active

$$i_e=i_B+i_c$$
$$i_B=i_c/\beta$$
$$i_C=I_Se^{\frac{v_{BE}}{V_T}}(1+\frac{v_{CE}}{V_A})$$
$$I_S=\frac{A_EqD_nn_i^2}{N_AW}$$

Bandgaps

$$V_{OUT}=V_{BE}+K\Delta V_{BE}$$
$$\frac{dV_{BE}}{dT}=-2\frac{mV}{°C}$$
$$\frac{d\Delta V_{BE}}{dT}=0.18\frac{mV}{°C}$$

Return Ratio Analysis



To find the return ratio:
1. Set all independent sources to zero
2. Disconnect the dependent source from the rest of the circuit, which introduces a break in the FB loop
3. On the side of the break that is not connected to the dependent source, connect an independent test source s_t
4. Find the return signal s_r generated by the dependent source.
5. $RR = -s_r/s_t$
6. d is found by setting the dependent source of the amplifier = 0
7. A_∞ is determined by the passive feedback network = 1/f

$$\frac{s_{out}}{s_{in}} = \frac{A_\infty RR}{1+RR} + \frac{d}{1+RR} \qquad Z_{CL} = Z_{OL}\frac{(1+RR_{short})}{1+RR_{open}}$$

Common Laplace Transform Pairs

$f(t)$	$F(s)$
$u(t)$	$\frac{1}{s}$
e^{-at}	$\frac{1}{s+a}$
$\sin(\omega t)$	$\frac{\omega}{s^2+\omega^2}$
$\cos(\omega t)$	$\frac{s}{s^2+\omega^2}$
$e^{-at}\sin(\omega t)$	$\frac{\omega}{(s+a)^2+\omega^2}$
$e^{-at}\cos(\omega t)$	$\frac{s+a}{(s+a)^2+\omega^2}$