Lab 2: Long Channel Amplifier Design

EE140/240A – Linear Integrated Circuits

Spring 2024

Objective

Since MOS technology plays a central role in today's analog integrated circuits, it is important to have a good understanding of MOS transistor amplifier analysis and design. The goal of this lab is to enable you to understand the relationships between gain, bandwidth, device dimensions and bias point specifications for MOS amplifiers through a design problem. Most of the knowledge obtained in this lab will be used in the design project later this semester.

Specifically, the objective of this lab is to analyze, design, and simulate a single-stage common source (CS) amplifier to satisfy a given set of specifications. Design objectives can be accomplished and verified using hand calculations and simulations.

Deliverable

Lab Report: The main goal of this lab is to give you experience designing a circuit, so we want to see clear evidence of your design procedure, such as any hand calculations you made, the assumptions you used, and what effects you find in your design choices have on the final amplifier design. This lab report will be graded on your ability to explain these design choices, as well as achieving the design specifications (i.e., proving them through ADE Explorer). In addition, there are other questions that will be asked of you throughout the lab that you must answer in your lab report.

There is no checkoff portion to this lab. Instead, the GSI (Matthew) will check-in with everyone in Week 2 to ensure you are on the right track in designing this amplifier.

Deadline

You will have a total of three weeks to do this lab. A written report should be submitted through bcourses (in a pdf), including LEGIBLE plots, the relevant design equations and a description of the design methodology you took.

The lab is split into two parts.

- In Part A, you'll apply hand-calculation methods and match them to simulated results to get a feel for the MOS models we are using. Then, you will learn how to determine and measure amplifier characteristics on designs we give to you.
- In Part B, we will give you a list of specifications and a circuit topology. Your job is to utilize hand calculations to achieve the specifications, and verify your circuit performance in Cadence.

The entire lab (Parts A and B) are due in 3 weeks (due February 27th at 11:59pm). However, Part A should take around 1 week, and Part B should take around 2 weeks. This means you might need to spend time outside of lab hours to work on the lab.

You are to work on this lab individually. Although you can discuss generalities with other students in the class, you are not to perform the design in teams or groups.

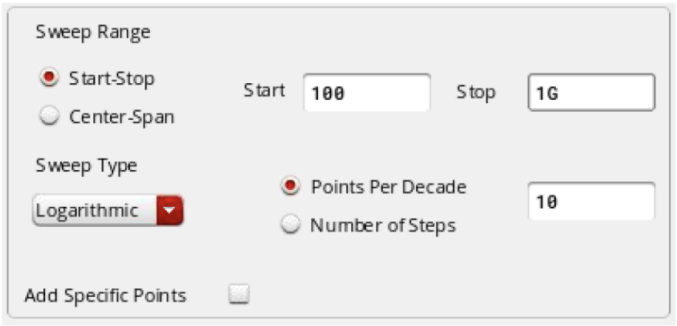
Background

In Lab 1, you learned how to set up a simulation testbench to run transient and DC simulations using ADE, and wrote expressions for circuit performance using the calculator. Both of these skills will be useful for this lab. Specifically, you will need to estimate small-signal voltage gain, 3 dB bandwidth, output resistance, and voltage swing of a few different amplifiers. Here are some tips on finding these paramters in simulation:

Voltage Gain and Bandwidth

In Lab 1, you calculated voltage gain via transient simulation. A faster way of determining gain is to use AC analysis, which allows you to view the frequency response (amplitude as a function of frequency) of any node in a circuit. To configure a testbench for AC simulation:

- Ensure that your testbench schematic contains one input source with "AC Magnitude" field set to 1. This field is present for both DC sources (like "vdc" in analogLib) or sinusoidal sources (like "vsin" in analogLib) that can be used in transient simulations. The "AC Magnitude" field is used specifically for AC simulation, so it will not affect any transient or DC simulations that are also running.
- Add an AC analysis in ADE using the "Choose Analyses" window. Choose "ac" for the analysis type, and select "Frequency" as the Sweep Variable. Sweep a range of frequencies suited to the circuit you are testing. The example below sets the AC source to sweep frequency logarithmically from 100 Hz to 1 GHz.



- Add the AC magnitude of the node you would like to test to your simulation outputs. For instance, if the output node is labeled "out," the AC output can be defined as follows.

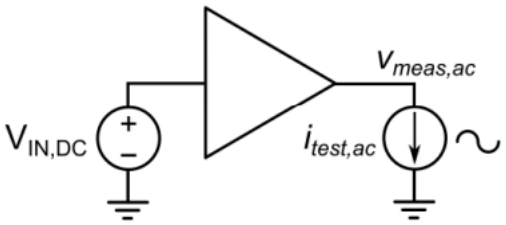
Name	Type	Details	Plot	Save	Spec
out	expr	mag(v("/out" ?result "ac"))	☑	☐	

Define calculator expressions for the variables you would like to measure: The mid-band or low-frequency voltage gain will be the maximum gain achievable, and can be found using the expression ymax(out). The 3 dB bandwidth can be calculated as bandwidth(out 3 "low").

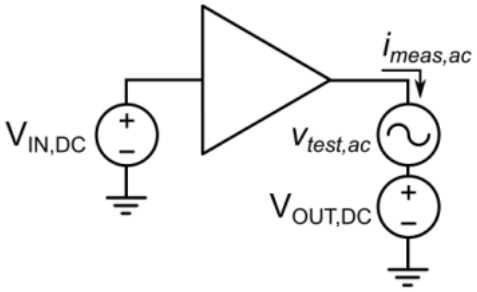
Output Resistance

The output resistance of an amplifier is a bit less straightforward to simulate, but there are a few approaches you can take:

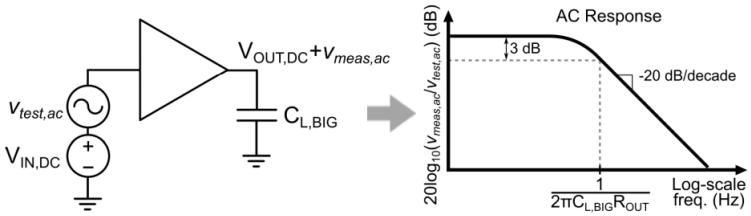
- **Direct measurement**: You can place a test source (current or voltage) at the output of the amplifier and measure the amplitude of the response (voltage or current) to find the output resistance directly. Remember that output resistance is a small-signal parameter, so this should be done with an AC or sinusoidal test source biased around the nominal DC operating point of your amplifier. Your output resistance will be a ratio of differences (max - min values), and not DC values. The amplifier's input should be set to its DC bias point. A sample test setup using a sinusoidal current source ("isin" in analogLib) is shown below R_{out} can be calculated via transient analysis using the equation shown below. In AC analysis, measurements are by default a ratio relative to the specified "AC magnitude" parameter. R_{out} is then $V_{\text{meas, ac}}/i_{\text{meas, ac}}$



  There is also a sample test setup using a voltage source. This method can be used, but is not recommended. The DC component of the output voltage source needs to be set to the measured DC output voltage exactly, unlike in the above method.



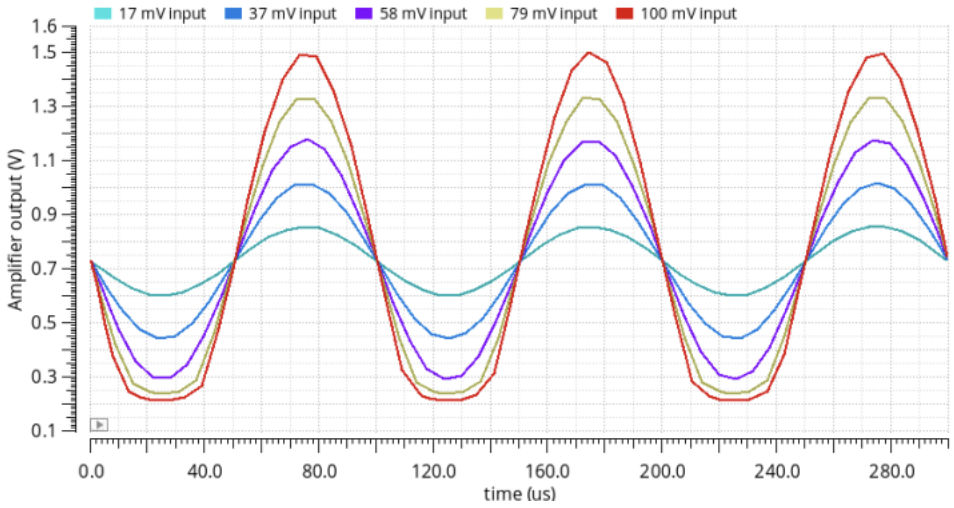
- **Output pole estimation**: The small-signal output resistance can be calculated from the RC time constant at the output of the amplifier. To measure this time constant, use a very large load capacitor. This will guarantee that the load capacitance is known and that $R_{out}C_L$ sets the dominant pole of your circuit. If this is the case, the amplifier's 3 dB bandwidth will be given by $1/(2\pi R_{out}C_L)$. If you use this method, be sure that C_L is sufficiently large (your bandwidth should vary with C_L so that the R_{out} you calculate is independent of C_L). Here is a diagram of this technique:



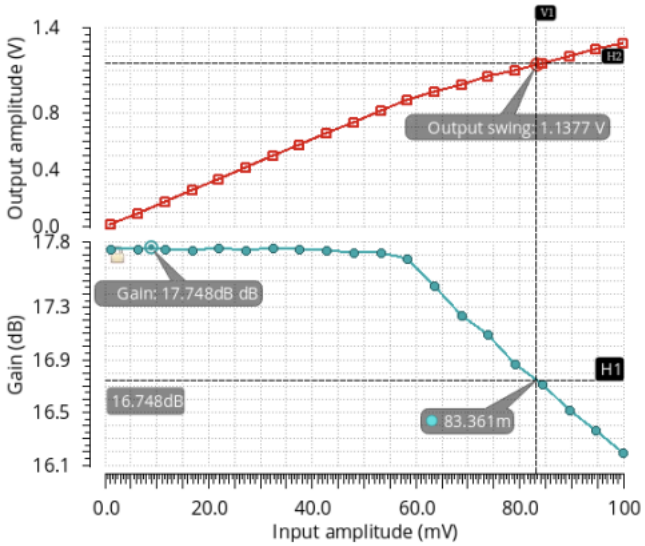
Voltage Swing

As you seen in Lab 1, voltage swing can be estimated by finding the range of output voltages that ensure all transistors are in saturation. In more realistic scenarios, voltage swing would be typically measured in terms of distortion or linearity. These are many metrics for characterizing the linearity of an amplifier. One of these is the "1-dB compression point," which considers how much an amplifier's gain degrades as a function of input signal swing due to compression at the output.

- This plot shows the output of the same amplifier in response to input sine waves of growing amplitudes. As the input amplitude exceeds 79 mV, the gain reduces because the amplifier's output cannot go beyond a certain point. Eventually, device bias points change and small-signal approximations are no longer valid.



- This plot shows gain and output swing as a function of input amplitude to illustrate the 1 dB compression point. If we define maximum output swing at the 1 dB compression point, this amplifier has a swing of 1.14 V.



Process Model

For this lab, assume the following parameters for the transistor when doing hand calculations and simulations:

Parameter	NMOS	PMOS
Model Level	3 (in HSPICE)	3 (in HSPICE)
VTO	$0.8\ V$	$-0.8\ V$
KP	$90\ \mu A/V^2$	$30\ \mu A/V^2$
Gamma	$0.8\ \sqrt{V}$	$0.4\ \sqrt{V}$
Lambda	$0.01\ V^{-1}$	$0.02\ V^{-1}$
TOX	200 Å	200 Å
XJ	$0.5\ \mu m$	$0.5\ \mu m$
LD	$0.3\ \mu m$	$0.3\ \mu m$
PHI	$0.7\ V$	$0.6\ V$
NSUB	$3.33 \times 10^{16}\ cm^{-3}$	$3.33 \times 10^{15}\ cm^{-3}$
RSH	$0\ \Omega$	$0\ \Omega$
CGSO	$500\ pF/m$	$500\ pF/m$
CGDO	$500\ pF/m$	$500\ pF/m$
CGBO	$0\ F/m$	$0\ F/m$
CJ	$500\ \mu F/m$	$500\ \mu F/m$
MJ	0.5	0.5
CJSW	$0\ F/m$	$0\ F/m$
MJSW	0.33	0.33

Lab Setup

This section describes how to use the transistor model we will be working with in Virtuoso. In Lab 1, you used a generic 45 nm CMOS PDK provided by Cadence. In this lab, we will use a spice file suited to long-channel devices that will align more closely with your hand calculations. Navigate to your Cadence directory and copy the netlist by typing:

```
cd  /cadence
cp /home/ff/ee140/fa18/lab1/ee140.sp .
```

Take a look inside the spice model by typing:

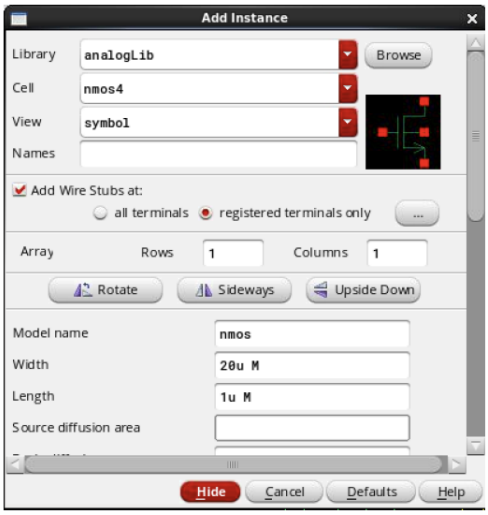
```
gedit ee140.sp &
```

Now you can open Cadence as shown below:

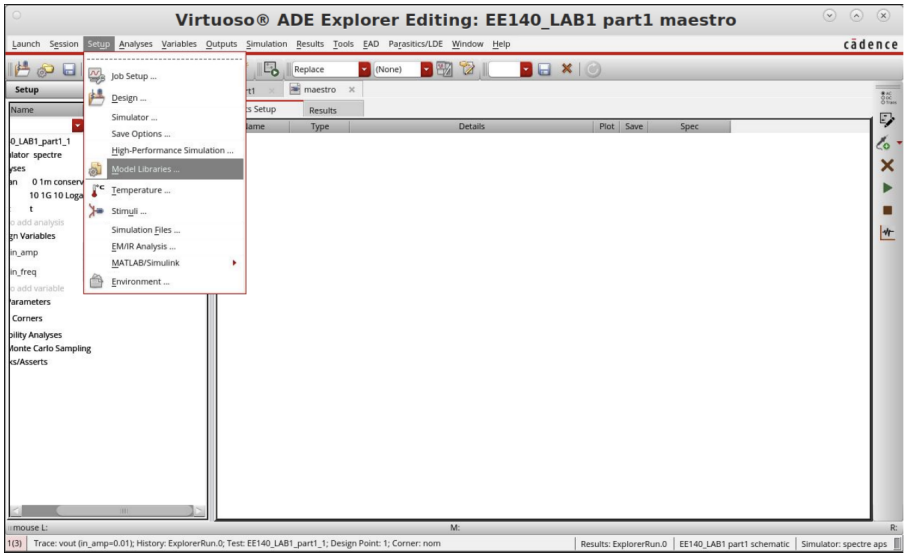
```
source /share/b/bin/cds/6
virtuoso &
```

Create a new library called “lab2”. Unlike Lab 1, select “Do not need process information” when asked about a Technology file. This library does not need to be attached to a particular technology file, since you will be using the provided spice model for the transistors.

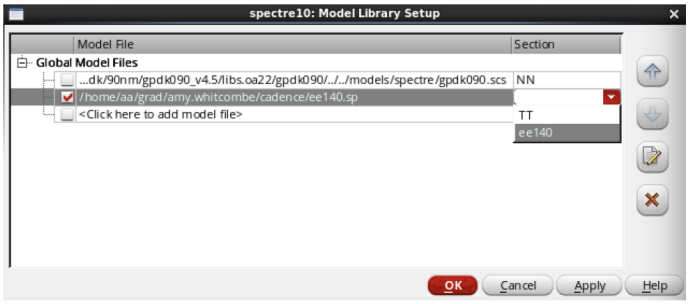
To use this spice model, instantiate the nmos4 (or pmos4) element from the analogLib library in your schematic. Enter “nmos” (or “pmos”) in the “Model name” field and specify the appropriate dimensions, as shown below. Note that the length in this case is in the μm range, because we are using a long-channel device model.



To simulate your circuits, go to Setup -¿ Model Libraries in the ADE Explorer window.



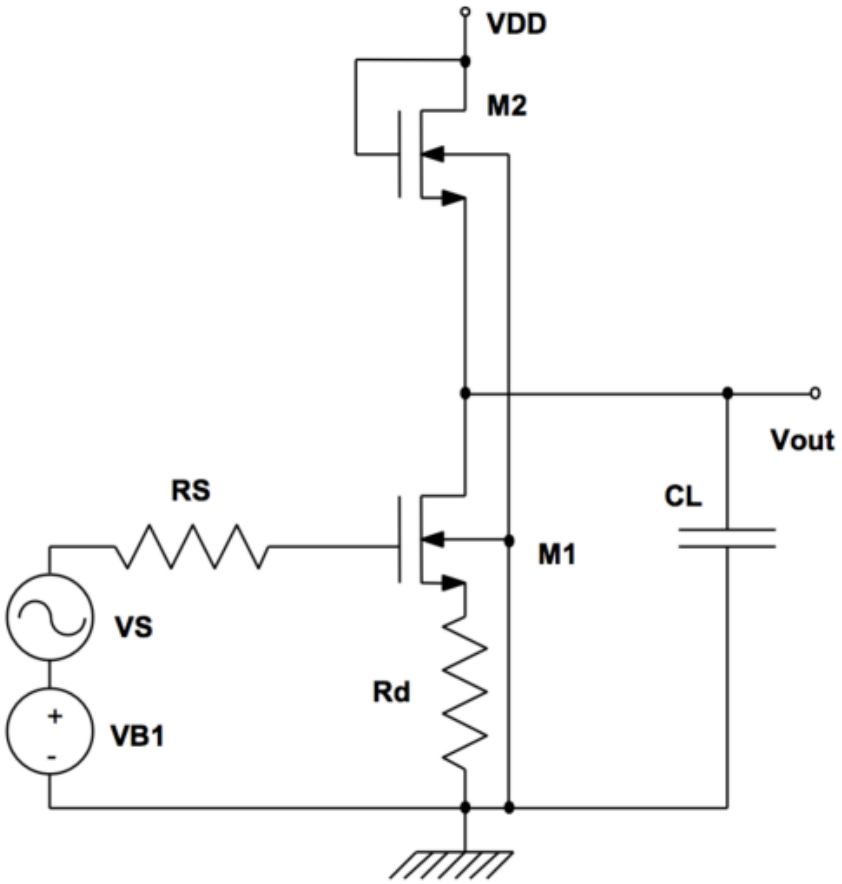
Include your copied ee140.sp file, and change the "section" parameter to ee140



You should now be able to run simulations referencing the provided SPICE model.

Part A: Analysis and Simulation

In this first part, you will analyze and simulate a saturated NMOS load degenerated-source amplifier, shown below.



Scenario 1.
Assume that $V_{B1} = 1.1\ V$, $R_d = 0$ (i.e. no degeneration), $(W/L)_1 = (50/5)\ \mu m/\mu m$, and $(W/L)_2 = (10/90)\ \mu m/\mu m$. $V_{DD} = 5\ V$, $R_s = 5\ k\Omega$ and $C_L = 2.5\ pF$.

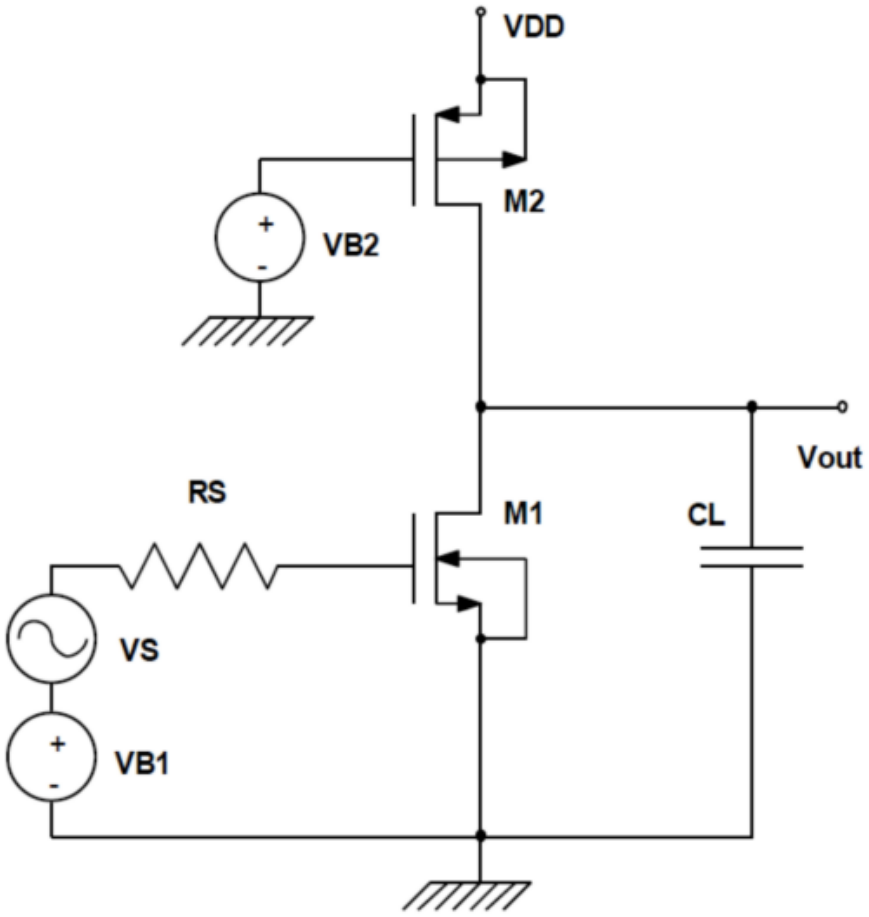
Scenario 2.
Assume that $V_{B1} = 1.2\ V$, $R_d = 2.5\ k\Omega$, $(W/L)_1 = (50/5)\ \mu m/\mu m$, and $(W/L)_2 = (10/90)\ \mu m/\mu m$. $V_{DD} = 5\ V$, $R_s = 5\ k\Omega$ and $C_L = 2.5\ pF$.

For each scenario, answer the following:

- Determine the small-signal gain v_{out}/v_s using both hand calculation and simulation. You should plot the magnitude of the gain (in dB) vs. log-scale frequency for this amplifier. You may make any reasonable approximations in your hand calculations, but be sure to write them down. Use the $G_m R_{out}$ method for your hand-calculations (see Ed Discussion for the method).
- Determine the cutoff frequency (3 dB bandwidth) using both hand calculations and simulation. You may make any reasonable approximations in your hand calculations, but be sure to write them down.
- Determine the maximum output voltage swing that this amplifier can deliver. You do not have to calculate output swing, only the simulated value and plot needs to be reported.

Part B: MOS Amplifier Design

In this part, you are asked to design a common-source amplifier with a saturated PMOS load as shown in the figure below:



You get two DC sources, VB1 and VB2. These can be biased to what your design sees fit. You have to determine the values of these two sources, and you can treat them as two external elements in the amplifier. Design the above comon-source amplifier so that it satisfies the following specifications:

Parameter	Specification – EE140	Specification – EE240A
Midband gain	≥ 120 V/V	≥ 140 V/V
3 dB cutoff frequency (bandwidth)	≥ 180 kHz	≥ 200 kHz
Output voltage swing	≥ 3 Vpp	
Load capacitance	2.5 pF	
Source resistance	5 kΩ	
Supply voltage	VDD = 5 V, VSS = Ground = 0 V	

Design Considerations

There are several important issues you have to remember as you design your amplifier:

1. Note that the Lambda value is given for $L = 5\ \mu m$. All of your transistors should have a length of $5\ \mu m$. You cannot use any other channel length for this problem. For Lambda calculations, you can ignore lateral diffusion and assume that the value of Lambda at $L = 4.4\ \mu m$ is the same as that at $L = 5\ \mu m$.
2. The gate oxide thickness is provided so that you can calculate the capacitances that you need in your calculations. Note that some of the capacitance paramters that are typically needed are already calculated for you. You may need some of these in your design.
3. When you perform the design, you should ensure that the circuit is biased such that all transistors are in saturation. This may require fine tuning of the bias voltages VB1 and VB2 down to the millivolt value. The reason for this is that the amplifier has such a high gain that the slightest shift in bias point will cause one of the transistors to come out of saturation. We will fix this issue later.
4. When biasing these transistors, you should not use a $|V_{GS} - V_T|$ of smaller than $200\ mV$ for either of the transistors. This means that the $|V_{GS}|$ across either transistor has to be higher than $1.0\ V$.

Discussion

In your lab report, please make sure to also answer and do the following:

- For your design, you need to determine the dimensions of M1 and M2, as well as the values for bias voltages VB1 and VB2. In addition to hand calculations and simulations showing that the design specifications have been met, calculate the output resistance of the final amplifier and compare it with the output resistance of the CS amplifier used in Scenario 1 of Part A. How does the output resistance affect the gain and bandwidth?
- Using explicit voltage sources to bias amplifiers is not good practice (think about why). The bias voltages should be generated locally using current mirrors. Now, assume that you are given a single reference current source. Rework the biasing network and simulate the gain and bandwidth of your amplifier. If these values are different from the gain and bandwidth of your original amplifier, explain why. Afterwards, achieve the specifications using the current mirror.
- When you have finished your design, please prepare a table comparing the design specifications to your circuit's calculated and simulated performance. You should show both hand calculations and simulations to demonstrate that the specifications have been satisfied. All equations should be in variable form before numerical evaluation. Record plots (or tables) of simulation results where necessary and make sure that all plots are labeled appropriately. Your hand calculations and simulation results may differ quite significantly; if you observe this, try to explain why this is the case.
- You should also describe your design procedure. Discuss your design tradeoffs and outline the design strategy you used. You should try your best to achieve the design specifications. If you cannot meet the design specifications, consider what critical factors prevented you from achieving your design goals and suggest directions for modifying your design to meet specifications. If after all attempts you fail to meet all the design specifications, be prepared to show us your final design and describe what you consider to have been the most restrictive and problematic spec to meet.

Grading

The lab report is 50pts. The breakdown is as follows:

- (15pts) Part A. Each scenario is 10 points each, and you must include both hand calculation and simulation results for the items listed in Part A. Include your circuit schematic with DC operating points annotated and include the required plots.
- (35pts) Part B. This includes your design being driven by hand calculations, meeting the specifications and showing the results correctly through ADE Explorer, answering the discussion questions, and modifying the circuit to meet the specifications with the current mirror. Points for not meeting the specifications can be earned back through a thorough explanation of what you could try to reach the specifications.