EE 140/240A Analog Integrated Circuits
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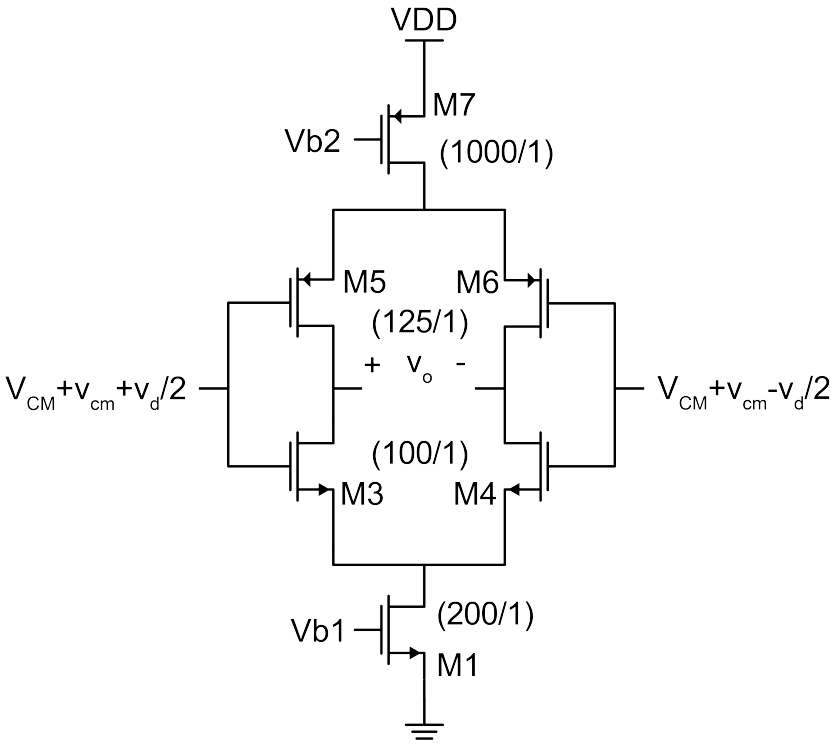
Review MT2

1 Problem 1

For this problem consider the circuit schematic below. The numbers next to each transistor are W/L. Let $VDD = 2\text{V}$, $\mu_n C_{ox} = 0.5\text{mA/V}^2$, $\mu_p C_{ox} = 0.4\text{mA/V}^2$, $V_{Tn} = 0.3\text{V}$, and $V_{Tp} = 0.4\text{V}$. For all transistors $\lambda = 0.1\text{V}^{-1}$. You may neglect channel length modulation when calculating DC operating points.



(a) Assume that Vb1= 0.5V and that M1 is in saturation. Compute the value of Vb2 such that M7 can be biased saturation.

(b) Compute the common mode input range of the amplifier. In other words, what is the range of values of V_{CM} for which all transistors remain in saturation. Assume that the DC common mode output voltage is always set to be equal to 1V (half the supply) through a feedback circuit not shown here.

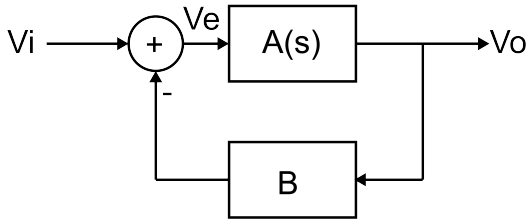
(c) Compute the differential gain, $A_d = \frac{v_o}{v_d}$. In your solution, please note any reasonable approximations that you made.

(d) Compute the common mode gain $A_{cm} = \frac{v_o}{v_{cm}}$. In your solution, please note any reasonable approximations that you made.

(e) Compute the CMMR. Suggest a way of increasing the CMMR without affecting the differential mode gain of the circuit.

2 Problem 2

For this problem, consider the generalized negative feedback system below. The amplifier has a transfer function $A(s)$ has a single pole such that $A(s) = \frac{A_o}{1+s/\omega_p}$.



(a) Compute the closed loop transfer function, $A_f(s) = \frac{Vo}{Vi}(s)$. How poles and zeros are there? What are their values in terms of the given variables?

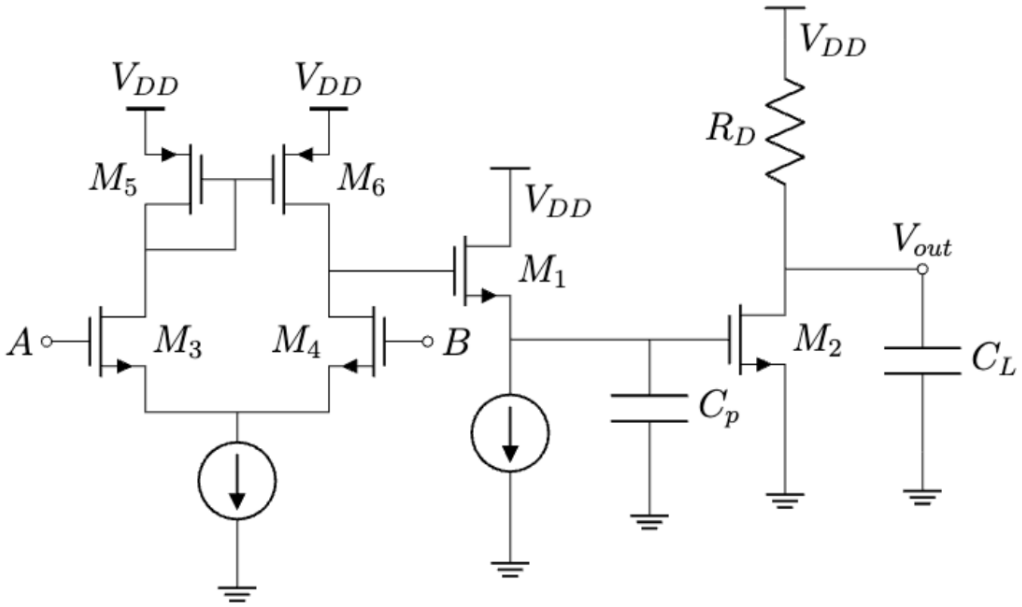
(b) Assume that $A_o = 1000$ and $\omega_p = 1000$rad/s. Plot the following vs. angular frequency: (a) the magnitude of the open loop transfer function $A(s)$ and the magnitude of the closed loop transfer function $A_f(s)$ when (b) $B = 1/100$, (c) $B = 1/10$ and $B = 1$. Mark all the 3dB points and DC gains in every case. Label your plot clearly.

(c) You want to design a unity gain buffer ($B = 1$) where the error v_e is less than 1%. How high does your DC gain of your open loop amplifier, A_o need to be? Assume operation within the 3dB bandwidth of the closed-loop system.

(d)

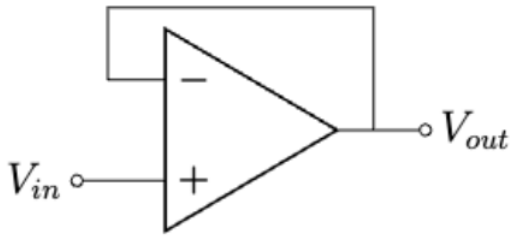
3 Compensation of an Amplifier

In this problem, we will analyze the 5T Workhorse Amplifier you have seen in lecture and lab. This is the first stage of our amplifier. We cascade it with a source follower and a common source amplifier. Only consider the explicitly drawn capacitors. Assume $C_L >> C_p$. All transistors have the same transconductance g_m. M_1 and M_2 do not have channel-length modulation, that is $r_{o1} = r_{o2} = \infty$. M_3, M_4, M_5, M_6 all have channel-length modulation, and $r_{o3} = r_{o4} = r_{o5} = r_{o6}$. Assume $g_m r_o >> 1$ and $g_m R_D >> 1$.



(a) Find the DC open-loop gain A_o.

(b) Assume we want to put the above circuit in unity-gain feedback as shown below. Circle below whether to tie node A or B to V_{in} or V_{out}, and explain why.



A : V_{in} V_{out}

B : V_{in} V_{out}

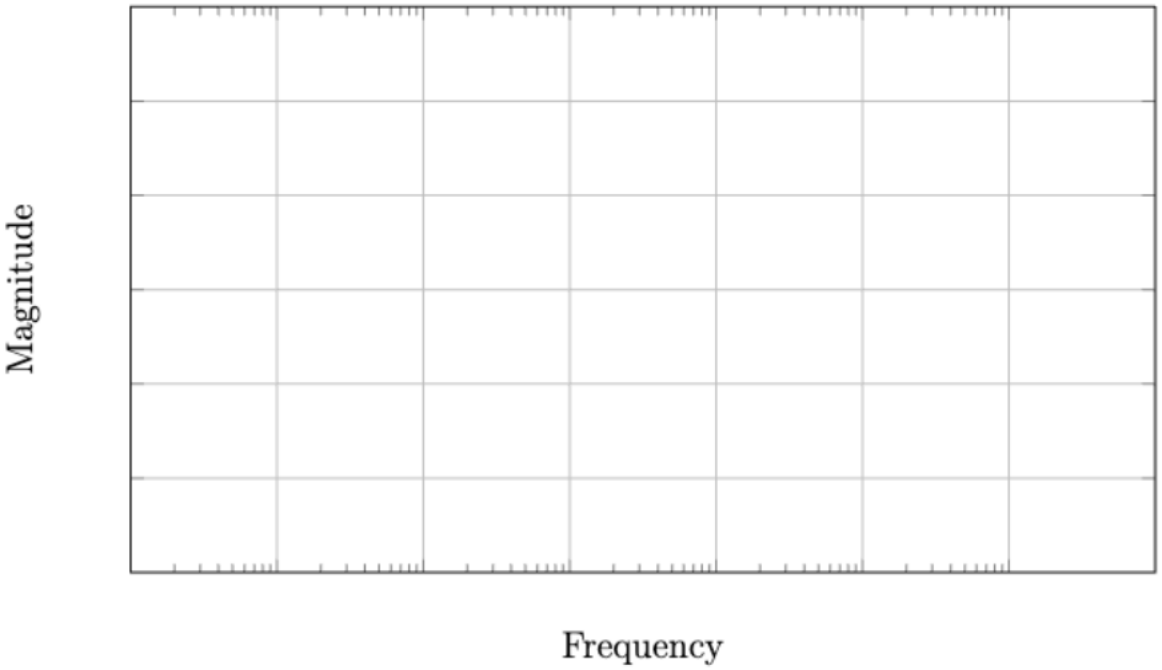
(c) Define loop gain to be $\beta H(s)$, where β is the feedback factor, and $H(s)$ is the open-loop transfer function. This quantity $\beta H(s)$ is an important quantity when talking about the stability of the op amp.

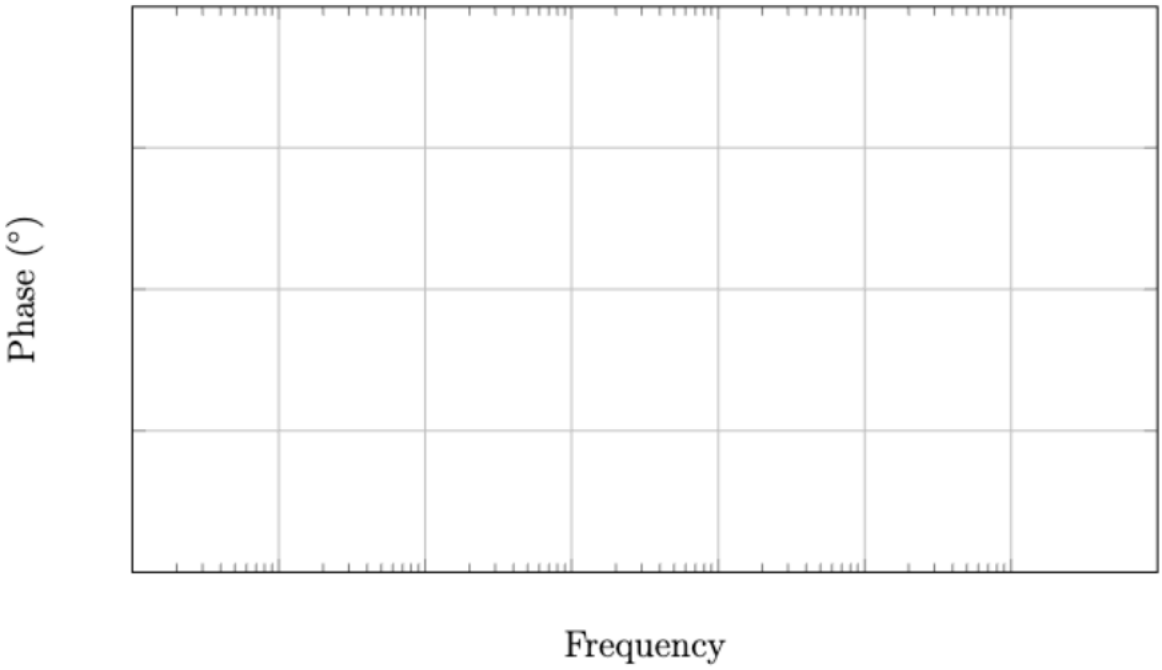
Identify the frequency of the two poles of the loop gain in units of rad/s. What is $LG(s)$? Write it in the form

$$LG(s) = \frac{K}{\left(1+\frac{s}{w_{p1}}\right)\left(1+\frac{s}{w_{p2}}\right)}$$

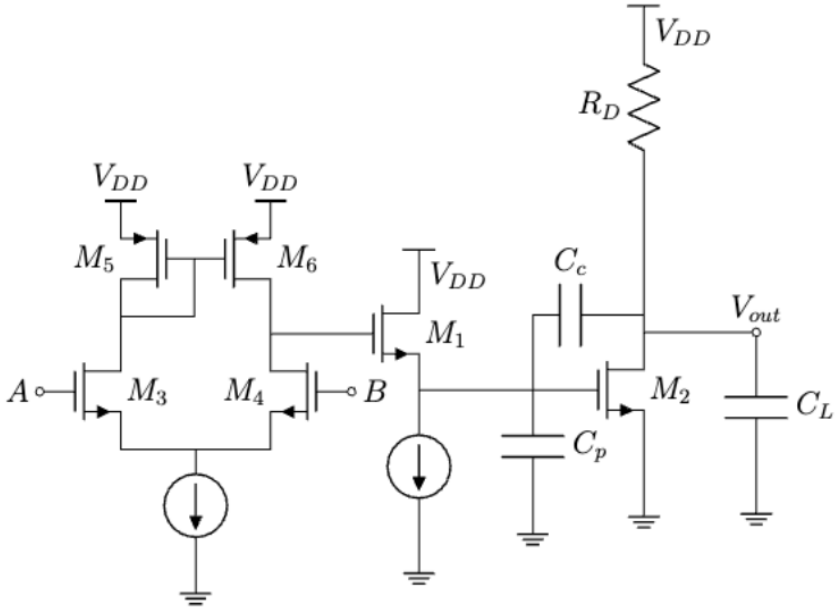
(d) Of the poles you found in part (c), which is the dominant pole?

(e) On the next page, plot the magnitude and phase Bode plot of the $LG(s)$. Assume that the poles are more than 2 decades apart from each other, and that the non-dominant pole is placed at the unity gain frequency. Be sure to label $LG(s=0)$, all poles (w_{p1}, w_{p2}), as well as important phase degrees.

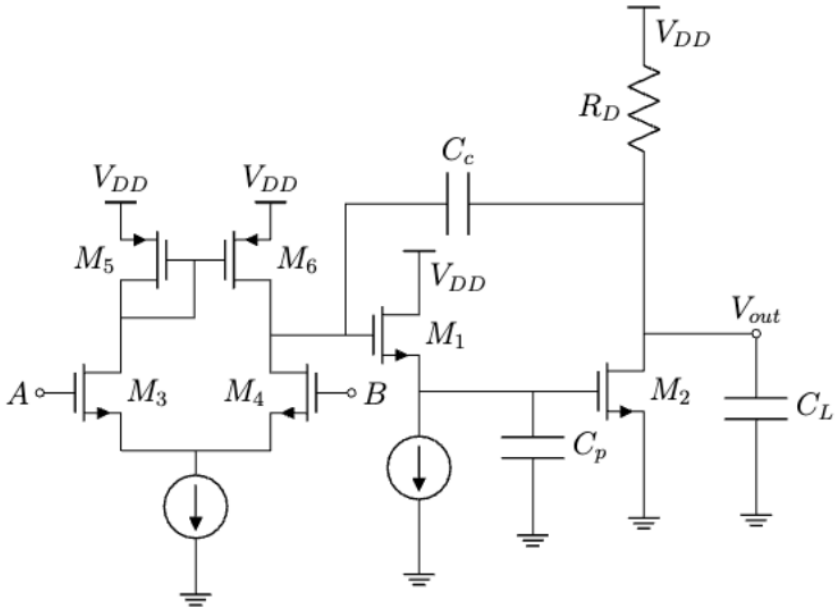

Magnitude
Frequency


Phase (°)
Frequency

(f) Now consider the following circuit with compensation capacitor C_c. Assume the node at the gate of M_2 contributes to the dominant pole. Use the Miller approximation to find the frequency this pole occurs at.



(g) Now consider the following circuit with compensation capacitor C_c. Assume now the node at the gate of M_1 contributes the dominant pole. At which frequency does this dominant pole occur? Use the Miller approximation.



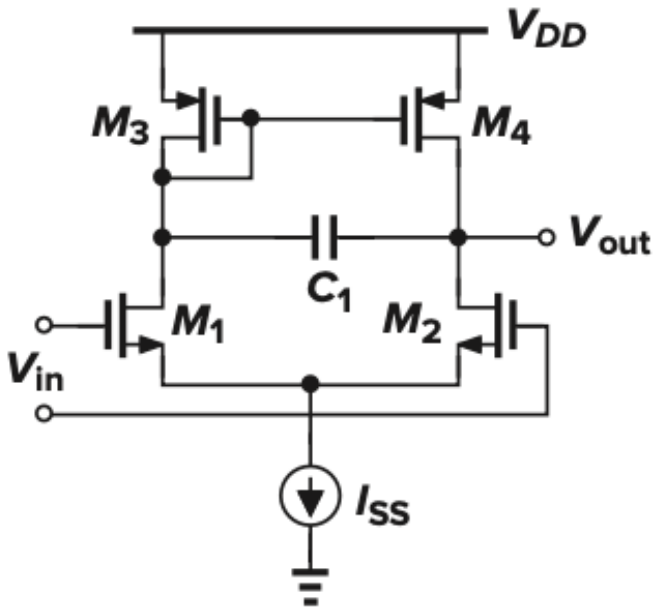
4 Half-Circuits

While snooping around Cadence, you found a bunch of random differential amplifier schematics. You want to take a look and see which ones might be cool to do your final project on.

For this question, we will look and determine the differential and common mode gain of various circuits. Assume all the biasing is done correctly, and that each transistor have the same small-signal parameters.

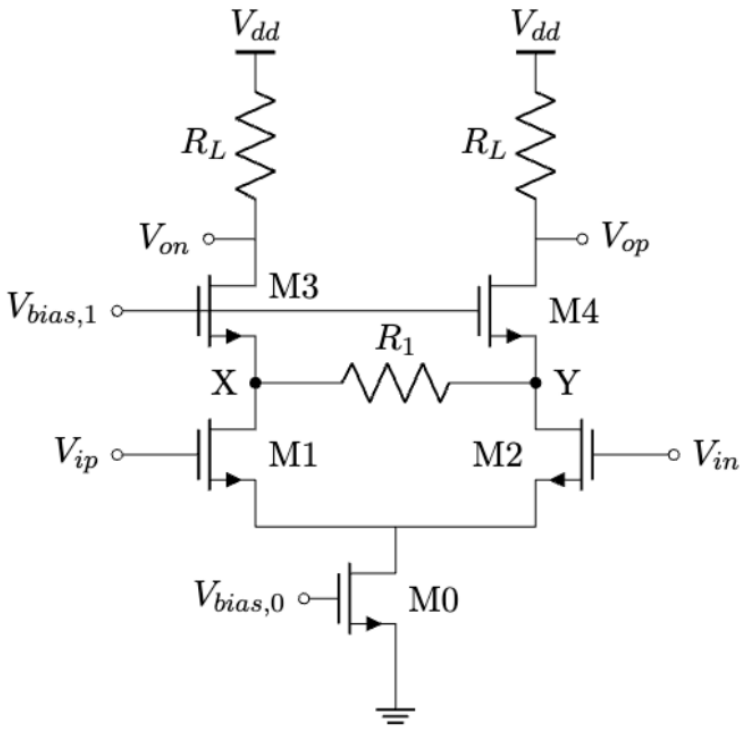
(a) There seemed to be a lab_3 Library, and you saw the 5T Workhorse amplifier. Draw the differential and common mode half-circuit and determine A_{vd}, A_{cd}, the differential and common mode gain.

(b) You also see another similar 5T amplifier, but there is a capacitance, and you think this is likely to model the effects of the capacitance produced during layout.



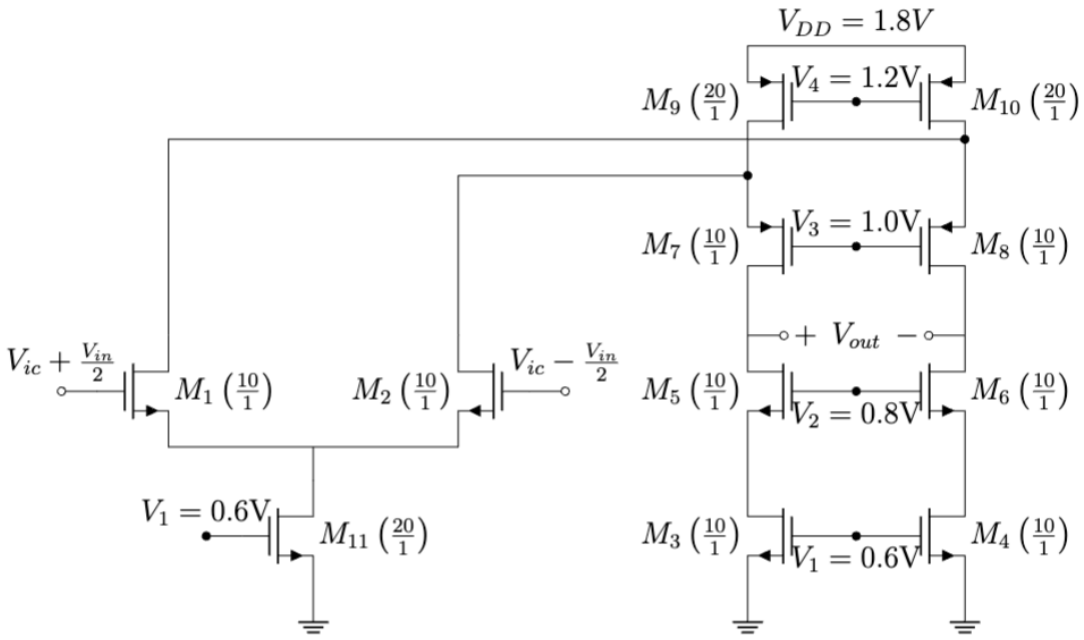
Draw the half-circuits. What is the gain at DC (s = 0) and at very high frequencies (s = ∞)?

(c) It seemed there is another similar amplifier you found within this library that includes a weird resistor connecting the outputs. You figured that due to an error while fabricating the differential amplifier shown below, R_1 was accidentally connected to the intermediate nodes X and Y.



Draw the half-circuits and determine A_{vd} and A_{cd}

(d) In a different library called ee140_project, you see a schematic of a folded cascode differential amplifier. It looks very complicated, but you wanted to analyze this one.



Draw the differential half circuit for this amplifier. Find the output impedance R_{out} of this amplifier (As a challenge, find the G_m of this amplifier.)