EE140 Fall 2023

Final Design Project

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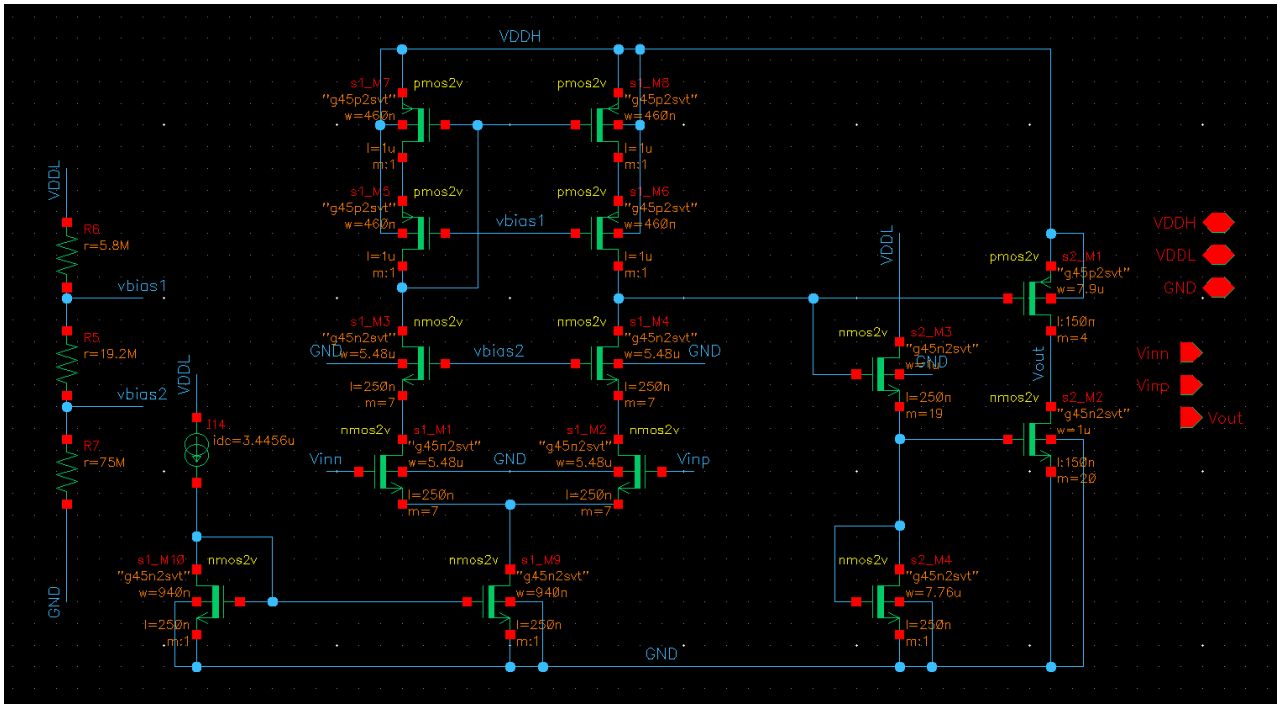
I. Overview

(1) Schematic:



(2) Description:

The first stage is a telescope NMOS amplifier. The voltage bias point is set to be vbias1= 1.13V and vbias2 = 0.9V. The second stage is a class AB amplifier with the input to the PMOS. A NMOS source follower is applied to set the vbias of the NMOS and keep the amplified value of stage 1.
The first stage contributes to most of the gain of the amplifier. The second stage is designed to have a good slew rate.

(3) Comparison Table:

	Project SPEC	Designed Value
Settling Time	180ns	173ns
Power Consumption	<=1.1mW	482.41uW
Total Capacitance	4pF	50fF
Total Resistance	100M Ohm	100M Ohm
CMRR at DC	>= 65dB	70.5221 dB
PSRR at DC	>= 50dB	59.78 dB
Phase Margin	>=45 degree	53.5 degree
FoM	$\frac{10^{-9}}{T_{settle} * P_{total}}$	11.98

II. Design

(1) Settling time

The frequency is 60Hz and the number of pixels is 272x340. So the settling time can be calculated from the equation below:

$$T_{settling} = \frac{1}{60 * 272 * 340} = 180ns$$

I design the static and dynamic error each set to be 0.1%.

The equation below shows the required DC gain to get a 0.1% static error.

$$\varepsilon_s = \frac{1}{1 + \beta A_{DC}}$$

$$A_{DC} = \frac{1}{\beta}\left(\frac{1}{\varepsilon_s} - 1\right) = \frac{1}{\frac{1}{3}}\left(\frac{1}{0.1\%} - 1\right) = 2997$$

The equation below shows the required closed loop gain dominant pole frequency.

$$\varepsilon_d = e^{-T_{settling}/\tau_{3dB}}$$

$$\tau_{3dB} = \frac{T_{settling}}{\ln \varepsilon_d} = \frac{180ns}{\ln 0.001} = 26.05ns$$

$$f_{3dB} = 38.39MHz$$

(2) gm of each stage

Since there is a compensate capacitor, the other poles are separate from the dominant pole and are way larger than the unity gain bandwidth. Thus, we can see the system as a single pole system.

For the single pole system, the loop gain is as follows:

$$\beta H = \frac{\beta A}{1 + sw_p}$$

The unity gain bandwidth of loop gain is $\beta A w_p$

The closed loop gain of the single pole system is as follows:

$$\frac{H}{1 + \beta H} = \frac{\frac{A}{1 + sw_p}}{1 + \frac{\beta A}{1 + sw_p}} = \frac{1}{1 + \beta A} * \frac{A}{1 + \frac{s}{w_p(1 + \beta A)}}$$

The dominant pole of the closed loop gain is located at $w_p(1 + \beta A) \approx \beta A w_p$

We can tell from the equation that the unity gain bandwidth of loop gain is equal to the dominant pole of the closed loop gain.

$$f_u = f_{3dB} = 38.39MHz$$

For a 45 degree of phase margin, the non-dominant pole $w_{p2} = w_u = 2 * pi * f_u$

From the lecture, the dominant pole is located at Cc, the nondominant pole is located at CL.

We can calculate the gm2:

$$gm_2 = w_{p2} * C_L$$

For gm1, we know that the DC gain is $\beta A_1 A_2$, and dominant pole $w_{p1} = \frac{1}{r_{o1} C_C A_2}$.

We can get:

$$w_u = \beta A_1 A_2 w_{p1} = \frac{\beta A_1 A_2}{r_{o1} C_C A_2} = \frac{\beta A_1}{r_{o1} C_C} = \frac{\beta gm_1 r_{o1}}{r_{o1} C_C} = \frac{\beta gm_1}{C_C}$$

$$gm_1 = \frac{w_u C_C}{\beta}$$

(3) sizing of the transistors

From (2), we get the wu. And we can apply an Cc on the circuit.

For stage 1, I follow the gm/id script to sweep my gm/id and pick a reasonable length so that the ft of the transistors can meet the fu specification and that the gain is maximum. Also, considering the phase margin, I also sweep the Cc to get a reasonable phase margin. Once I pick the gm/id, then use the script to find the CDD/W and JD. By doing iterations of calculating gm, I can calculate the gain.

For stage 2, I sweep the gm/id of the PMOS to get the input voltage is bias at the same as the output voltage of the first stage. For the NMOS, I pick a small gm/id to reduce the power. Then use the parameter of the PMOS and NMOS to size the source follower.
I will describe more about the sizing in the discussion part.

III. Transistor and Bias Summary

MOS name	I_D	V_{GS}	g_m	g_{ds}
S1_M1	1.2351u	377.02m	33.672u	1.9146u
S1_M2	1.2352u	377.02m	33.675u	1.9145u
S1_M3	1.2351u	395.20m	34.441u	625.26n
S1_M4	1.2352u	395.13m	34.479u	621.79n
S1_M5	1.2350u	587.14m	14.611u	329.80n
S1_M6	1.2349u	587.21m	14.603u	332.89n
S1_M7	1.2351u	578.33m	12.635u	2.2231u
S1_M8	1.2349u	578.33m	12.632u	2.2256u
S1_M9	2.4703u	545.56m	39.857u	3.5274u
S1_M10	3.4456u	545.56m	52.831u	1.9606u
S2_M1	221.21u	573.97m	3.3865m	84.092u
S2_M2	228.63u	610.17m	2.8979m	84.606u
S3_M3	57.663u	615.85m	932.41u	33.034u
S4_M4	57.663u	610.17m	728.40u	25.284u

IV. Discussion

(1) Design Flow:

I try to design a large gain amplifier at stage 1, which provides most of the gain needed to meet the static error. Thus, I choose the NMOS telescope amplifier as my first stage. Then I design a Class AB Common Source as my second stage to get a better slew rate. The gain of second stage is not necessarily to be large. However, we should apply a large current, small length device to get a better slew rate.

(2) Optimize the gain of stage 1 amplifier:

We know the gm1 value from beta, Cc, fu. Then the matlab script can help sweep the gm/id to try the best Av, filtering the gm/id that doesn't pass the fu. We know the gain of a telescope amplifier as follows:

$$A_V \approx g_{m2}(g_{mb}r_{o6}r_{o8} \parallel g_{m4}r_{o2}r_{o4})$$

$$= g_{m2}\frac{g_{mb}r_{o6}r_{o8}g_{m4}r_{o2}r_{o4}}{g_{mb}r_{o6}r_{o8}+g_{m4}r_{o2}r_{o4}}$$

$$= \frac{(g_{m2}/I_D \times g_{mb}/I_D \times g_{m4}/I_D)/(g_{ds6}/I_D \times g_{ds8}/I_D \times g_{ds2}/I_D \times g_{ds4}/I_D)}{(g_{mb}/I_D)/(g_{ds6}/I_D)(g_{ds8}/I_D)+(g_{m4}/I_D)/(g_{ds2}/I_D)(g_{ds4}/I_D)}$$

The highest gain in matlab is 1760(V/V) in matlab. And the simulation gain is 460(V/V)

(3) Sizing the Compensate Capacitor:

The increase of the Cc will provide another track for s1_Vout to discharge. This will cause the increase of the tail current, which will increase the power. In addition, the position of the non-dominant pole will affect the phase margin. We know that the non-dominant pole is located at $w_{p2} = \frac{gm_2}{C_L}$, increase of the Cc will increase the CL, which lower the location of w_{p2}. This will make the phase margin be smaller since you pull the second pole lower than the unity gain bandwidth. In my experience, if I use a 1pF Cc, I will not be able to meet the specification. However, apply a 50fF can easily meet the specification.

(4) Sizing the gm/id of the second stage:

I design my stage 1 amplifier first and get an output voltage bias at 1.21V. The design flow is to make the slew rate enough and make sure the input voltage is bias at 1.21V.
The gain of the second stage class AB common source amplifier is as follows:

$$A_V \approx (g_{m1} + g_{m2})(r_{o1} /\!/ r_{o2})$$
$$= (g_{m1} + g_{m2}) \frac{\frac{1}{g_{ds1}} * \frac{1}{g_{ds2}}}{\frac{1}{g_{ds1}} + \frac{1}{g_{ds2}}}$$
$$= \frac{g_{m1}/I_D + g_{m2}/I_D}{g_{ds1}/I_D + g_{ds2}/I_D}$$

Since we need a phase margin of 45 degree, the wp2 is set to be at unity gain bandwidth. And the CL is provided. From the equation above, we can get the overall GM2:

$$GM2 = w_p * C_L$$
$$GM2 = gm_n + gm_p$$

gm_p/id controls the VGS of the PMOS, we need the VGS to be 0.59V so that the Vin is the same as stage 1 output. From this, we can sweep the gm_p and see if the output is matched.
gm_N/ID controls the current of the stage2 amplifier, we need a large current to increase the slew rate. I sweep the gm_n/ID and see if the slew rate meets the specification.

(5) Sizing the Length of the second stage:

Another design parameter is the length of the MOS. The larger the length, the larger the parasitic capacitor, which will decrease the charging speed. I applied the minimum length to minimize the parasitic capacitor.

(6) Design Issues and Tradeoffs:

Design Issues:

(a) The output voltage of first stage and the input voltage of the second stage must be matched.
(b) The location of the second pole must be larger than the unity frequency.
(c) The gain of the loop gain must be large enough to secure the static error.
(d) The 3dB bandwidth of the loop gain must be large enough to keep the dynamic error in spec.

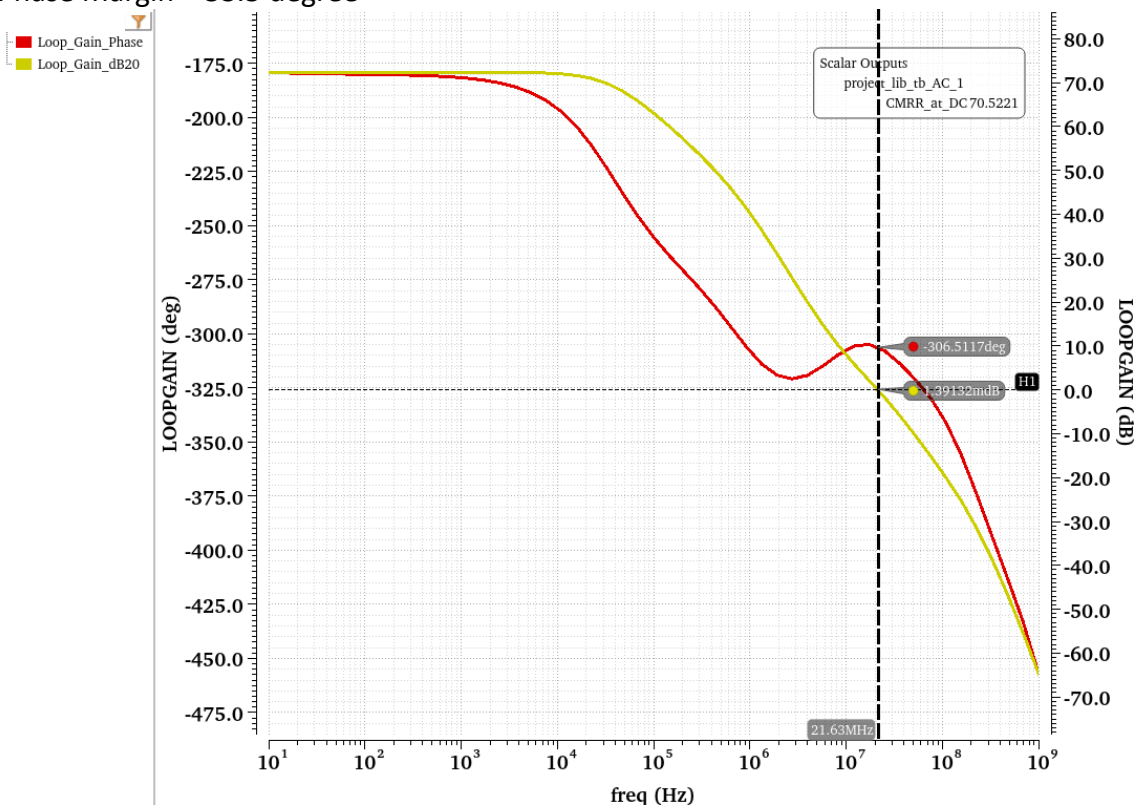
Tradeoffs:

(a) The slew rate of second stage is a tradeoff with the power. A larger slew rate requires a larger power.
(b) The size of the compensate capacitor is a tradeoff with the first stage tail current. A larger compensate capacitor requires a larger tail current.

(7) Bode plots of the loop gain:

Unity gain bandwidth = 21.63MHz

Phase Margin = 53.5 degree

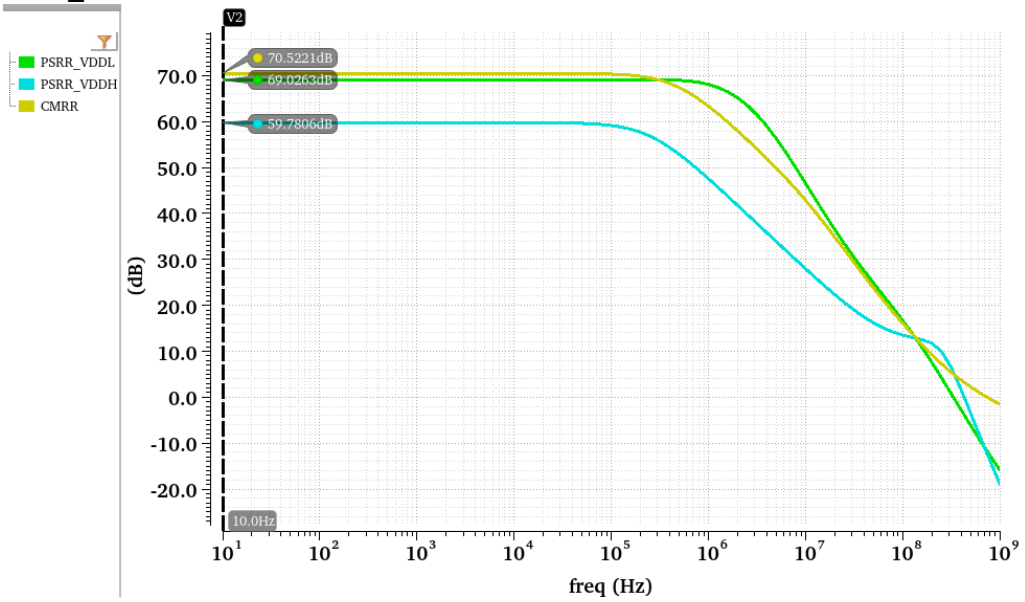


(8) CMRR and PSRR vs frequency:

CMRR at DC = 70.52dB

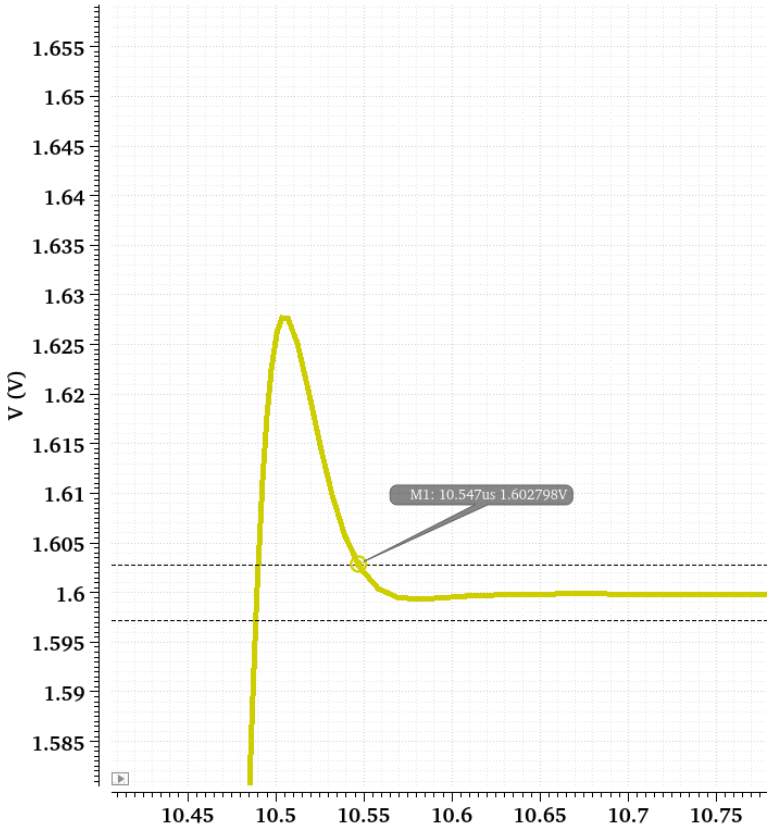
PSRR_VDDL = 69.04dB

PSRR_VDDH = 59.78dB



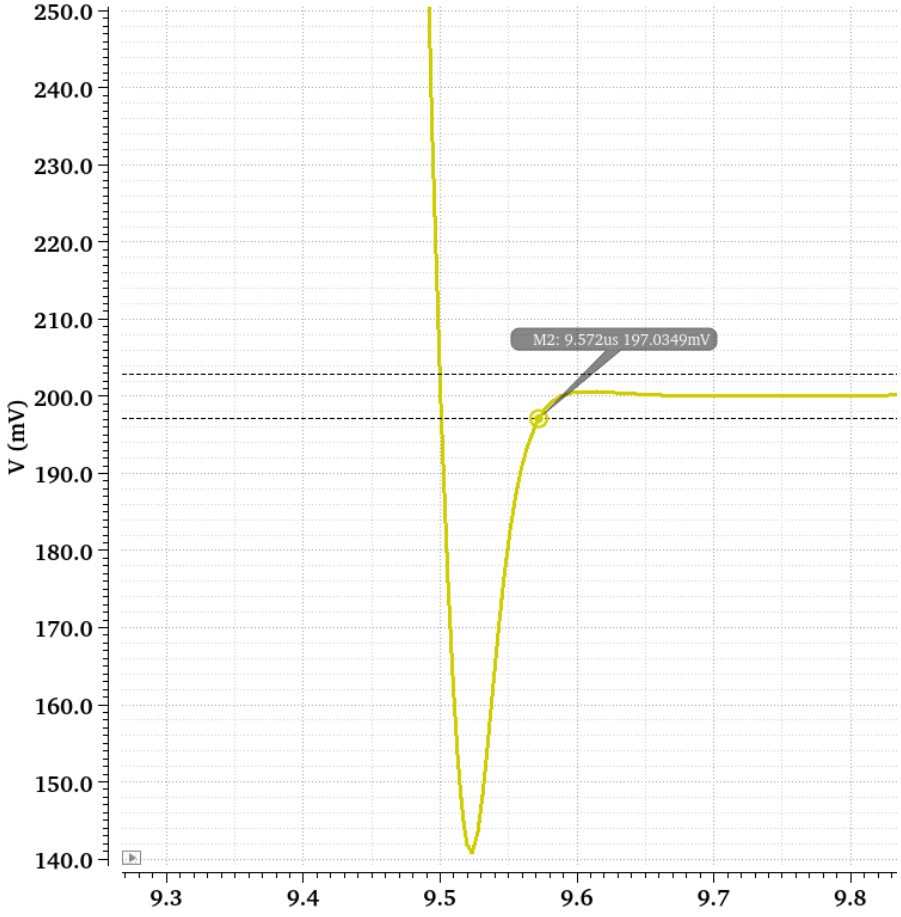
(9) Vout_Load (1.4V rising):

Settling time = 10.547 u – 10.4u = 147ns



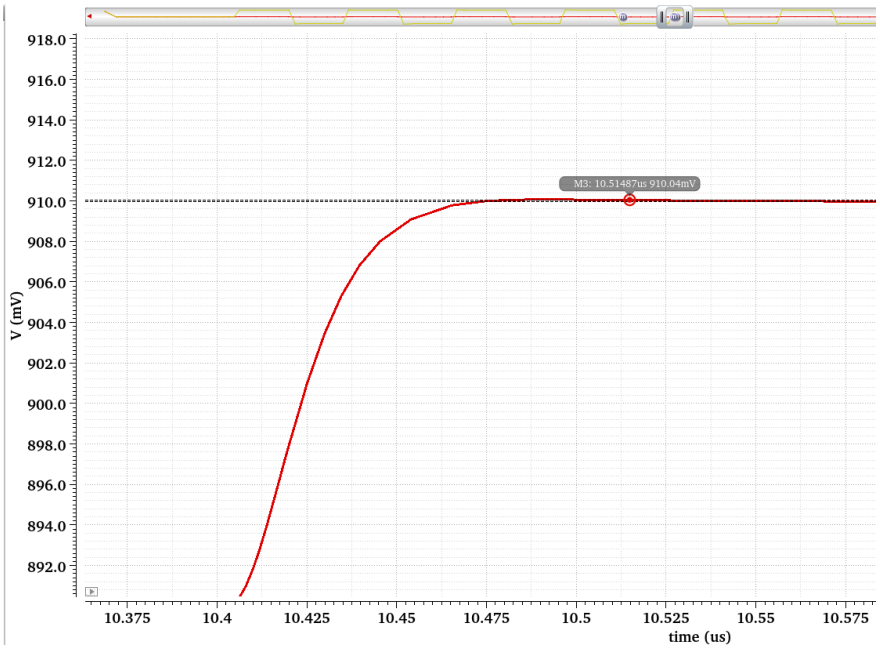
(10) Vout_Load (1.4V falling):

Settling time = 9.572u – 9.4u = 172ns



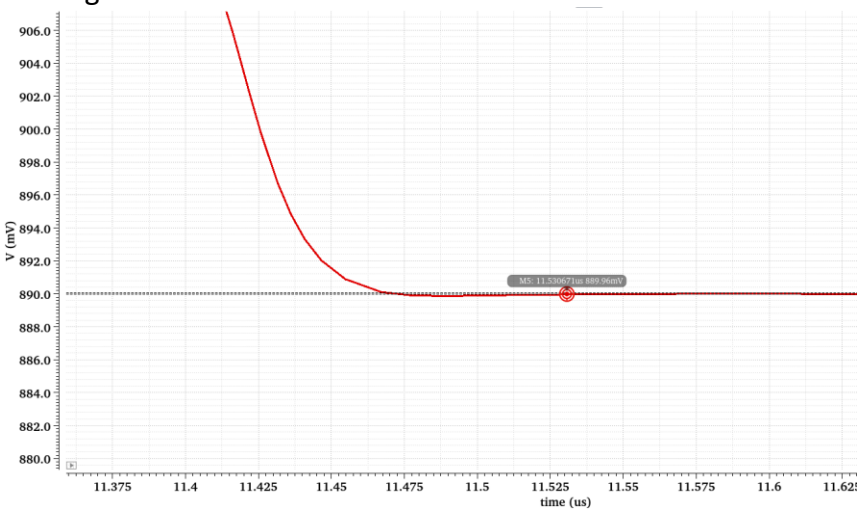
(11) Vout_Load (20mV rising):

Settling time = 10.515u – 10.4u = 115ns



(12) Vout_Load (20mV falling):

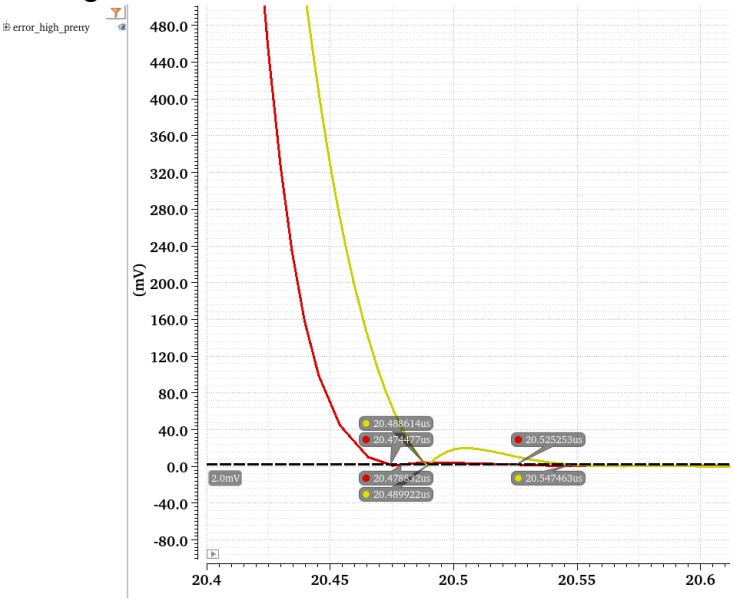
Settling time = 11.53u – 11.4u = 113ns



(13) Settling error (high to low):

Settling error = 0.2%

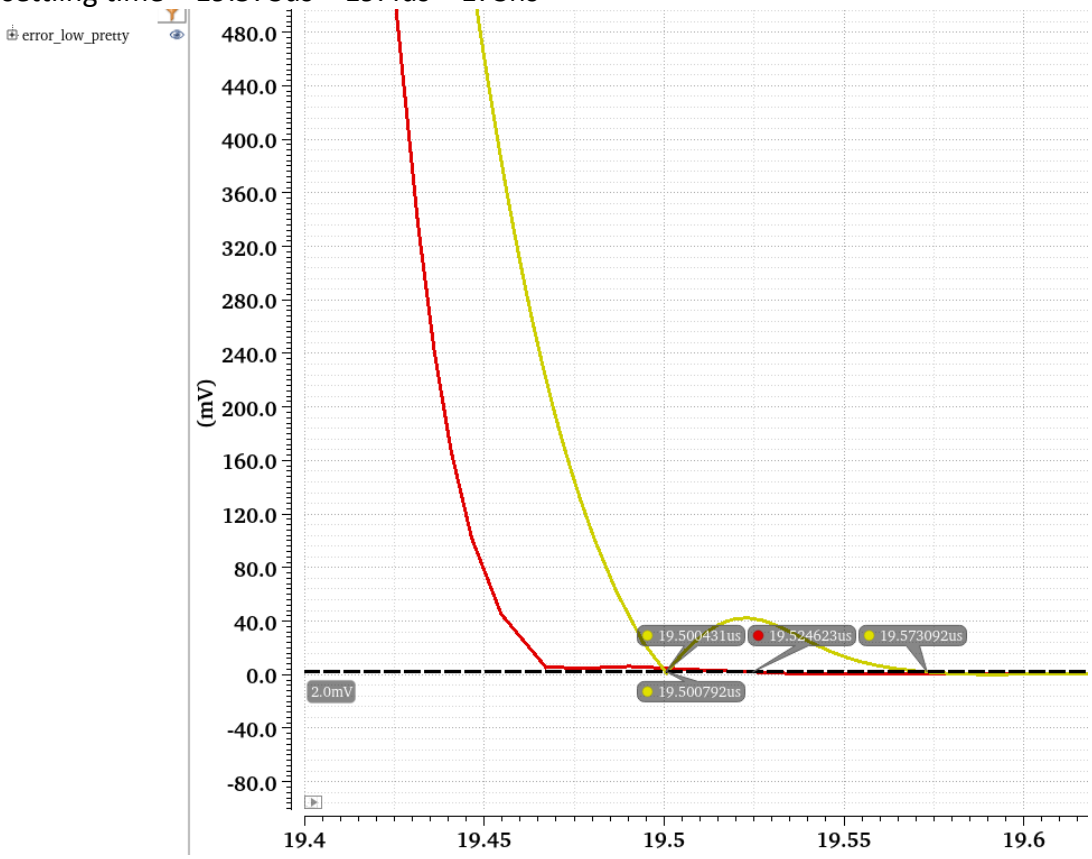
settling time = 20.547us – 20.4us = 147ns



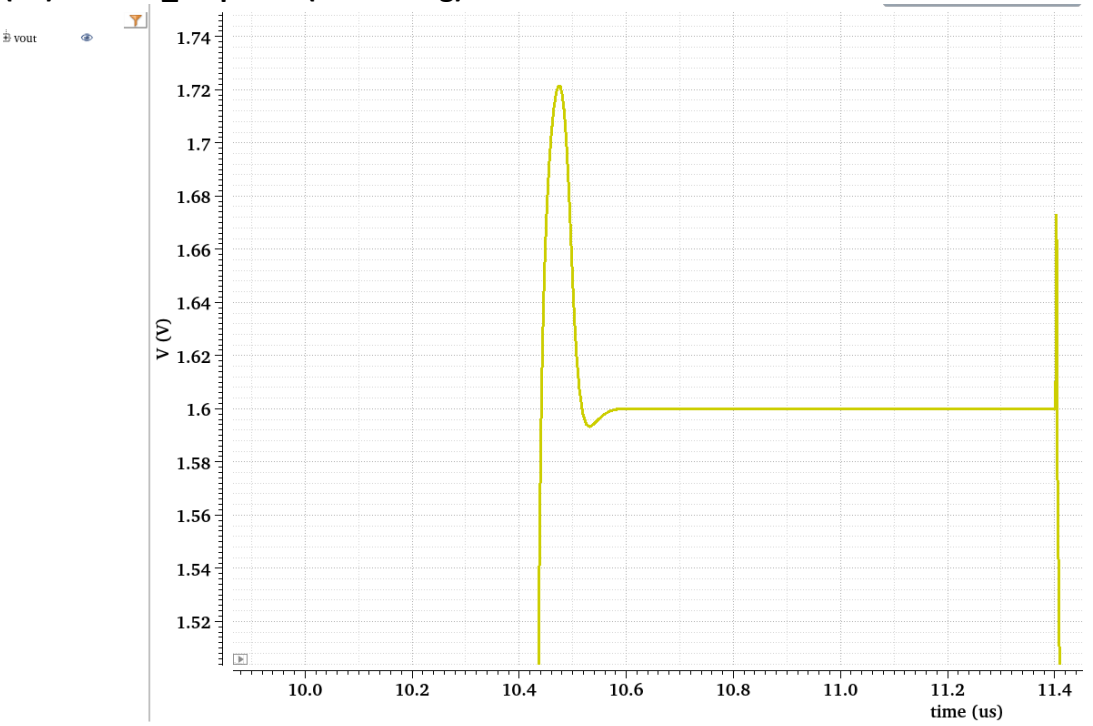
(14) Settling error (low to high):

Settling error = 0.2%

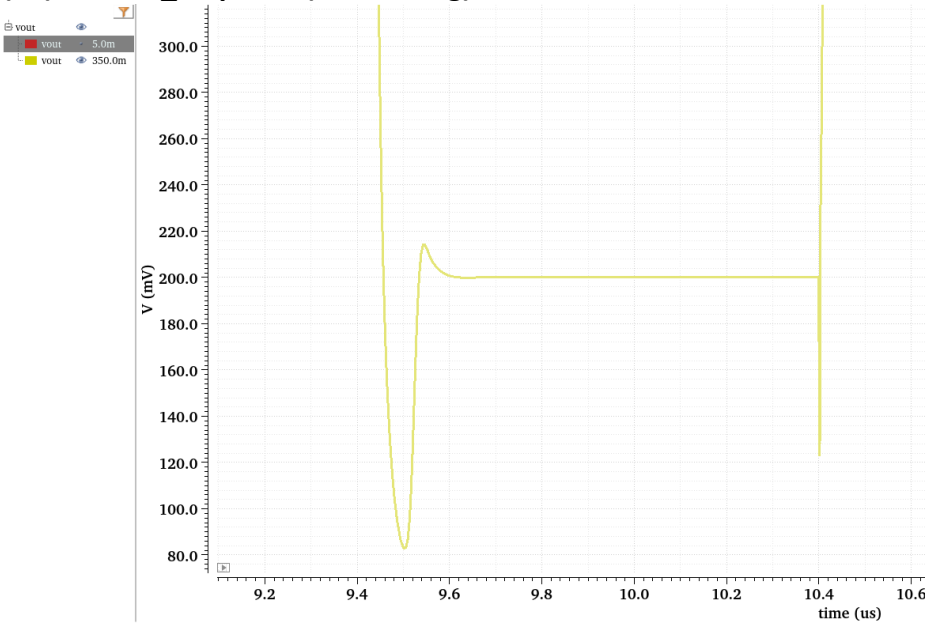
settling time = 19.573us – 19.4us = 173ns



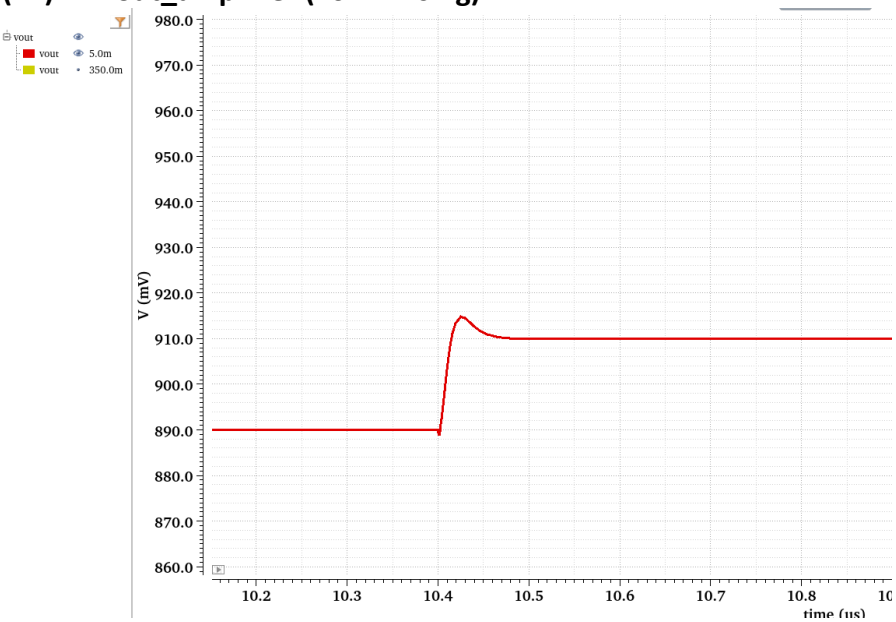
(15) Vout_amplifier (1.4V rising):



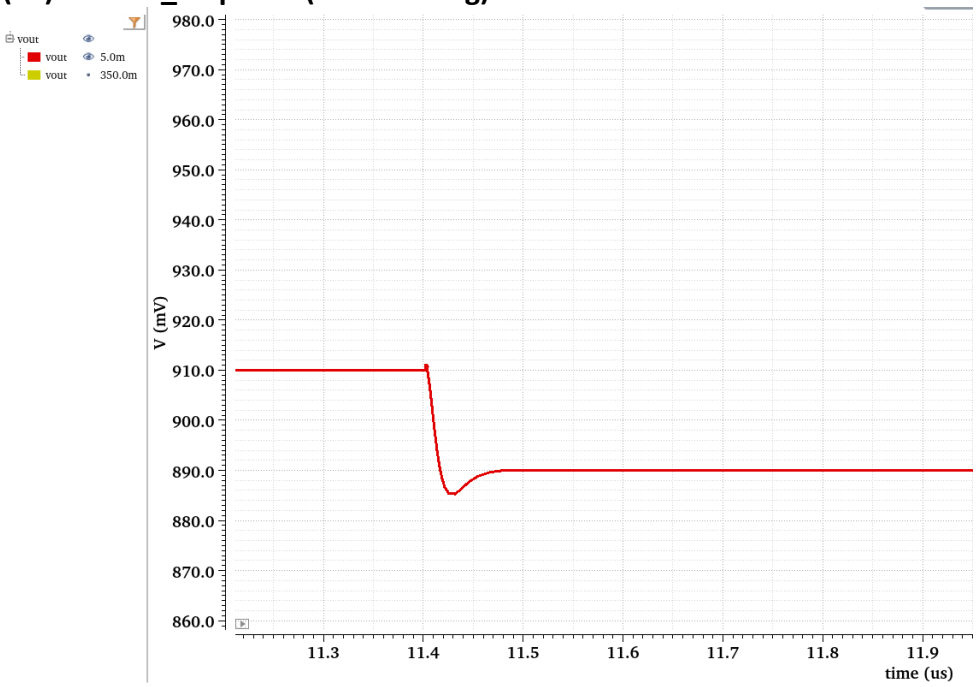
(16) Vout_amplifier (1.4V falling):



(17) Vout_amplifier (20mV rising):

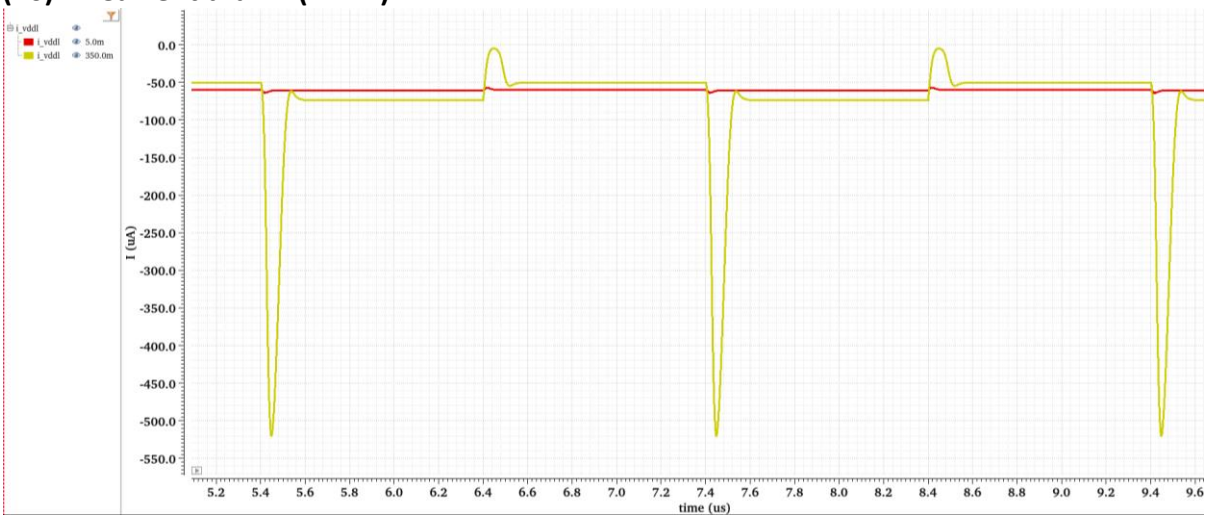


(18) Vout_amplifier (20mV falling):



(19) Current drawn (VDDH):

(20) Current drawn (VDDL):



(21) Test bench:

Name	Type	
vout	expr	vtime("tran "/out_int")
vout_load	expr	vtime("tran "/out_load")
vin	expr	vtime("tran "/in")
vin_n	expr	vtime("tran "/in_n")
reset	expr	vtime("tran "/reset")
i_vddl	expr	getData("/V1/PLUS" ?result "tran")
i_vddh	expr	getData("/V0/PLUS" ?result "tran")
avg_pow_vddl	expr	((VAR("vddl") * integ(i_vddl 2.4e-06 1.04e-05 nil)) / 8e-06)
avg_pow_vddh	expr	((VAR("vddh") * integ(i_vddh 2.4e-06 1.04e-05 nil)) / 8e-06)
settling_error	expr	((value(vout 2.2e-05) - vout) / value(vout 2.2e-05))
vout_high	expr	value(vout_load 2.14e-05)
vout_low	expr	value(vout_load 2.04e-05)
error_high	expr	(abs((vout_load - vout_high)) / (4 * VAR("vamp")))
error_low	expr	(abs((vout_load - vout_low)) / (4 * VAR("vamp")))
error_high_pretty	expr	clip(error_high 2.04e-05 2.14e-05)
error_low_pretty	expr	clip(error_low 1.94e-05 2.04e-05)

Name	Type	Details
CM_Gain	expr	vfreq("ac "/vcm_out")
DM_Gain	expr	vfreq("ac "/vdm_out")
CMRR	expr	dB20((DM_Gain / CM_Gain))
CMRR_at_DC	expr	value(CMRR 10)
VDDL_Gain	expr	vfreq("ac "/vps_out_vddl")
VDDH_Gain	expr	vfreq("ac "/vps_out_vddh")
PSRR_VDDL	expr	dB20((DM_Gain / VDDL_Gain))
PSRR_VDDH	expr	dB20((DM_Gain / VDDH_Gain))
Loop_Gain_Phase	expr	phaseDegUnwrapped(getData("loopGain" ?result "stb"))
Loop_Gain_dB20	expr	db(mag(getData("loopGain" ?result "stb")))

The test bench help calculate and plot all the SPEC value.

I add two parameters, error_high_pretty and error_low_pretty, in test bench for plotting the error for high to low and low to high. The x axis is the time and the y axis is the error.

(22) SPEC Table:

	Project SPEC	Designed Value
Settling Time	180ns	173ns
Power Consumption	<=1.1mW	482.41uW
Total Capacitance	4pF	50fF
Total Resistance	100M Ohm	100M Ohm
CMRR at DC	>= 65dB	70.5221 dB
PSRR at DC	>= 50dB	59.78 dB
Phase Margin	>=45 degree	53.5 degree
FoM	$\frac{10^{-9}}{T_{settle} * P_{total}}$	11.98

V. Conclusion

This project's goal is to design a two-stage amplifier. The first stage amplifier aims to provide a large gain, and the second stage contributes to the output slew rate. The settling time specification decide the 3db bandwidth, which decide the location of the first pole. With the compensate capacitor, we can design the location of the second pole to get a reasonable phase margin. I've learned a lot from this final project. By implementing the circuit and designing the position of the poles, I can fully understand the lecture material.