Project: Liquid-Crystal Display Driver

EE140/240A – Linear Integrated Circuits

Spring 2024

1. Project Introduction

A liquid-crystal display (LCD) is a common display technology used in flat panel displays, TVs, computers and mobile devices. LCD screens use the light-modulating properties of liquid crystals, which do not emit light directly; they require external light (backlight) to produce a visible image. Voltage applied across an LCD pixel polarizes the light and determines the amount of light that passes through the pixel. LCDs can require high voltages to fully polarize and maximize contrast. A description of how LCD displays work can be found at LCD Displays

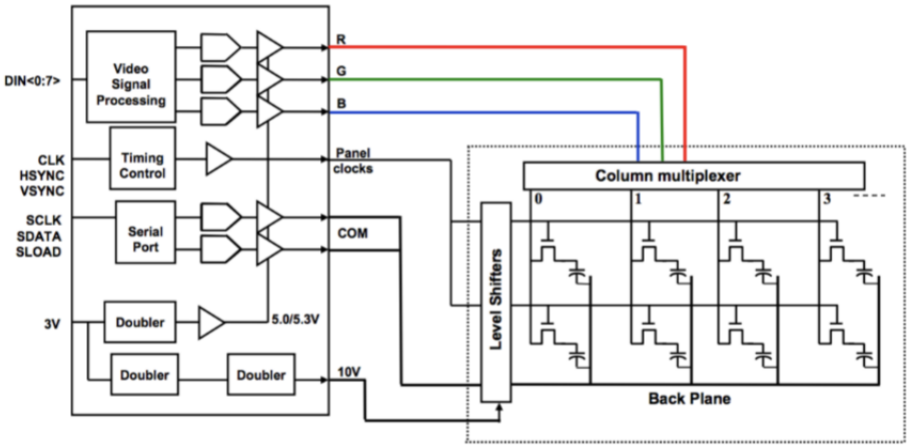

Figure 1: Example LCD driver

LCD pixels are often organized in an active matrix as shown in Figure 1. Each composite LCD pixel is comprised of a red, a green and a blue pixel, each driven by an individual amplifier. These amplifiers scan across all pixels in the array, updating the voltage stored on the pixel capacitance, thus updating the image. This rapid scanning requires the amplifier to set an accurate pixel voltage within a short period of time. LCD displays commonly operate at a refresh rate of 60 Hz. In this project, you will be designing a driver for a 38-mm smartwatch display, which has 272 x 340 pixels. Your driver must drive all pixels sequentially in the display in one period of the refresh rate. Image processing is computed in the digital domain and a display driver includes Digital to Analog converters. Therefore, the amplifier takes it's input from an ideal 0.7V fullscale 10-bit digital to analog converter (DAC). The most difficult transition that the amplifier must make is a full swing of 1.4V, creating a dark to light transition. Each pixel in an LCD display has a capacitance from 10s to 100s of pF. The interconnect and transistors in the array add a large series resistance on the order of hundreds of ohms. In our model, we will use a series resistance of 400 Ohms and a capacitance of 60 pF as shown in Figure 2. You will be designing the amplifier depicted below to the specifications in Table 1.

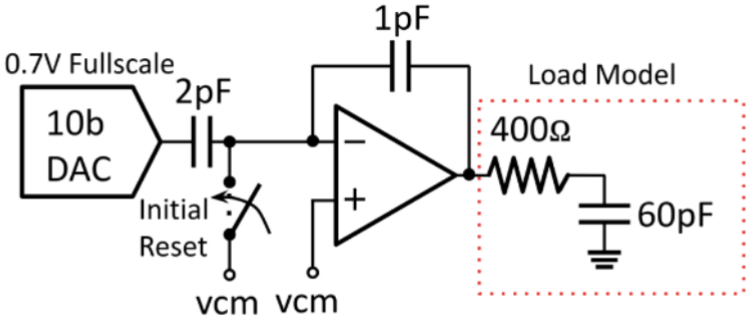

Figure 2: LCD driver amplifier with pixel load model. The output is at the pixel capacitor terminal after the series resistance.

Technology	gpdk045
Power Supplies	VSS (0V), VDDL ($\leq$ 1.1V), VDDH ($\leq$ 1.8V)
Closed Loop DC Gain	2
Load	400 Ω, 60 pF (output at capacitor)
Settling Time $T_{settle} = max\{T_{\text{settle, rise}}, T_{\text{settle, fall}}\}$	180.22 ns
Total Error	$\leq 0.2\%$
Power Consumption	$P_{total} \leq$ 1.1 mW
Output Voltage Swing	$\geq$ 1.4 V
Maximum Current Mirror Ratio	20
Maximum total capacitance	2 pF
Maximum total resistance	10 MΩ
CMRR at DC	$\geq$ 65 dB
PSRR at DC	$\geq$ 50 dB
Phase Margin	$\geq 45^o$

Table 1: Design Specifications

There will be a figure of merit (FOM) we would like you to maximize, which will be dependent on the settling time and the power consumption. Settling time is defined as the maximum of the rising and falling settling times for a 1.4V output step.

$$FOM = \frac{10^{-9}}{T_{\text{settle}} \times P_{\text{total}}}$$

2. Instructions

1. You are to work on this design project individually. Although you can discuss generalities with other students in the class, you are not to perform the design in teams or groups. The chances of any two people coming up with the same exact design are very slim. Therefore, we expect to see different designs from each one of you. However, you are encouraged to talk with one another and discuss generalities.

2. You should use the gpdk045 process provided in this class. You may use any device provided in the library. All components (including any resistors or capacitors you add to the design) should be from gpdk045. You can use mimcap for a passive capacitor with voltage-independent capacitance, and the cells starting with "res" can be used for passive resistors. Do not use ideal components from analogLib in designing your amplifier. (You don't need to change the ideal capacitors and resistors given to you in the testbenches.)

3. You must keep the VGS and VDS of all devices lower than the limits of their device types (1.1V for the 1v devices and 1.8V for the 2v devices). Additionally, the power supply voltages should not exceed the corresponding operating range of the devices (for example, you can't place a 1V device between 1.8V and GND, even if its VGS and VDS are both smaller than 1.1V).

4. **Use only nmos2v transistors as your input devices**. Any other device choice results in gate leakage currents that add errors to the output voltage in your transient simulation.

5. You can use any amplifier topology, and any transistor lengths and widths that you choose. Wide devices should be implemented using multiple fingers, with a finger width ≤ 5 μm.

6. You may use exactly 1 ideal current source in your design, with 1 terminal tied to either VDDL, VDDH or GND. You cannot use ideal voltage sources, except the 2 ideal voltage sources VDDL and VDDH which are connected in the provided testbenches. These ideal voltage sources cannot exceed 1.1V and 1.8V as power supplies. You may choose to only use one of these ideal voltage sources (such as VDDH). If you use 2 voltage supplies, you have to make sure the PSRRs corresponding to both supplies meet the specification. Your voltage sources are to be used as only the power supplies, not for any other purpose.

3. Testbenches

You will receive 2 testbench examples, which set up simulations that may be helpful for verifying specifications. You are also certainly not limited to these testbenches, and may find it helpful to generate your own. However, do note that your final specifications may be checked with these setups. You can copy these testbenches into your cadence directory using the following command:

cp -r /home/ff/ee140/fa23/project_lib ~/cadence

To make this library show up in cadence, from the CIW window (the main cadence window), click Tools and then Library Path Editor and type the "library name" as exactly "project_lib" into one of the blank boxes in the first column and the library path (e.g., "/home-/cc/ee140/sp24/class/YOUR_ID/YOUR_CADENCE_PATH").

This will cause a library called "project_lib" to appear in your library manager containing two testbenches

- **Transient testbench (tb_transient)**: This will include the resetting required to set the common mode for your capacitive feedback amplifier. This testbench is useful in verifying the settling error and output swing specs, and computing your power consumption. This testbench is set up to measure your specs for a full-scale (0.7V input, 1.4V output) transition as well as a 10mV input (20 mV output) transition to make sure your amplifier works well for smaller input steps. The settling time spec is defined at the capacitor terminal, after the series resistance, however you should also check the output voltage of the amplifier and show both waveforms in your report.
- **AC testbench (tb_ac)**: This testbench is useful for verifying the stability, common mode rejection, and power supply rejection specifications. Note that while the simulations are set up, they will not contain simple "pass/fail" checks - you will be required to appropriately interpret the output results to confirm that you have met the specifications.

To comply with the testbench, your amplifier must have 6 pins. A cellview containing an empty schematic with these pins, and a symbol for the amplifier, will be provided. You can build your final amplifier in this schematic:

- Vinn - negative input to your amplifier
- Vinp - positive input to your amplifier
- Vout - amplifier's single ended output
- GND - your amplifier's ground
- VDDH - input for the high voltage supply, the nominal value is 1.8V but you can change this supply voltage to a value between 0V and 1.8V
- VDDL - input for the low voltage supply, the nominal value is 1.1V you can change this supply voltage to a value between 0V and 1.1V.

4. Design Approach

Your design approach should be outlined in your final report on this project. It is recommended that you use the following approach:

1. Perform MATLAB/Python simulation and/or hand calculations to determine the target amplifier specs (DC gain, bandwidth, phase margin, pole locations, slewing, etc.)
2. Choose an appropriate circuit topology based on the above specifications.
3. Use g_m/I_D methodology and LUTs from Lab 3 to size and design the amplifier.
4. Confirm the operation of your circuit using CADENCE simulation
5. Iterate on the steps above, until all design specifications are met.
6. Write your report. You must show simulation results for all listed specifications, preferably exported to MATLAB/Python, but screen captures from CADENCE may also be acceptable if they are **legible and labeled with a white background**. Settling time must be shown for rising and falling 1.4V and 20mV output steps.

5. Final Report

Your final report will be due by 11:59pm on Sunday, May 5th uploaded to Gradescope. It should be concise and complete. The report should be typed, and divided into the following sections (with page limits strictly observed using 12pt font, 1" margin sizes and reasonably-sized figures):

- **Overview (1-2 pages)**: Complete schematic and basic description of circuit operation (including biasing), followed by the comparison table between the design specifications and your design. Your schematic should include legible device types (nmos/pmos, 1V//2V) and sizes for transistors, and resistances/capacitances for the passives next to each transistor. This section should not contain design discussion.
- **Design (1-3 pages)**: A brief discussion of your design approach, particularly how you mapped the provided specifications to amplifier level specifications. Note that you should provide some basic and important equations used in your design, and the high-level methodology you used to choose your transistor sizes.
- **Transistor and Bias Summary (1 page)**: A table listing for each transistor, the dimensions, drain bias current ($|I_D|$), the magnitude of the gate-to-source voltage ($|V_{GS}|$), the transconductance (g_m), and the output conductance (g_{ds}).
- **Discussion ($\leq$ 10 pages including figures)**: A discussion of circuit performance with special attention paid to unique areas in your design which helped/hurt your attempts to meet the specifications. This is the most important section, in that it provides the validation for your design. The following simulatinos for verifying each of the perforamnce specifications should be included here:

  - AC: (1) Bode plots of loop gain with markers showing mid-band gain and phase margin. (2) CMRR and PSRR vs. frequency
  - Transient: (1) Waveform of the voltage **at the load capacitor** with legible markers for the settling time of the rising and falling 1.4V and 20mV output steps. (2) Settling error for rising and falling 1.4V and 20mV output steps at **at the load capacitor** with legible markers. (3) Waveform of the votlage **at amplifier output** for the rising and falling 1.4V and 20mV output steps (you don't need to report settling time for amplifier output). (4) Waveform of the currents drawn from VDDH and VDDL.

  Include a diagram of the testbench you used, the justification for its use, and the simulation results or output data showing that it has met the needed specifications. Your final results should be summarized in a table together with the target specifications. In addition, report the total area of your amplifier. Your calculation must include the area of the transistors (W*L) and any resistors or capacitors that you add to your design. You don't have to include the area of the feedback capacitors or the load resistor and capacitor that are already provided for you in the testbenches.
- **Conclusion (1 page)**: A summary of your design experience. You should summarize the overall op amp characteristics, and should describe your overall experience and what you learned in doing this design. It would be good to get some feedback from you, both good and bad. Tell us if the design problem was worth the effort. (Your comments here will not adversely affect your grade.)
- **Scripts, Code, etc. (no limit)**: Please paste all the scripts that you used in your design here. There is no page limit here as you might have many pages of scripts and plots. You should not need to describe how the code works (since that should be in the Design section of the report).

You should try your best to achieve the design specifications. If after all attempts you fail to meet all the design specifications, describe your optimum and final design and describe in your report what you consider to have been the most restrictive and problematic spec to meet. Also discuss how that particular spec could be improved, i.e., discuss tradeoffs between various parameters. If you fail to meet the specifications, your report should indicate the techniques that you tried.

6. Project Check-In Requirements

By **April 16, 2024** you need to have completed a check-in to confirm by this time that your testbenches simulate correctly with a preliminary transistor-level design. This design can but is not required to meet specifications at this stage but this will be a check that (1) you are performing your simulations correctly and have a transistor-level design started, and (2) you have some hand (or MATLAB, Python, etc.) analysis that motivates your design.

7. Evaluation

This project is graded out of 100 points. The grading scheme below will be used to grade the design project reports. Note that you should make sure that all components that were mentioned above are included in your report even if they are not specifically mentioned in the table below. Write the best report you can.

- **Check-In (10 points):** Show (1) Your testbench simulations in transient and ac, (2) that you understand the system-specifications and how that translates to your design, and (3) your hand/coding analysis, which should be related to your testbench simulations.
- **Design Methodology (35 points):** Describing how you took the system level specifications and translated this into your design methodology. You can use the methodology you learned in Lab 3, but you can opt for your own as well. Your design/matlab/python analysis will be graded for accuracy and completeness. Sweeping every value in Cadence is not a valid methodology, but it is alright to sweep a few variables for optimization purposes.
- **FOM Achievement and Optimization (40 points):** Achieving the bare minimum specifications will grant you the bulk of these points. For a naive 2-stage operational amplifier that reaches the specifications exactly, the FOM is around 5. Achieving the specifications is far more important that the maximization of this number. However, achieving the bare minimum FOM will not receive full credit for the FOM Optimization scoring. You will need to make an effort to minimize the other specifications (like CMRR and PSRR, phase margin, etc.) while maximizing the FOM (power and settling time). There should be effort in achieving a high FOM while minimizing the other specifications. No matter the FOM you achieve, you should describe the design issues and tradeoffs that limit you from achieving a higher FOM.
- **Report Style and Formatting (15 points):** This includes having all sections in your typed report, including plots with title and labeled axes, markers on the plot that specify important points, obeying the page limits in each section.