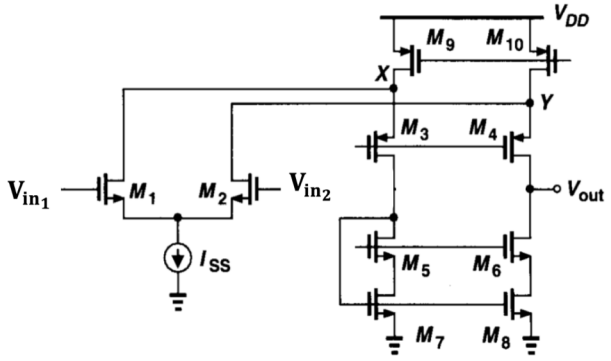
***Problem 3*: Folded Cascode Amplifier**
In this problem, you may neglect body effect.

Consider the folded cascode differential amplifier below. Assume $I_9 = I_{10} = I_{SS}$, and all transistor pairs (M_1 and M_2, M_3 and M_4, M_5 and M_6, M_7 and M_8, M_9 and M_{10}, M_{1p} and M_{2p}) are matched. Assume $V_{DD} = 1.8V, |V_{th}| = 0.4V, V_{ov} = (V^*) = 0.1V$ for all transistors, $\lambda_p = \lambda_n \neq 0$ and $g_m r_o \gg 1$. Express your answers in terms of g_m and r_o if needed, where $g_m = \frac{I_{ss}}{V^*}$ *and* $r_o = \frac{1}{\lambda \frac{I_{ss}}{2}}$. The current source I_{SS} is an ideal current source but needs a minimum voltage of $V_{ov} = 0.1V$ to operate.



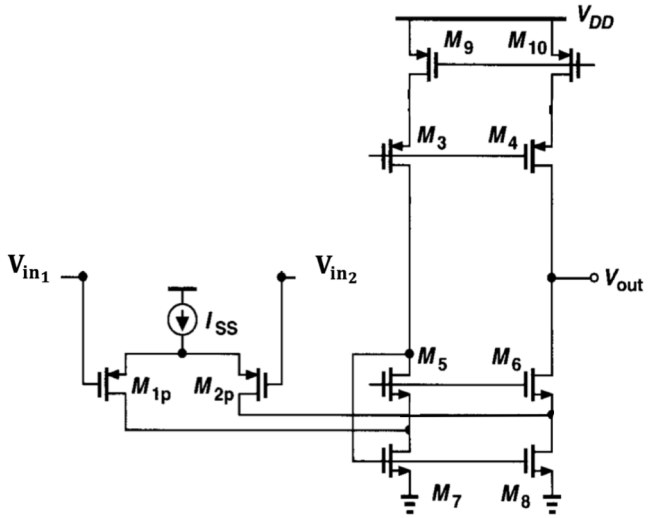
a) (3 points) Find the differential gain of this circuit. Express your answer in terms of small signal parameters.

$$A_{v_{diff}} =$$

c) (2 points) What are the highest and lowest allowed common-mode input level of this amplifier? You can assume you can set the bias voltages of the gates of M_{3-6} to any allowed desired value.

$V_{i_{CM_{High}}} =$ $V_{i_{CM_{Low}}} =$

d) (2 points) For the modified amplifier below, what are the highest and lowest allowed common-mode input level? You can assume you can set the bias voltages of the gates of M_{3-6} to any allowed desired value.



$V_{i_{CM_{High}}} =$ $V_{i_{CM_{Low}}} =$

Problem 1 - Stability Compensation [14 pts]

For this problem, all the transistors shown in the figures are in the saturation region with the same g_m and r_o. You can assume that $g_m r_o \gg 1$, and you can ignore all the other parasitic capacitors that are not specified or shown in the figures.

Below is the diagram of a simple 2-stage amplifier designed for a unity-gain voltage amplifier that drives a load capacitor C_L. V_B is a DC voltage . C_C is the compensation capacitor, and we have $C_C > C_L$.

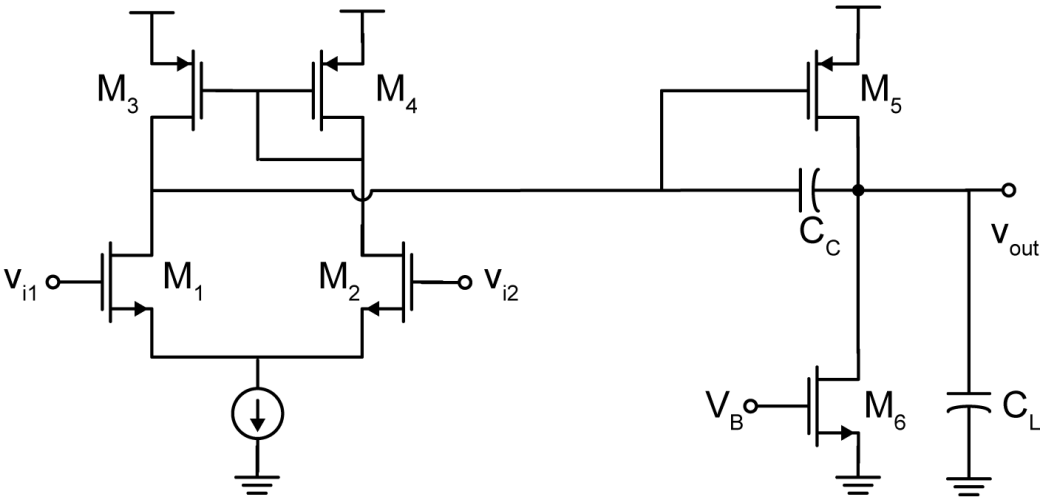


Figure 1: Diagram of the 2-Stage Amplifier

(a) (2 pts) The connection of this unity-gain voltage amplifier is not complete yet. Circle around the correct answer to finalize the connection.

Connect v_{out} to:	v_{i1}	v_{i2}

(b) (4 pts) Draw the bode plot of the loop gain $LG(s)$ of the circuit shown in Figure 2. Clearly label and specify the DC loop gain, the poles and zeros using g_m, r_o, C_C and C_L.

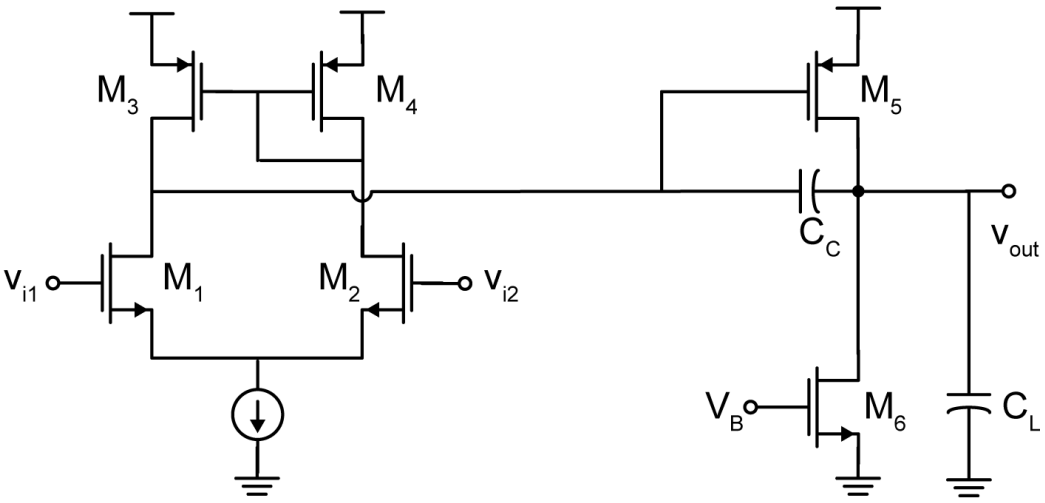


Figure 2: Diagram of the 2-Stage Amplifier

(Additional space for Problem 1 part b)

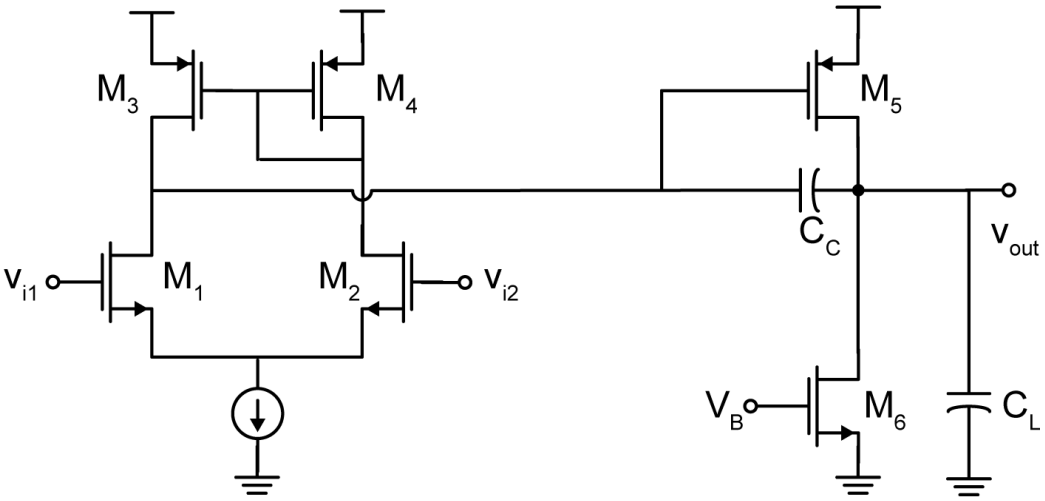


Figure 3: Diagram of the 2-Stage Amplifier

(c) (2 pts) You decided to cancel out the zero in the original loop gain expression, so you placed a resistor as shown in figure 4. What is the resistance R_C to cancel the zero?

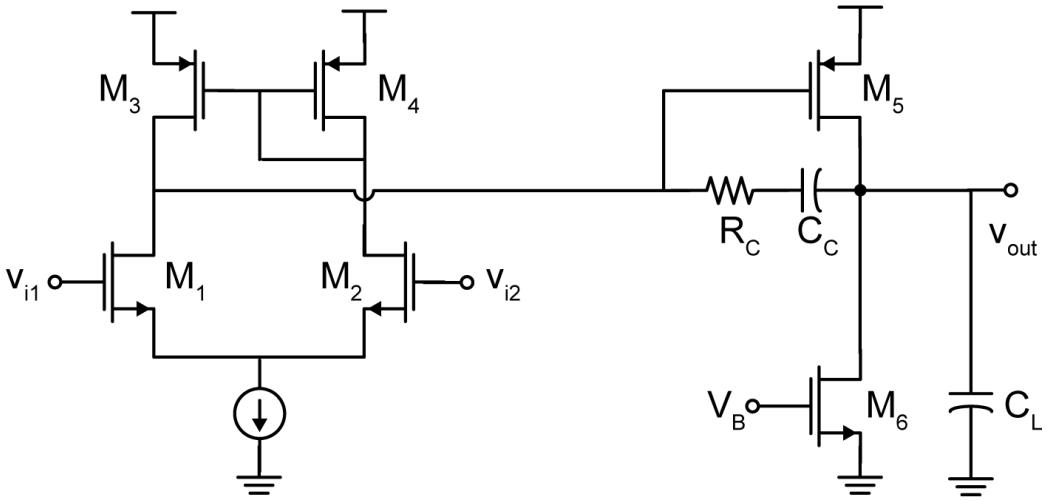


Figure 4: Diagram of the 2-Stage Amplifier with Additional Resistor

$R_C =$

(d) (2 pts) You decided to add a source follower to drive M_6 so your design has a class-AB output. The design parameters (transistor sizes, $I_D, g_m, r_o, R_C, C_C, C_L$) don't change compared to the design shown in Figure 4. The g_m and r_o of M_7 are both the same as those of other transistors. What is the DC loop gain now?

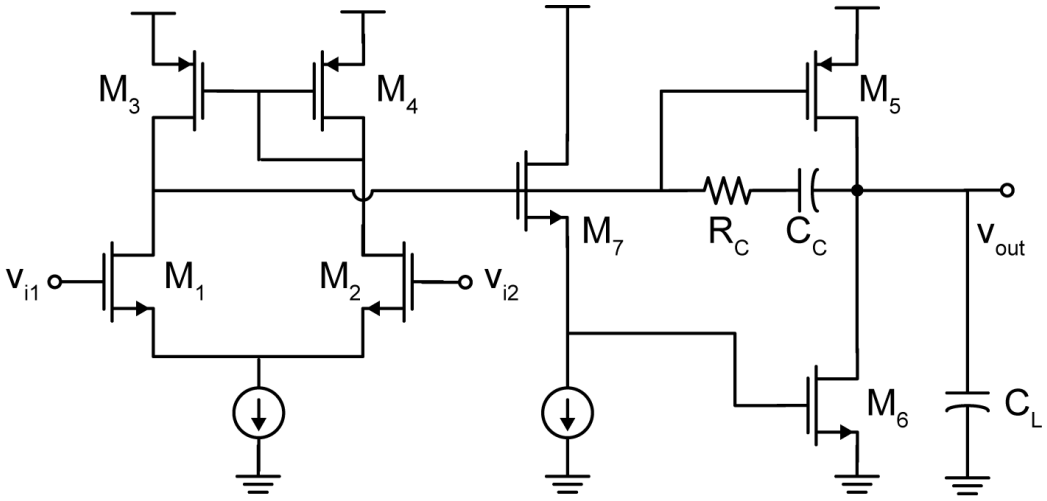


Figure 5: Diagram of the 2-Stage Amplifier with Class-AB Output

$LG_0 =$

(e) (4 pts) Draw the bode plot of your loop gain $LG(s)$ with class-AB output. Clearly label and specify the DC loop gain, the poles and zeros using g_m, r_o, R_C, C_C and C_L

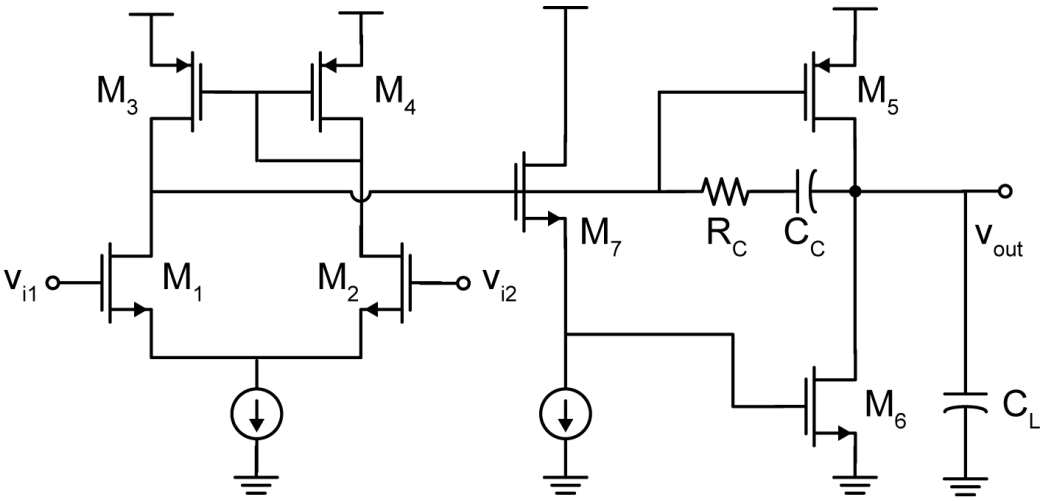
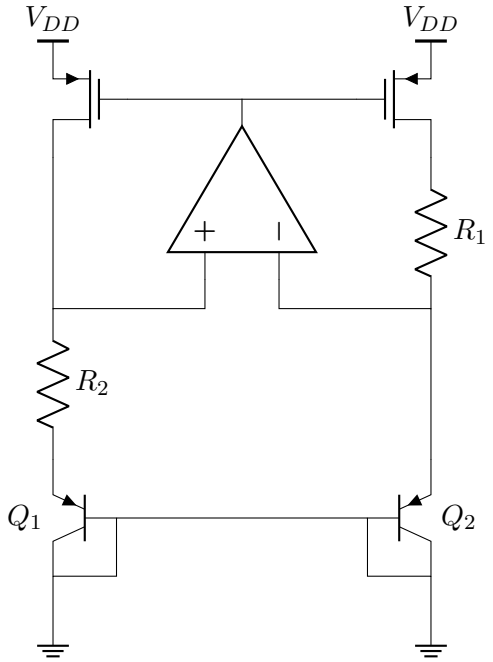


Figure 6: Diagram of the 2-Stage Amplifier with Class-AB Output

3 Bandgap References

Consider the bandgap circuit shown below, which uses PNP BJTs available in a CMOS process.



Don't worry about the BJTs, just treat them as diodes as was done in class.

The emitter area of Q_1 is N times larger than that of Q_2, and the dimensions of the PMOS devices are equal. Assume that the amplifier is ideal and the base current of the BJTs is zero.

(a) (2 points) What is the ratio of the currents through the right and left branches of the circuit I_{Q1}/I_{Q2}?

$\frac{I_{Q1}}{I_{Q2}} =$

(b) (2 points) This circuit generates a PTAT current. Find an expression for the current flowing through R_1.

$I_{R1} =$

(c) (3 points) With a correct choice of R_1 and R_2, this circuit can also generate a temperature independent bandgap voltage at one of its nodes. Identify and mark this node on the schematic on the previous page. Then write an expression for V_{bg}.

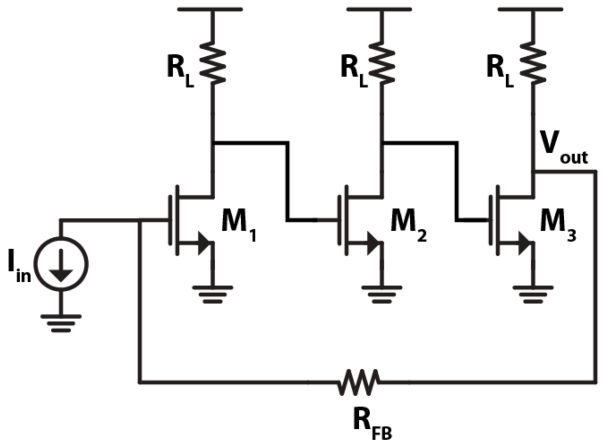
$V_{bg} =$

(d) (2 points) Now, determine the ratio of R_1/R_2 such that the node identified in part (c) becomes a bandgap reference voltage.

$\frac{R_1}{R_2} =$

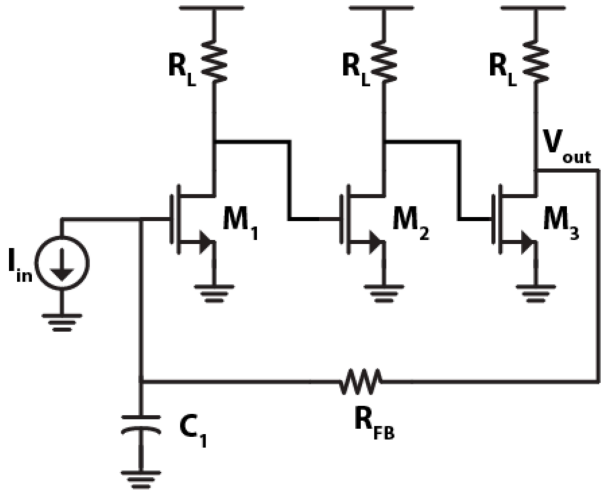
Problem 5 (13 pts; 15pts)

Three identical common source stages (M_1, M_2 and M_3 are identical) are cascaded as shown below. You may write your answers for all parts in terms of gm, C_{gs}, R_L, R_{FB}. You should assume that $R_{FB} \gg R_L$ and $ro = \infty$ to simply your calculations.



a) (2pts) Compute the DC loop gain of the above circuit.

$Loop\ Gain =$



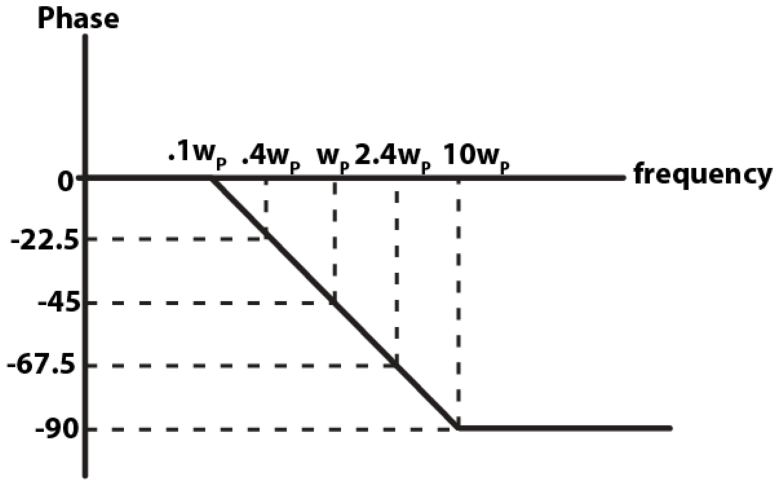
b) (3pts) Assume you compensate with a capacitor C_1. Write the location of each of the 3 **open-loop** poles. Consider only C_1 and C_{GS} of each device.

$p_1 =$

$p_2 =$

$p_3 =$

c) (4pts) What is the value of C_1 to compensate the loop for 45 degrees phase margin? Consider only C_1 and C_{GS} of each device. *Hint: assume that the phase of a pole looks like the linear approximation below:*



$C_1 =$