

# EE140 Lab Report: Lab2

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Parameter	NMOS	PMOS
Model Level (in HSPICE)	3	3
$V_{TO}$ (V)	0.8	-0.8
$K_P$ ( $\mu\text{A}/\text{V}^2$ )	90	30
$\Gamma$ ( $\sqrt{\text{V}}$ )	0.8	0.4
$\Lambda(V^{-1})$	0.01	0.02

## Part A

Given the part-a scenario, we can construct circuits in Cadence. The first step is to construct cadence schematics, which is as figure2 shows. The left circuit is scenario 1 and the right circuit is scenario 2. From the circuit given in the part-a, we can also get the equivalent circuit and calculate gain to make comparison.

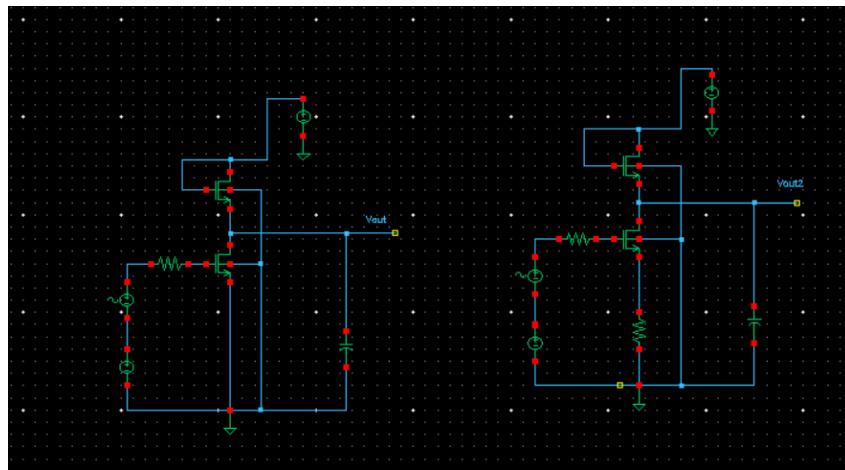
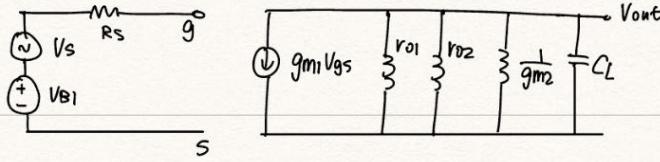


Figure 1: Schematics overview

### Schematic1 calculation and simulation

- Hand calculation of gain is as follows, from this calculation we know that in Scenario1 the gain is approximately 19.2986 dB.
- Hand calculation of bandwidth is also as follows, from this calculation we know that in Scenario1 the bandwidth is approximately 1.9MHz

Scenario 1:



$$\text{Gain: } \frac{V_{\text{out}}}{V_{\text{in}}} = G_m R_{\text{out}}, \quad G_m = g_m$$

$$\text{apply test Voltage source, } R_{\text{out}} = \frac{V_t}{I_t} = (r_{o1} \parallel r_{o2} \parallel \frac{1}{g_m2} \parallel Z_C)$$

$$\text{for } M_1 \& M_2: I_D = \frac{1}{2} \mu n C_{\text{ox}} \frac{W_1}{L_1} V_{\text{ds}}^2 = \frac{1}{2} \mu n C_{\text{ox}} \frac{W_2}{L_2} V_{\text{ds}}^2 = 4.05 \times 10^{-5} \text{ A}$$

$$V_{\text{out}1} = V_{\text{gs}1} - V_{\text{t}1} = 1.1 \text{ V} - 0.8 \text{ V} = 0.3 \text{ V}, \quad \frac{W_1}{L_1} \cdot V_{\text{out}1}^2 = \frac{W_2}{L_2} V_{\text{out}2}^2.$$

$$V_{\text{out}2} = \sqrt{\frac{\mu n (L_2)}{(L_1) (W_2)}} V_{\text{out}1} = \sqrt{90} V_{\text{out}1} \approx 2.846 \text{ V.}$$

$$g_{m1} = \mu n C_{\text{ox}} \frac{W_1}{L_1} \cdot V_{\text{out}1} = 90 \times 10^{-6} \text{ A/V}^2 \times \frac{50 \mu \text{m}}{5 \mu \text{m}} \times 0.3 \text{ V} = 2.7 \times 10^{-4} \text{ A/V}$$

$$g_{m2} = \mu n C_{\text{ox}} \frac{W_2}{L_2} V_{\text{out}2} = 90 \times 10^{-6} \text{ A/V}^2 \times \frac{10 \mu \text{m}}{90 \mu \text{m}} \times 2.846 \text{ V} = 2.846 \times 10^{-5} \text{ A/V}$$

$$r_{o1} = r_{o2} = \frac{1}{\lambda I_D} = \frac{1}{0.01 \times 4.05 \times 10^{-5}} \Omega = \frac{1}{4.05 \times 10^{-7}} \Omega.$$

$$\text{Set frequency} = 1 \text{ kHz. } \frac{1}{Z_C} = j\omega Q = j \cdot 2.5 \times 10^9 \Omega$$

$$R_{\text{out}} = \left| \frac{1}{\frac{1}{r_{o1}} + \frac{1}{r_{o2}} + g_{m2} + \frac{1}{Z_C}} \right| = \left| \frac{1}{2.927 \times 10^{-5} + j(2.5 \times 10^9)} \right| \approx 34164 \Omega.$$

$$V_{\text{out}}/V_{\text{in}} = G_m R_{\text{out}} = g_{m1} R_{\text{out}} = 2.7 \times 10^{-4} \times 34164 = 9.22428.$$

$$\rightarrow 20 \log \left( \frac{V_{\text{out}}}{V_{\text{in}}} \right) = 20 \log (9.22428) = 19.2986.$$

$$CL \quad \frac{1}{\frac{1}{r_{o1}} + \frac{1}{r_{o2}} + \frac{1}{Z_C}} \quad \tau_1 = R_{\text{out}} C_L = \left( r_{o1} \parallel r_{o2} \parallel \frac{1}{g_{m2}} \right) C_L$$

$$\approx \frac{1}{2.846 \times 10^{-5}} \times 2.5 \times 10^{-2}$$

$$= 8.784 \times 10^{-8}.$$

$$f_1 = \frac{1}{2\pi\tau_1} = 1.9 \text{ MHz.}$$

Figure 2: handout1

- Simulated Results of gain and bandwidth and output voltage swing in Schematic1 are as follow. Set up the circuit according to the schematic diagram, then construct the corresponding ac and trans simulation analysis, write the corresponding representation function, and then run the simulation.

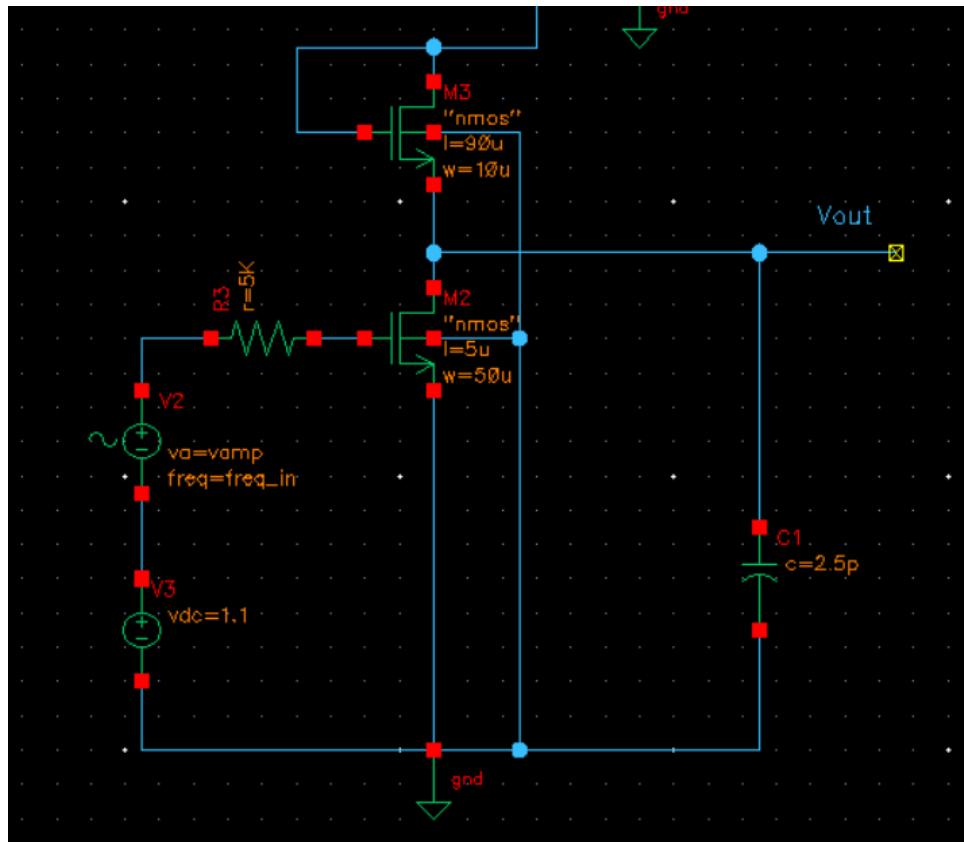


Figure 3: Schematic<sub>1</sub>

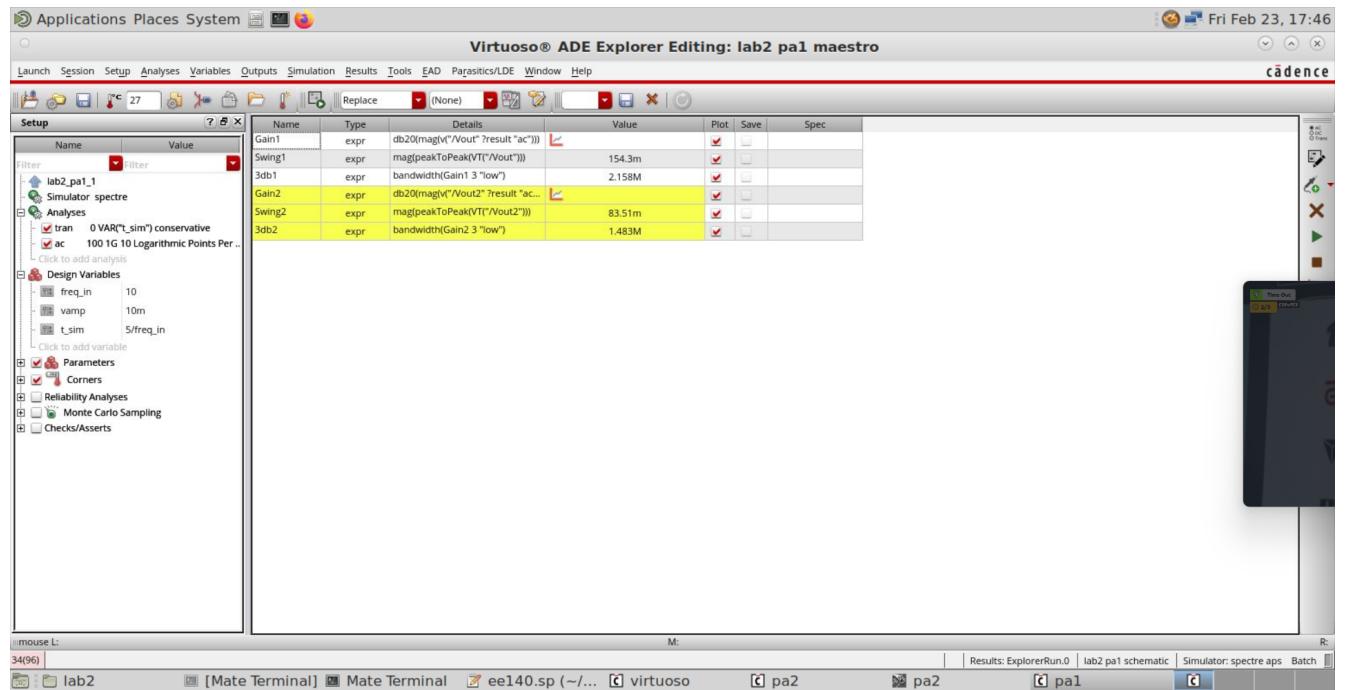


Figure 4: Simulation result

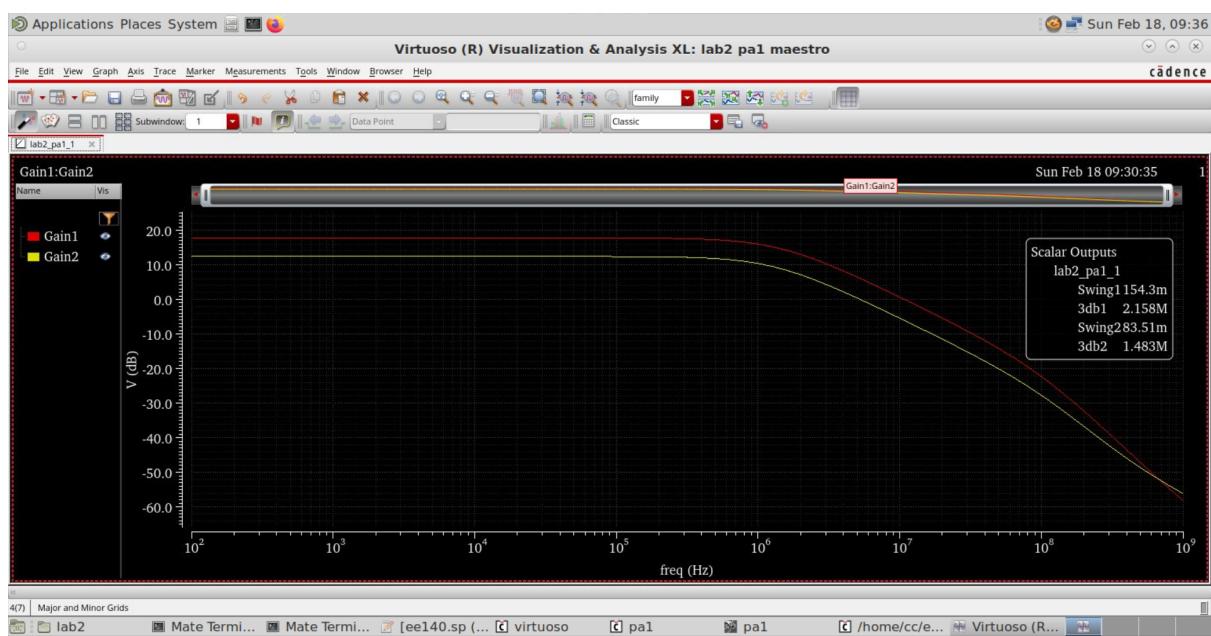


Figure 5: Gain, bandwith and output swing

## Schematic2 calculation and simulation

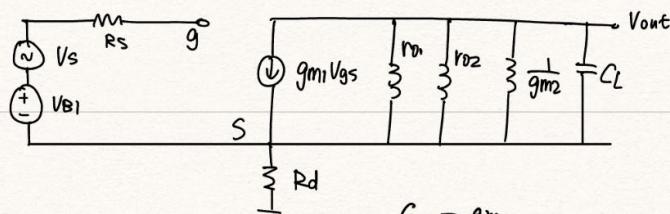
- Hand calculation of gain is as follows, from this calculation we know that in Scenario1 the gain is approximately 19.2986 dB.

Scenario 2:

$$\text{Likewise. } V_{B1} = 1.2V, \quad I_D = \frac{1}{2} M_n C_o \left( \frac{W_1}{L_1} \right) V_{DS}^2 = \frac{1}{2} \times 90 \times 10^{-6} \times 10 \times (1.2 - V_S - 0.8)^2 \quad ①$$

$$V_S = I_D \cdot R_d = I_D \times 2.5k\Omega \quad ②$$

From ①②.  $V_S \approx 0.1V$ ,  $V_{DS1} = 0.3V$ . So.  $V_{DS2}$ ,  $g_{m1}$ ,  $g_{m2}$  are as same.



$$G_m = g_{m1}$$

$$\text{gain } \frac{V_{out}}{V_{in}} = G_m R_{out}. \quad R_{out} = (r_{o1} \parallel r_{o2} \parallel \frac{1}{g_{m2}} \parallel C_L) + R_d = 36664 \Omega.$$

$$\rightarrow 20 \lg \left( \frac{V_{out}}{V_{in}} \right) = 20 \lg (g_{m1} R_{out}) = 19.9121 \text{ dB},$$

$$C_L \quad \boxed{\frac{1}{r_{o1}} \quad \frac{1}{r_{o2}} \quad \frac{1}{g_{m2}}} \quad \tau_1 = R_C L = \left( r_{o1} \parallel r_{o2} \parallel \frac{1}{g_{m2}} \right) C_L \\ \approx \frac{1}{2.846 \times 10^{-5}} \times 2.5 \times 10^{-12} \\ = 8.784 \times 10^{-8}.$$

Figure 6: handout2

- Hand calculation of bandwidth is also as follows, from this calculation we know that in Scenario1 the bandwidth is approximately 1.9MHz
- Simulated Results of gain and bandwidth and output voltage swing in Schematic1 are as follow. Set up the circuit according to the schematic diagram, then construct the corresponding ac and trans simulation analysis, write the corresponding representation function, and then run the simulation.

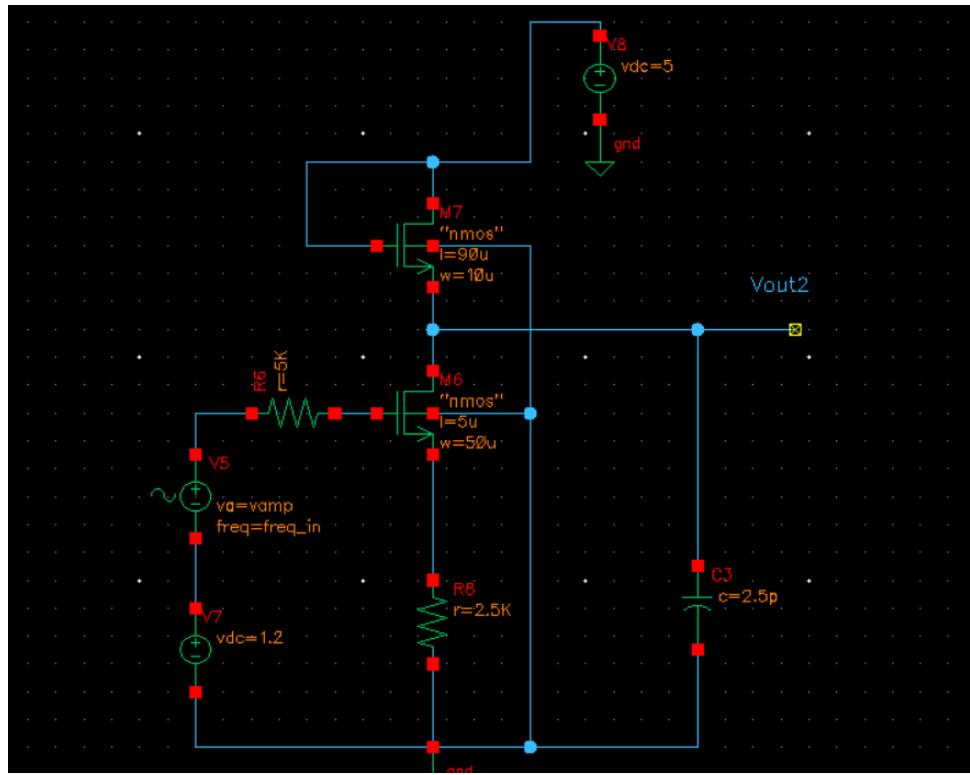


Figure 7: Schematic<sub>2</sub>

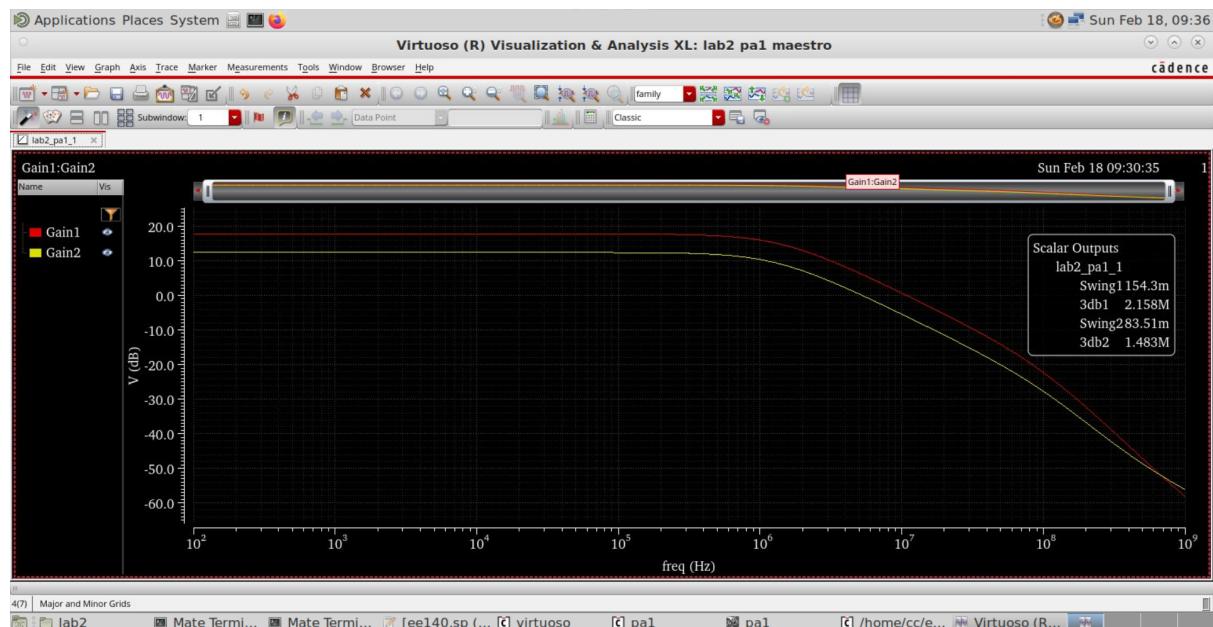


Figure 8: Gain, bandwidth and output swing

## Part B

### Meeting Design Specifications in Simulation

The design of the entire circuit and the final circuit value are shown in schematic figure.

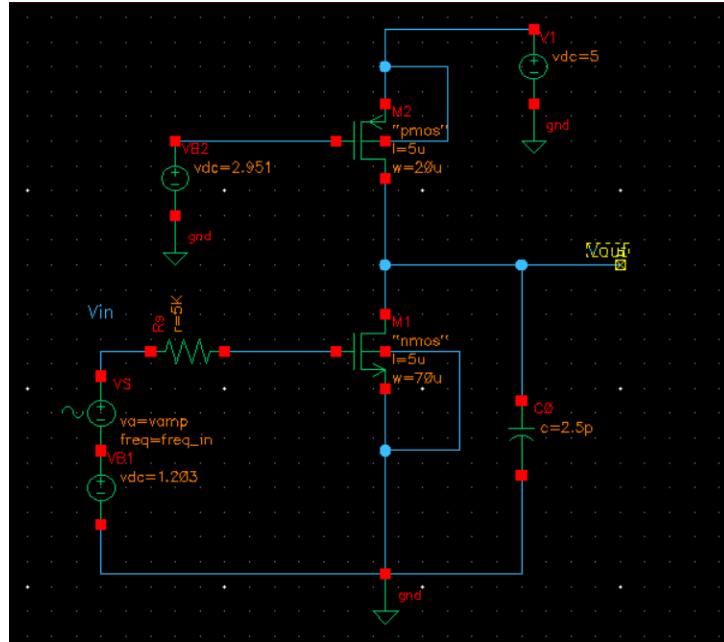


Figure 9: Designed circuit schematic

### Simulation result

The simulation results are shown in the figure below. It can be seen from the figure that the simulated results meet the requirements.

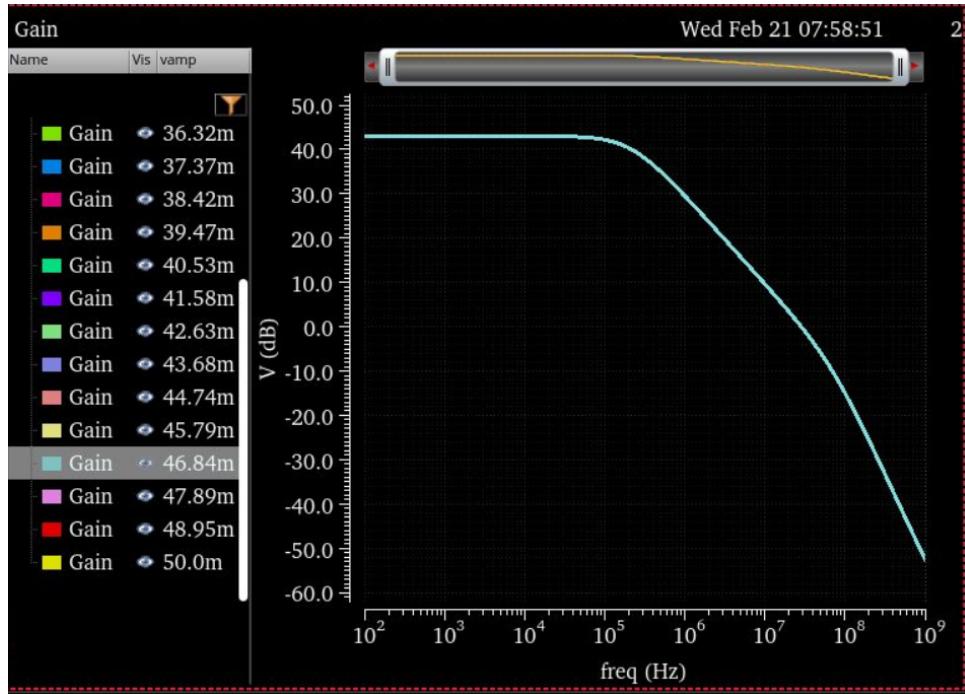


Figure 10: Simulation1

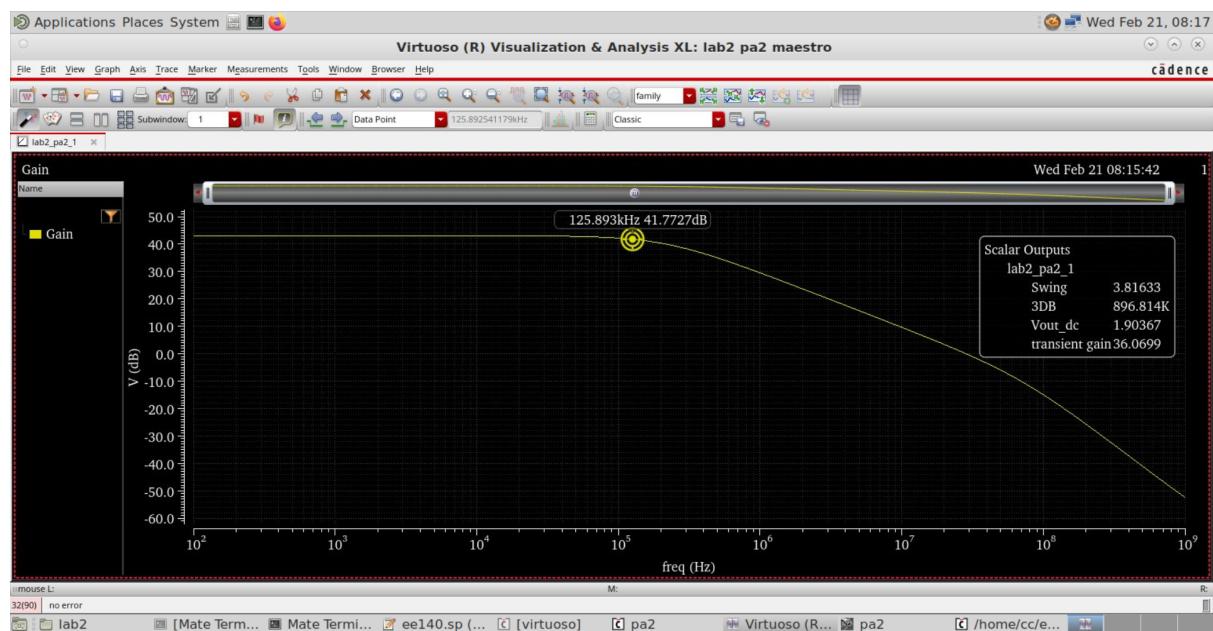


Figure 11: Simulation3

## Handout calculation

In that case, we get circuit parameters so we can get gain, bandwidth and output voltage swing through handout calculation.

From Cadence setting parameters:

$$V_{B1} = 1.203V, \quad V_{B2} = 2.951V. \quad \text{So, } V_{O1} = 1.203 - 0.8 = 0.403V.$$

$$V_{out} = V_{ds1} = 1.901V \quad V_{O2} = 5 - V_{B2} - 0.8 = 1.249V.$$

$$\text{So, } g_{m1} = \mu_n C_{ox} \left( \frac{W_1}{L_1} \right) V_{O1} = 90 \times 10^{-6} \times 14 \times (0.403) = 5.0778 \times 10^{-4} S$$

$$g_{m2} = \mu_n C_{ox} \left( \frac{W_2}{L_2} \right) V_{O2} = 30 \times 10^{-6} \times 4 \times (1.249) = 1.4988 \times 10^{-4} S$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \left( \frac{W_1}{L_1} \right) V_{O1}^2 = 0.5 \times 90 \times 10^{-6} \times 14 \times 0.403^2 = 1.023 \times 10^{-4} A.$$

$$r_{o1} = \frac{1}{\lambda_1 I_D} = \frac{1}{0.07 \times 1.023 \times 10^{-4}} = 977348 \Omega. \quad r_{o2} = \frac{1}{\lambda_2 I_D} = 488674 \Omega.$$

$$R_{out} = r_{o1} \parallel r_{o2} \parallel Z_L = 977348 \Omega \parallel 488674 \Omega \parallel 2 \Omega = 325768 \Omega.$$

$$\Rightarrow \text{gain: } \frac{V_{out}}{V_{in}} = g_{m1} R_{out} = 165.426. \rightarrow 20 \lg \left( \frac{V_{out}}{V_{in}} \right) = 44.372 \text{ dB.}$$

$$\Rightarrow \text{bandwidth: } T_2 = (r_{o1} \parallel r_{o2}) C \quad f_2 = \frac{1}{2\pi T_2} = 195 \text{ kHz.}$$

$$\Rightarrow \text{Output Swing: } \left| \begin{array}{l} \text{for M1: } V_{dd} - 1.5V_{pp} > V_{g1} - |V_{tp}| \\ \qquad \qquad \qquad V_{out} > V_{B1} - 0.8 + 1.5. \rightarrow \text{Correct.} \\ \text{for M2: } (5 - V_{ds2}) - 1.5V_{pp} > (5 - V_{g2}) - |V_{tp}| \\ \qquad \qquad \qquad V_{out} < V_{g2} - 2.3. \rightarrow \text{Correct} \end{array} \right.$$

So from handout calculation, gain is 44.372 dB,

bandwidth  $f_2 = 195 \text{ kHz}$ . and output swing meet requests.

Figure 12: handout

## Discussion

### 1. Output resistance comparison between Part B and Part A.1

Through comparison through the handout calculation process, it can be found that the structures of the small signal equivalent models of Part B and Part A.1 are similar. If we compare the output resistance, the main difference lies in the two resistors  $r_{o1}$  and  $r_{o2}$ .

$r_{o1}$  and  $r_{o2}$  mainly depend on the lambda parameters and  $I_{ds}$  of the MOS tube itself. It is obvious that in Part B and Part A.1, the lambda parameters of PMOS and NMOS are different; regarding  $I_{ds}$ , since the values of the DC power supply are different, that is, the DC operating points are different, then the  $I_{dc}$  in these two circuits is different.

That is, these two factors cause the output resistance of the two parts to be different.

### 2. Replacing circuit with current mirror topology

In the circuit below, I use a current mirror instead of a DC voltage source, and its value basically meets the requirements of the lab.

#### Explanation:

- Current mirror can provide a higher Power Supply Rejection Ratio (PSRR), which means they are better at isolating the impact of power supply voltage variations on circuit performance, enhancing the circuit's immunity to power noise. Circuits biased with a DC voltage source might be more susceptible to fluctuations in power supply voltage.
- Output Impedance: Current mirror can possess a high output impedance, making them ideal as current sources. High output impedance helps maintain a stable bias current even if load conditions change. In contrast, the output impedance of a DC voltage source is relatively low, which may lead to unstable bias condition.

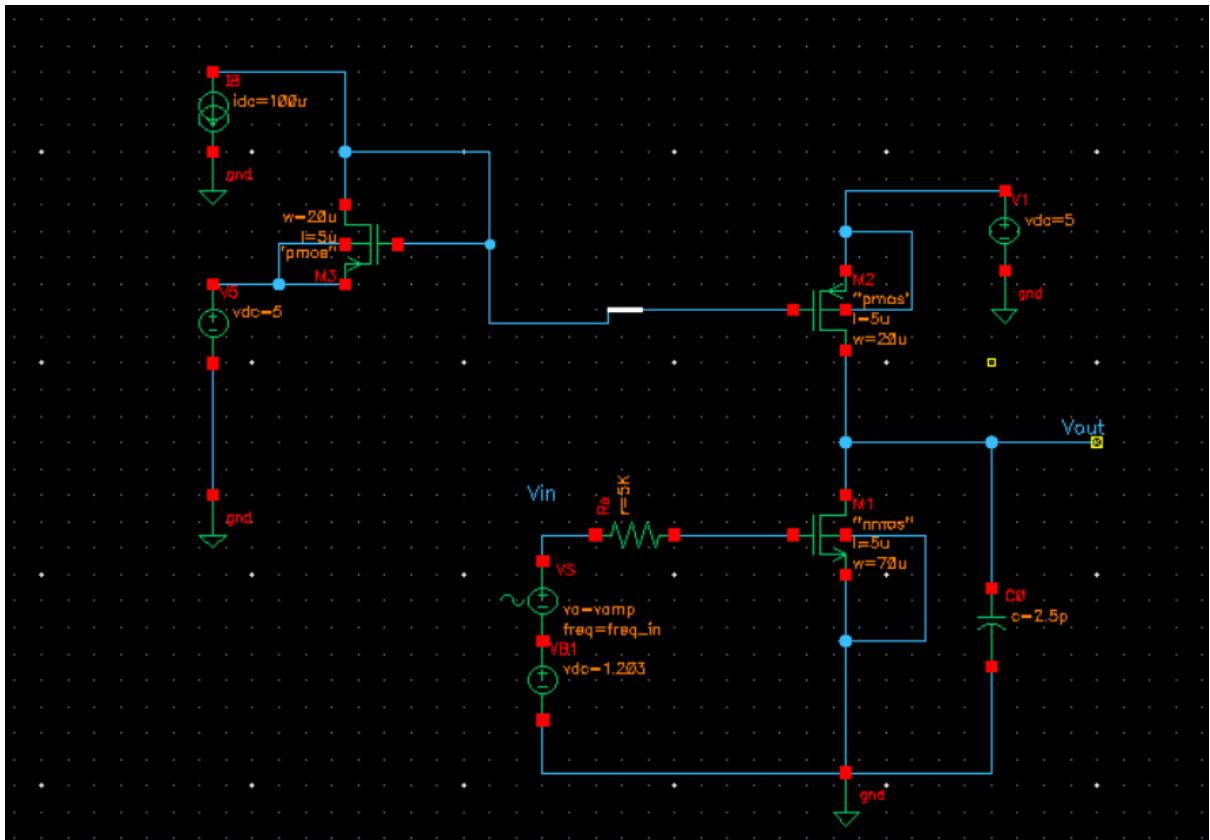


Figure 13: Current mirror bias

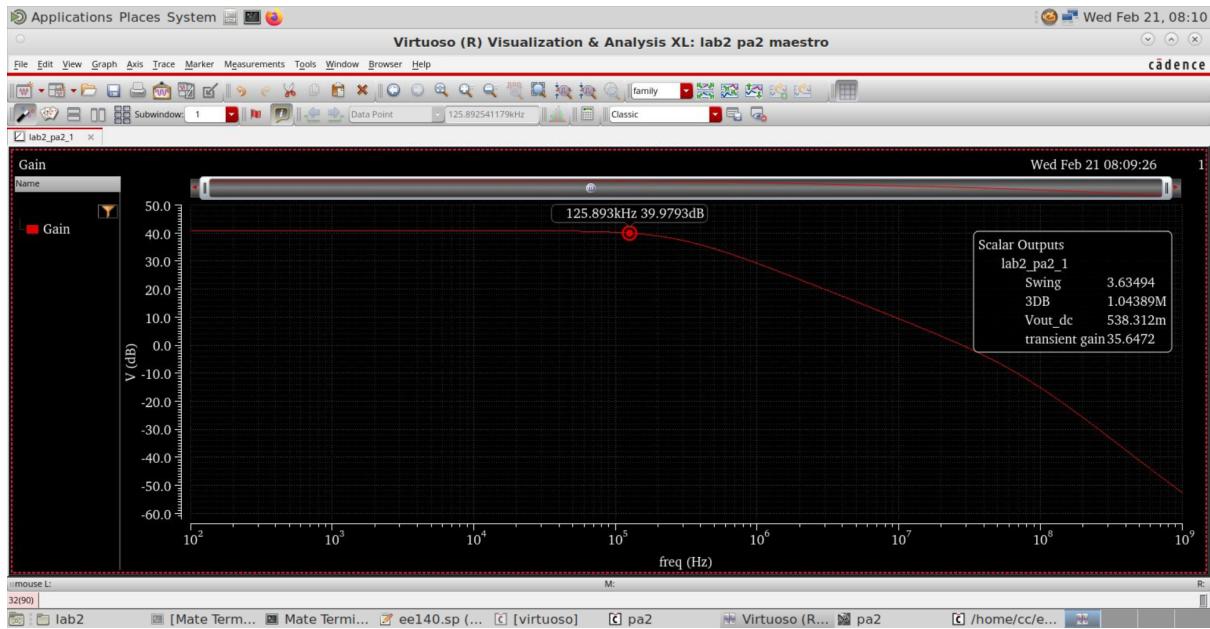


Figure 14: Simulation2

### 3. Table of calculated and simulated performance for Part B

Parameter	Simulated performance	Calculated performance
Midband gain	41.7727dB	44.372dB
3 dB cutoff frequency (bandwidth)	1.04389M	1.95M
Output voltage swing	3.63494 V	3.1321

Table 2: Table of calculated and simulated performance.

- (a) The difference in mid-band gain may be due to non-idealities in the transistor, and calculations usually assume ideal conditions. Parameters such as transistor gain and body effects in MOSFET do not exist in the ideal model but affect the actual gain.
- (b) The difference in bandwidth may be due to parasitic capacitance and inductance that are present in the circuit but ignored in the calculations. These parasitic effects can be caused by the internal capacitance of the transistor itself.
- (c) The difference in output voltage swing may be caused by the approximation in the calculation, because in our calculation assumption,  $v_{out}$ , that is,  $v_{ds}$ , should be around 2.5V, which will best meet the swing requirements of the question. However, in the subsequent calculation design and simulation, we found that it was around 1.9-2.0V. Although it was gradually corrected during the subsequent design process to still meet the requirements, there are still errors.

4. Describing design procedure The design process, designed circuit diagram, and final simulation result display diagram are as follows:

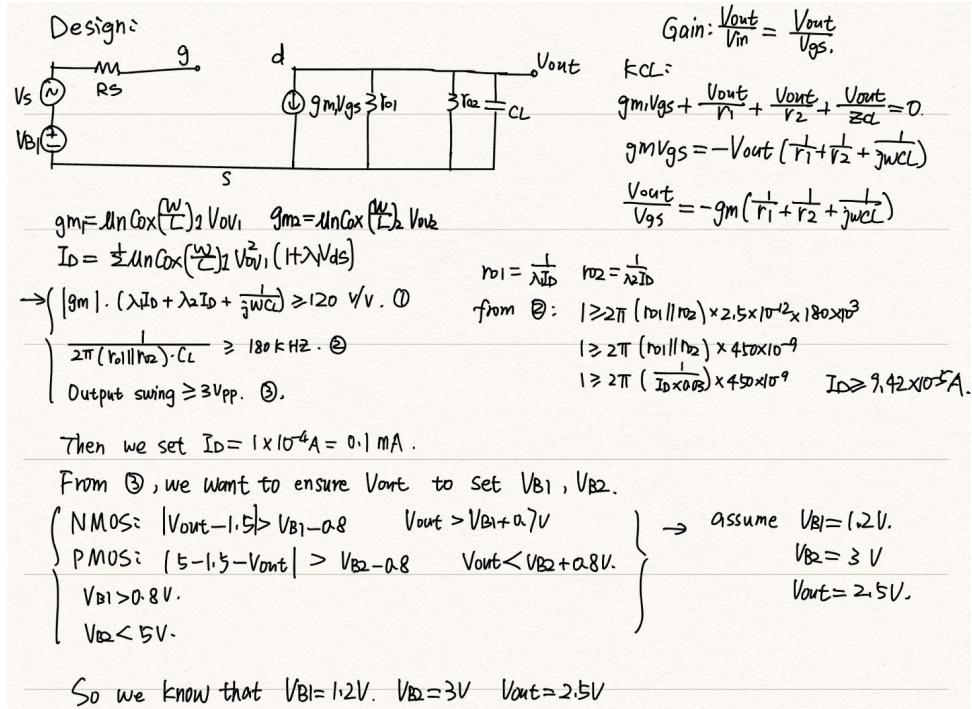


Figure 15: Preliminary design steps

In this step, we can set  $V_{B1} = 1.2V$ ,  $V_{B2} = 3V$ ,  $V_{out} = 2.5V$ .

Then we can deduce and determine the  $W/L$  parameters of  $M1$  and  $M2$ . In the next step, we set  $W1 = 70 \mu m$ ,  $W2 = 20 \mu m$ .

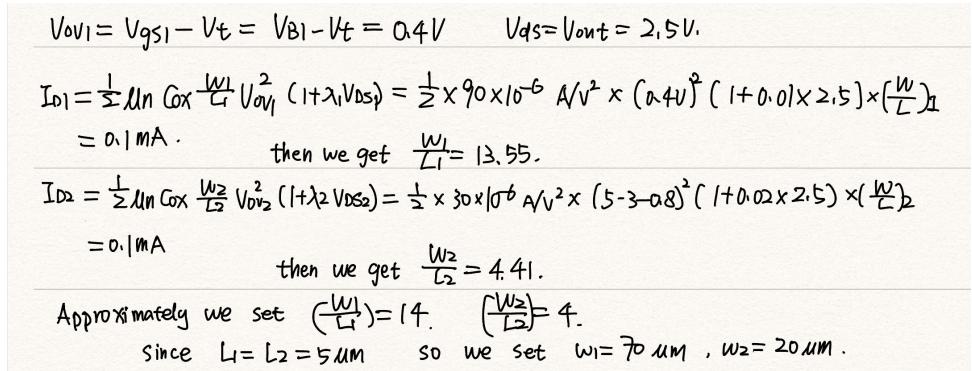


Figure 16: W/L setting step

However, these parameters only determine the basic operations that can be used for simulation and cannot completely guarantee that the simulation will be successfully completed and the indicators required by the question will be met.

So next, we need to perform a sweep operation to determine the specific voltage parameters through scanning simulation, so that the circuit can obtain the desired optimal parameters and complete the requirements of the question.

**Sweep analysis:**

In order to determine the real values of VB1 and VB2, we determine the value of W/L, and then scan the range of VB1 and VB2 to maximize the gain. In this case, bandwidth far meets the requirements. What we focus on is how to select VB1, VB2, and check Vout to make gain meet the requirements and maximize output voltage swing.

After sweep analysis, we finally selected a set of suitable values for VB1 and VB2, and we can get the final DC operating point value of Vout.