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Thursday, December 14, 2017.
8:00-11:00am

EE140/240A—Fall 2017: Final Exam

NAME	Last First

GRAD/UNDERGRAD	

Problem 1:	**/ 14**
Problem 2:	**/ 24 (28)**
Problem 3:	**/ 12**
Problem 4:	**/ 16**
Problem 5:	**/ 11 (17)**
Total:	**/ 77 (87)**

Problem 1 (14 pts)

You've landed your dream job as an analog design engineer at Keysight! Because of your design experience from EE140/240A, you are tasked with designing a low-power two-stage amplifier to drive a large capacitive load. However, you're working with short-channel devices that can't really be modeled with square-law I-V characteristics. After running some simulations, you find that the following short-channel device model gives a reasonable approximation of the I-V characteristics of the MOSFETs in your design kit:

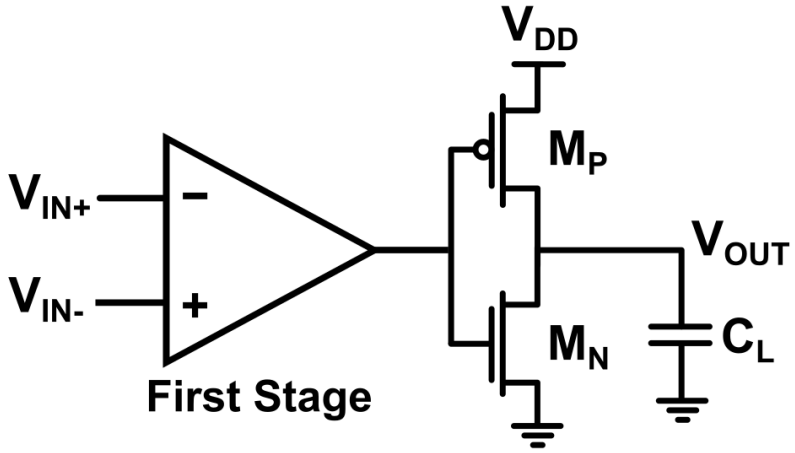
$$I_D = k' \frac{W}{L} (|V_{GS}| - |V_{TH}|) V_{d,sat} (1 + \lambda V_{DS})$$

You have found that $k'_N = 2k'_P$, $|V_{TH,P}| = |V_{TH,N}|$, $V_{d,satP} = V_{d,satN}$, and $\lambda_P = 2\lambda_N$. Note that $V_{d,sat}$ is a constant parameter. You may ignore any subthreshold effects for this problem unless told otherwise (e.g., assume that if $|V_{GS}| < |V_{TH}|$, $I_D = 0\ A$).

a) (2 points) What is the minimum current required to drive a load of C_L the full output swing of $V_{sw,out}$ in t_{settle} seconds? Express your answer in terms of these parameters. You may assume the amplifier is slewing the entire time.

$I_{min} =$

b) (5 points) To improve your settling time, you initially try to use an inverter for the output stage, as illustrated below.



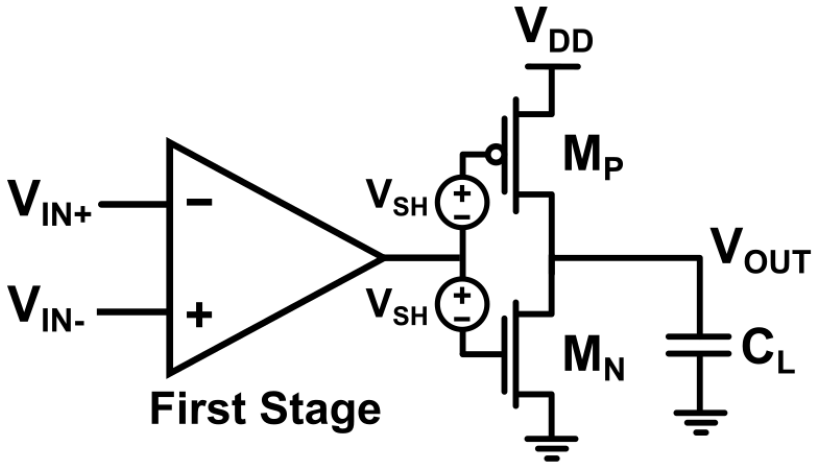
i. (1 point) What is the ratio between W_N and W_P needed to guarantee that output stage has equal rising and falling edge drive current? Assume that the output of the first stage is biased around $\frac{V_{DD}}{2}$ and that $L_P = L_N = L$.

$W_N/W_P =$

ii. (4 points) Assuming W_N/W_P is chosen appropriately, what choice of W_P is needed to provide a peak drive current of I_{pk} if the peak output swing of the first stage is V_{SW} (so that the output of the first stage swings between $\frac{V_{DD}}{2} + V_{SW}$ and $\frac{V_{DD}}{2} - V_{SW}$)? Express your answer in terms of device parameters, I_{pk}, V_{sw}, and V_{DD}. You may assume that $V_{SW} < \frac{V_{DD}}{2} - V_{TH}$ and that $\frac{V_{DD}}{2} > V_{TH}$.

$W_P =$

c) (3 points) To lower the quiescent current, you introduce the level shifters shown below.



i. (1 point) What choice of V_{SH} will lower the nominal quiescent current to 0 A (still using the simplified short-channel I-V model)? Assume that one device should always be on if $V_{sw} > 0\ V$.

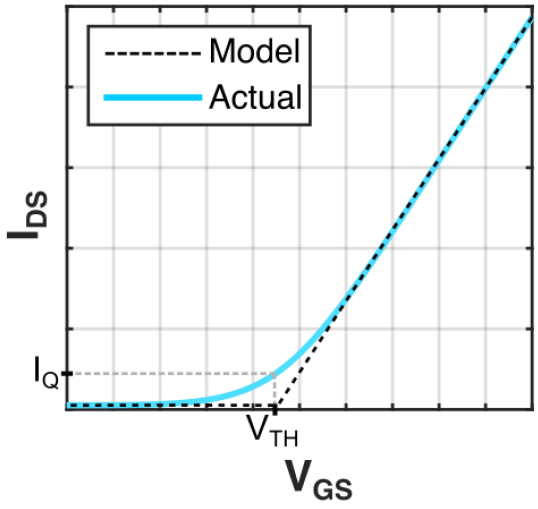
$V_{SH} =$

ii. (2 points) Will introducing the level shifters cause W_P (and W_N) to increase, stay the same, or decrease if I_{pk}, V_{sw} and V_{DD} are fixed? Explain your answer. All assumptions described in part (b) apply to this problem.

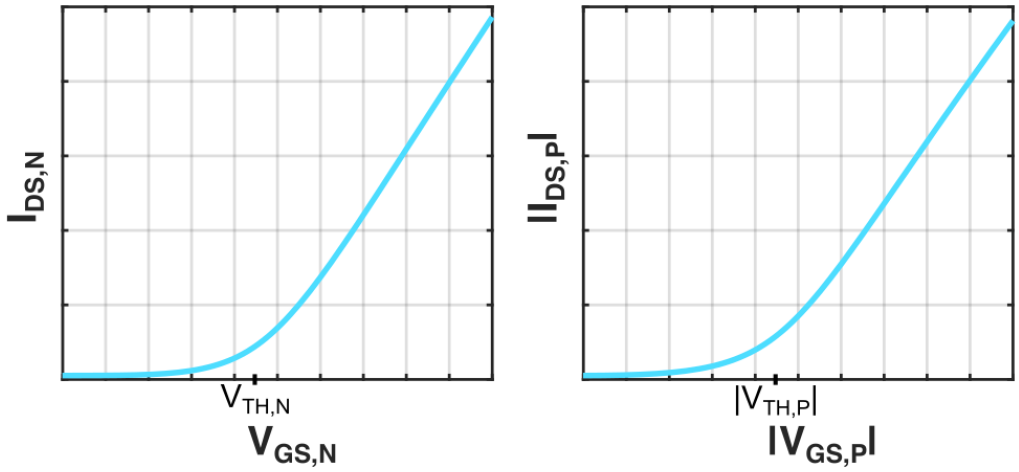
Circle one: Increase Stay the same Decrease

Explanation:

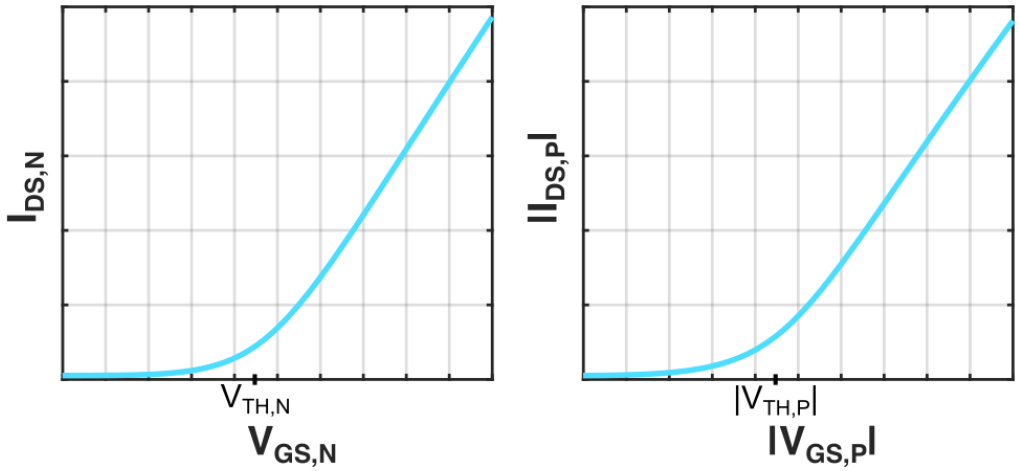
d) (4 points) Due to subthreshold operation, the actual I_{DS} vs. V_{GS} characteristic of the devices looks more like the following, so the level-shifted output stage actually draws some nonzero (but small) quiescent current I_Q that the simplified model presented at the beginning of the problem does not capture.



i. (2 points) Using the provided plot of PMOS and NMOS $|I_D|$ vs. $|V_{GS}|$, briefly explain how you would calculate the effective transconductance of the output stage in (c) when a very very small input step is applied. Feel free to sketch on the plots.

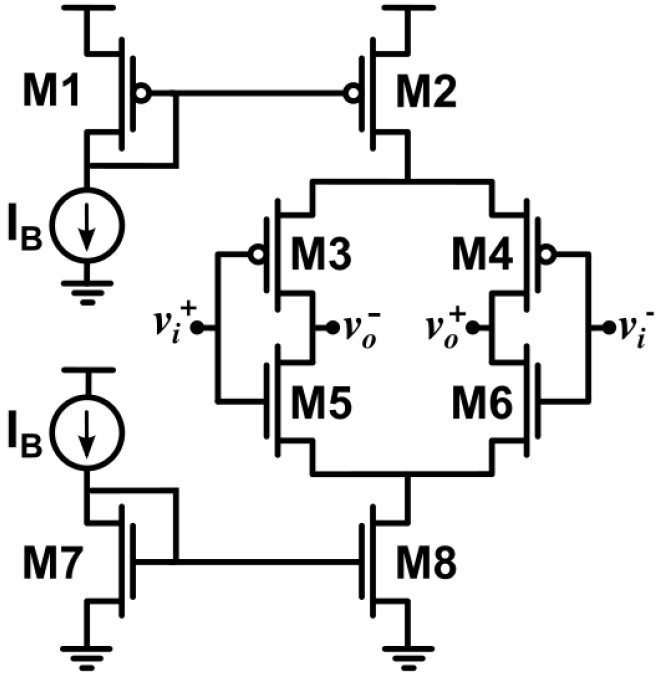


ii. (2 points) Now explain how you would calculate the transconductance of the same circuit when a very large positive input step is applied to the input of the first stage ($V_{IN+} > V_{IN-}$ in the diagrams from parts (b) and (c)). Again, feel free to sketch on the plots.



Problem 2 (24, 28 pts)

You are taking EE 240B, and designing your final project with a partner, Anna Logue. As part of your project, you need to design a low-power 2-stage op-amp and Anna suggests the topology shown below.



Assume $(W/L)_2 = 2(W/L)_1$; $(W/L)_3 = (W/L)_4$; $(W/L)_5 = (W/L)_6$; $(W/L)_8 = 2(W/L)_7$. You may assume all devices exhibit square-law behavior.

a) (2 pts) Assume all devices are in saturation. Compute I_{D2} and I_{D3} in terms of I_B. Ignore Vds mismatch between M1 and M2.

$I_{D2} =$

$I_{D3} =$

b) (2 pts) Compute ΔV_3 and ΔV_2 in terms of I_B, device sizes, and ΔV_1. (*note: $\Delta V = V^* = v_{ov}$)*

$\Delta V_3 =$

$\Delta V_2 =$

c) (4 pts) Compute the maximum and the minimum common-mode input voltage for normal operation of this circuit. Your answer should be in terms of V_{ThN}, V_{ThP}, and ΔV_M (where M=device number).

$Max\ V_{cm,in} =$

$Min\ V_{cm,in} =$

d) (4 pts) Compute the maximum peak-to-peak differential output swing in terms of V_{CM}, V_{ThN}, V_{ThP}, and ΔV_M.

$Max\ swing =$

For the following parts (e-h) your answers should be in terms of small-signal device parameters, (e.g. g_{mnM}, g_{mpM}, r_{onM}, r_{opM}, g_{mbnM}, g_{mbpM}, where M=device number.)

e) (4 pts) Compute the differential short-circuit output transconductance of the circuit, G_m, and the differential circuit output resistance R_o.

$G_m =$

$R_o =$

f) (4 pts) Compute the gain from the power supply (positive rail) to the differential output of the amplifier, $A_{V_{DD}-dm,out}$. What is the corresponding power supply rejection ratio ($PSRR = A_{dm,in-dm,out}/A_{V_{DD}-dm,out}$) of the circuit?

$A_{V_{DD}-dm,out} =$

$PSRR =$

g) (4 pts) Name one advantage and one disadvantage of this circuit over an ordinary differential pair with an active load. While there are many possible answers, try to pick the ones you think are the most important considerations for using this circuit as the first stage in a 2-stage op-amp design.

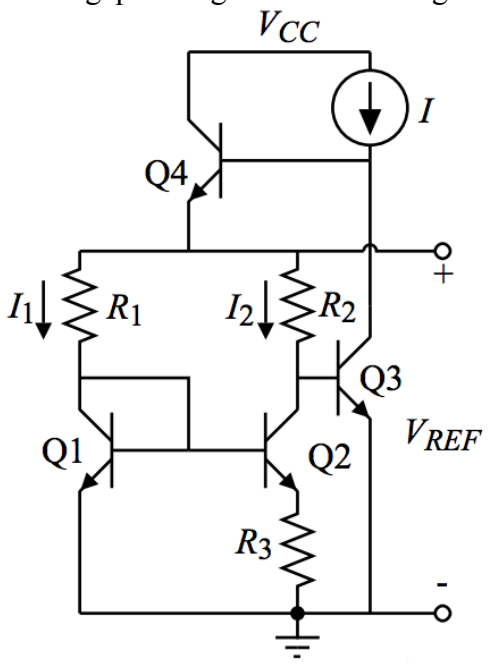
Advantage:

Disadvantage:

h) (4 pts) **EE240A only:** How does this topology impact input-referred noise compared to a diff pair with active load? Be quantitative in your answer.

Problem 3 (12 pts)

The circuit below is called a Widlar Bandgap Voltage Reference. Neglect the Early effect.



a) (4 pts) Compute the voltage drop across R_3 (V_{R3}) in terms of BJT device parameters and the currents labeled in the circuit.

$V_{R3} =$

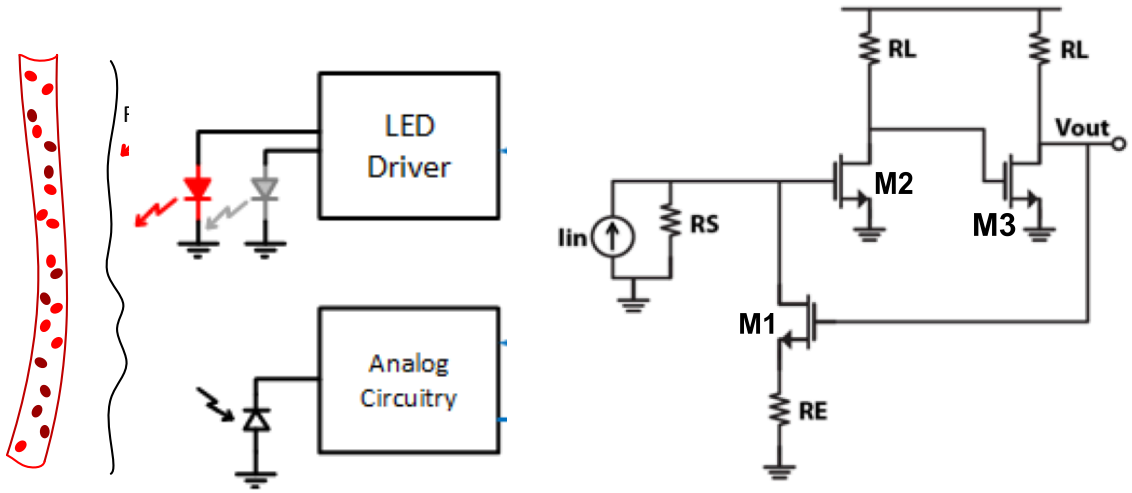
b) (4 pts) What is the purpose of Q3?

c) (4 pts) The PTAT reference $V_{REF} = KV_t + V_{BE}$. Compute K in terms of device parameters and resistances in the circuit.

$K =$

Problem 4 (16 pts)

You are designing a readout circuit for a pulse oximeter (a non-invasive method to measure a person's oxygen saturation. The oximeter functions by shining two wavelengths of light through the body part (typically finger or earlobe) to a photodiode. The photodiode converts the unabsorbed light to a current, which can be amplified by a transimpedance amplifier (TIA). A simple TIA is shown in the figure below. A photodiode can be modeled by a current source and shunt impedance as shown below (*note: real photodiodes have significant shunt capacitance, which we are ignoring in this problem*).



The signal of interest (i_{in}) is typically small compared to the DC value of the input current (I_{IN}). For the problems below, do not ignore r_o, but you may ignore the body effect. Assume that $g_m r_o$, $g_m R_L$, and $g_m R_E$ are large, $R_L \ll r_o$, and R_S is very large. All transistors are identical.

a) (2 pts) Identify the type of feedback.

b) (4 pts) Calculate the mid-band <u>input impedance</u> exclusive of the source resistance RS.

$R_{in} =$

c) (4 pts) Calculate the output impedance. Do not neglect R_S.

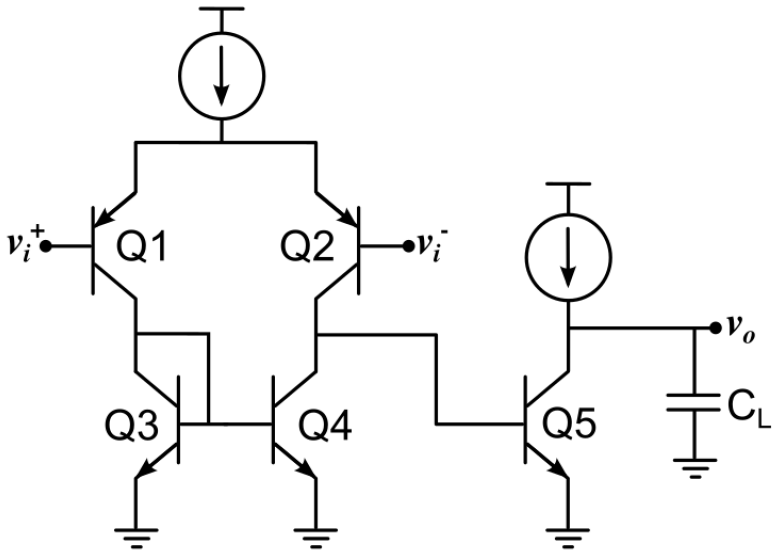
$R_{out} =$

d) (4 pts) Calculate the closed-loop gain Vout/Iin. You should include R_S in this calculation.

$V_{out}/V_{in} =$

e) (2 pts) Why is this type of feedback advantageous in this application?

Problem 5 (11, 17 pts)



The BJT op amp shown above is a simplified version of many early op amp designs which were done in a bipolar process. You may assume that all transistors are identical, with the same small signal parameters. You may also assume that differential transistors are perfectly matched.

Do not neglect r_π. Neglect all capacitors except for the device C_π and the load C_L. Assume that the input is driven by an ideal voltage source and that all devices are in forward active operation.

a) (2pts) Calculate the DC open-loop gain of this circuit.

$Gain =$

b) (3 pts) There are three poles in this circuit. Find the three pole frequencies, expressing your answers in terms of the small signal parameters of the transistors and C_L.

$\omega_{p1} =$

$\omega_{p2} =$

$\omega_{p3} =$

c) (2 pts) There is one zero in the circuit as drawn, what is its frequency?

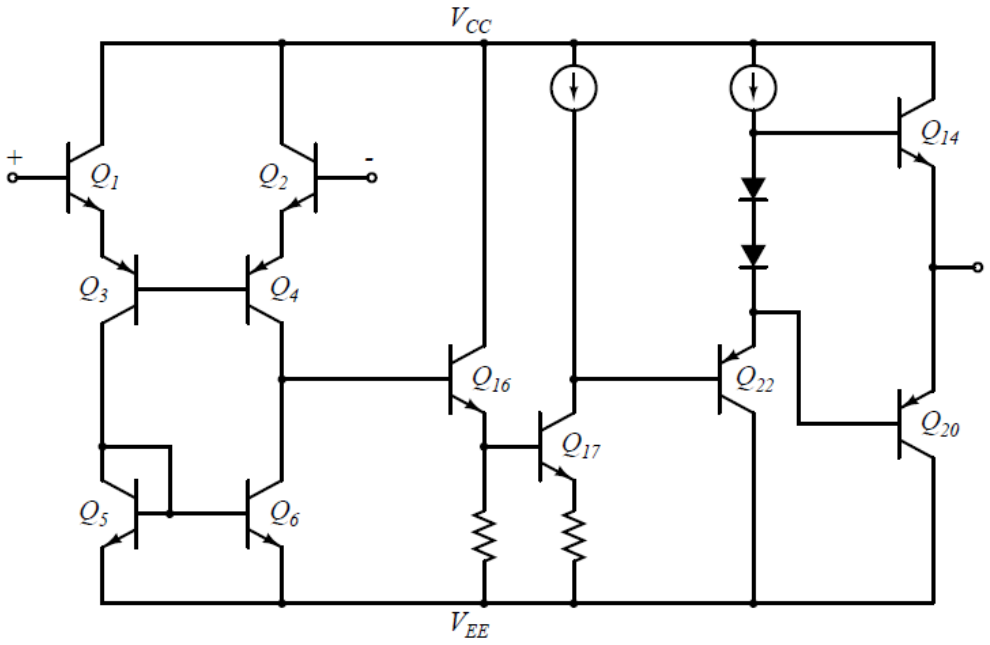
$\omega_z =$

d) (4 pts) Place a capacitor and size it for dominant pole compensation to achieve phase margin of 45 degrees. Your goal is to minimize the size of C_C. Note: do not use the Miller effect (i.e., your capacitor should be connected to ground). Where is the best location for this capacitor? State your assumptions. You may assume that the second pole does not impact the location of the unity-gain frequency.

$C_C =$

C_C should be placed between _____ and ground because:

e) (4 pts) **EE240A only:**



The above circuit represents a simplified schematic of the famous Fairchild uA741 op amp. For each of the legs containing transistors Q16, Q17, Q22, Q20, give a one sentence explanation explaining the function.

Q16 branch:

Q17 branch:

Q22 branch:

Q20 branch:

f) (2 pts) **EE240A only:** Draw in the schematic the best location for a Miller compensation capacitor and justify your answer. Do you have to worry about the RHP zero? Why or why not?

Reason for Miller capacitor placement:

RHP zero explanation:

Extra page for work, clearly label problem number

Extra page for work, clearly label problem number

EE 140 / 240A Equation Sheet
Prof. Rikky Muller, Fall 2017

MOSFET Large Signal - Saturation

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

$$V_{TH} = V_{t0} - \gamma(\sqrt{2|\Phi_F|+V_{SB}} - \sqrt{2|\Phi_F|})$$

$$V_{OV} = \Delta V = V_{GS} - V_{TH}$$

MOSFET Small Signal - Saturation

$$g_m = \mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH}) = \sqrt{2\mu C_{ox}\frac{W}{L}I_D}$$

$$g_{mb} = \frac{\gamma g_m}{2\sqrt{2|\Phi_F|+V_{SB}}};\ \gamma = \frac{\sqrt{2\epsilon_s N_A}}{C_{ox}}$$

$$r_o = \frac{1}{\lambda I_D}$$

MOSFET Large Signal – Velocity Saturation

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH})V_{dsat,l}(1+\lambda V_{DS})$$

$$V_{dsat,l} \approx \frac{(V_{GS}-V_{TH})LE_{sat}}{(V_{GS}-V_{TH})+LE_{sat}}$$

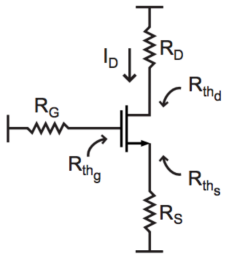
MOSFET Large Signal – Triode

$$I_D = \mu C_{ox}\frac{W}{L}\left(V_{GS}-V_{TH}-\frac{V_{DS}}{2}\right)V_{DS}$$

MOSFET Small Signal – Triode

$$r_{ds} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH}-V_{DS})}$$

Thevenin Resistances - Saturation



$$R_{thd} = r_o(1+(g_m+g_{mb})R_S)+R_S$$

$$R_{thg} = \infty$$

$$R_{ths} = \left(1+\frac{R_D}{r_o}\right)(r_o \| \frac{1}{g_m+g_{mb}})$$

MOSFET Capacitance

$$C_{OV} = C_{OL} = WL_D C_{ox} + WC_{fringe}$$

$$C_{gs} = \frac{2}{3}C_{ox}W(L+2L_D)+C_{OV}$$

$$C_{gd} = C_{ov}$$

$$C_{jsb/jsdb} = \frac{C_j(0)WE + C_{jsw}(0)(W+2E)}{\sqrt{1+\frac{V_{SB\{DB\}}}{|\Phi_F|}}}$$

MOSFET G_m, Source Degeneration

$$G_m = \frac{g_m}{1+(g_m+g_{mb})R_S}$$

BJT Large Signal – Forward Active

$$i_E = i_B + i_C$$

$$i_B = i_C/\beta$$

$$i_C = I_S e^{\frac{V_{BE}}{V_T}}\left(1+\frac{V_{CE}}{V_A}\right)$$

$$I_S = \frac{A_E q D_n n_i^2}{N_A W}$$

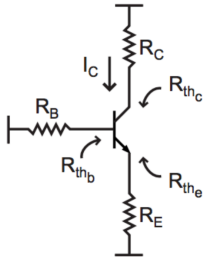
BJT Small Signal – Forward Active

$$g_m = \frac{I_C}{V_T};\ V_T = \frac{kT}{q}$$

$$r_o = \frac{V_A+V_{CE}}{I_C} \approx \frac{V_A}{I_C}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{V_T}{I_B}$$

Thevenin Resistances – Forward Active



$$R_{thb} = (r_e+R_E)(\beta+1) = r_\pi+(\beta+1)R_E$$

$$R_{the} = \frac{r_\pi+R_B}{\beta+1} \cong \frac{1}{g_m}+\frac{R_B}{\beta+1}$$

$$R_{thc} = r_o + R_E \| (r_\pi+R_B) + g_m r_o \frac{R_E}{1+\frac{R_E+R_B}{r_\pi}}$$

BJT Gains – Forward Active

$$\frac{v_c}{v_b} = -G_M R_C;\ g_m = \frac{g_m}{1+g_m R_E}$$

$$\frac{v_c}{v_e} = -G_m R_C;\ G_m = \frac{g_m}{1+g_m R_E}$$

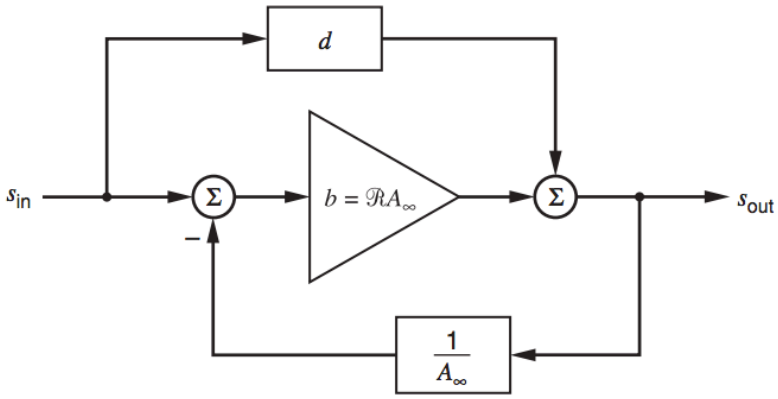
$$\frac{v_e}{v_b} = \frac{R_E \| r_o}{R_E \| r_o + r_e}$$

BJT Capacitance – Forward Active

$$C_\pi = \tau_p g_m + \frac{C_{je0}}{\left(1+\frac{V_{EB}}{\psi_0}\right)^m}$$

$$C_\mu = \frac{C_{\mu 0}}{\left(1+\frac{V_{CB}}{\phi_j}\right)^m}$$

Return Ratio Analysis



To find the return ratio:
1. Set all independent sources to zero
2. Disconnect the dependent source from the rest of the circuit, which introduces a break in the FB loop
3. On the side of the break that is not connected to the dependent source, connect an independent test source s_t
4. Find the return signal s_r generated by the dependent source.
5. RR = $-s_r/s_t$
6. d is found by setting the dependent source of the amplifier = 0
7. A_∞ is determined by the passive feedback network = 1/f

$$\frac{s_{out}}{s_{in}} = \frac{A_\infty RR}{1+RR} + \frac{d}{1+RR} \qquad Z_{CL} = Z_{OL}\frac{(1+RR_{short})}{1+RR_{open}}$$

Noise

Resistor noise:

$$\overline{v_n^2} = 4kTRB$$

$$\overline{i_n^2} = \frac{4kTB}{R}$$

MOSFET noise:

$$\overline{v_n^2} = \frac{4kT\left(\frac{\gamma}{\alpha}\right)B}{g_m}$$

$$\overline{i_n^2} = 4kT\left(\frac{\gamma}{\alpha}\right)g_m B$$

Mismatch

$$\sigma_{\Delta V_{TH}} \approx \frac{A_{V_{TH}}}{\sqrt{WL}}$$

$$\sigma_{\Delta W/L} \approx \frac{A_K}{\sqrt{WL}}$$

Bandgaps

$$V_{OUT} = V_{BE} + K\Delta V_{BE}$$

$$\frac{dV_{BE}}{dT} = -2\frac{mV}{°C}$$

$$\frac{dV_T}{dT} = 0.18\frac{mV}{°C}$$