EECS140 Midterm 2

Spring 2015

|  |  |
| --- | --- |
| Prob. | Score |
| 1 | /20 |
| 1 | /30 |
| 2 | /15 |
| 3 | /15 |
| 4 | /20 |
| Total |  |

Name\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

SID\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

2B

2A

CC

C2

5

1A

4

1B

3

6

RZ

Iref

1. For the two-stage op-amp above, assuming Iref=20uA and (W/L)6= (10u/1u), design the amplifier so that the tail current is 20uA, the second stage current is 100uA, and the PMOS devices have Vov=100mV.
   1. What are the W/L values for all devices?
   2. What are gm1, Ro1, gm4, Ro4?
   3. What is the gain of the 1st stage, 2nd stage, and overall gain?

Process specs nCox=200A/V2, pCox=100A/V2, =1/(10V), -Vtp=Vtn=0.5V, VDD=2V, Lmin=1um, Cox=5fF/um2, C’ol=0.

1. A different implementation of the same two-stage opamp has the parameters on the following page. Plot the magnitude of the 2nd stage gain, the

1

100

10,000

|Av2|

|Av2|

1E) Second stage gain – |Av2,0|

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| gm1 | Ro1 | gm4 | Ro2 | C2 | CC | Cgs4 |
| 1S | 100M | 10S | 100M | 1pF | 10fF | 100fF |

rad/s

rad/s

rad/s

1G) First stage gain, |Av1|

1

1k

1M

1G

1

1k

1M

1G

1

1k

1M

1G

1F) Impedance at first stage output, |Zo1|

|Zo1|

10M

1K

100K

|Zo1|

1

100

10,000

|Av1|

|Av1|

2) For the following questions, give a short answer and justification (2 sentences max).

Label any poles and zeros clearly!

rad/s

rad/s

1H) op amp Bode plot

10,000

100

1

1

1k

1M

1G

-180

-90

0

Phase(Av)

1

1k

1M

1G

Phase(Av)

-270

|Av|

|Av|

configurations, and that current sources are ideal. Calculate the common mode and differential gain for each amplifier.

2B

2A

1A

1B

3

VoutD

1A

1B

I0

2B

2A

1A

1B

3

2B

VoutC

1A

1B

R2

R1

VoutB

VoutA

VB

VB

Amp A

Amp B

Amp C

Amp D

VB2

VB2

OPA340



1

103

106

10

The OPA334 is a single-ended CMOS op-amp similar to what you’ve been designing in class.

What is the open loop gain?

What is the lowest frequency pole?

What is the phase margin?

Is the amplifier unity-gain stable?

With a 0 to 5V supply, the input common mode range for the OPA334 is from -0.1V to 3.5V. Based on the different op-amp topologies that you know (single stage, two stage, folded cascode), which topologies could this op-amp use? Is the input differential pair made with NMOS or PMOS transistors?