EECS140 Midterm 1

Spring 2016

|  |  |
| --- | --- |
| Prob. | Score |
| 1 | /4 |
| 2 | /8 |
| 3 | /15 |
| 4 | /12 |
| 5 | /20 |
| 6 | /8 |
| Total |  |

Name\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

SID\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. [4] A single-pole amplifier has a low frequency gain magnitude of 10,000 and a gain magnitude of 10 at 10 MHz. What are the pole and unity gain frequencies?
2. [8] You have made a new 3-terminal device from DNA and carbon nanotubes. With one terminal grounded, you determine that the output current in the device follows the equation IB=I0 VA3/2 ln VB in the region of operation with VA and VB between 2 and 10V.
   1. Write an expression for the transconductance in terms of IB and VA
   2. Write an expression for the output resistance in terms of IB and VB
   3. Write an expression for the intrinsic gain in terms of the bias point
   4. To maximize the gain, where would you bias this device (what voltages)?
3. [15] You have an NMOS-input common source amplifier with a PMOS load. Both transistors are biased in saturation, and the quadratic model is appropriate. The magnitude of the gain is large (>100). You try two independent changes to the circuit: doubling the current by changing the bias voltages, and doubling the length of both transistors without changing anything else. How do these changes affect the operating point and performance of the amplifier?

Process specs nCox=200A/V2, pCox=100A/V2, =1/(10V)(Lmin/L), -Vtp=Vtn=0.5V, VDD=2V, Lmin=1um, Cox=5fF/um2, C’ol=0.5 fF/um.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | ID | L | Vov | gm | Ro | Av | p | u | Cin |
| Case 1 | 2 | 1 |  |  |  |  |  |  |  |
| Case 2 |  | 2 |  |  |  |  |  |  |  |

1. [12] Fill in the following table for a single-pole amplifier. Each row is a different amplifier.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| gm | Ro | CL | Av0 | p | u |
|  |  | 10 p | 10 |  | 10 G rad/s |
| 1mS |  |  | 1000 | 1M rad/s |  |

1. [12] You measure the drain current of one NMOS and one PMOS transistor that you intend to use in a common source amplifier. You bias the PMOS source at 10V, the gate at 5V, and sweep the drain voltage. You bias the NMOS source at ground, and the gate at 2 and 2.1V (two different curves), and sweep the drain voltage. The resulting curves are shown below.
   1. Estimate the PMOS output resistance rop
   2. Estimate the magnitude of the PMOS threshold voltage
   3. Estimate gm of the NMOS transistor when VGS=2V and VDS=5V
   4. Estimate the gain of an NMOS-input common source amplifier made with these two transistors under similar bias conditions to those used below.
   5. Estimate the output swing of the amplifier (Vmin to Vmax). Try for 2 digits of precision on Vmin.

0

1

5

10

VOUT

|IDP|

IDN

2mA

1mA

3mA

1. [8] The four transistors shown below are all biased at a current of 1uA. The NMOS device M1 is in sub-threshold, with VGS-Vt=-200mV, and n=1.5. The NMOS device M2 is velocity saturated with VGS-Vt=100mV. The NMOS device M3 is in saturation, with a channel field of approximately 0.1V/um and VGS-Vt=100mV.

A) Approximately what change in VBE will cause the collector current to increase by a factor of 10?

B) Approximately what change in VGS1 will cause the drain current in M1 to increase by a factor of 10?

C) Approximately what change in VGS2 will cause the drain current in M2 to increase by a factor of 10?

D) Approximately what change in VGS3 will cause the drain current in M3 to increase by a factor of 10?

**VBE**

**VGS1**

**2V**

**VGS2**

**VGS3**

**M1**

**M2**

**M3**

VGS3 =

VGS2 =

VBE =

VGS1 =