# EECS 151/251A Exam 1 Information

Exam Date: 7–10 PM Mar 12, 2024

The exam will be closed book, closed notes, but you are allowed to bring a single 8.5 by 11 inch piece of paper with handwritten notes on both sides. You are not allowed to use calculators, cell phones, or another devices.

The questions are assigned points with one point per expected minute of completion time. The exam will be approximately 120 points. You will be given 3 hours.

Topics:

1. Moore's Law Definition and Consequences
2. Dennard Scaling and Consequences
3. Cost/Performance/Power Design Tradeoffs and Pareto Optimality
4. NRE and Recurring costs for ICs
5. Definitions and representations of combinational logic
6. Principle of restoration in logic circuits
7. Basic principle behind edge-triggered clocking and RTL design methodology
8. Digital system implementation technology alternatives and relative strengths and weaknesses
9. FPGA versus ASIC cost analysis
10. Principle behind structural versus behavioral hardware description
11. Basic Verilog descriptions for combinational logic
12. Verilog generators blocks
13. Verilog instantiation of state elements
14. Simple sequential circuits using registers (counters for instance)
15. FPGA reconfigurable fabric architecture

16. Details of FPGA fabric interconnect switches
17. Details of FPGA logic blocks with LUT
18. Logic circuit partitioning for and mapping to FPGA fabric
19. Ripple Adder Circuits
20. Laws of Boolean algebra
21. Boolean algebra representation of logic circuit and manipulation
22. Canonical forms
23. K-map method for 2-level logic simplification
24. Multi-level logic circuits
25. Bubble-pushing method for converting from AND/OR to NAND/NOR
26. FSM state transition diagram (STD) representation
27. FSM implementation in circuit based on STD
28. FSMs description in Verilog
29. FSM Moore versus Mealy styles
30. FSM one-hot encoding design method
31. Basics of planar CMOS IC processing
32. Basics of transistor and wire layout
33. Static switch-level complementary CMOS logic gates
34. Transmission-gate logic circuits
35. Tri-state buffers
36. Edge-triggered Flip-flop implementation and operation