

ECEN 474/704: Lab 02

Layout Design, Simulation and Verification in Cadence

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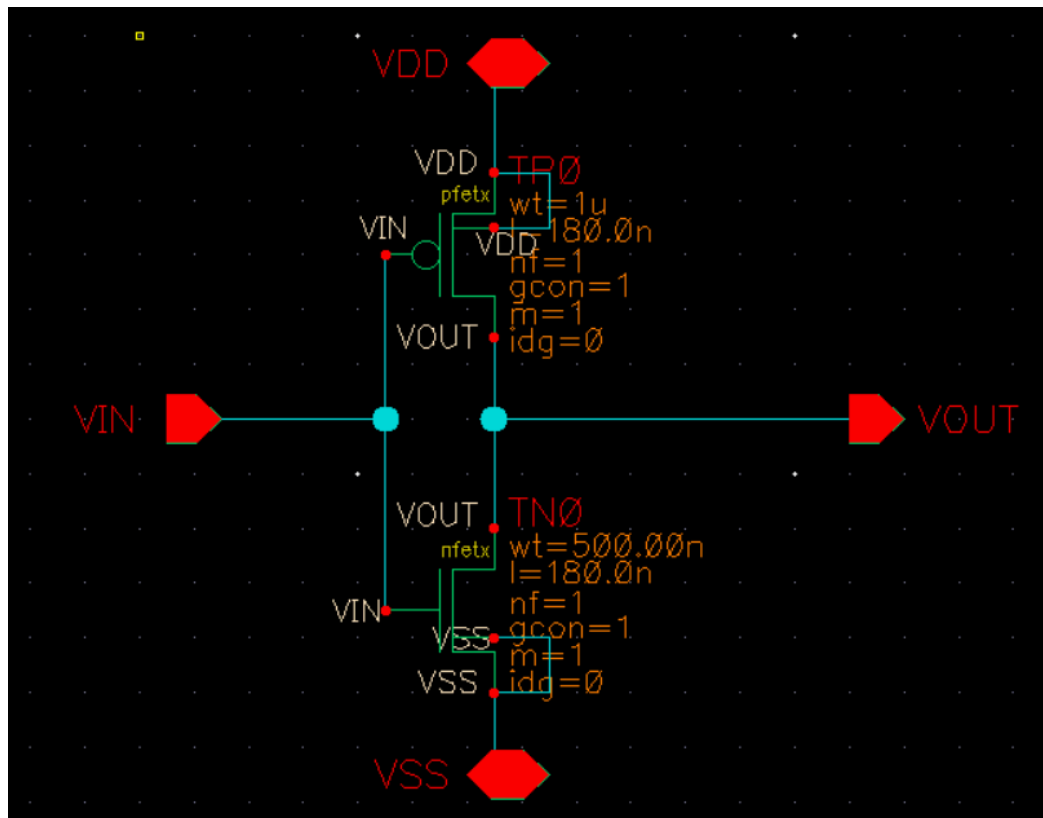
I. DISCUSSION OF THE LAB AND RESULTS

The point of this lab was less about learning the hardware, and more about the software cadence and the manufacturing process's limitations. Designing transistor layouts such that the selected manufacturing process will be able to guarantee functionality. Therefore learning how to make the layout, verify it and ensure that the layout we design is equivalent to the schematic we based it off of.

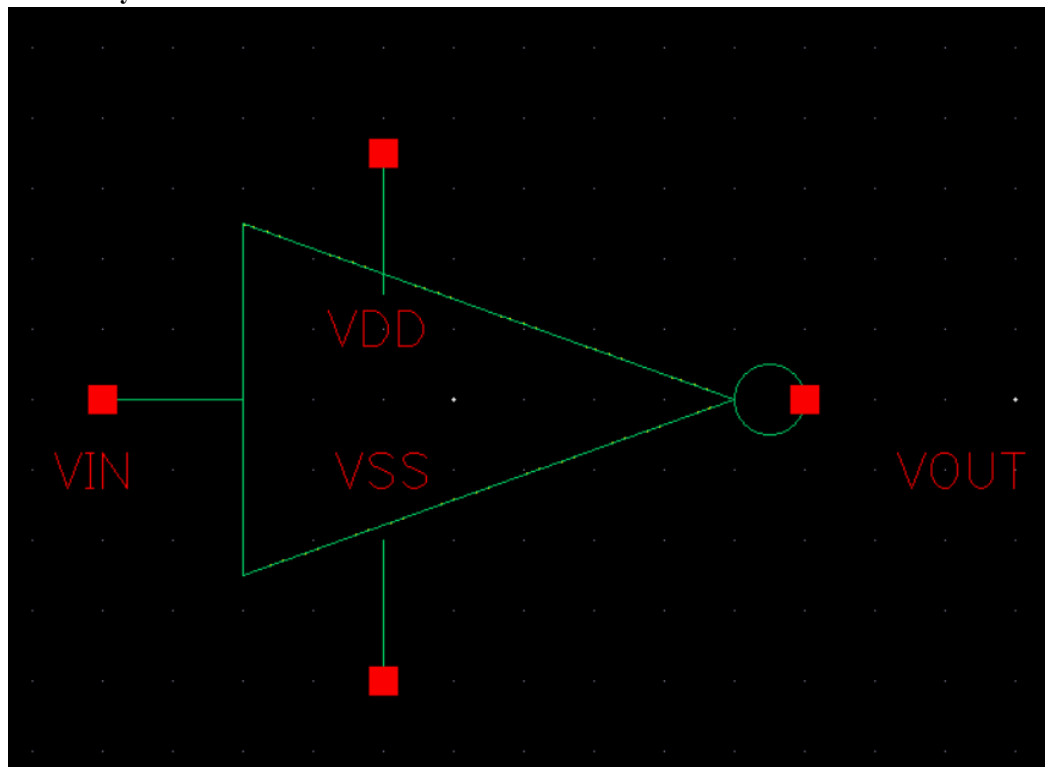
The results showed the layout designed performing slightly worse than the ideal transistor, which is to be expected. You can note that in the rise and fall of the simulations, the layout we designed had a little more "delay" in switching signals. The propagation is most likely due to non-ideal conditions about the layout being performed. However these differences are barely noticeable and will only affect us in higher frequencies when fast mobility is a requirement.

II. SUB-CIRCUIT AND TEST BENCH SCHEMATICS

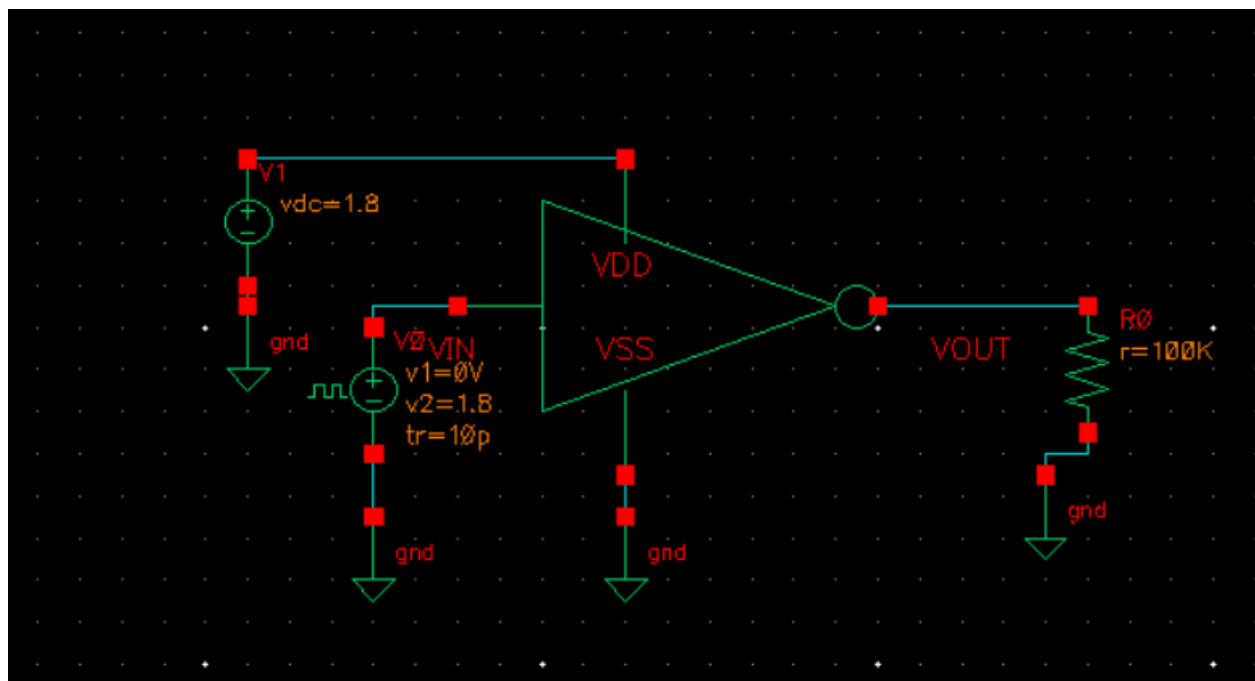
Inverter Schematic



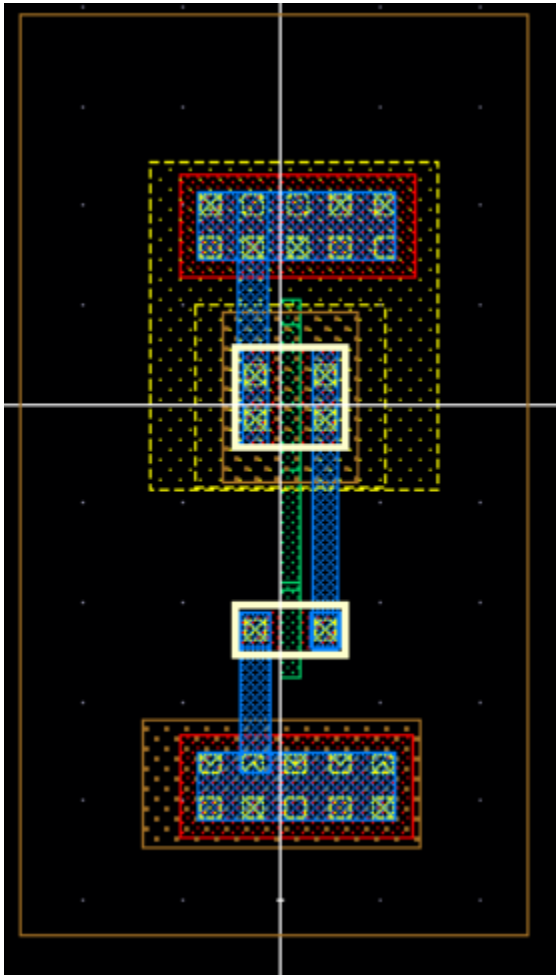
Inverter Symbol



Test bench schematic



III. LAYOUT(S) AND FLOOR PLAN(S)



IV. DRC AND LVS RESULTS

Calibre - RVE v2024.2_29.16 : inverter.drc.results

File View Highlight Tools Window Setup Help

Filter: Show Unresolved inverter, 2 Results (in 2 of 2503 Checks), 2 Waived

Check / Cell	Results
Check GREPDL_RX_minR	1
Check GREPDL_PC_minR	1

Rule File Pathname: _cmhv7sf.drc.cal_
Local PC minimum estimated density with 126 um tiling within (CHIPEDGE, CRACKSTOP), need to be >= 5 %

Calibre Run Completed Successfully -- Results are Valid

Check GREPDL_PC_minR

File Settings Configurations Help

Rules
Inputs
H-Cells
Outputs
ERC
Signatures
Run Control
Search
Transcript
Files

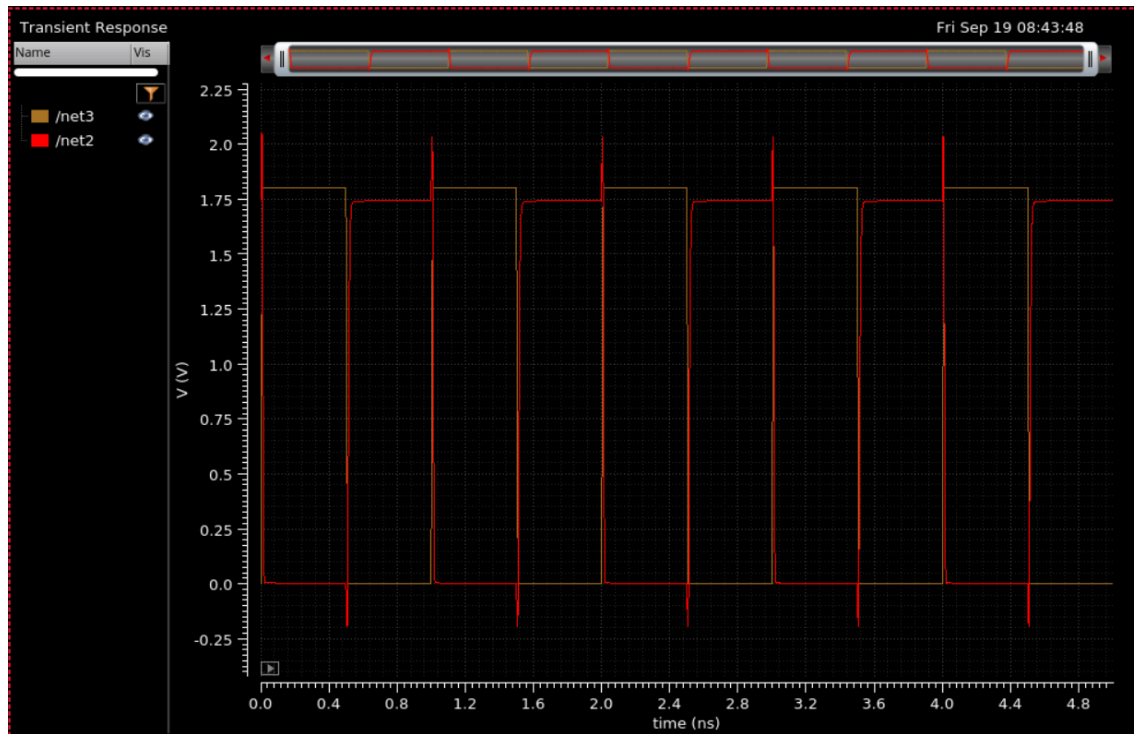
Run LVS
Show RVE

inverter.lvs.report x

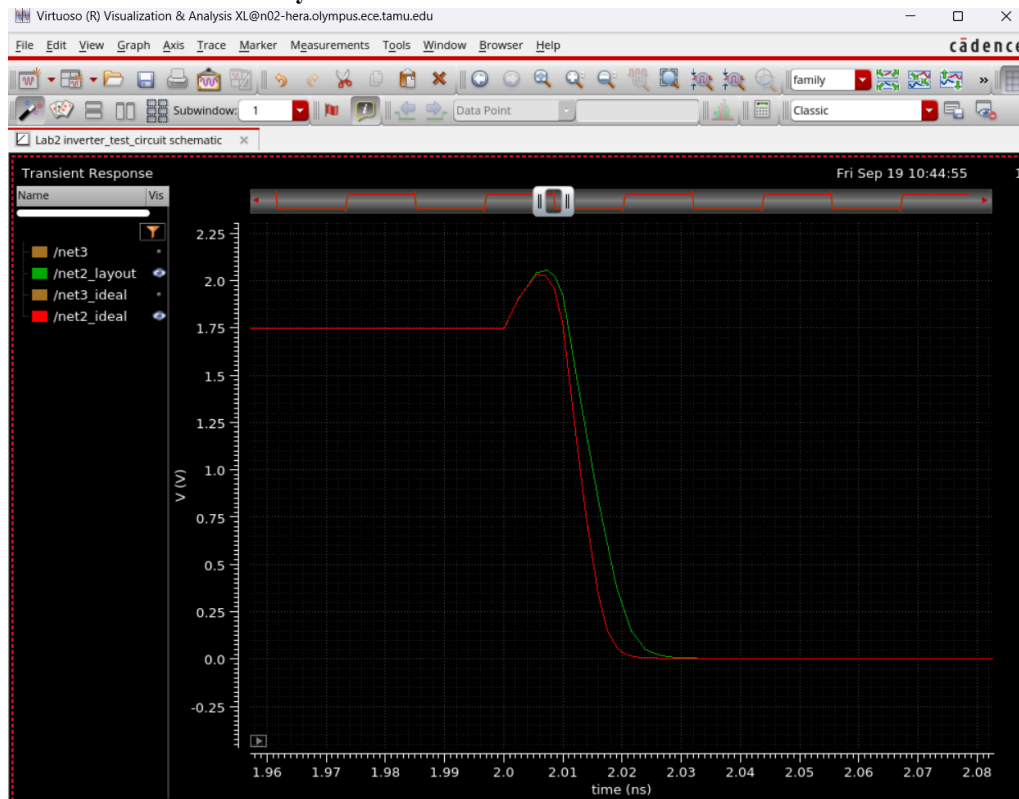
```
##  
## LVS REPORT ##  
##  
#####  
REPORT FILE NAME: inverter.lvs.report  
LAYOUT NAME: inverter.sp ('inverter')  
SOURCE NAME: inverter.src.net ('inverter')  
RULE FILE: _cmhv7sf.lvs.cal_  
CREATION TIME: Fri Sep 19 10:31:42 2025  
CURRENT DIRECTORY: /home/ugrads/s/skywalker499/CAL  
USER NAME: skywalker499  
CALIBRE VERSION: v2024.2_29.16 Thu May 2 07:35:42 PDT 2024  
  
OVERALL COMPARISON RESULTS  
  
# #####  
# # * *  
31 # # # CORRECT # |  
32 # # #  
33 # #####
```

VI. SIMULATION RESULTS

Before layout design



Fall difference between layout and ideal



Rise difference between layout and ideal

