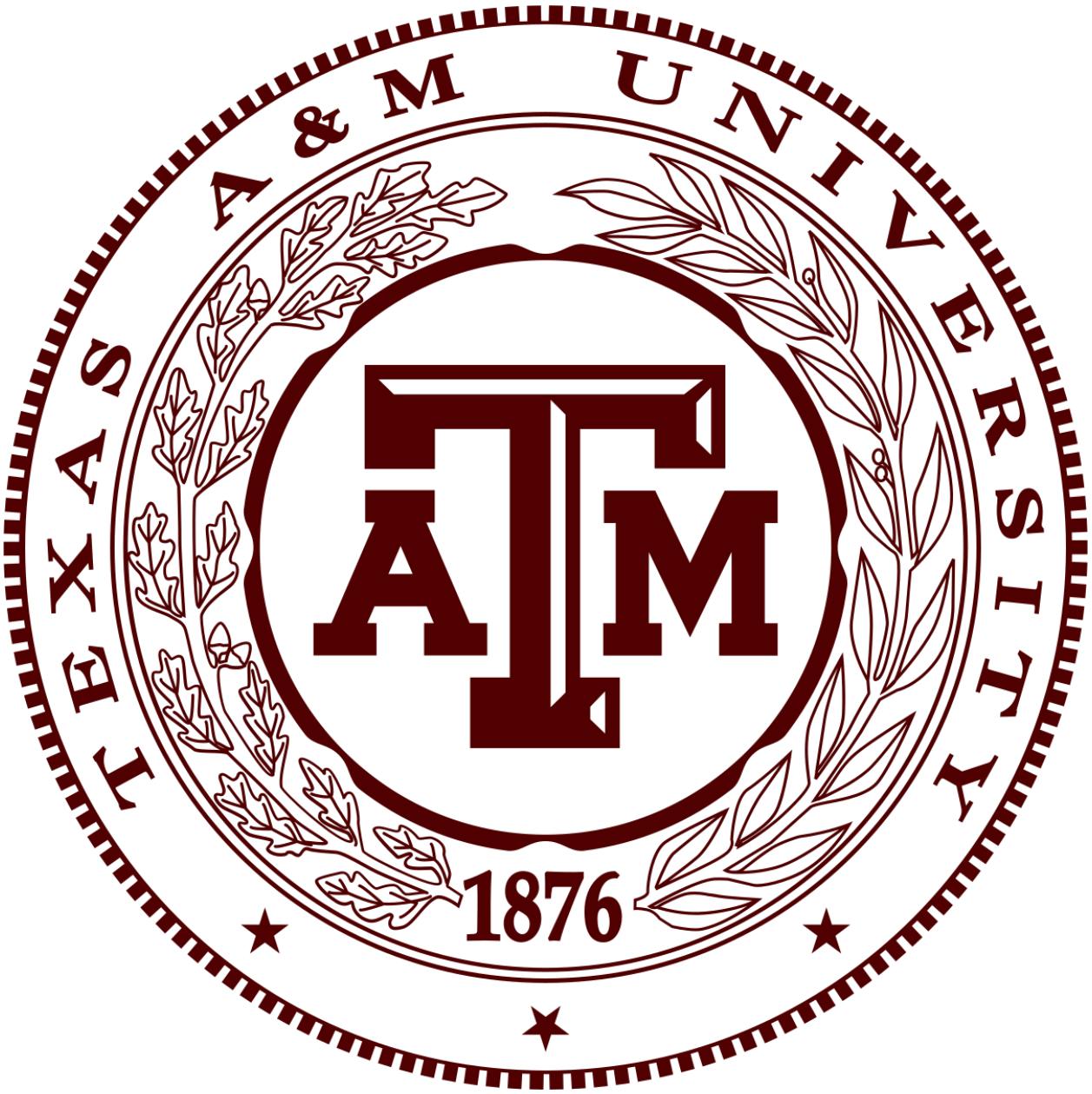


ECEN 454 - Lab 4 Report

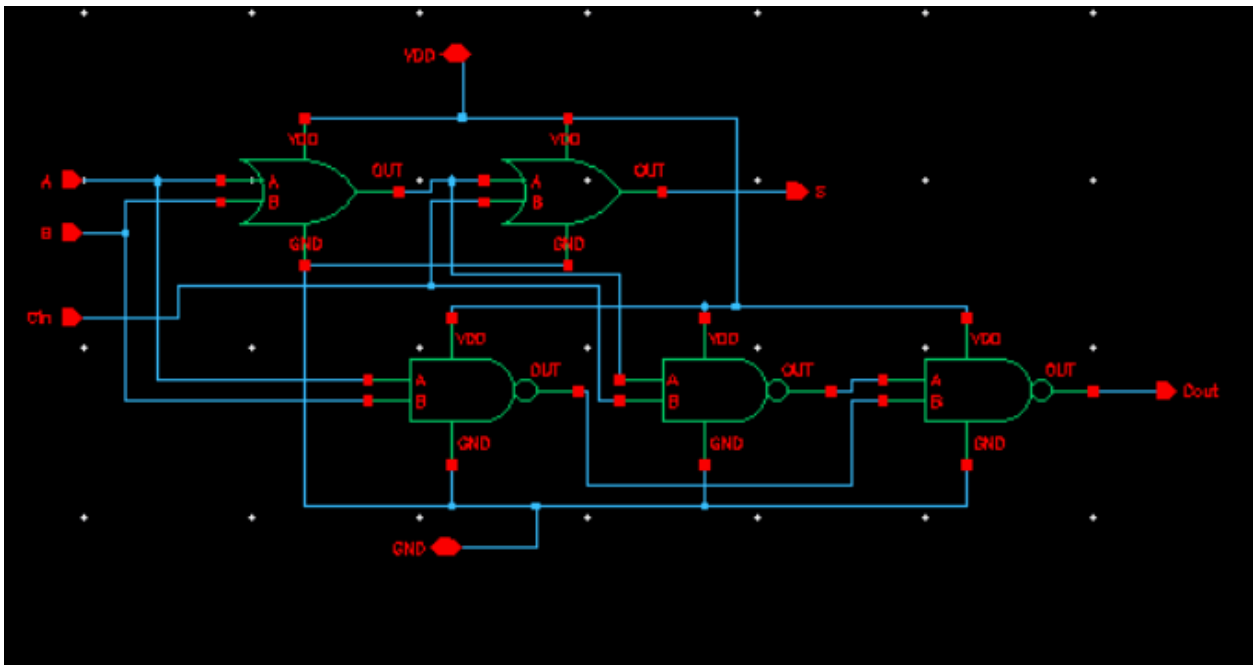
Luke Lopez

Report

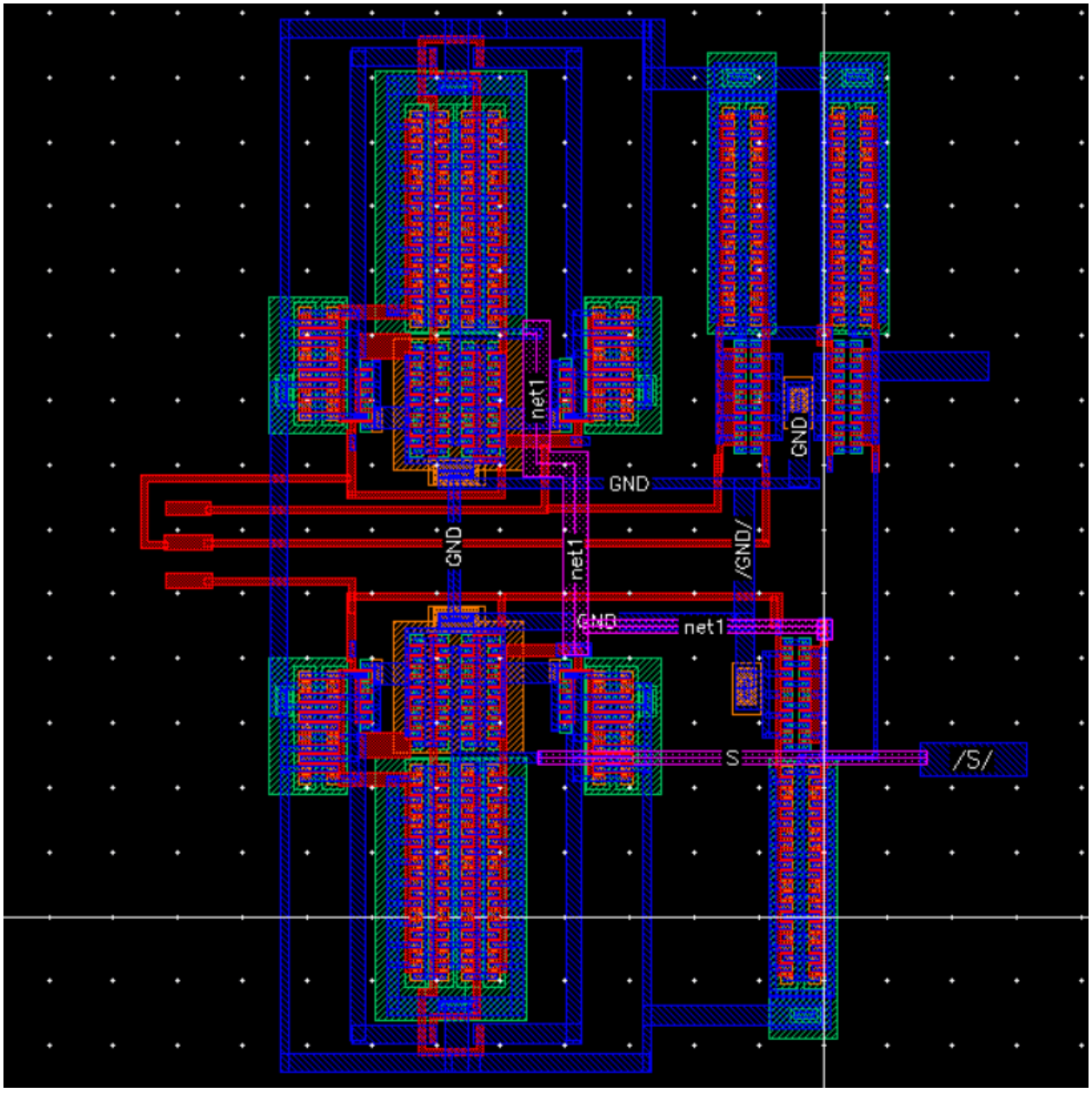
Some changes have been made to the fundamental circuit designs, to see these changes and the new models, see **Appendix A** at the bottom of this report.

1 Bit adder

Schematic



Layout



DRC

```
DRC started.......Wed Oct 22 22:21:31 2025
    completed ....Wed Oct 22 22:21:31 2025
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "1bAdder layout"   *********
   Total errors found: 0
```

LVS

```
Compiling Diva LVS rules...

    Net-list summary for /home/ugrads/s/skywalker499/454-ECEN/LVS/layout/netlist
       count
        40              nets
        7               terminals
        360             pmos
        164             nmos

    Net-list summary for /home/ugrads/s/skywalker499/454-ECEN/LVS/schematic/netlist
       count
        25              nets
        7               terminals
        18              pmos
        18              nmos


    Terminal correspondence points
    N36       N2        A
    N35       N5        B
    N37       N6        Cin
    N38       N4        Cout
    N33       N1        GND
    N34       N3        S
    N39       N0        VDD

Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.
```

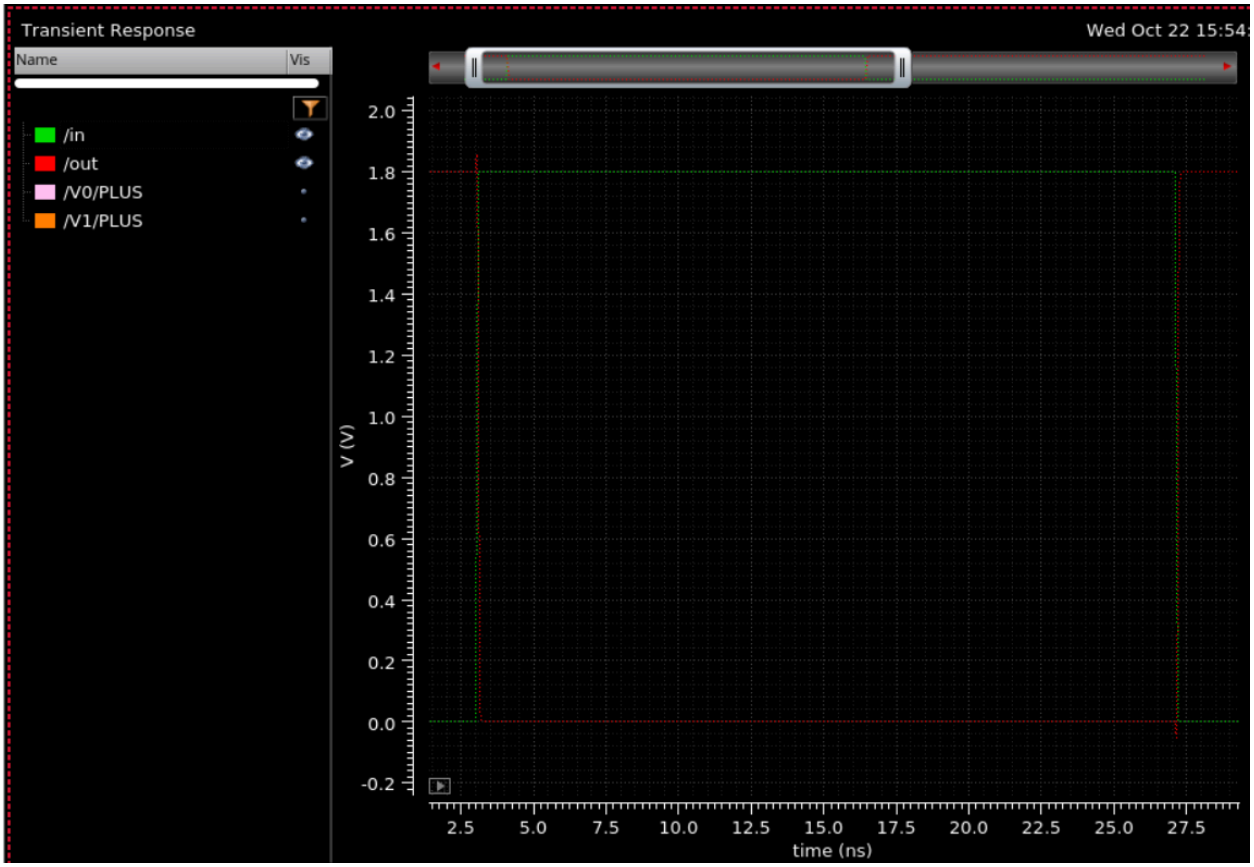
Rising and Falling Delays

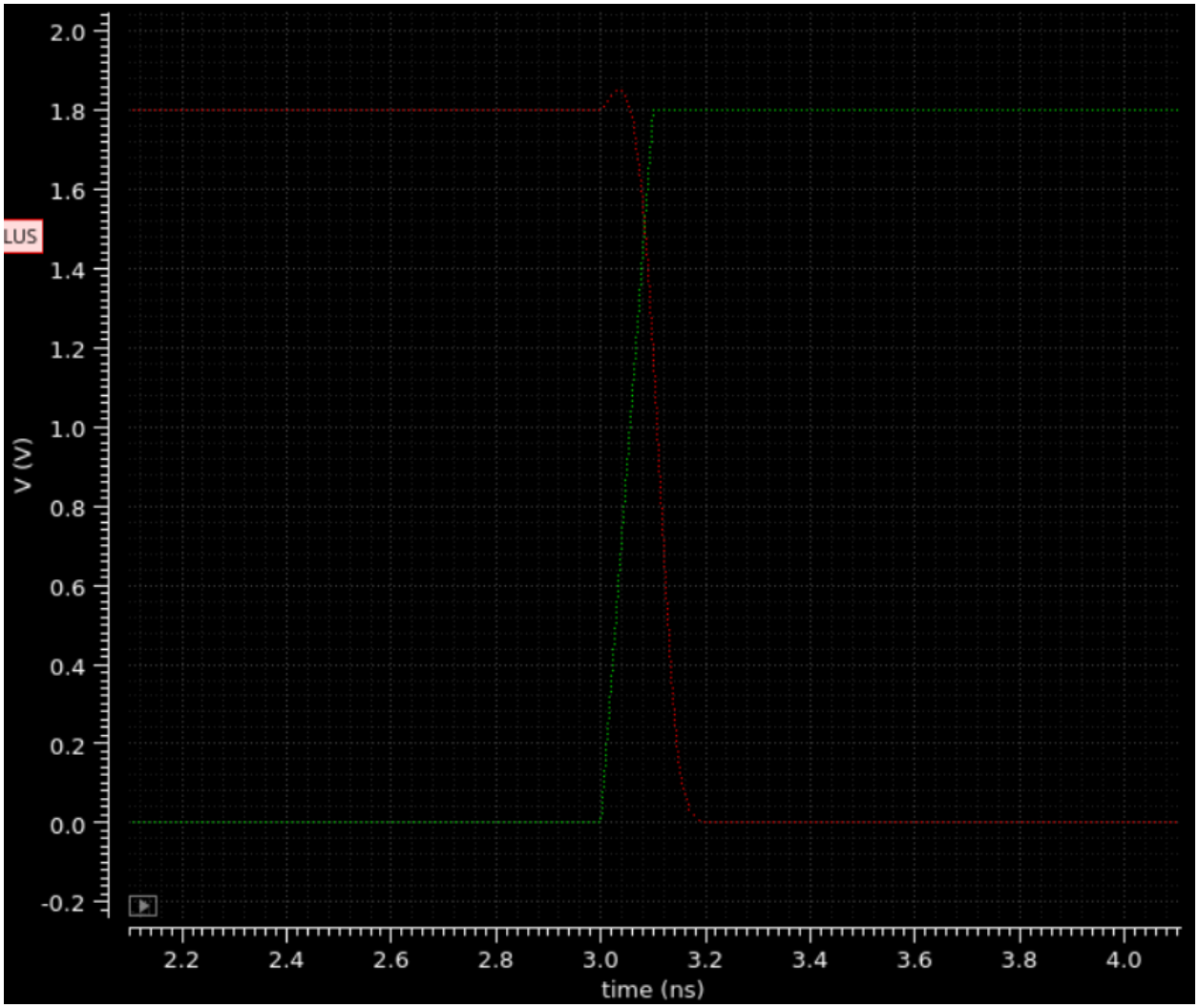
Device	Rising Delay	Falling Delay	Error
Inverter	60.65 ps	55.15 ps	9.97%
NAND2	425.1 ps	486.3 ps	7.56%
XOR2	152 ps	147 ps	3.4%

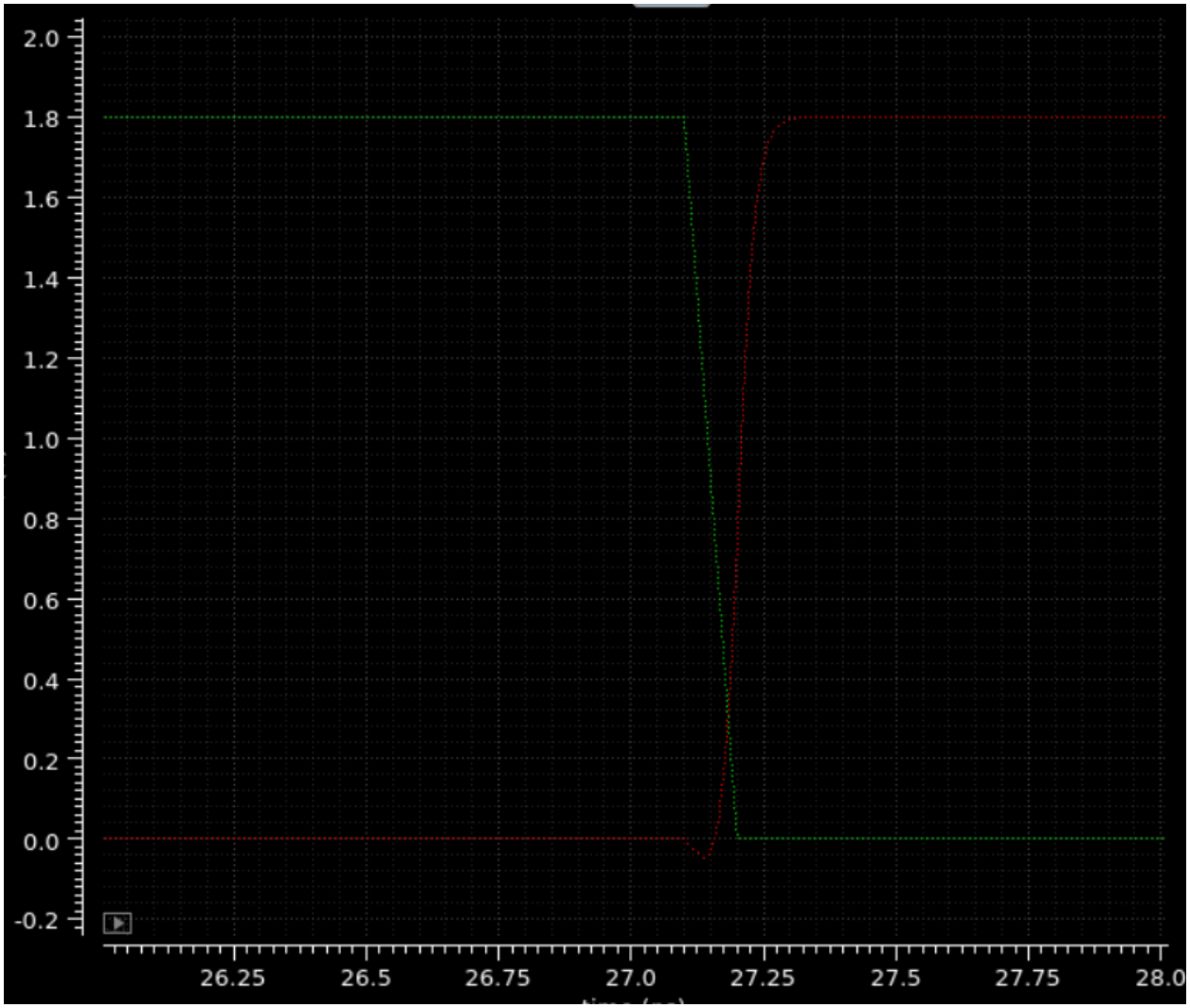
1bAdder	Rising	Fall
S	178 ps	165.8 ps
Cout	139.4 ps	129.7 ps

Waveform of outputs

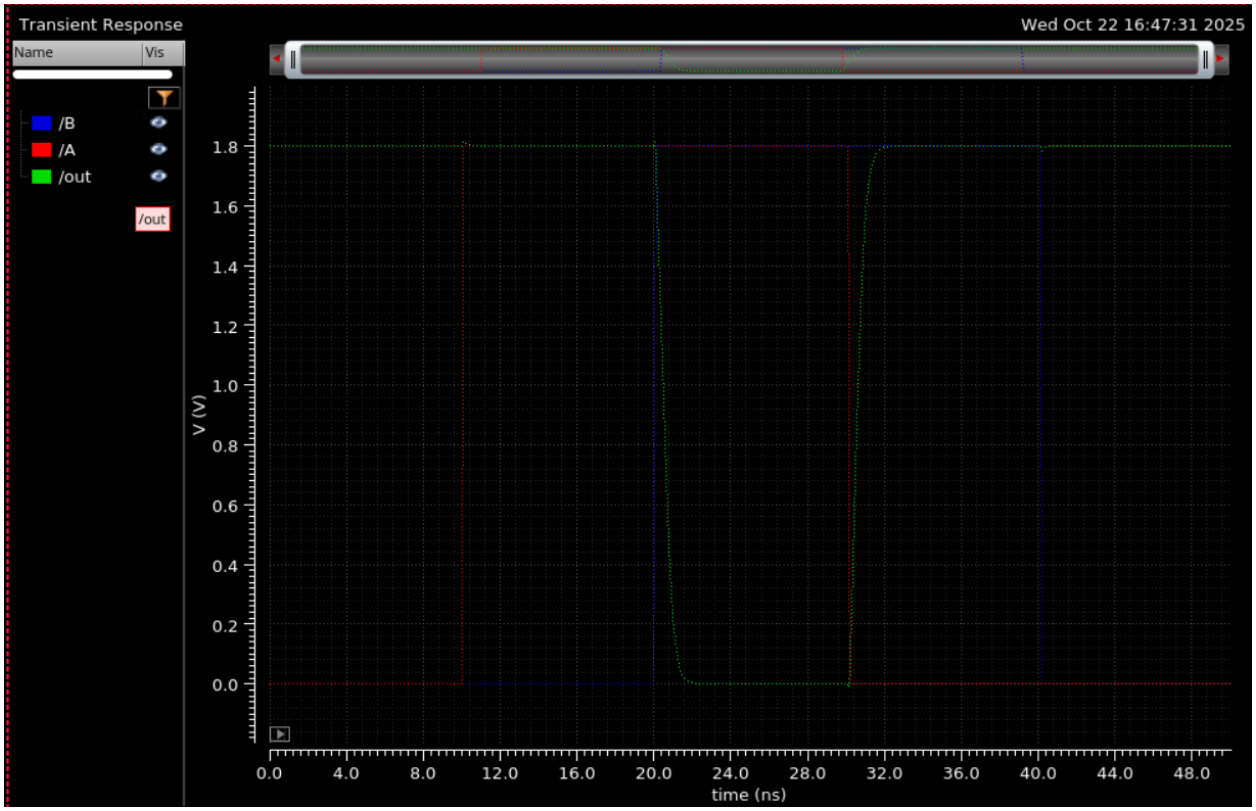
Inverter



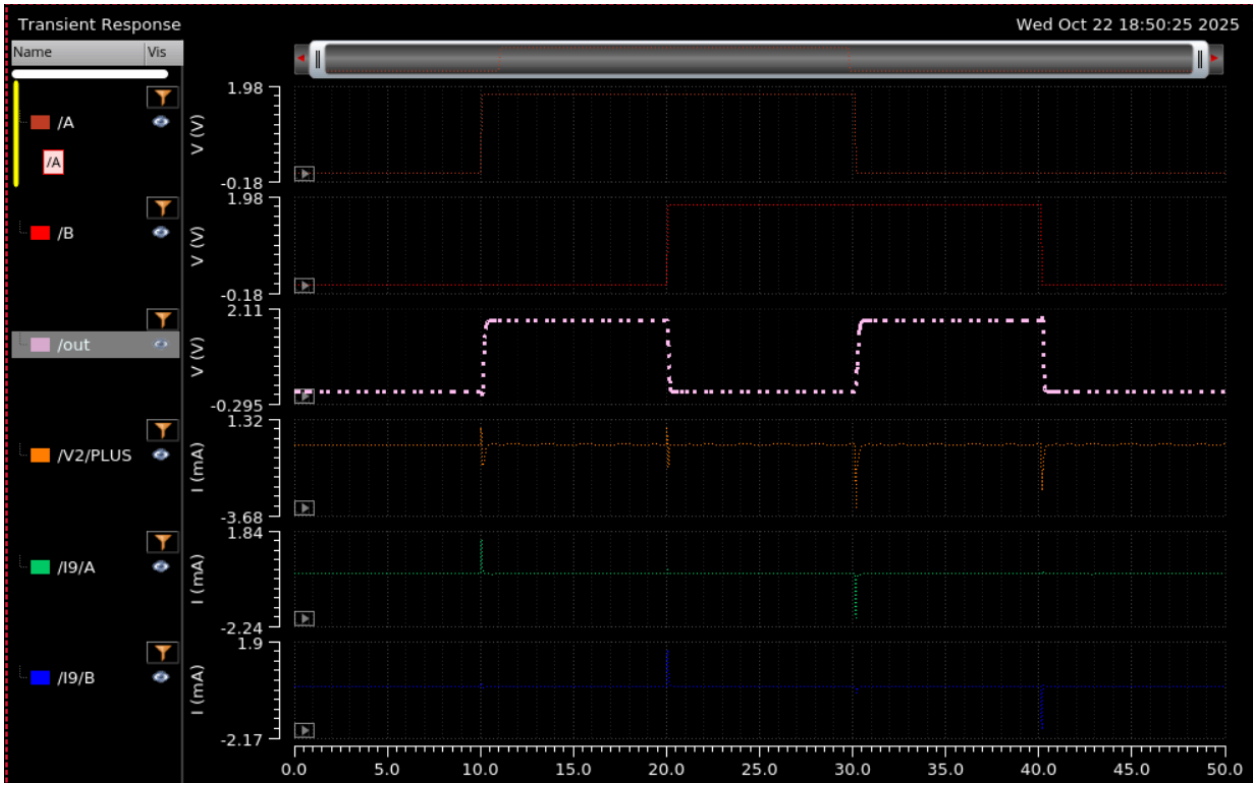

LUS
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
V (V)
2.2
2.4
2.6
2.8
3.0
3.2
3.4
3.6
3.8
4.0
time (ns)


2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
26.25
26.5
26.75
27.0
27.25
27.5
27.75
28.0

NAND2


Transient Response
Wed Oct 22 16:47:31 2025
Name
Vis
/B
/A
/out
/out
V (V)
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
0.0
4.0
8.0
12.0
16.0
20.0
24.0
28.0
32.0
36.0
40.0
44.0
48.0
time (ns)

XOR2

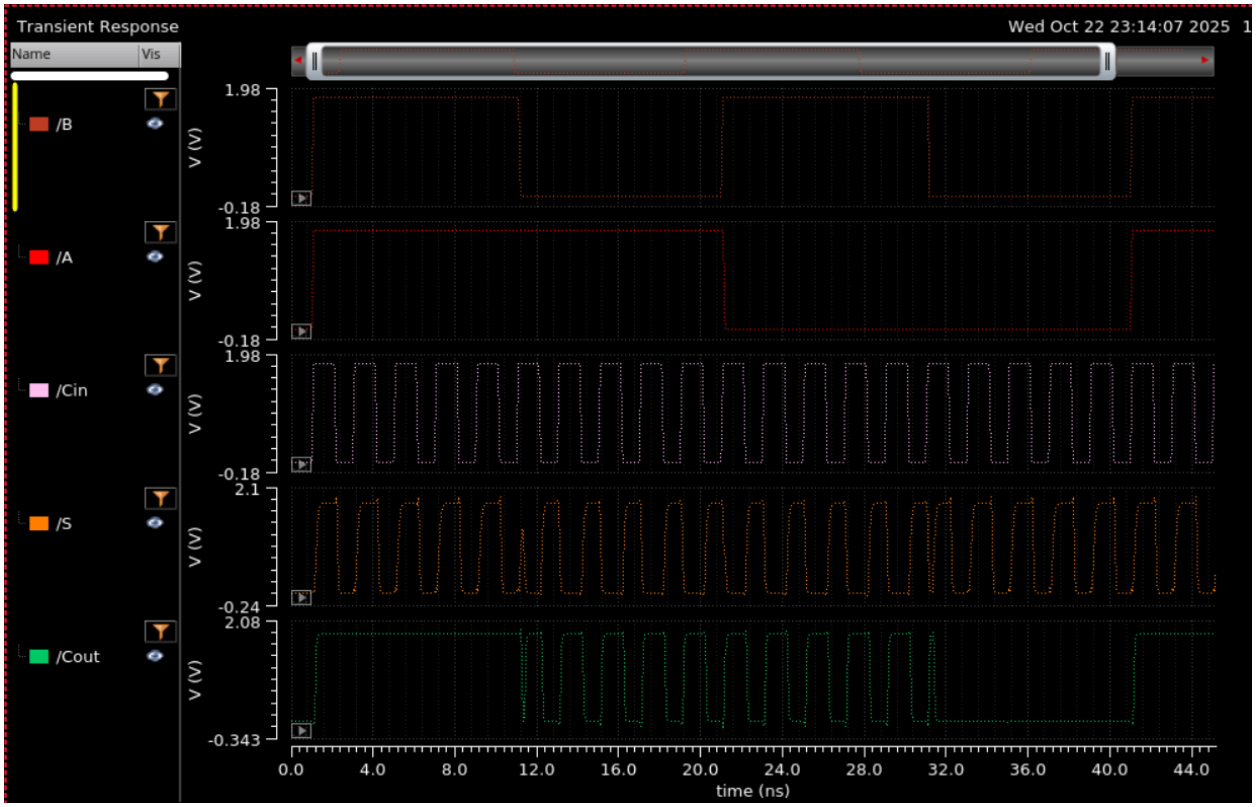


1 Bit adder

Power Dissipations

Device	Power of Vdd	Power A	Power B	Power Cin
Inverter	5.103 uW	0.813 uW	N/A	N/A
NAND2	68.61 uW	0.565 nW	34.03 nW	N/A
XOR2	25.34 uW	0.01122 uW	0.01202 uW	N/A
1 Bit Adder	80.5 uW	0.25 uW	0.33 uW	0.576 uW

Maximum Frequency : 1/2ns = 500 MHz



Note: there are some anomalies when two signals are changing not at the same time, but their values overlap. However it can be seen that when the signals change at the same time (like when a clock is implemented) the system works fine.

APPENDIX A: Changes to previous systems

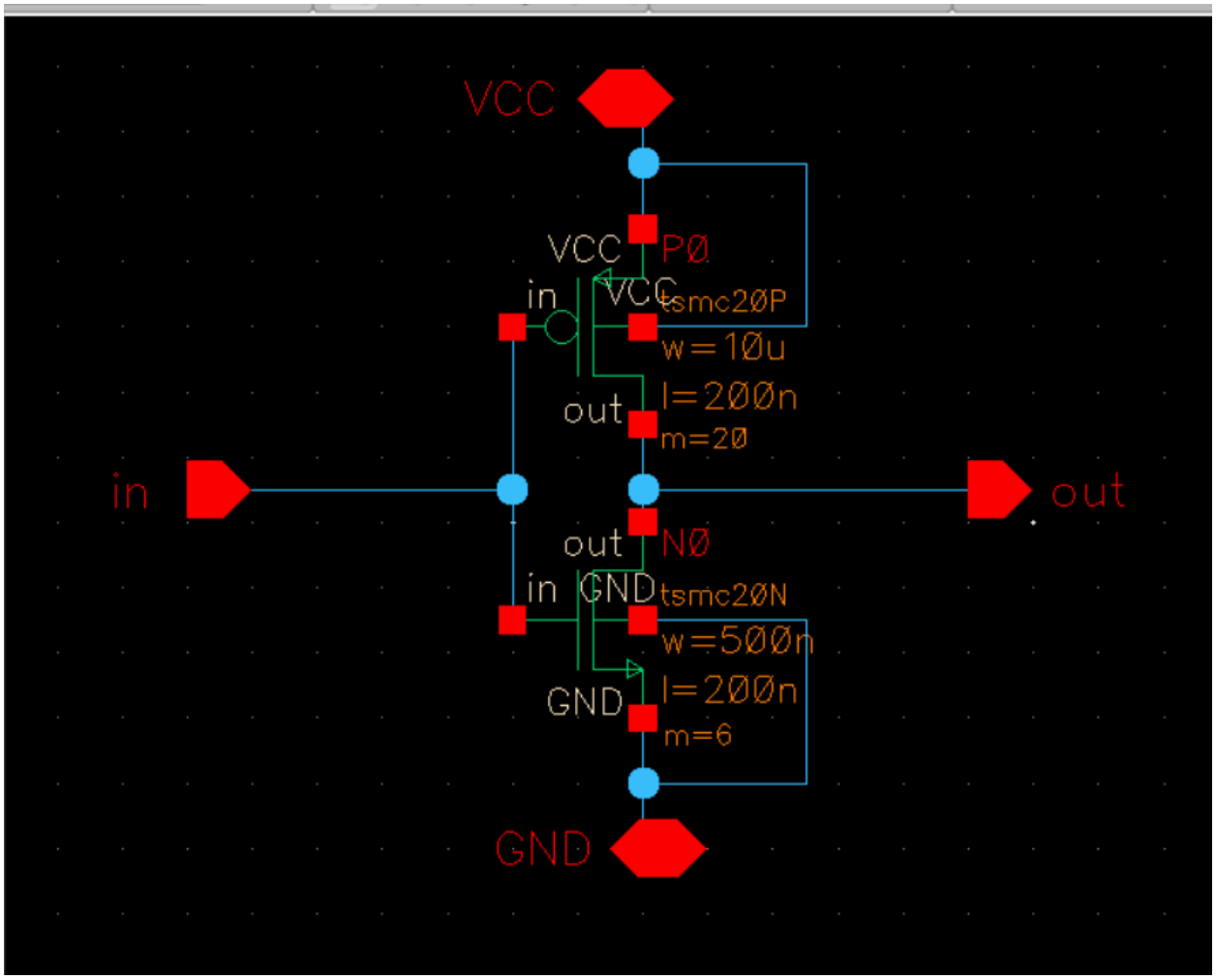
Notes on changes:

All lengths are the same at **0.2u m**
Additionally, to increase the speed, and maximum frequency, I reduced the capacitance of the transistors by having an intertwined layout design, where some transistors share drains or sources. This reduces the total capacitance area of the transistors. This is easily seen in the layout pictures.

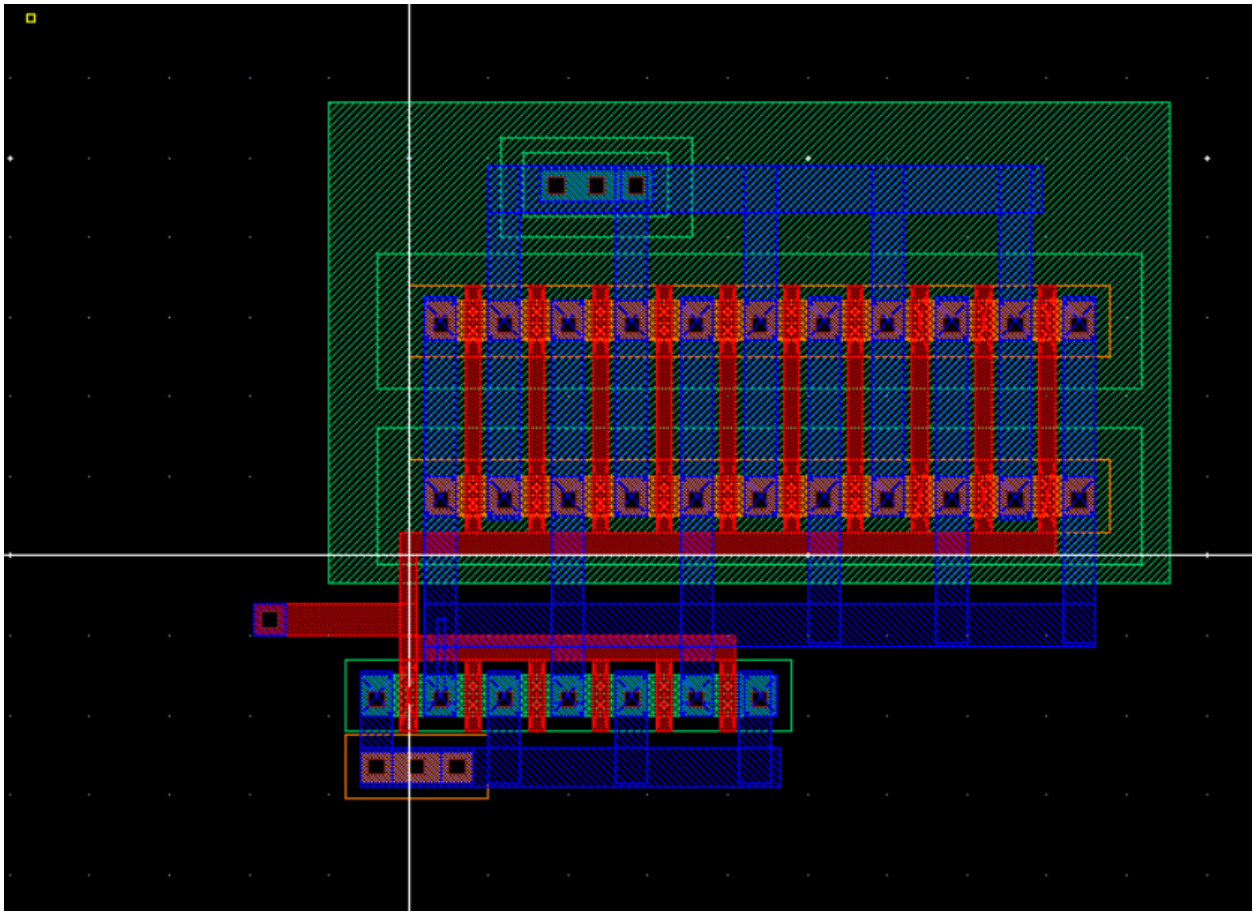
Device	Pmos	Nmos
XOR	10u	3u
Inverter	10u	3u
NAND	10u	5u

Inverter

Schematic



Layout



DRC

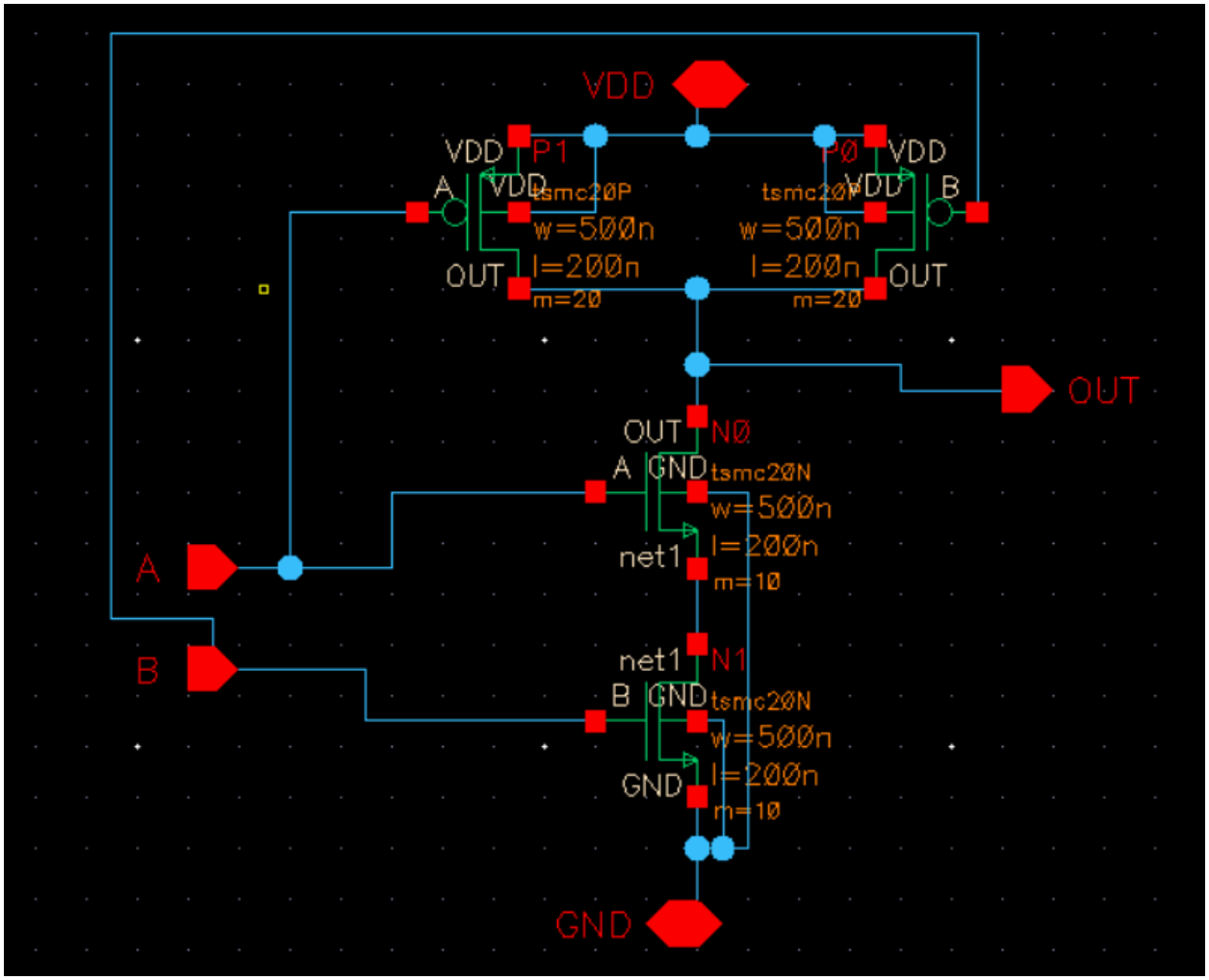
```
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Wed Oct 22 15:31:34 2025
    completed ....Wed Oct 22 15:31:34 2025
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "inverter layout"   *********
   Total errors found: 0
```

LVS

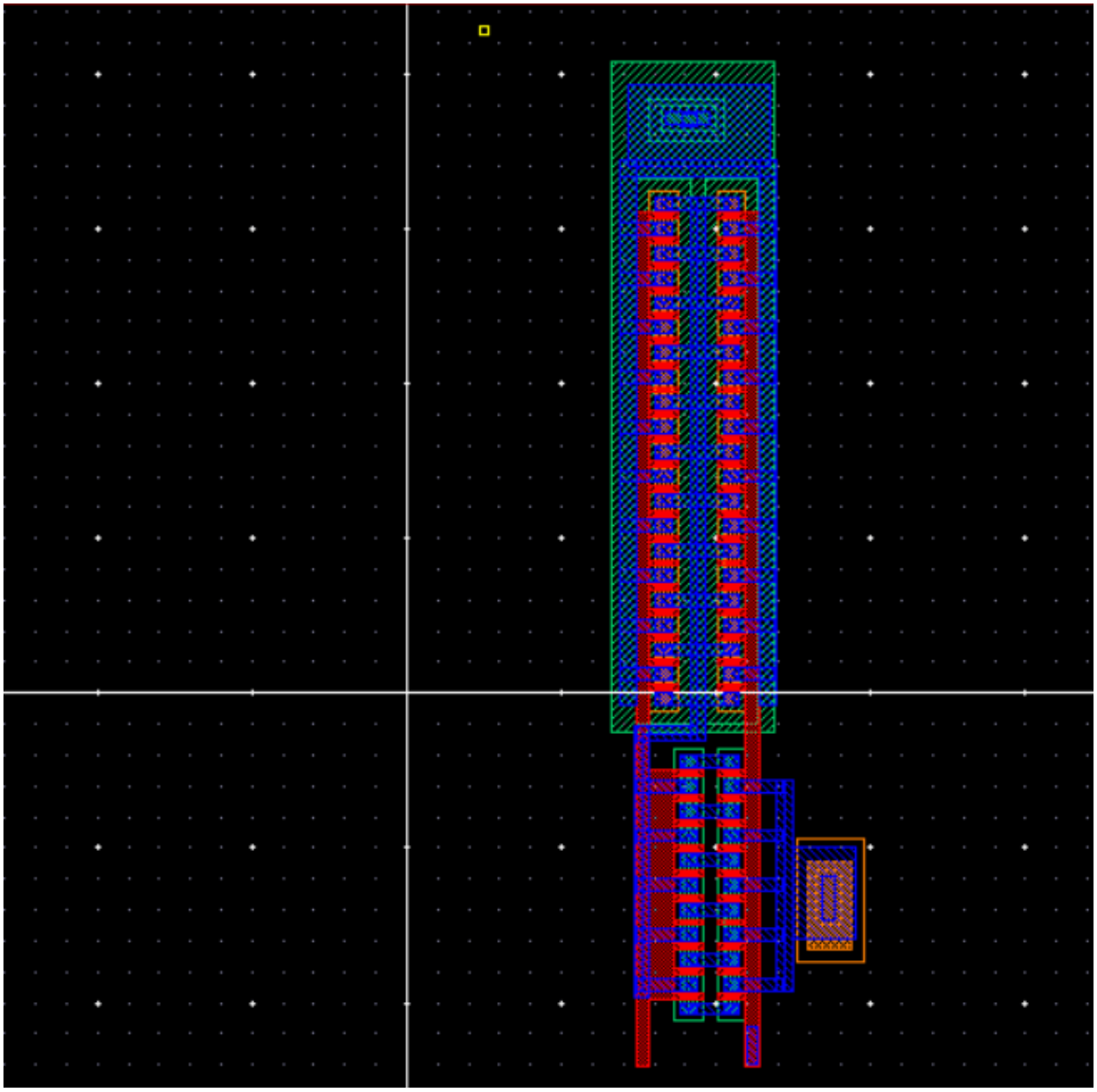
```
Compiling Diva LVS rules...

    Net-list summary for /home/ugrads/s/skywalker499/454-ECEN/LVS/layout/netlist
       count
         4               nets
         4               terminals
         20              pmos
         6               nmos

    Net-list summary for /home/ugrads/s/skywalker499/454-ECEN/LVS/schematic/netlist
       count
         4               nets
         4               terminals
         1               pmos
         1               nmos


    Terminal correspondence points
    N1          N1          GND
    N0          N0          VCC
    N3          N3          in
    N2          N2          out

Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.
```

NAND2

Schematic


VDD
VDD
P1
A
VDD
tsmc20P
w=500n
l=200n
OUT
m=20
P0
VDD
VDD
B
tsmc20P
w=500n
l=200n
OUT
m=20
OUT
OUT
N0
A
GND
tsmc20N
w=500n
l=200n
m=10
net1
A
B
net1
N1
B
GND
tsmc20N
w=500n
l=200n
m=10
GND
GND

Layout



DRC

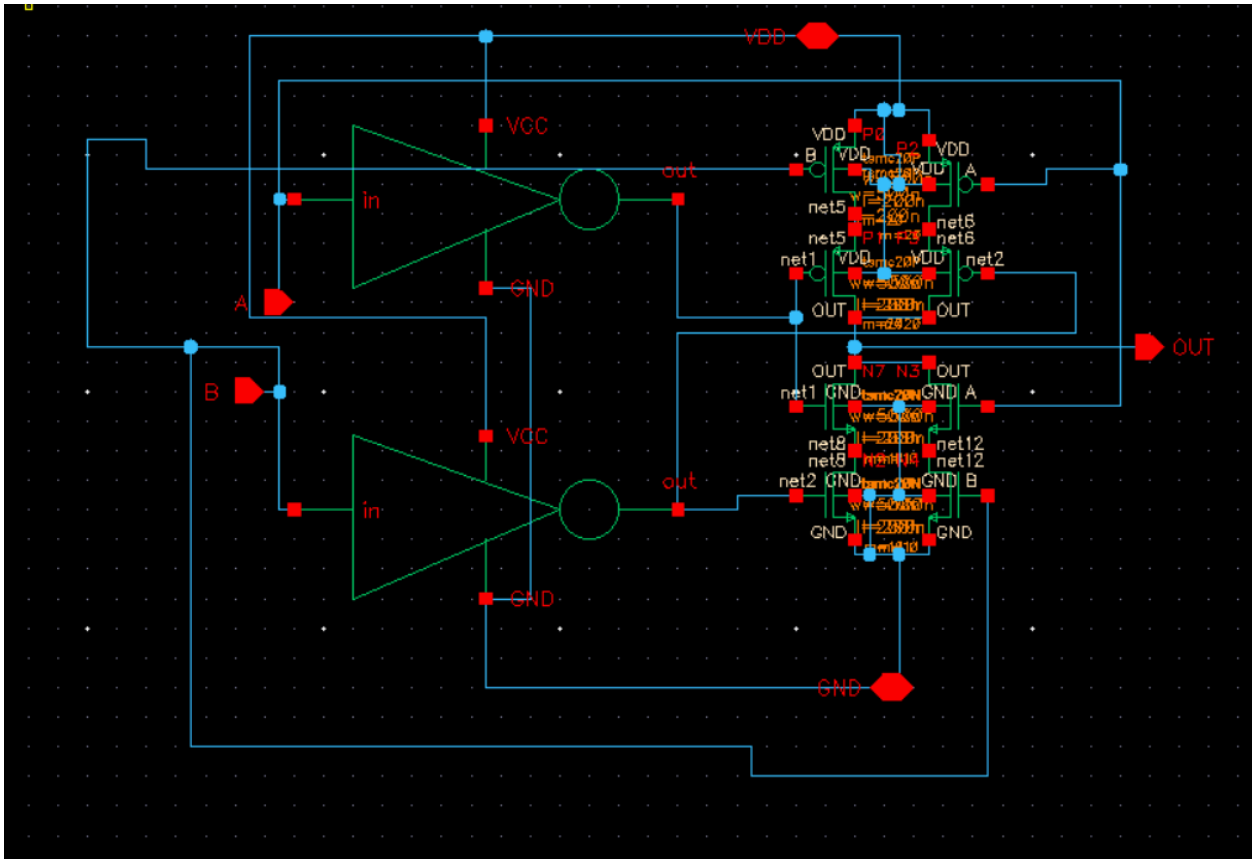
```
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Wed Oct 22 15:39:43 2025
    completed ....Wed Oct 22 15:39:43 2025
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "NAND2 layout"   *********
   Total errors found: 0
```

LVS

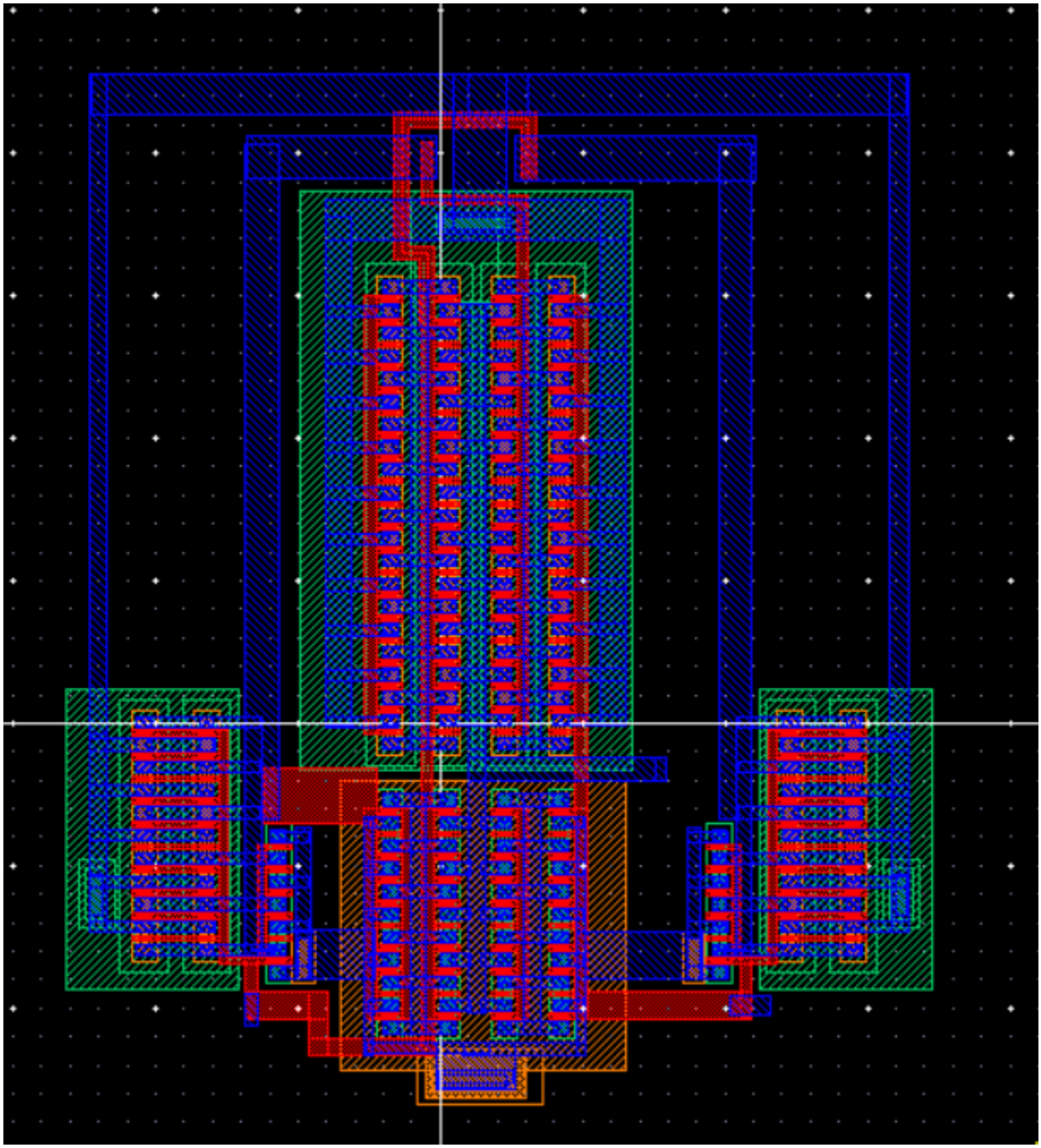
```
Compiling Diva LVS rules...

    Net-list summary for /home/ugrads/s/skywalker499/454-ECEN/LVS/layout/netlist
       count
        4               nets
        4               terminals
        20              pmos
        6               nmos

    Net-list summary for /home/ugrads/s/skywalker499/454-ECEN/LVS/schematic/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos


    Terminal correspondence points
    N1          N1          GND
    N0          N0          VCC
    N3          N3          in
    N2          N2          out

Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.
```

XOR2

Schematic



Layout



DRC

```
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Wed Oct 22 15:45:09 2025
    completed ....Wed Oct 22 15:45:09 2025
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "XOR2 layout"   *********
   Total errors found: 0
```

LVS

```
Compiling Diva LVS rules...

    Net-list summary for /home/ugrads/s/skywalker499/454-ECEN/LVS/layout/netlist
       count
         4               nets
         4               terminals
         20              pmos
         6               nmos

    Net-list summary for /home/ugrads/s/skywalker499/454-ECEN/LVS/schematic/netlist
       count
         4               nets
         4               terminals
         1               pmos
         1               nmos


    Terminal correspondence points
    N1          N1          GND
    N0          N0          VCC
    N3          N3          in
    N2          N2          out

Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.
```

APPENDIX B: General Calculator input used

Delay_F

value(delay(?wf1 v("/out" ?result "tran") ?value1 0.9 ?edge1 "rising" ?nth1 1 ?td1 0.0 ?tol1 nil ?wf2 v("/A" ?result "tran") ?value2 0.9 ?edge2 "falling" ?nth2 1 ?tol2 nil ?td2 nil ?stop nil ?period1 1 ?period2 1 ?multiple t ?xName "trigger") 0)

Delay_R

value(delay(?wf1 v("/out" ?result "tran") ?value1 0.9 ?edge1 "falling" ?nth1 1 ?td1 0.0 ?tol1 nil ?wf2 v("/B" ?result "tran") ?value2 0.9 ?edge2 "rising" ?nth2 1 ?tol2 nil ?td2 nil ?stop nil ?period1 1 ?period2 1 ?multiple t ?xName "trigger") 0)

Power_vdd
(average(i("/V2/PLUS" ?result "tran")) * 1.8)

Power_A
(average(i("/I1/A" ?result "tran")) * average(v("/A" ?result "tran")))

Power_B
(average(i("/I1/B" ?result "tran")) * average(v("/B" ?result "tran")))