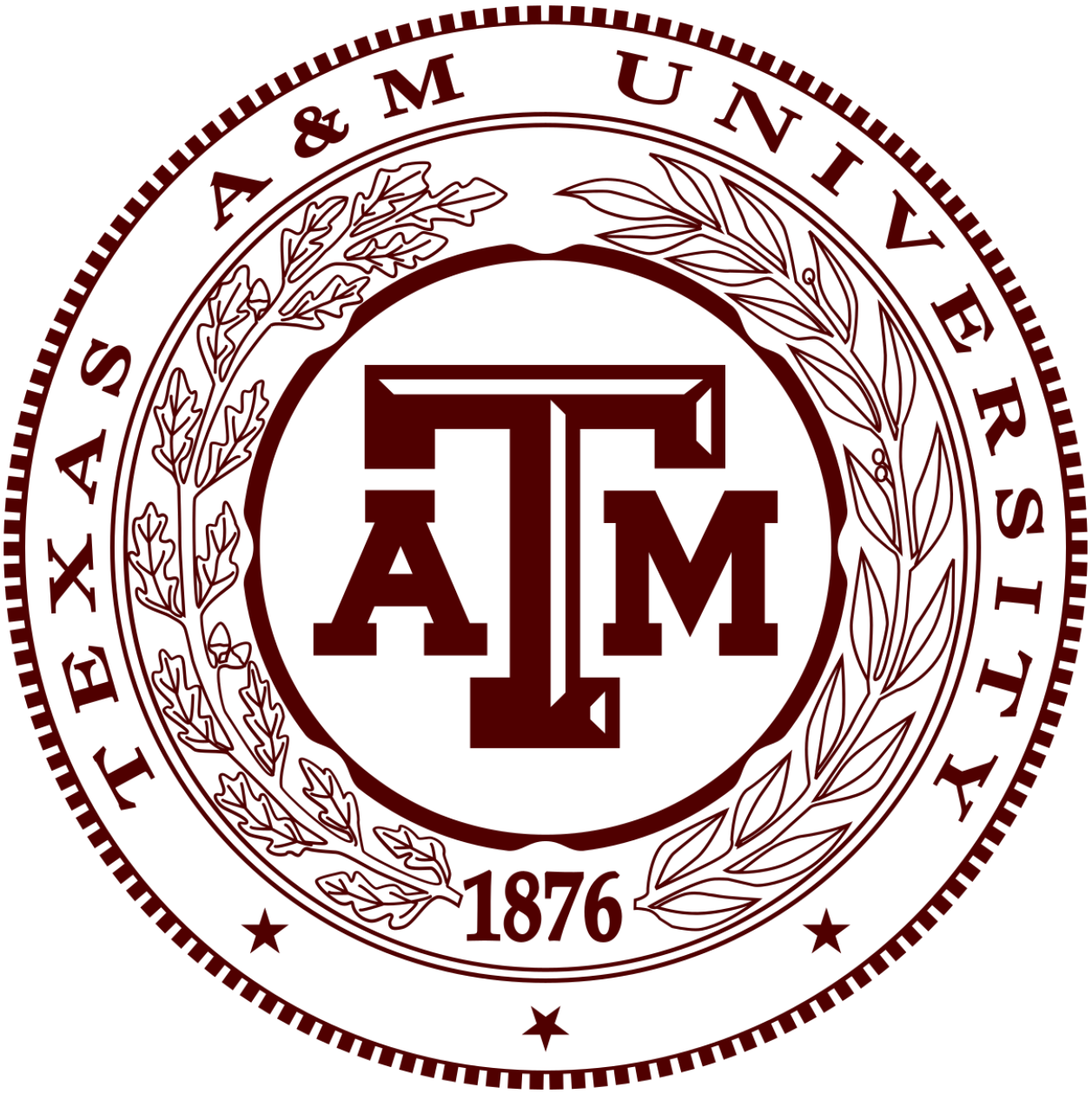
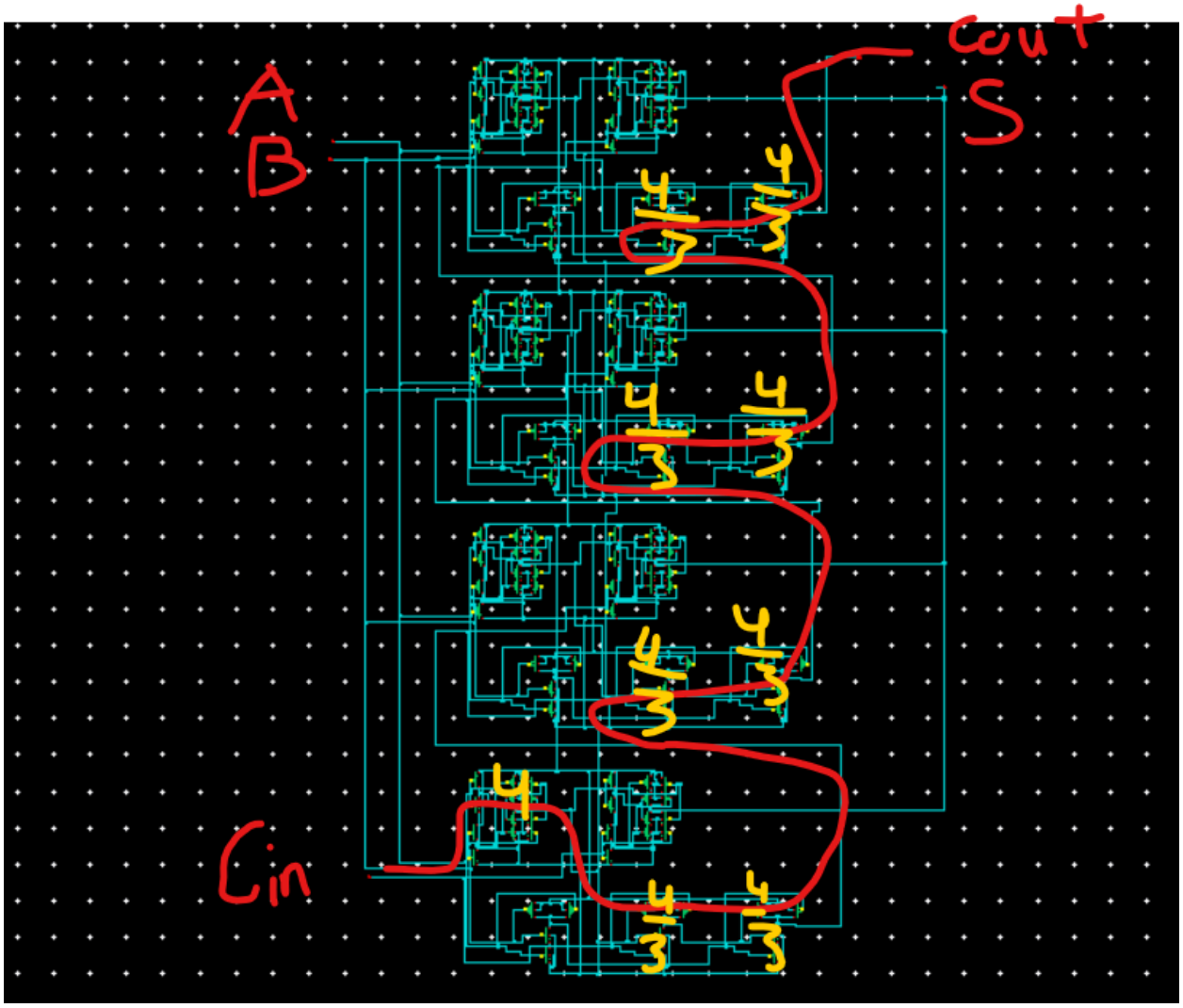


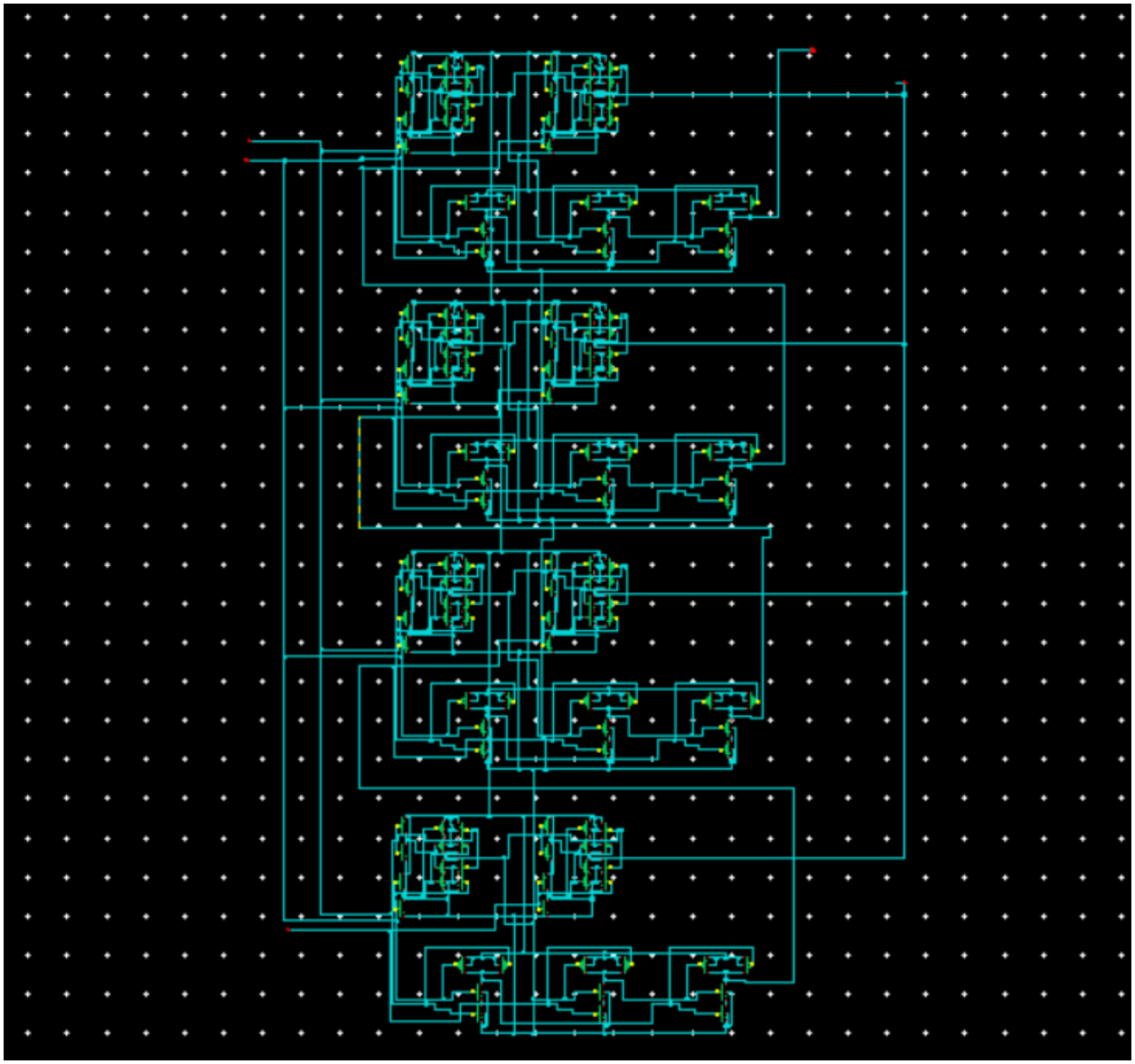
ECEN 454 - Lab 9 Report

Luke Lopez

Delay Route



Schematics



Calculation of G

G = ∏ gi (i = 1, 2, 3, 4, ..., 9)

$G = 4 * (\frac{4}{3})^{8}$ = 40

H = C_load / C_xor

= 30 fF / 2 fF

= 15

b1 = (C_xor + C_nand2) / C_xor

= (2 fF + 2 fF) / 2 fF
= 2

b2, b4, b6, b8 = (C_xor + C_nand2) / C_nand2
= (2 fF + 2 fF) / 2 fF
= 2

b3, b5, b7, b9 = 1

B = b1 × b2 × b3 × b4 × b5 × b6 × b7 × b8 × b9
= 2 × 2 × 1 × 2 × 1 × 2 × 1 × 2 × 1
= 2^5
= 32

Calulations

G	40
H	15
B	32

GHB = 19200 = F

$F^{1/9} = 2.99$ which is within bounds of what we desired, so no resizing necessary.

The transistors were all ideally sized using techniques learned in lecture. The base w/l = 500n/200. With W having a multiplier of 10 as a base. Then ideally sizing them for each stage.