

# ECEN 474/704: Lab 08

## Transconductance Amplifier

Luke Lopez

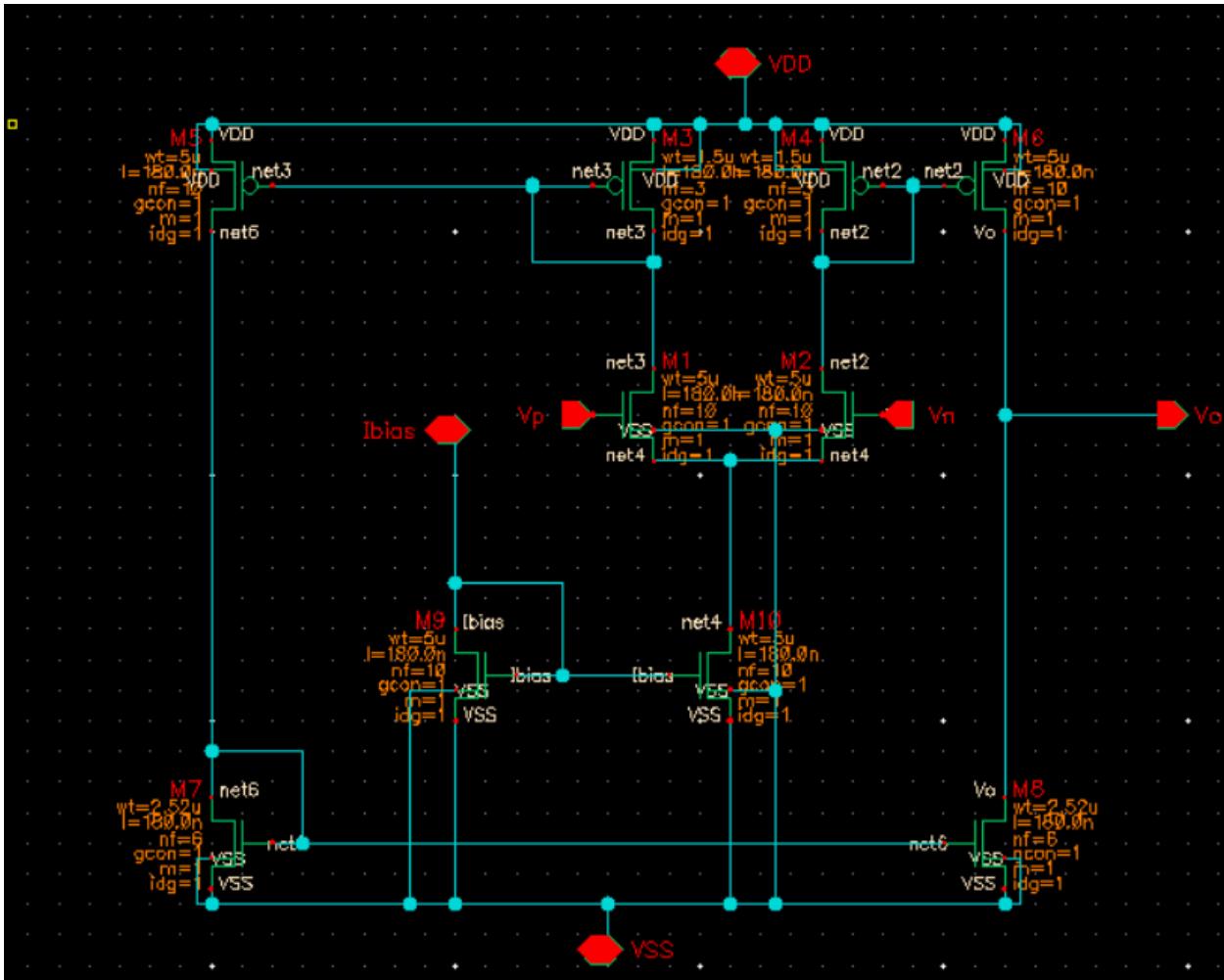
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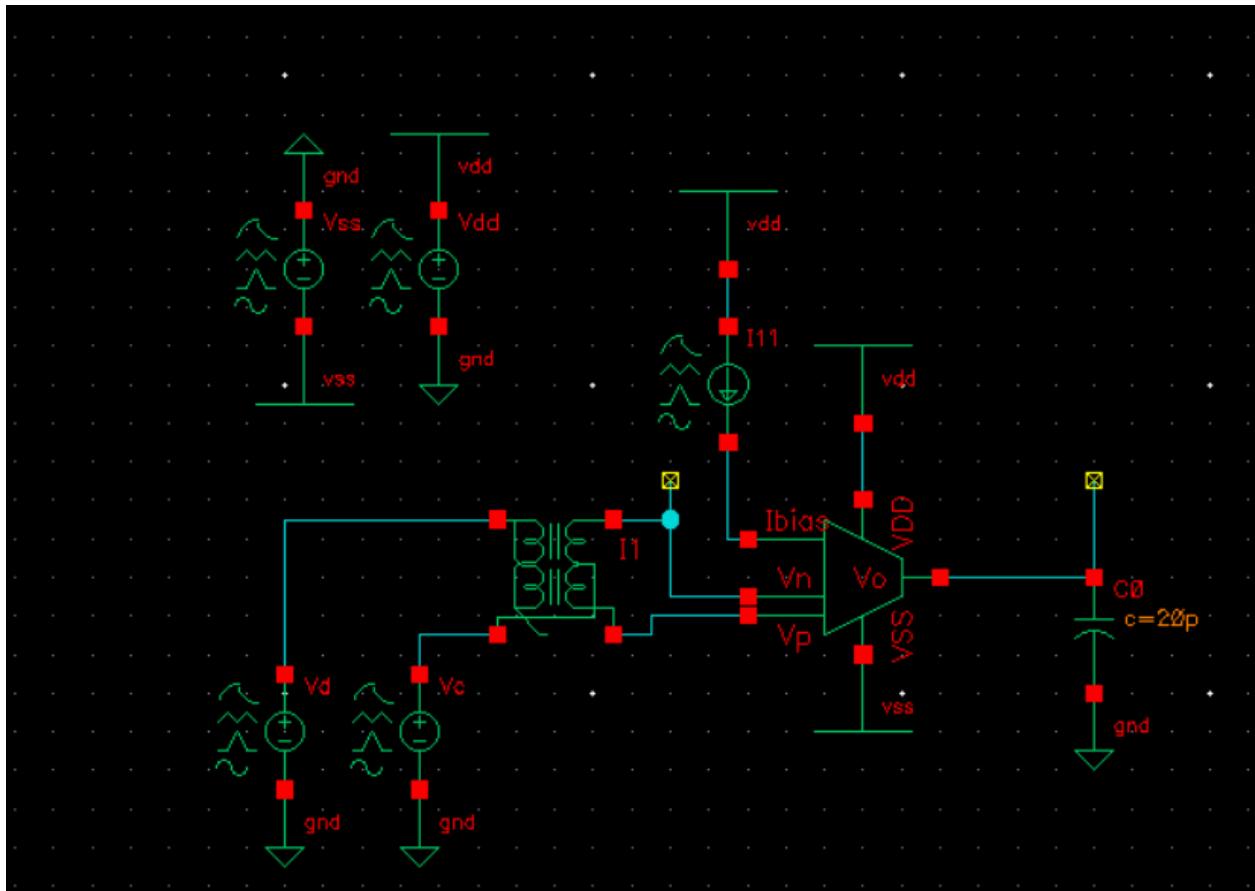
Due date: 11/21/25

### I. DISCUSSION OF THE LAB AND RESULTS

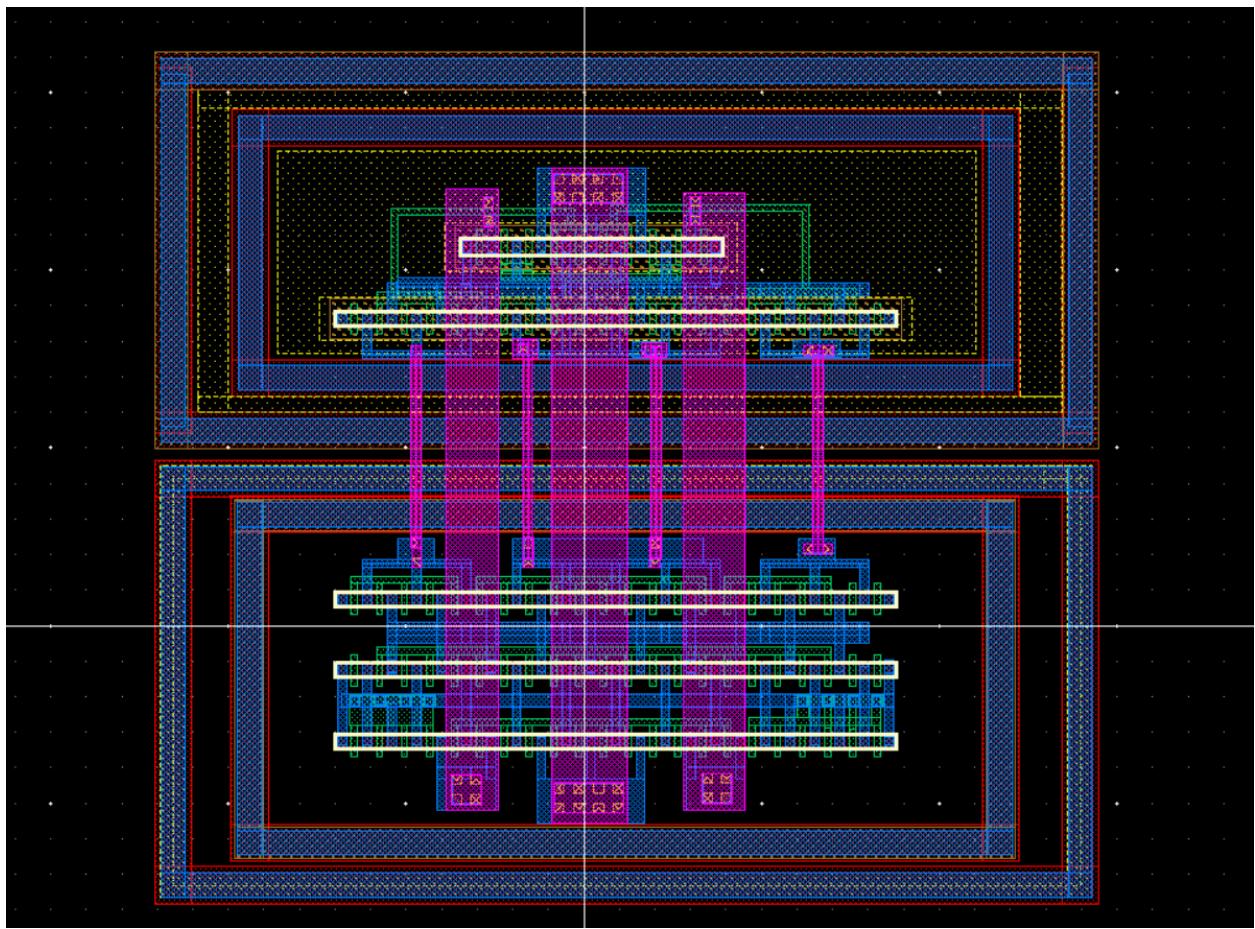
The purpose of this lab was to attain familiarity with OTA circuits. These are powerful since they can allow us to manipulate our transconductance of circuits and are very similar to gain amplifiers. The main design choices will be the ratio of a couple transistors and the desired output current.

### III. SUB-CIRCUIT AND TEST BENCH SCHEMATICS





#### IV. LAYOUT(S) AND FLOOR PLAN(S)



V. DRC AND LVS RESULTS

Calibre - RVE v2024.2\_29.16 : TransAmp.drc.results

File View Highlight Tools Window Setup Help

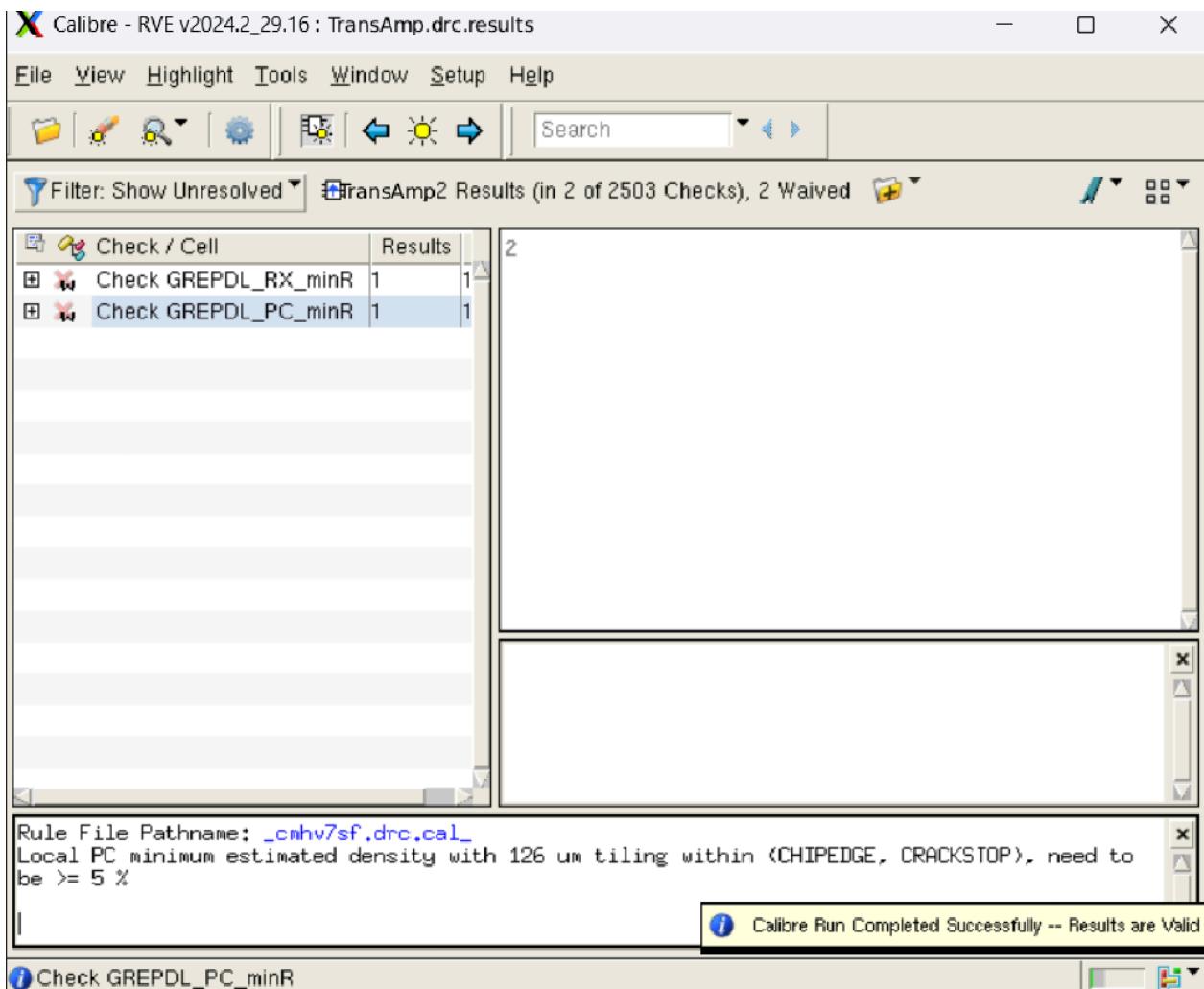
Filter: Show Unresolved ▾ TransAmp2 Results (in 2 of 2503 Checks), 2 Waived

Check / Cell	Results
Check GREPDL_RX_minR	1
Check GREPDL_PC_minR	1

Rule File Pathname: \_cmhv7sf.drc.cal  
Local PC minimum estimated density with 126 um tiling within (CHIPEDGE, CRACKSTOP), need to be >= 5 %

Calibre Run Completed Successfully -- Results are Valid

Check GREPDL\_PC\_minR



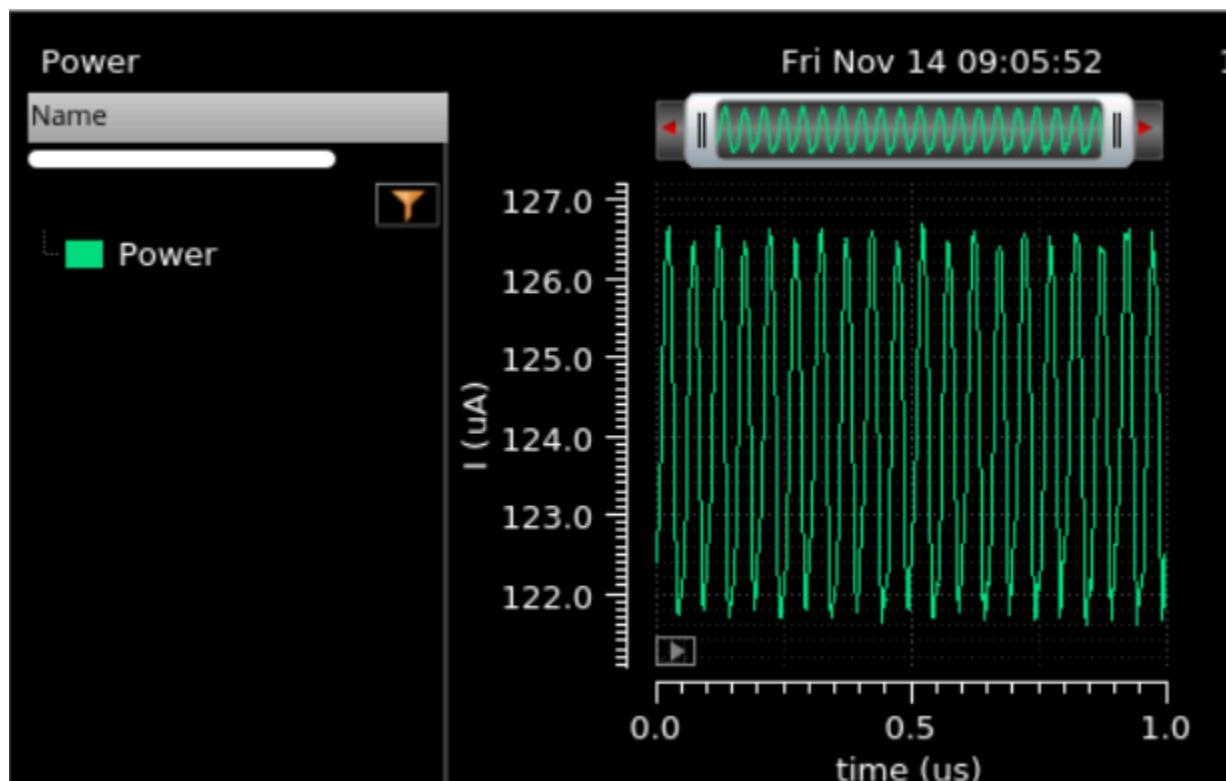
File Settings Configurations Help

TrampsAmp.lvs.report x

```
7      ##          ##
8      ##      L V S   R E P O R T      ##
9      ##          ##          ##
10     #####;#####;#####;#####;#####;#####
11
12
13
14 REPORT FILE NAME: TrampsAmp.lvs.report
15 LAYOUT NAME: TransAmp.sp('TransAmp')
16 SOURCE NAME: TransAmp.src.net ('TransAmp')
17 RULE FILE: _cmhv7sf.lvs.cal
18 CREATION TIME: Fri Nov 14 08:30:21 2025
19 CURRENT DIRECTORY: /home/ugrads/s/skywalker499/CAL
20 USER NAME: skywalker499
21 CALIBRE VERSION: v2024.2_29.16 Thu May 2 07:35:42 PDT 2024
22
23
24
25          OVERALL COMPARISON RESULTS
26
27
28
29      #      #####;#####;#####;#####
30      #      #      #      *      *
31      #      #      CORRECT      #      |
32      #      #      #      \_/
33      #
34      #####;#####;#####;#####
35
```

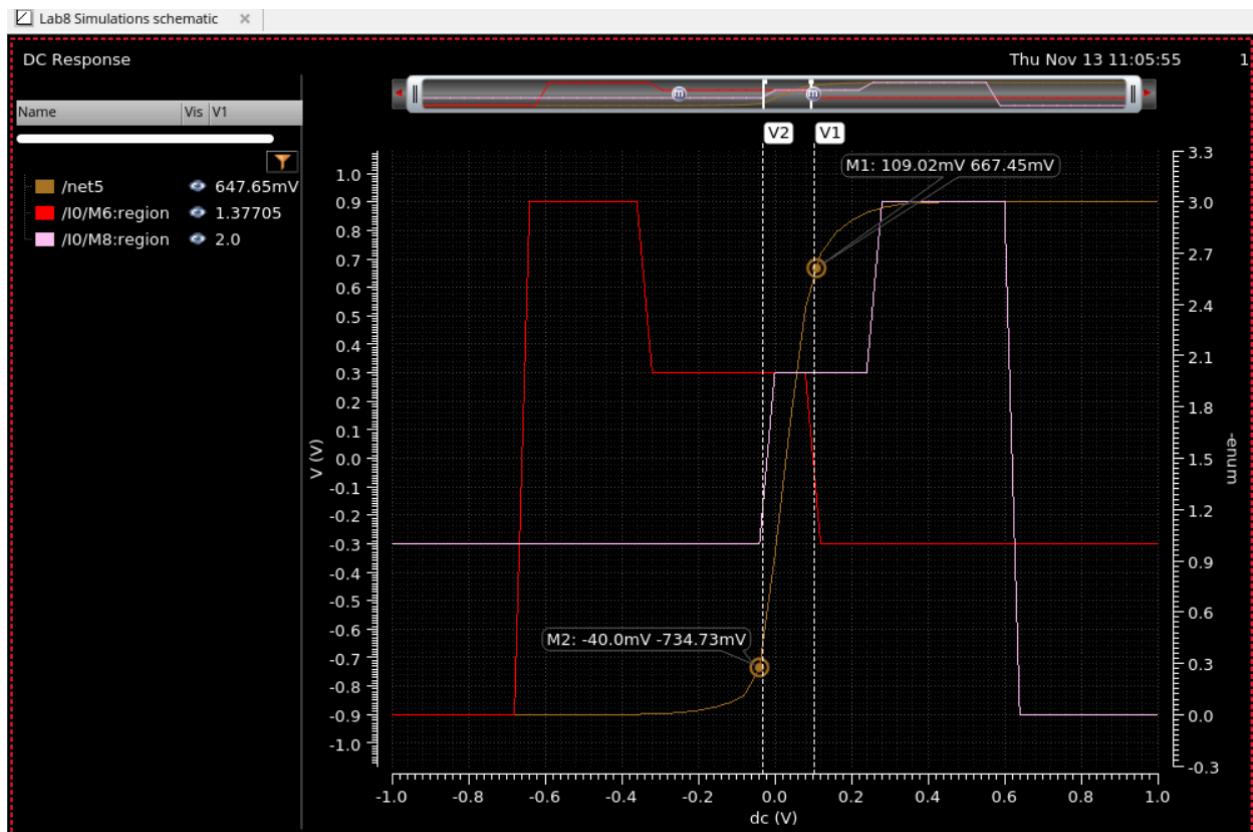
## VI. SIMULATION RESULTS

## Power Consumption:

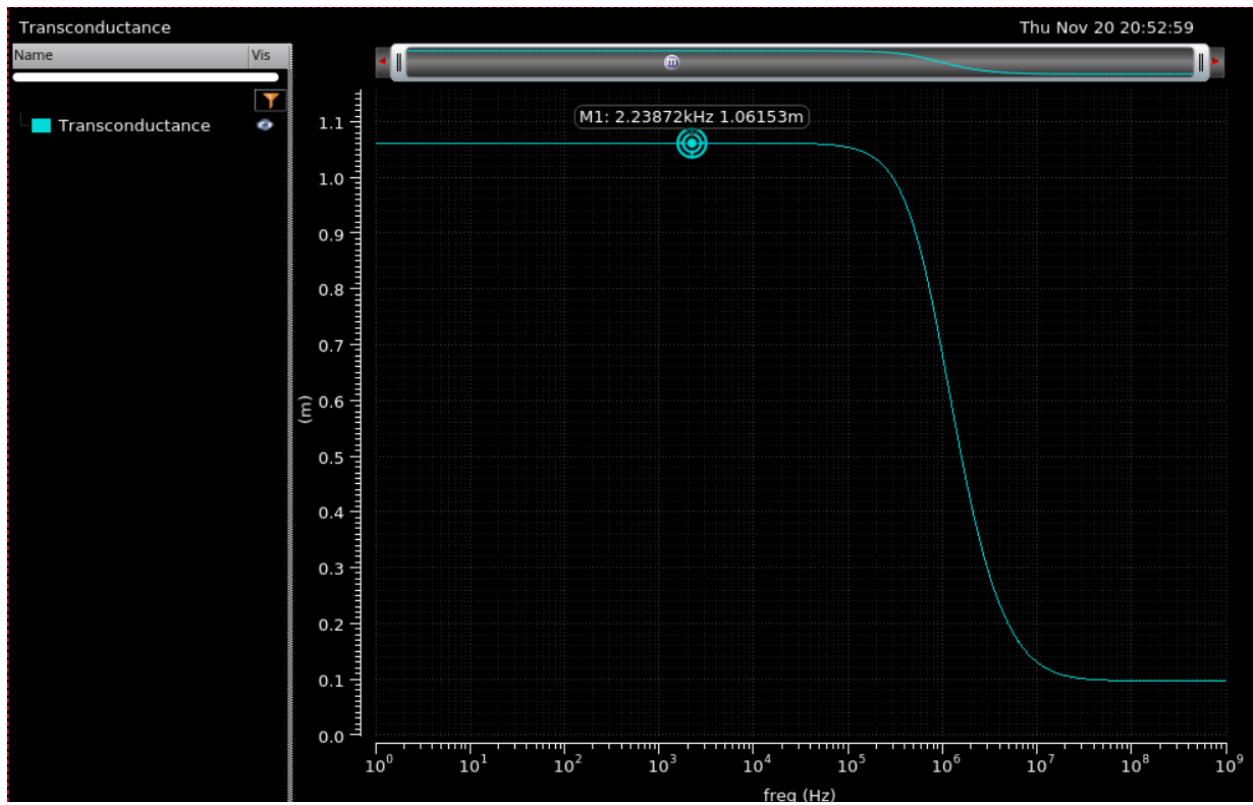


Note: Power stays within 127 - 122 uW, well under the 500uW limit.

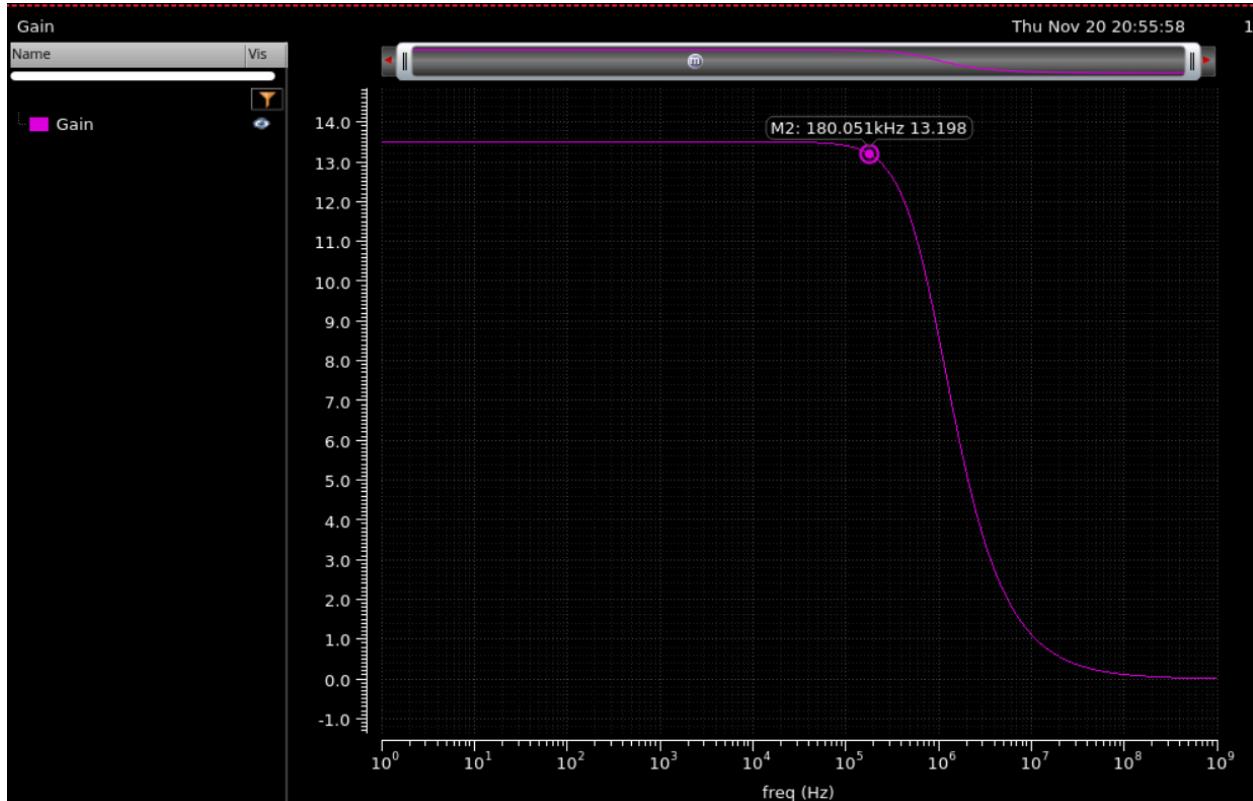
## Output swing:



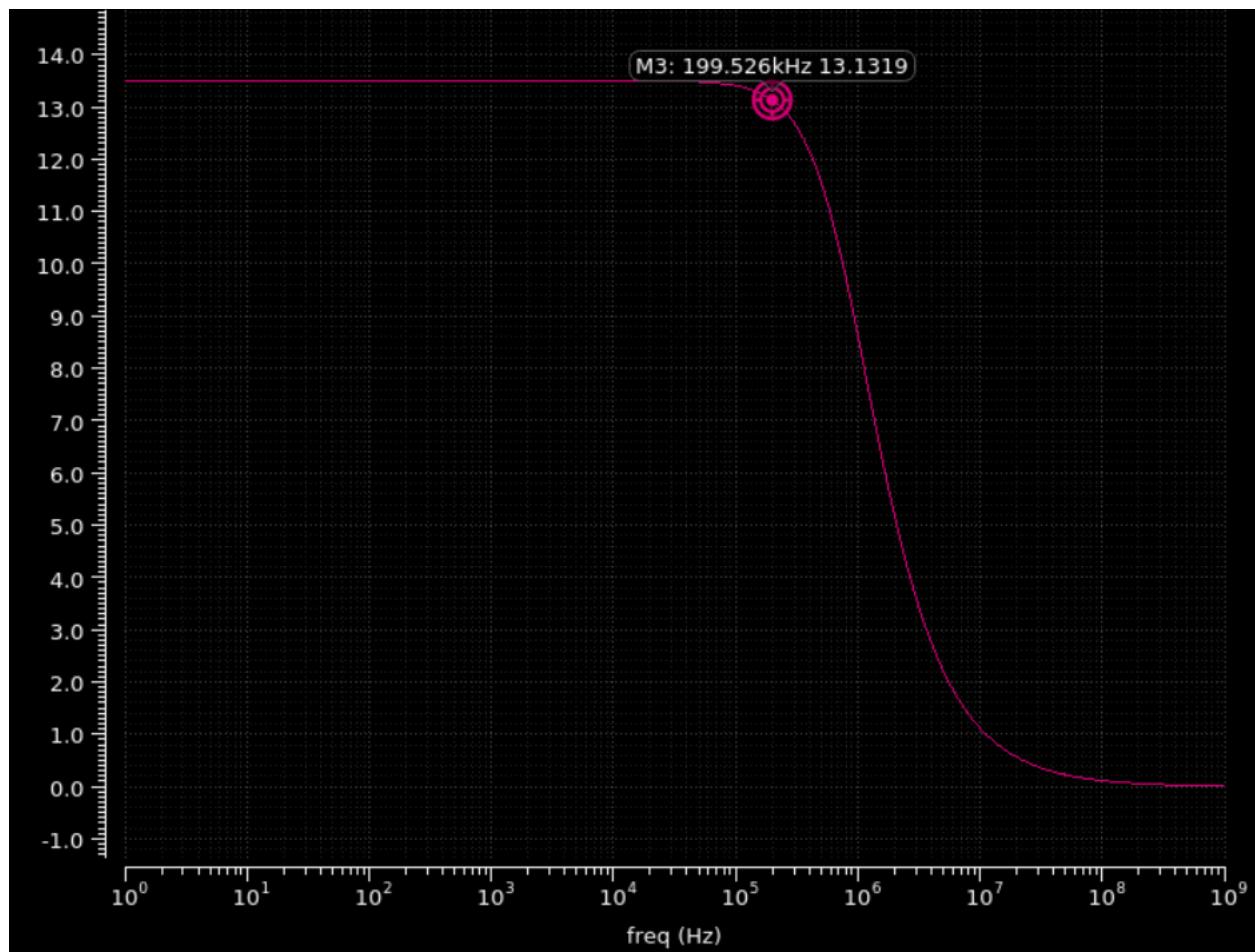
## Open loop Transconductance vs Frequency



## Open Loop Voltage gain vs Frequency

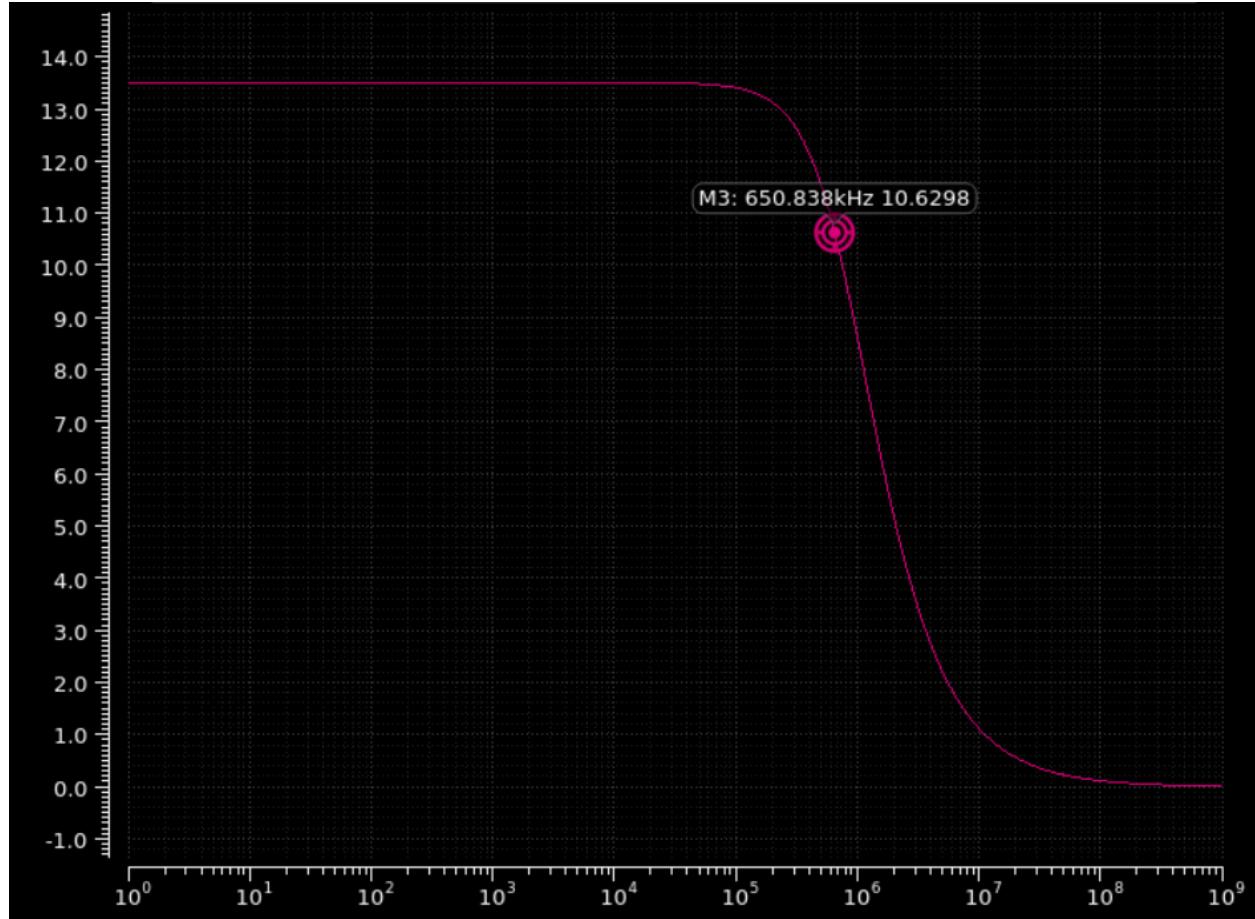


Dominant Pole Frequency =~200kHz



## GBW product

650kHz \*10 = 6.50 GHz



## Slew-Rate

$$SR = N \frac{I_{tail}}{C_L} = 3 \frac{100\mu A}{20pF} = 15 V/\mu s$$

## Phase Margin

