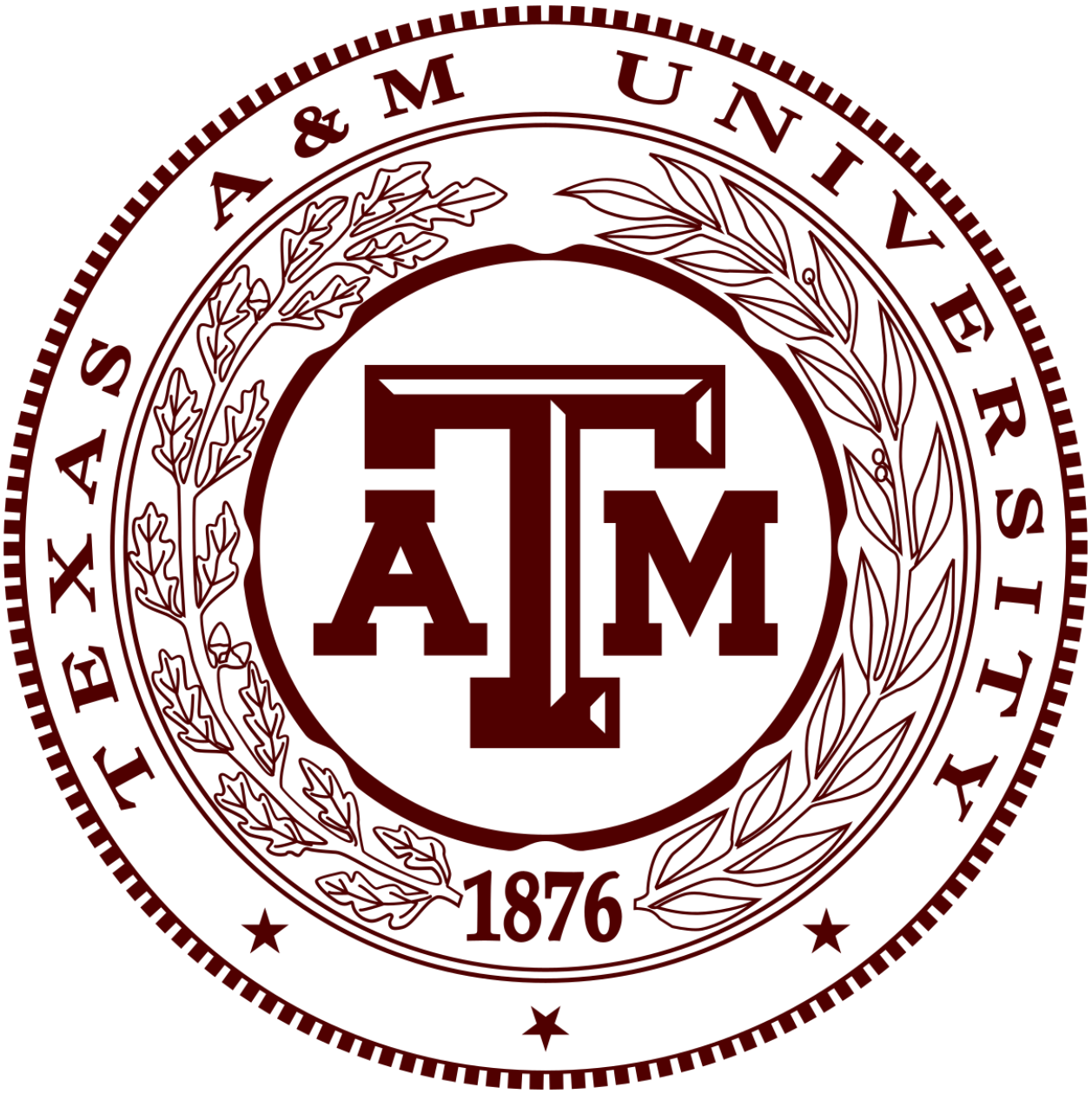


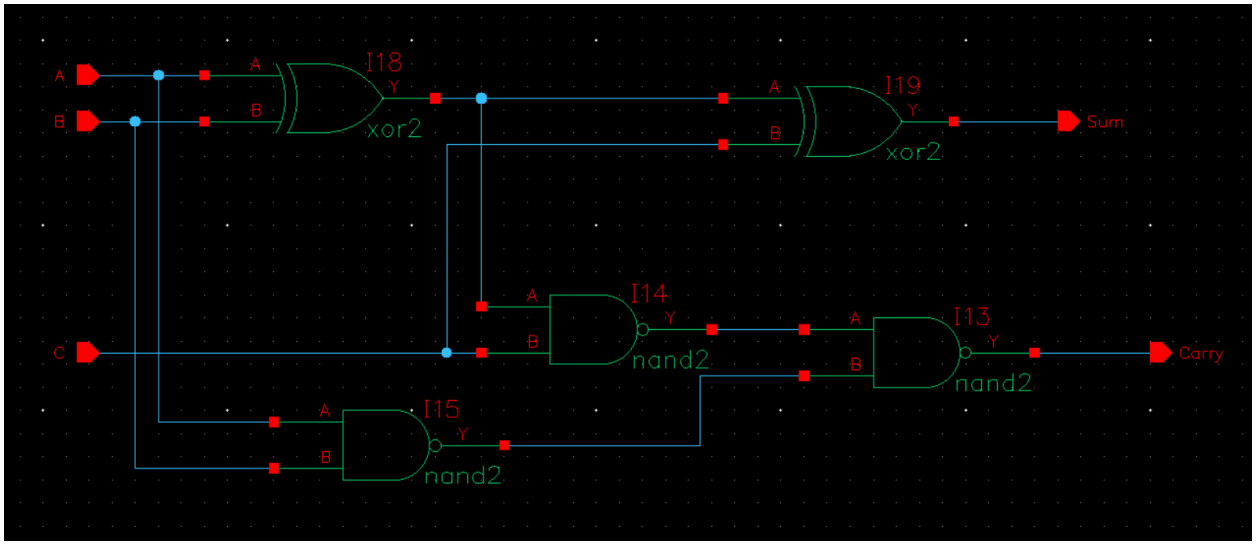
ECEN 454 - Lab 1 Report

Luke Lopez

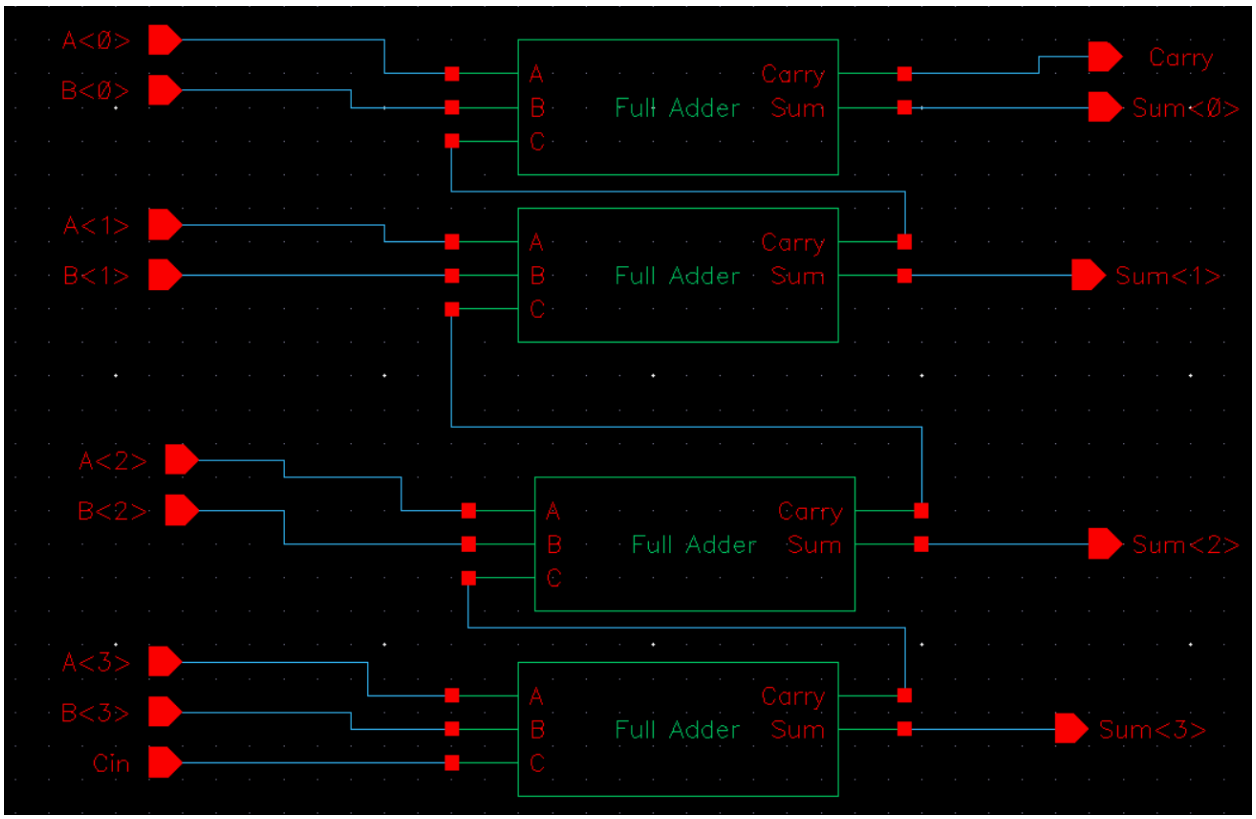
09/08/2025

Schematics

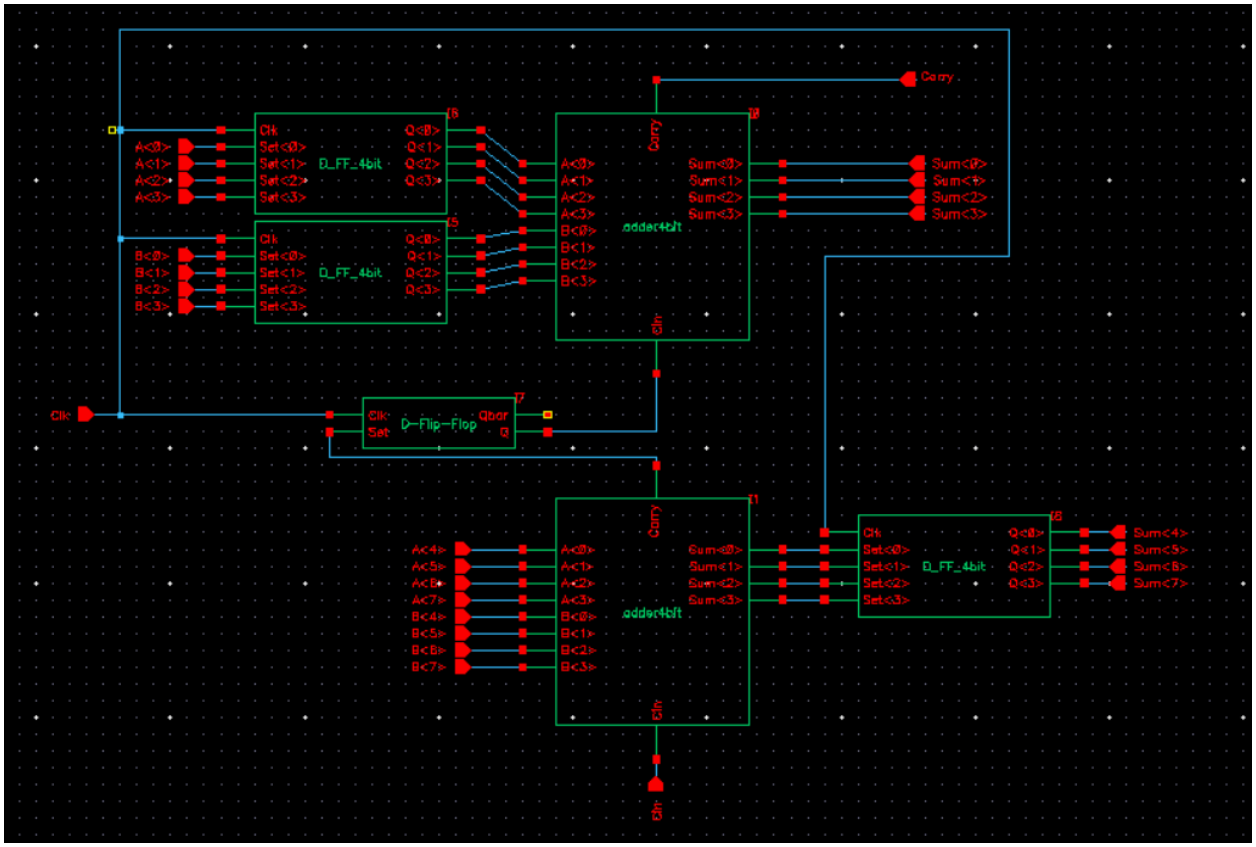
Full Adder



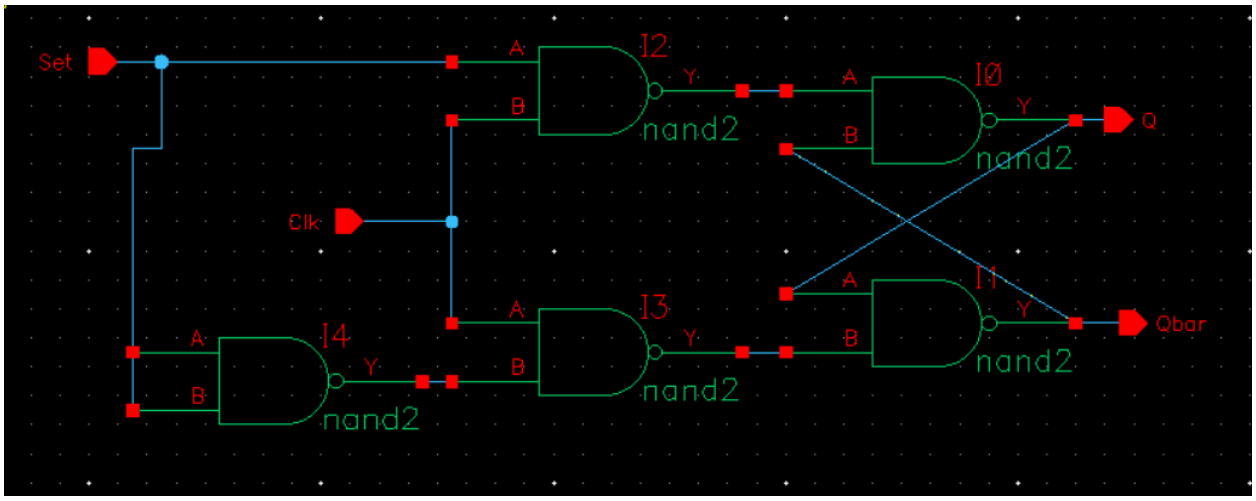
4-Bit-Adder



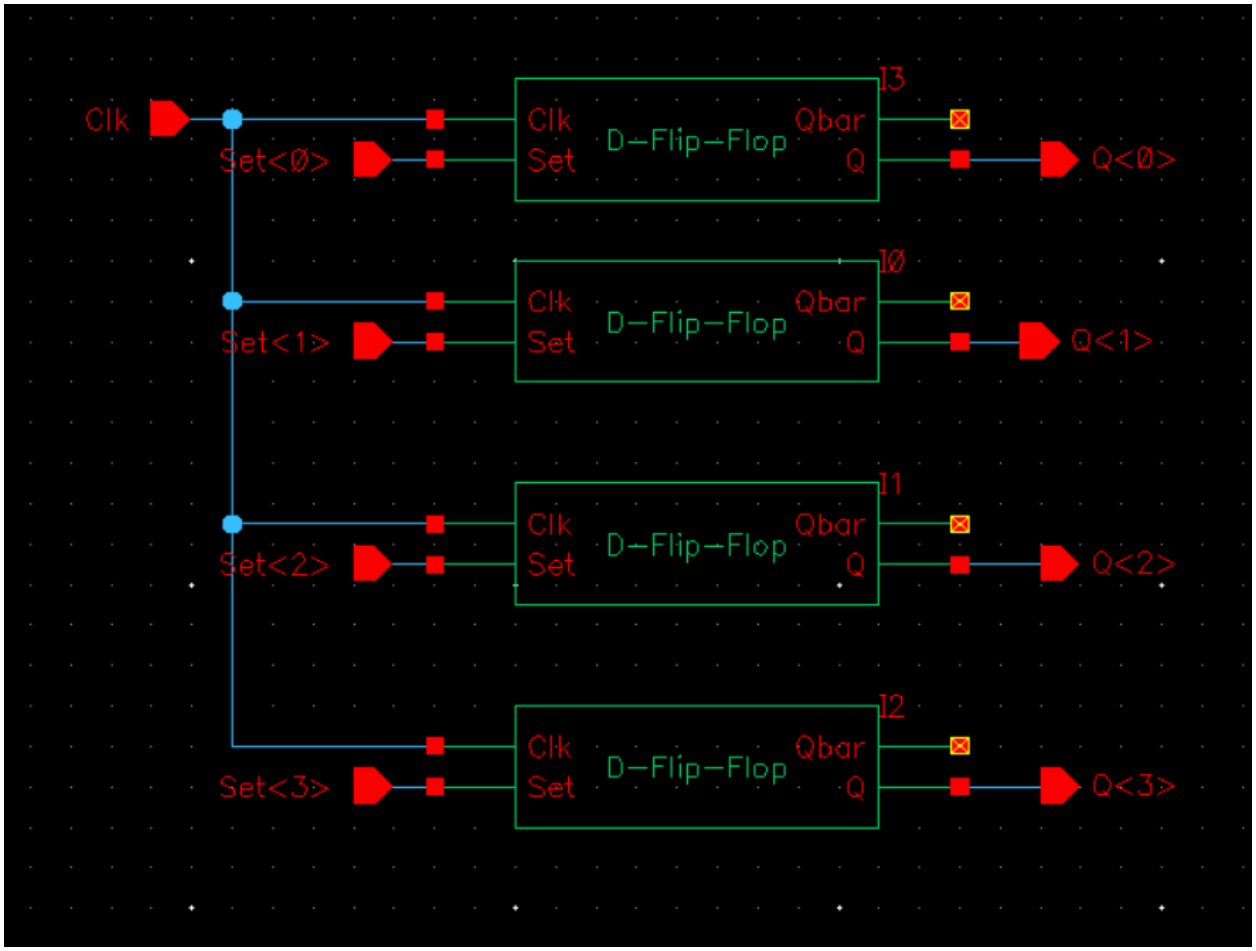
8-Bit-Adder



D-Flip Flop



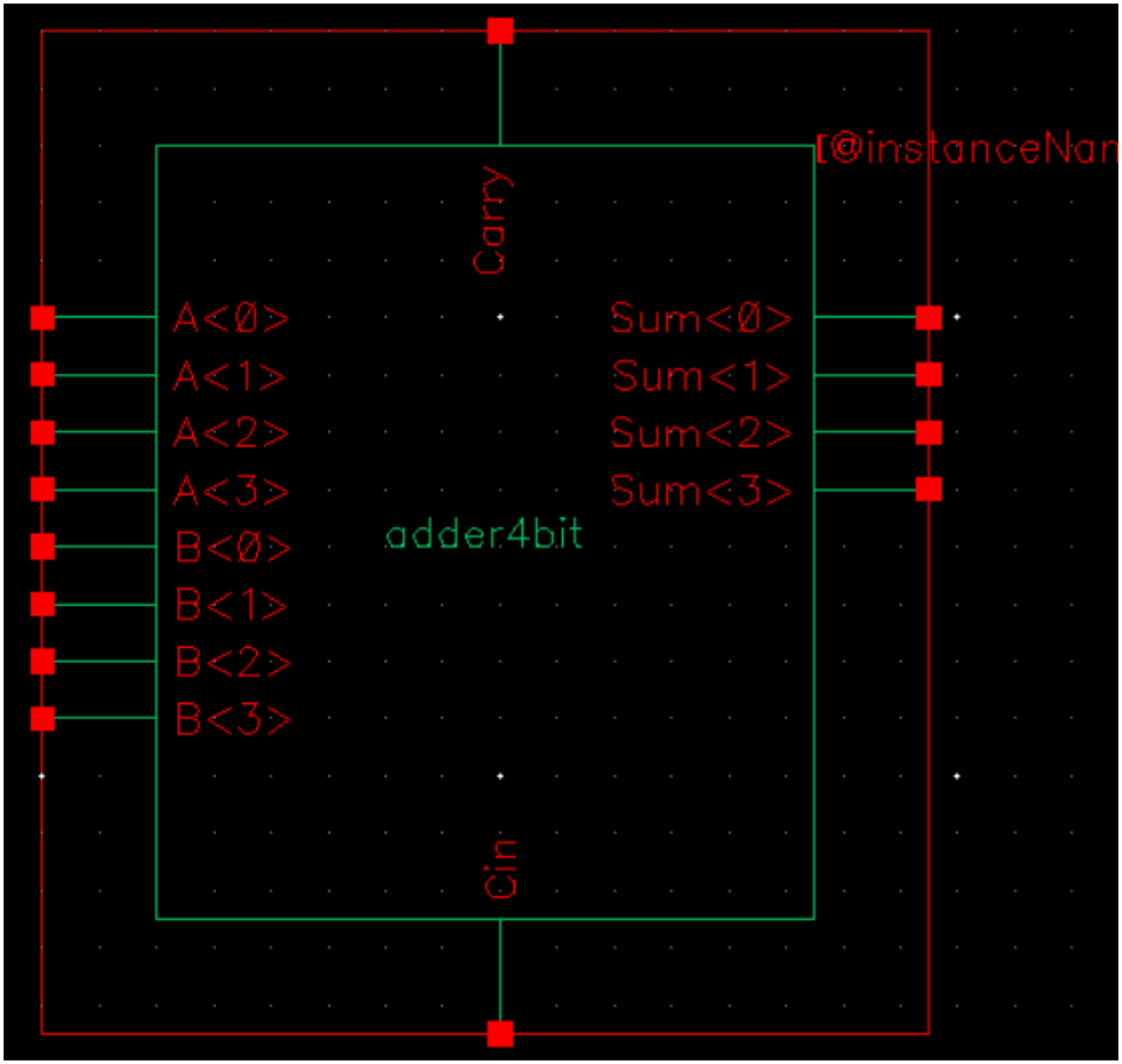
4Bit-Flip-Flop



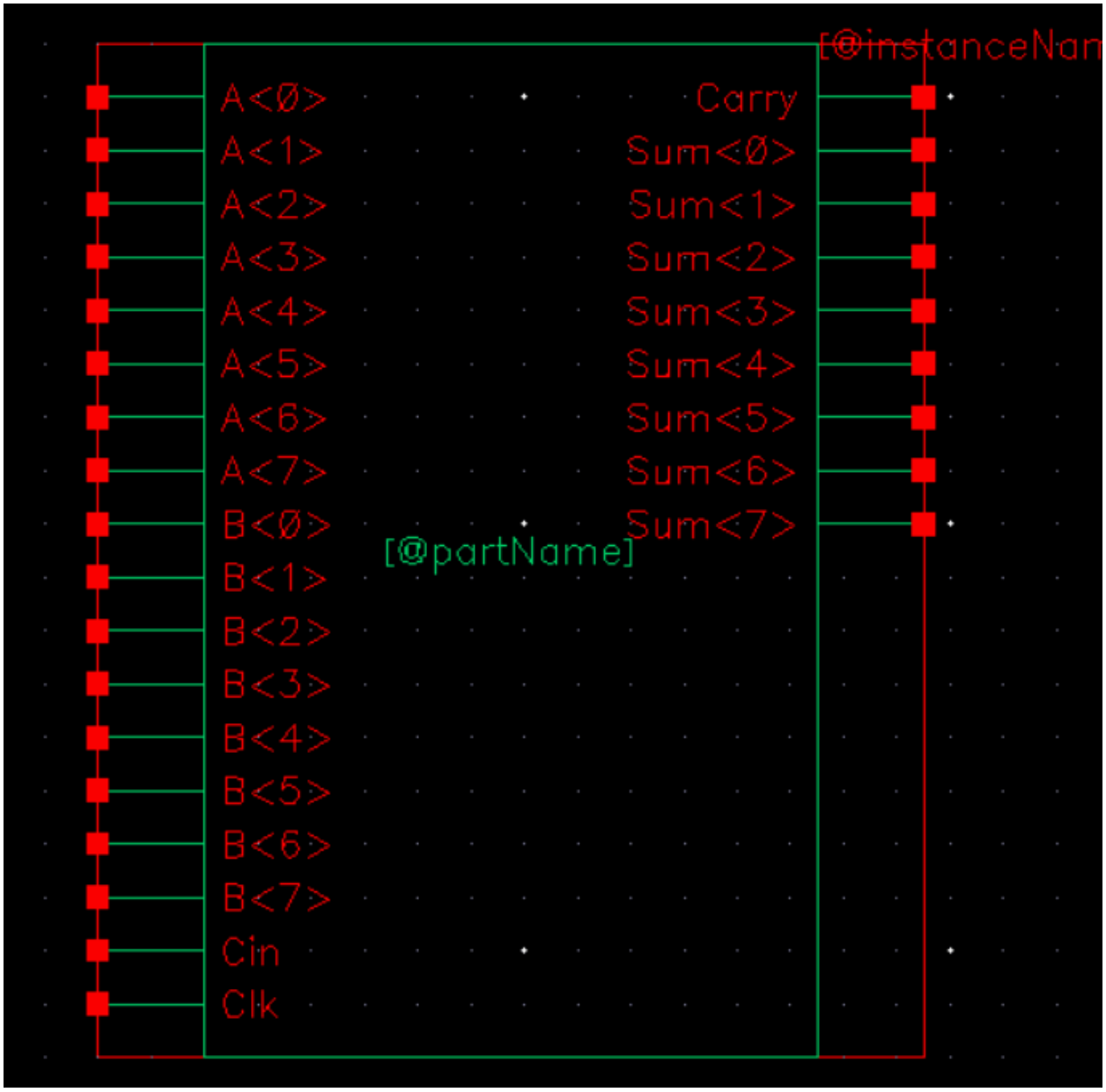
Symbols

Full Adder

4-Bit Adder


I@instanceNan
Carry
A<0>
A<1>
A<2>
A<3>
B<0>
B<1>
B<2>
B<3>
adder4bit
Sum<0>
Sum<1>
Sum<2>
Sum<3>
Cin

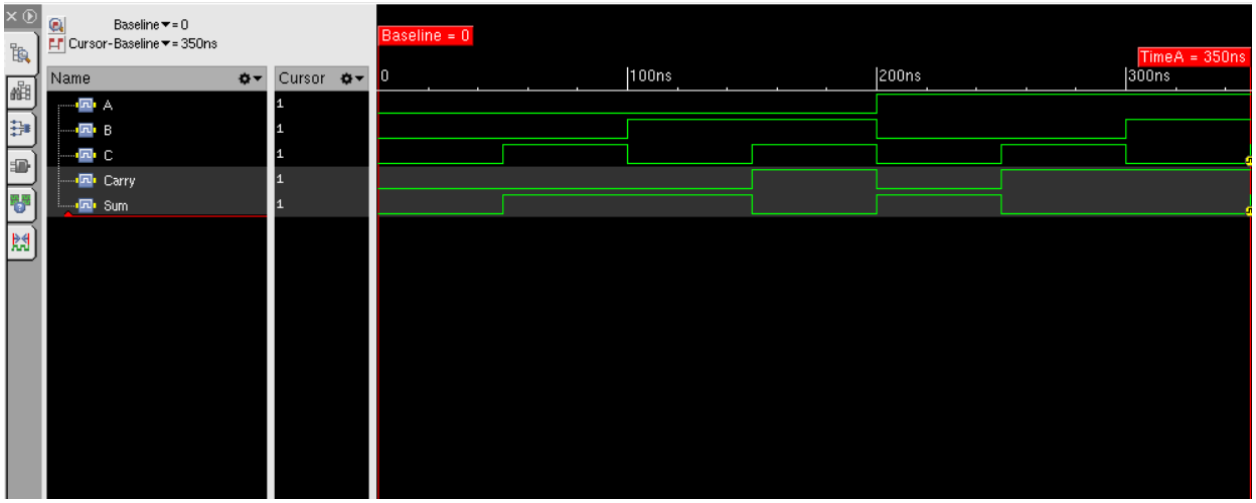
8-Bit-Adder


[@instanceNam
A<0>
A<1>
A<2>
A<3>
A<4>
A<5>
A<6>
A<7>
B<0>
B<1>
B<2>
B<3>
B<4>
B<5>
B<6>
B<7>
Cin
Clk
Carry
Sum<0>
Sum<1>
Sum<2>
Sum<3>
Sum<4>
Sum<5>
Sum<6>
Sum<7>
[@partName]

Simulation Results

NOTE: In most simulations, there is a “Fail” variable that shows the number of fails done while testing. In all graphics it can be seen that no fails occurred.

Full-Adder



Test type: Directed Full Adder (A, B, C inputs)

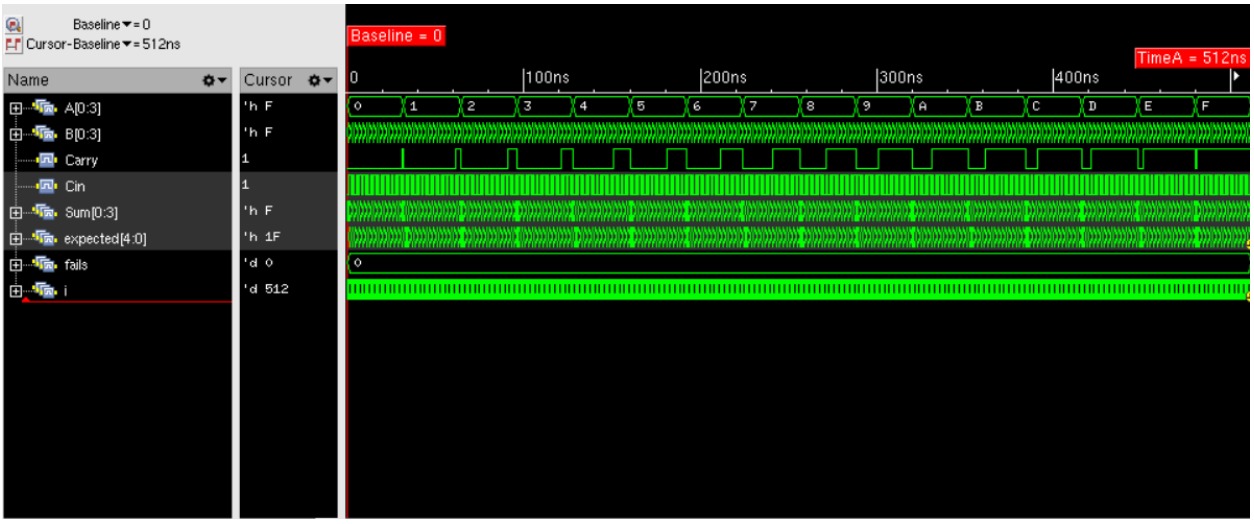
Full adder: 0 + 0 + 0 (Cin) = Sum=0 Carry=0
Full adder: 0 + 0 + 1 (Cin) = Sum=1 Carry=0
Full adder: 0 + 1 + 0 (Cin) = Sum=1 Carry=0
Full adder: 0 + 1 + 1 (Cin) = Sum=0 Carry=1
Full adder: 1 + 0 + 0 (Cin) = Sum=1 Carry=0
Full adder: 1 + 0 + 1 (Cin) = Sum=0 Carry=1
Full adder: 1 + 1 + 0 (Cin) = Sum=0 Carry=1
Full adder: 1 + 1 + 1 (Cin) = Sum=1 Carry=1

All tests complete. Total fails: 0

Notes

The test results all come out correct. Whenever there is more than 1 inputs with VAL 1, Carry = 1. Additionally, the Sums are all calculated correctly.

4-Bit-Adder

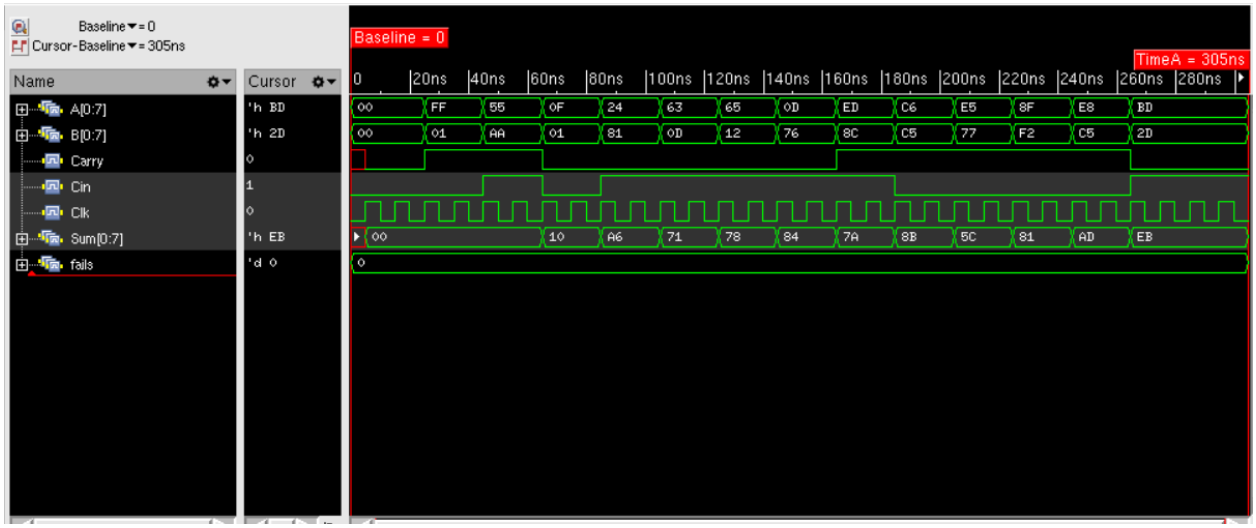


4bit adder: 0000 + 0000 + 0 (Carry In) = 0000 (Carry Out = 0)
4bit adder: 0000 + 0000 + 1 (Carry In) = 0001 (Carry Out = 0)
4bit adder: 0000 + 0001 + 0 (Carry In) = 0001 (Carry Out = 0)
4bit adder: 0000 + 0001 + 1 (Carry In) = 0010 (Carry Out = 0)
4bit adder: 1111 + 1111 + 0 (Carry In) = 1110 (Carry Out = 1)
4bit adder: 1111 + 1111 + 1 (Carry In) = 1111 (Carry Out = 1)
4bit adder: 1110 + 0100 + 1 (Carry In) = 0011 (Carry Out = 1)
4bit adder: 1110 + 0101 + 0 (Carry In) = 0011 (Carry Out = 1)
4bit adder: 0101 + 0101 + 1 (Carry In) = 1011 (Carry Out = 0)
4bit adder: 0101 + 0110 + 0 (Carry In) = 1011 (Carry Out = 0)

Notes

I did an exhaustive test on the 4 bit adder and had the verilog code check the outputs and all of them passed. However I did print out some edge cases and random ones too, and as you can see, the addition checks out.

8-Bit adder



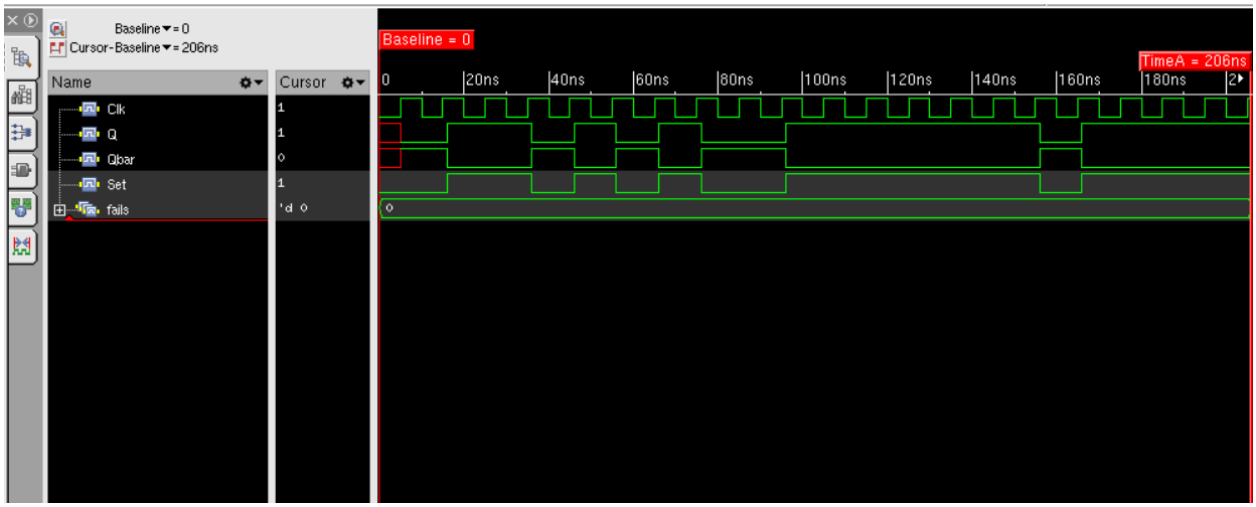
Starting 8-bit adder test with pipeline delay...

8bit adder: 01111110 + 11100111 + 0 (Carry In) = 01100101 (Carry Out = 1)
8bit adder: 11111111 + 00000000 + 1 (Carry In) = 00000000 (Carry Out = 1)
8bit adder: 10101010 + 01010101 + 0 (Carry In) = 11111111 (Carry Out = 0)
8bit adder: 10101010 + 01010101 + 1 (Carry In) = 00000000 (Carry Out = 1)
8bit adder: 11001100 + 00110011 + 0 (Carry In) = 11111111 (Carry Out = 0)
8bit adder: 11001100 + 00110011 + 1 (Carry In) = 00000000 (Carry Out = 1)
8bit adder: 00100100 + 10000001 + 1 (Carry In) = 10100110 (Carry Out = 0)
8bit adder: 01100011 + 00001101 + 1 (Carry In) = 01110001 (Carry Out = 0)
8bit adder: 01100101 + 00010010 + 1 (Carry In) = 01111000 (Carry Out = 0)
8bit adder: 00001101 + 01110110 + 1 (Carry In) = 10000100 (Carry Out = 0)

Test complete. Total fails: 0

Notes:
Since there are to many cases, I did not do an exhaustive test like the 4 bit adder, but did have most edge cases. Some of which you can see here. Again i had the verilog code check if there was any errors as it was testing, which as we can see, none occurred.

D-Flip-Flop


Baseline = 0
Cursor-Baseline = 206ns
Name
Cursor
Clk
Q
Qbar
Set
fails
Baseline = 0
TimeA = 206ns
0
20ns
40ns
60ns
80ns
100ns
120ns
140ns
160ns
180ns