

# ECEN 474/704: Lab 01

## Introduction to Cadence and MOS Device Characterization

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### I. DISCUSSION OF THE LAB AND RESULTS

The purpose of this lab was to show how certain parameters affect the performance of a transistor, both for nMOS and pMOS transistors. First the lab teaches how to attain the required measurements to see the effects of the changes. The parameters we are interested in are shown below in **Table 1**. Additionally, the conditions it was measured in are recorded in **Table 2**. We are concerned with the effects of :  $\mu C_{ox}$ ,  $V_{th}$ ,  $\theta$ ,  $\lambda$ ,  $f_T$ ,  $A_i$ . Personally, I am most intrigued by the effects on the  $f_T$  parameter.

When the **width** is adjusted we find that although  $\mu C_{ox}$  is dependent on all parameters set, it seems to be more dependent upon the  $W$ . This makes sense because there is more surface area for the transistor to attain a higher oxide capacitance. Additionally, with a bigger width, there are more paths for the electrons to travel, meaning a higher mobility of electrons. For the  $V_{th}$  not much changes as it's more based on the effectiveness of the gate to channel to allow current through. So influencing the width doesn't affect it much since the gate covers the entire width of the channel anyways, despite its size. The thermal resistance  $\theta$  however is greatly affected by the geometry of the transistor. With an increased surface area, there is a lot more for the transistor to heat up and it's easier to dissipate the energy. Width also seems to have a positive relationship with  $f_T$ . This makes sense since, as mentioned before, increasing the width of the transistor allows for more current to flow and have a higher mobility. With a higher mobility, it's easier to oscillate from on and off faster and faster. This could be shown as to increase the transconductance of the transistor ( $gm$ ) which is inversely proportional to the gain  $A_i$ . Therefore, this explains the dip in the intrinsic gain of the transistor.

The number of **fingers** is really important mainly for the  $V_{th}$  since the gate now has a "firmer grasp" upon the channel in which it's created. With a higher control over the channel it can allow for higher mobility which is seen in  $\mu C_{ox}$  and  $f_T$ . Since this doesn't necessarily change the physical amount of flow electrons through the channel, the thermal ( $\theta$ ) and channel modulation ( $\lambda$ ) characters remain relatively unchanged.

Changing the **length** of the transistor has a massive effect on the intrinsic gain  $A_i$  and the channel length modulation  $\lambda$ . For the channel modulation this makes sense since the modulation has a longer channel to cover over. However I must say that I was surprised by its significant effect on intrinsic gain. In fact I would say that it has the highest effect upon intrinsic gain. However the effect is completely valid since a longer length gives a higher output resistance through the transistor, attaining a bigger gain. Trade off comes with it, usually decreasing the transconductance and dramatically lowering  $f_T$ . Length does seem to be the most powerful influencer of the transistor's characteristics, where we can trade off higher speeds for greater gains.

Overall when a transistor is a **pfetx** the same trends mentioned above apply similarly, but across the board, performs less optimally than its **nfetx** counterparts. The only advantage it seems to have is a lower threshold voltage to activate. At first glance a high benefit could be a lower oxidised capacitance, but I believe that simply the mobility  $\mu$  was lowered since it conducts less effectively, and the  $C_{ox}$  stayed the same.

## II. SUMMARY OF RESULTS

Table 1  
Transistor Characteristics

Parameter	$\mu C_{ox}$	$V_{th}$	$\theta$	$\lambda$	$f_T$	$A_i$
Condition 1	$167.4\mu$	460.4 mV	0.920	0.3562	49.54 GHz	19.82   24.01
Condition 2	$217.2\mu$	460.1 mV	1.295	0.6067	46.31 GHz	17.08   29.74
Condition 3	$181.2\mu$	442.3 mV	0.9365	0.4043	52.54 GHz	18.53   33.47
Condition 4	$214.3\mu$	447.0 mV	0.9942	0.1608	25.49 GHz	49.48   121.23
Condition 5	$47.37\mu$	432.2 mV	1.386	0.6516	8.809 GHz	17.02   27.55
Condition 6	$56.49\mu$	414.3 mV	1.474	0.5982	9.646 GHz	16.25   26.31
Condition 7	$47.37\mu$	432.2 mV	1.386	0.5566	10.88 GHz	17.01   27.52
Condition 8	$47.53\mu$	421.6 mV	1.267	0.2012	4.317 GHz	44.29   56.05

**Note:** For the  $A_i$ , the values are {approximated} | {simulation}, i wanted to see how off the error was of the approximation since i could.

Table 2  
Transistor set properties

Condition #	W/L	fingers	nfetx/pfetx
1	$0.5\mu/0.18\mu$	1	nfetx
2	$5\mu/0.18\mu$	1	nfetx
3	$5\mu/0.18\mu$	10	nfetx
4	$5\mu/0.27\mu$	1	nfetx
5	$0.5\mu/0.18\mu$	1	pfetx
6	$5\mu/0.18\mu$	1	pfetx
7	$5\mu/0.18\mu$	10	pfetx
8	$5\mu/0.27\mu$	1	pfetx

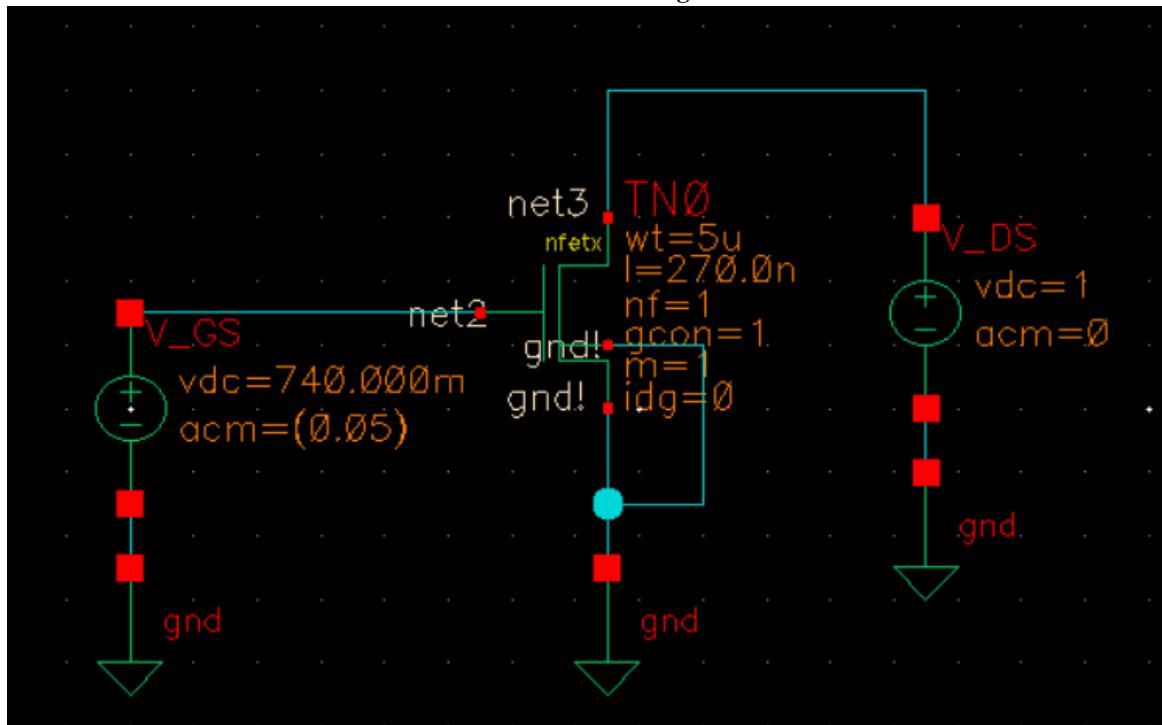
Table 3  
Set conditions to find  $A_i$ , along with table 2 conditions

Condition #	$V_{gs}$	ID	$V_{eff}$
1.1	684.45 mV	14.801 uA	224.05
2	460.00 mV	9.301 uA	0
3	442.3 mV	10.47 uA	0
4	447.0 mV	6.873 uA	0
5	432.2 mV	0.3038 uA	
6	414.3 mV	3.42 uA	
7	432.2 mV	3.038 uA	
8	421.6 mV	2.069 uA	

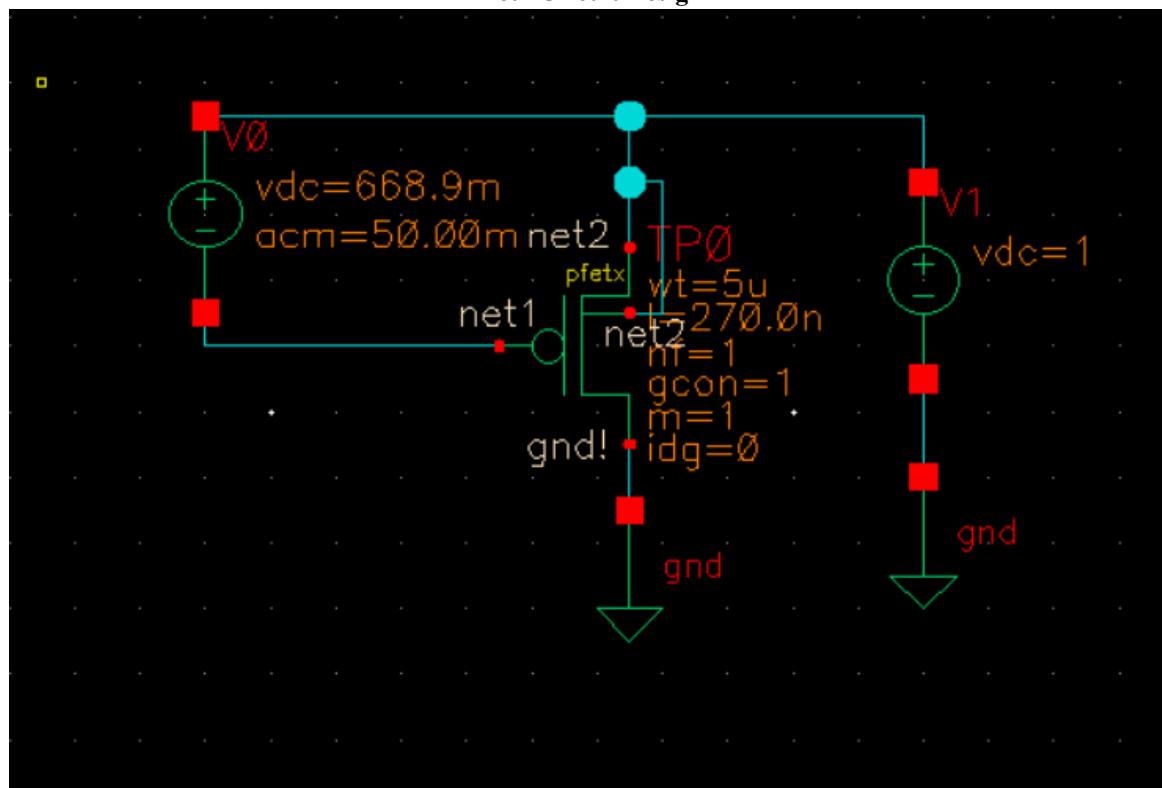
**Note:** These values are determined at the most mobile point found in the DC simulation. Therefore  $V_{gs} = V_t + 1/4\theta$ , and the current source will be set to the respective value found in previous simulations.

### III. SUB-CIRCUIT AND TEST BENCH SCHEMATICS

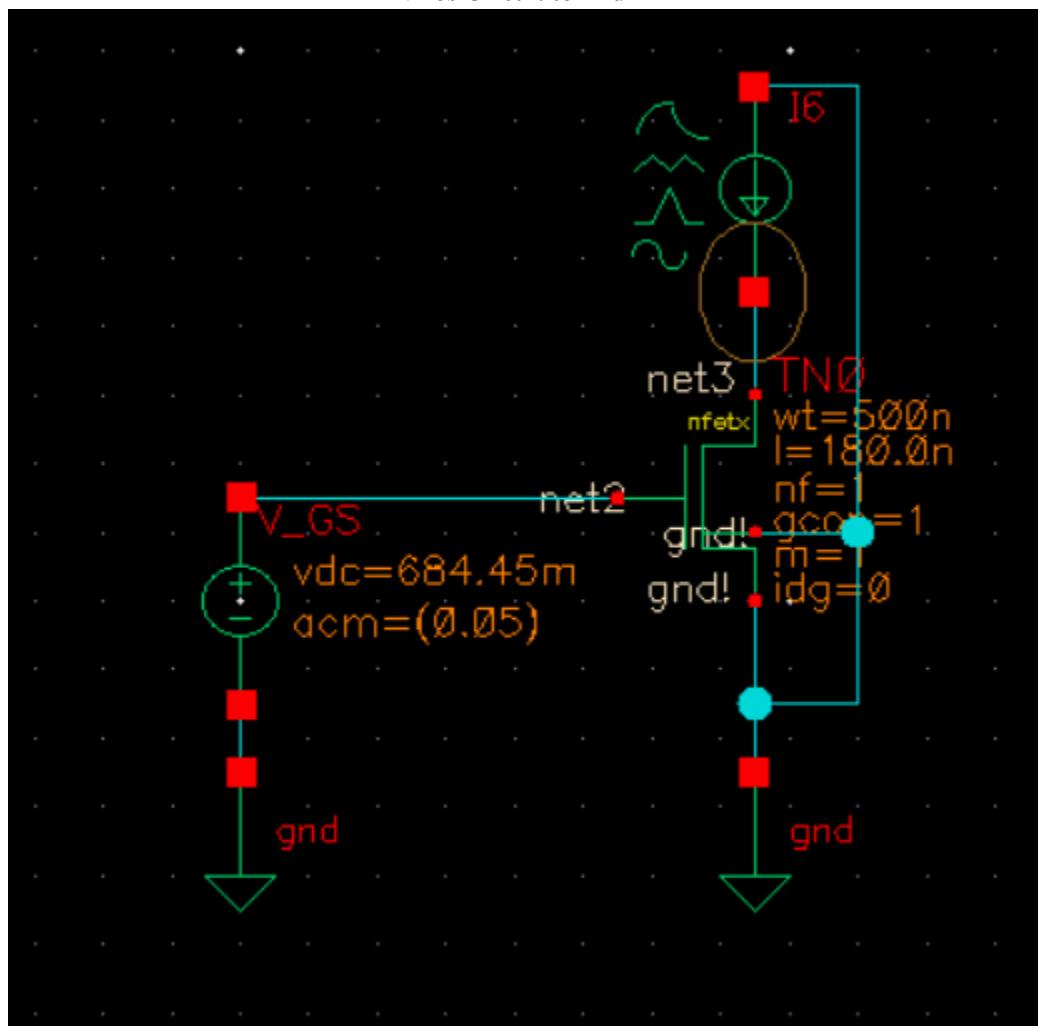
Nfetx Circuit Design



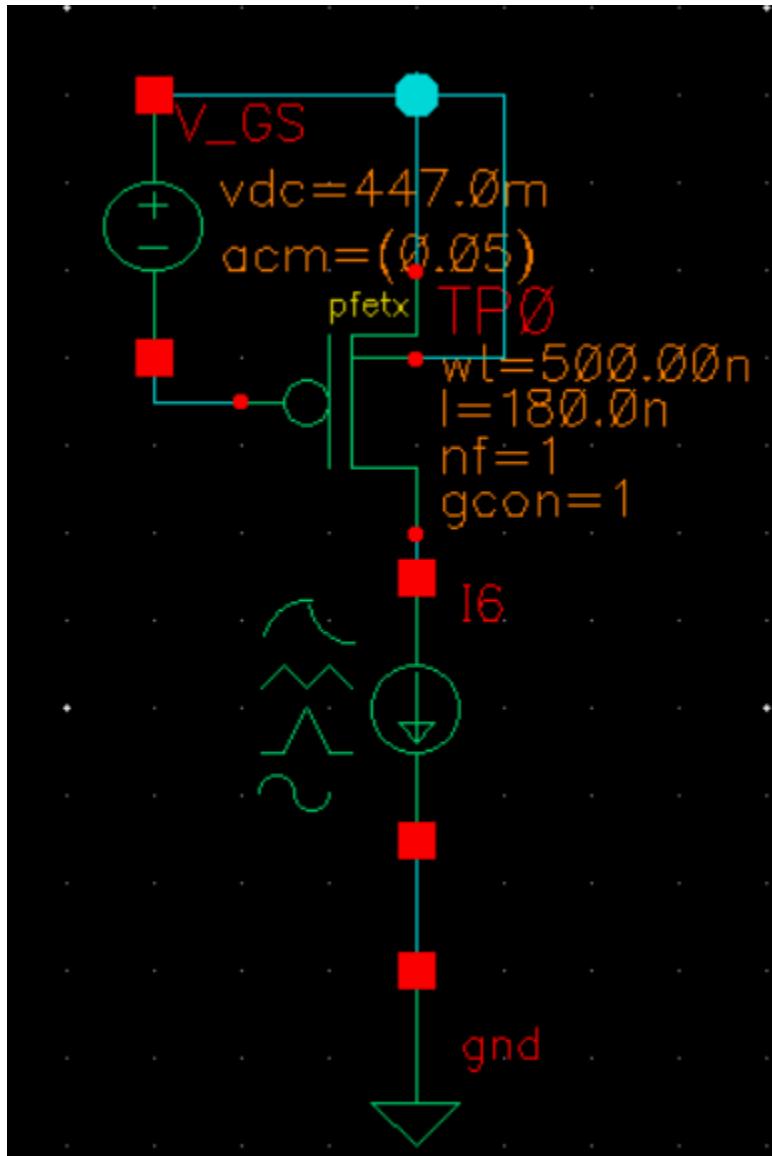
Pfetx Circuit Design



Nmos Circuit to find Ai



### Pmos Circuit to find Ai



### IV. SIMULATION RESULTS

#### Equations used in lab

##### $V_{GS}$ sweep simulation:

```

I_D_1 = i("/TN0/D" ?result "dc")
D1_1 = deriv(I_D_1)
D2_1 = deriv(D1_1)
Max_slope_1 = cross(D2_1 ymax(D2_1)) //Gives the  $V_{GS}$  coordinates I will use later
TL = tangent(D1_1 ?x Max_slope_1 ?y value(D1_1 Max_slope_1) ?slope value(D2_1 Max_slope_1))
V_t_1 = cross(TL 0)
uCox = ((value(D2_1 Max_slope_1) * L) / W)
HzL_pt = cross(D2_1 0) //gives the point for the horizontal line to exist at
HzL = tangent(D1_1 ?x HzL_pt ?y value(D1_1 HzL_pt) ?slope value(D2_1 HzL_pt))
thetaEq = cross(TL value(HzL 1) 1 "either" nil nil 0.01) // gives val to be use in the theta equation.
Theta_1 = ((1 / (thetaEq - V_t_1)) * 0.5)
W = (whatever the condition is)
L = (whatever the condition is)

```

```
ID_for_Ai = value(I_D_1(V_t_1 + ((1 / 4) * theta_1))) // For when we need Ai  
VGS_for_AI = (V_t_1 + ((1 / 4) * theta_1))
```

#### V<sub>DS</sub> / AC sweep simulation:

```
Input = IF("/V_GS/PLUS")  
Output = IF("/TN0/D")  
Gain = mag((output / input))  
Ft = cross(gain 1)  
Plot2 = (deriv(i("/TN0/D" ?result "dc")) / i("/TN0/D" ?result "dc")) //Plot used to find lambda  
lambda = (value(plot2 1) / (1 - value(plot2 1)))  
Theta = (whatever we found in previous step)  
Ai = (2 / (lambda * (1 / (4 * theta))))
```

#### Ai circuit calculation

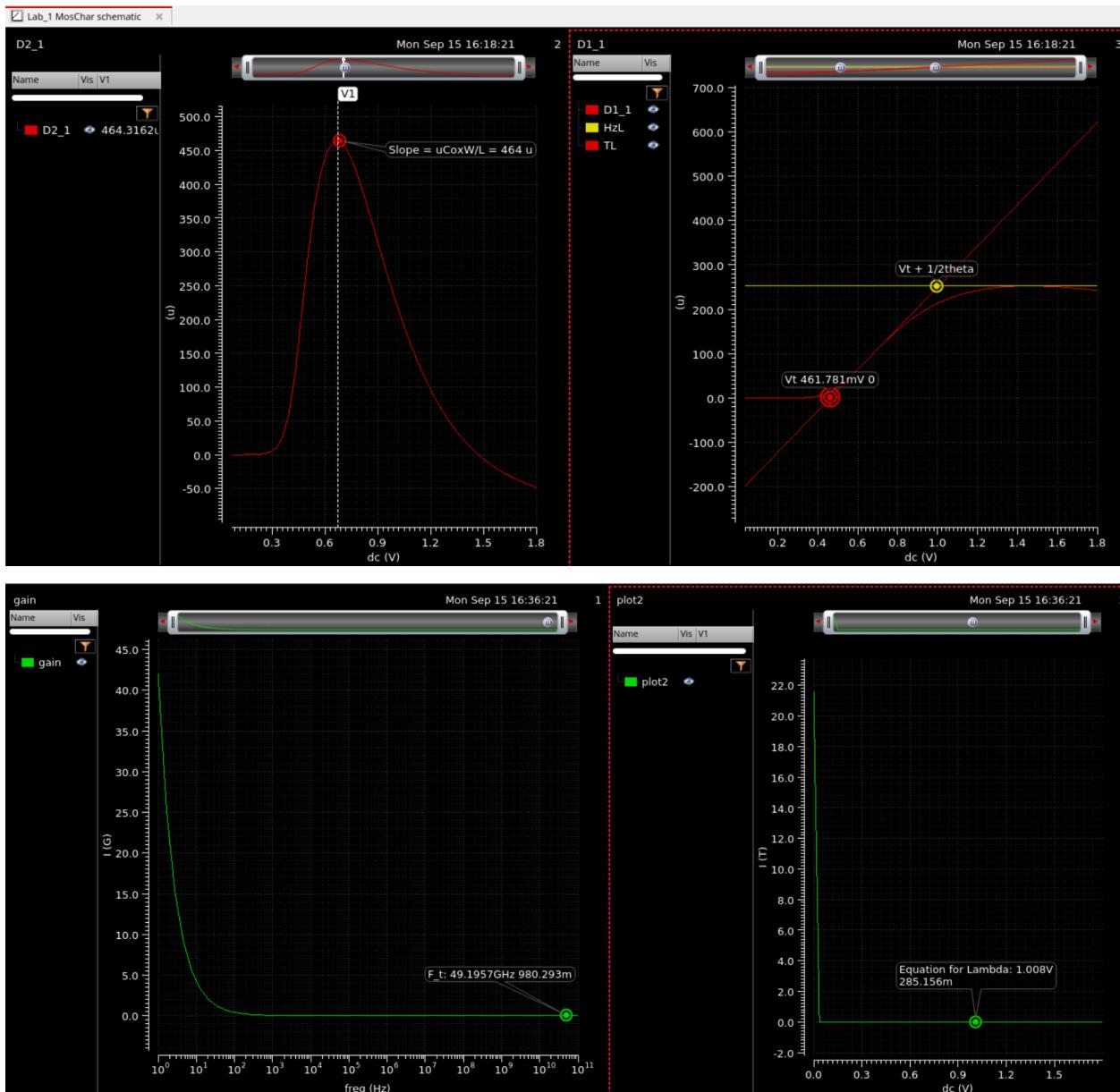
```
V_gs = mag(v("/net2" ?result "ac"))  
ID = (whatever value we set it too)  
V_out = 1V since thats what we force it to be with the set ID  
ac_V_out = mag(v("/net3" ?result "ac"))  
R_ds = 1V / ID  
Gm = (ac_V_out / (r_ds * V_gs))  
Ai = (gm * r_ds)
```

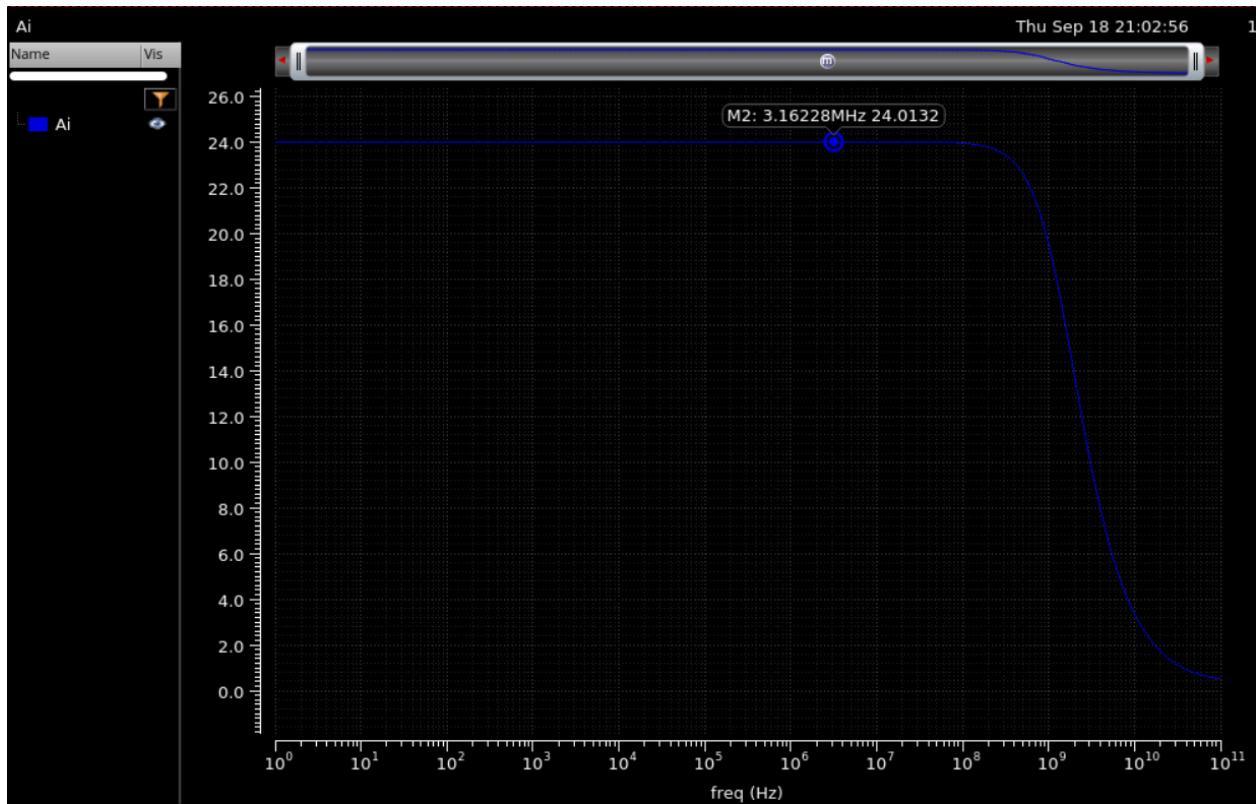
## Screenshots

**Note:**the values submitted are calculated by the computer and might not match exactly what is shown in graphs.

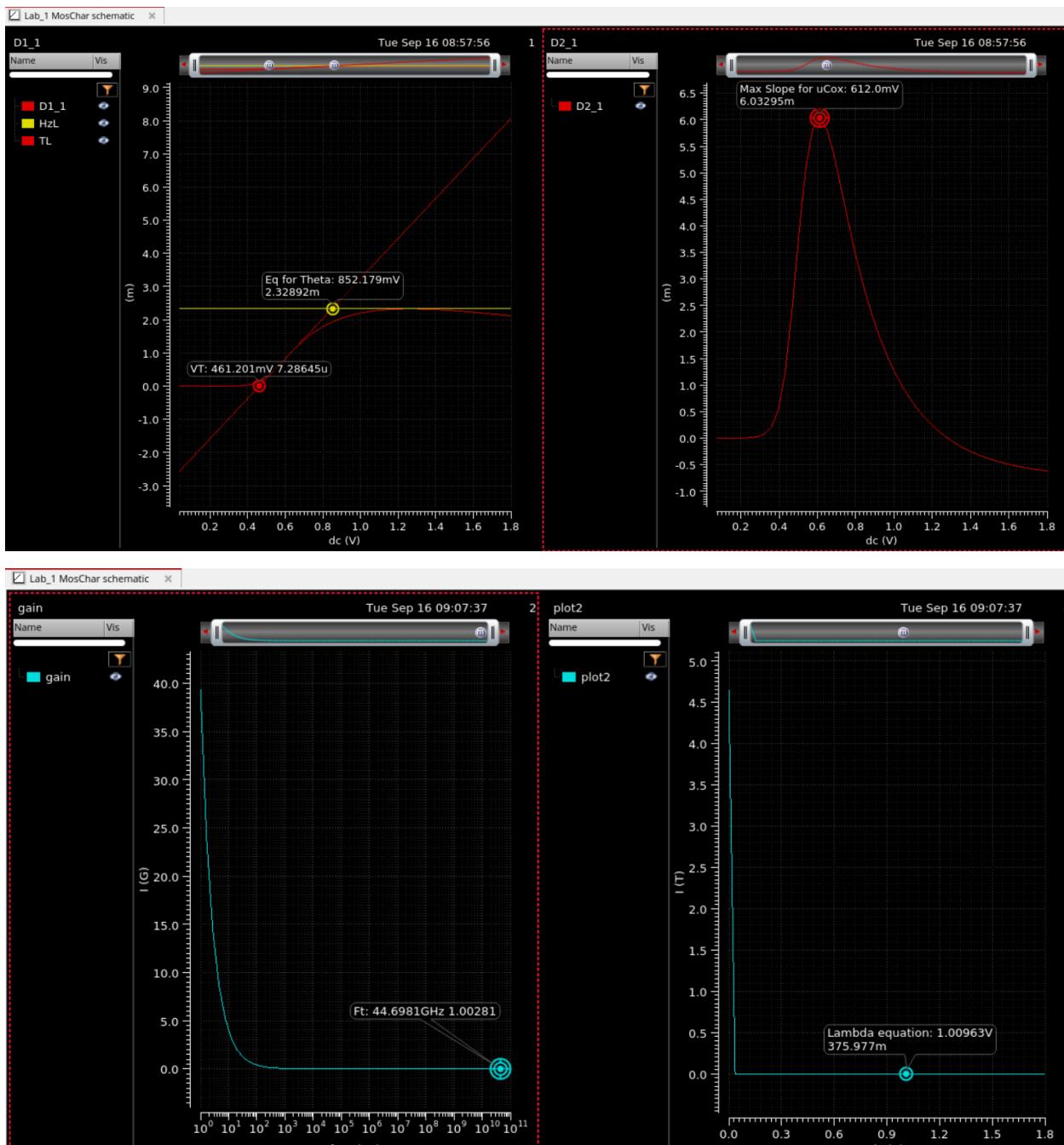
Additionally, the values shown in the graph could be equations to SOLVE its respective variables.

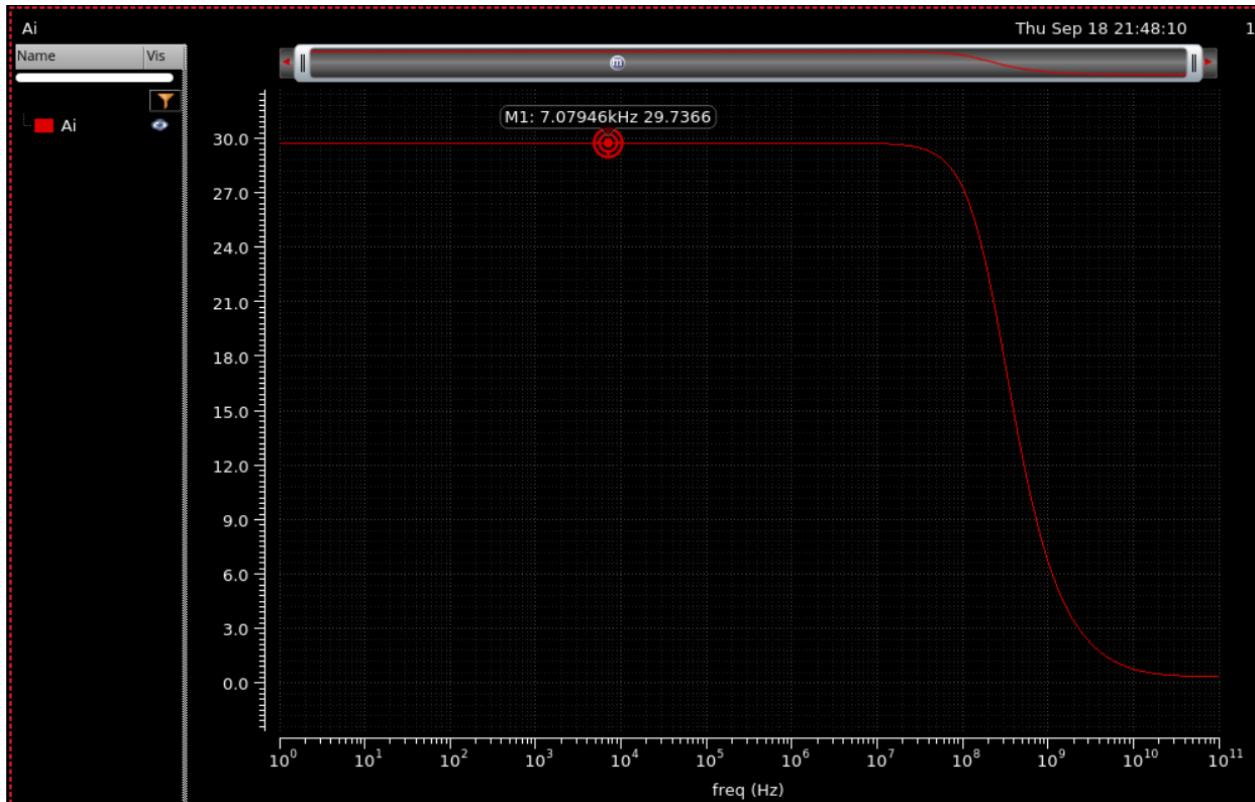
### Condition 1



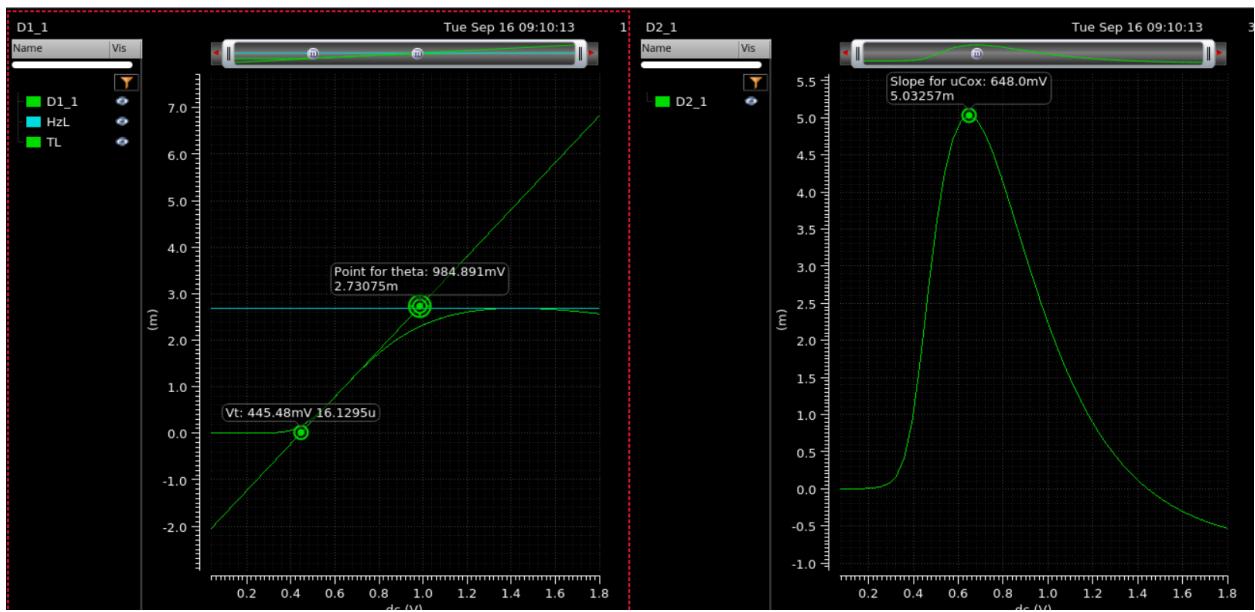


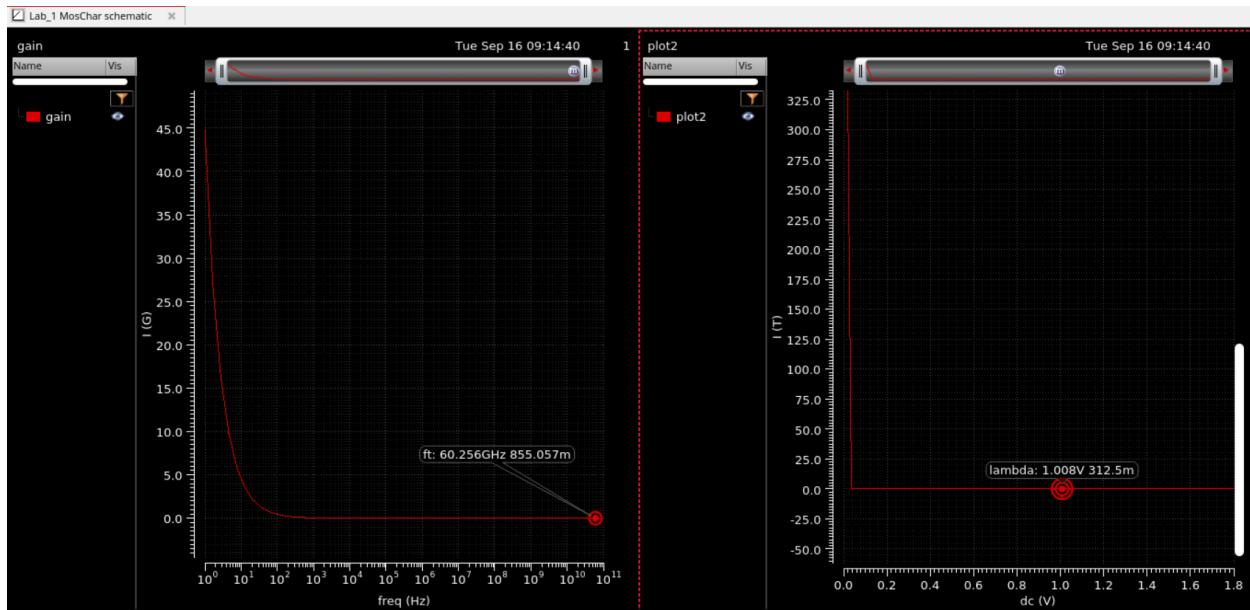
## Condition 2

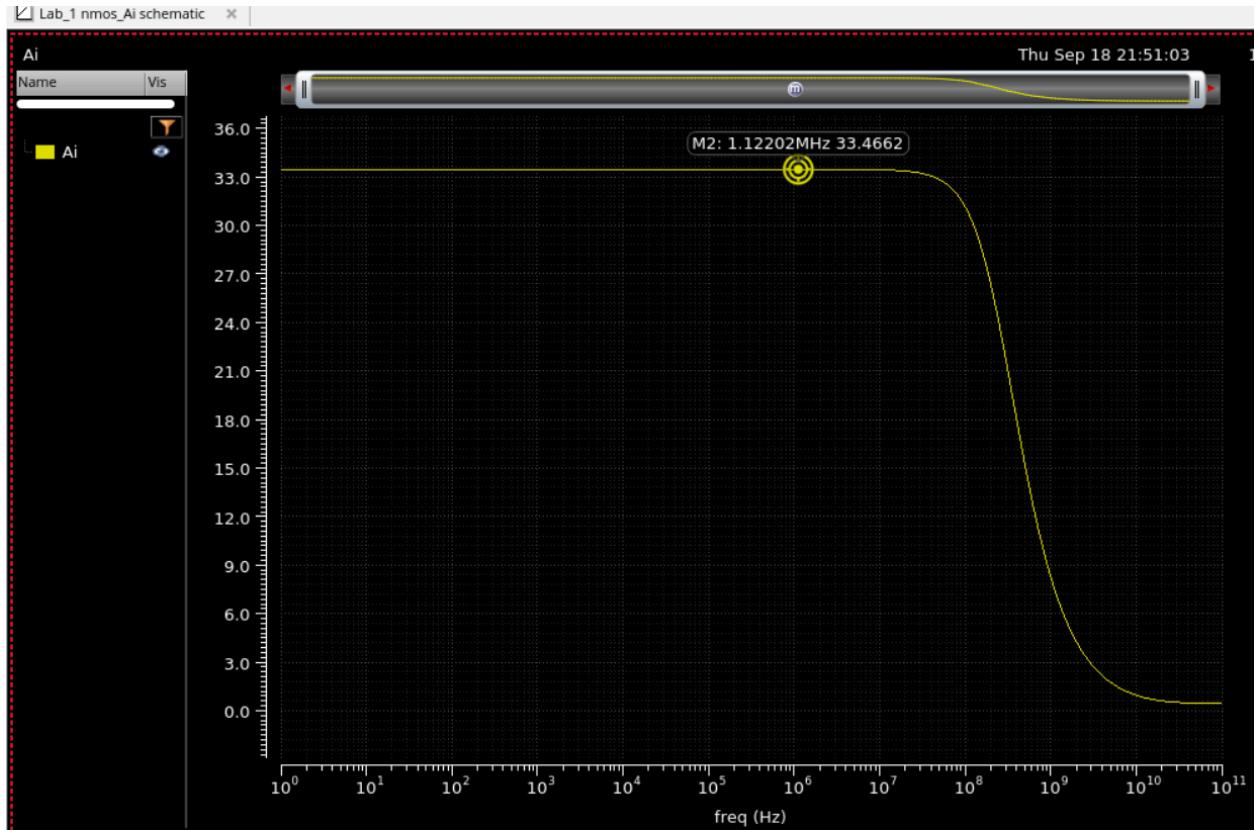




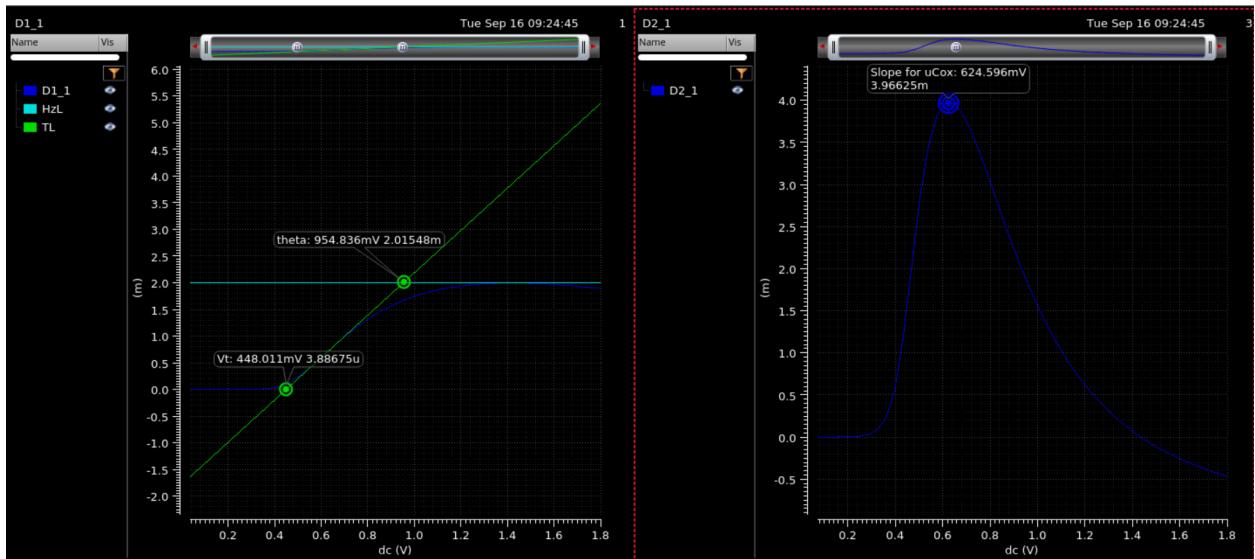
### Condition 3





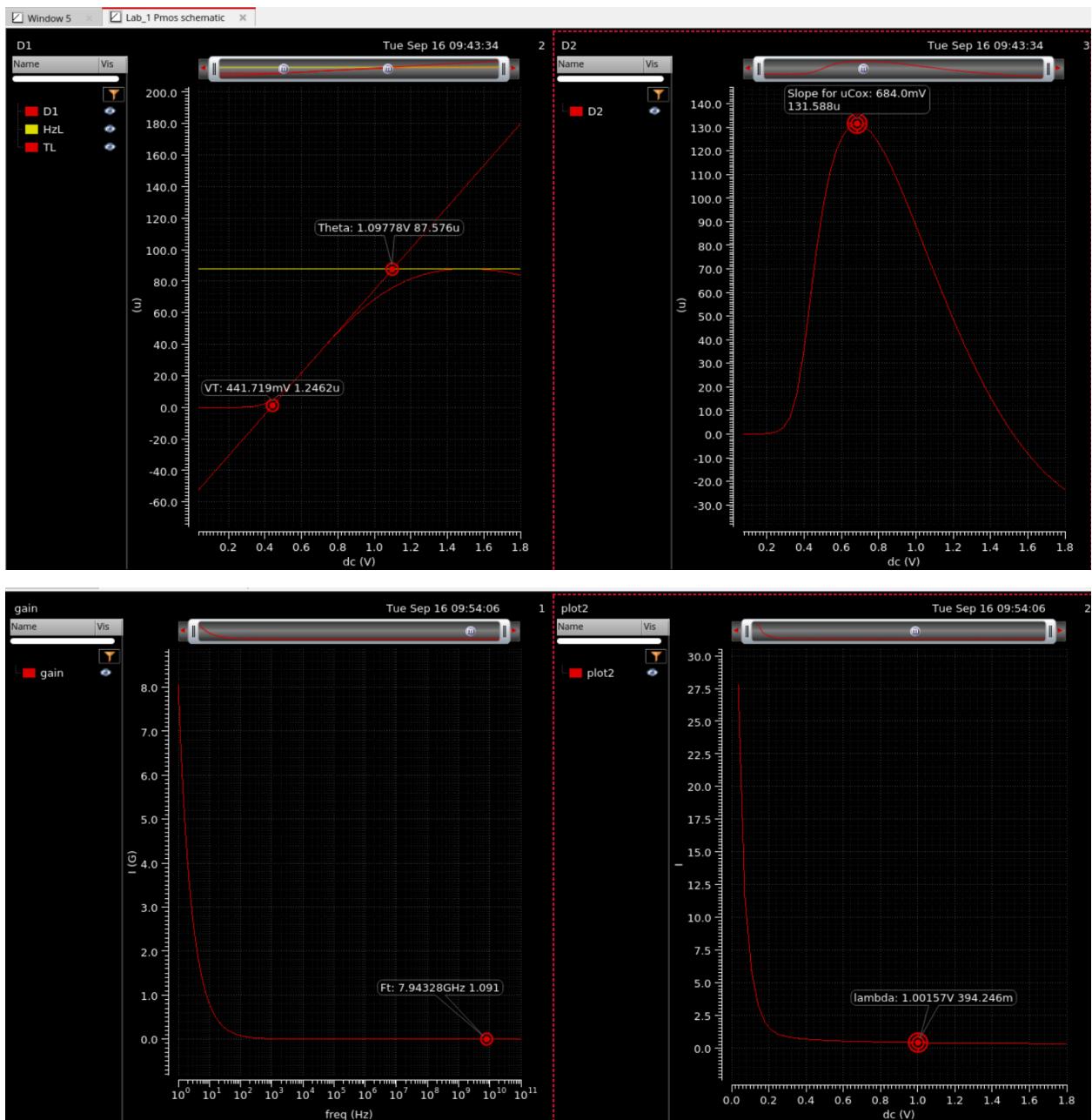


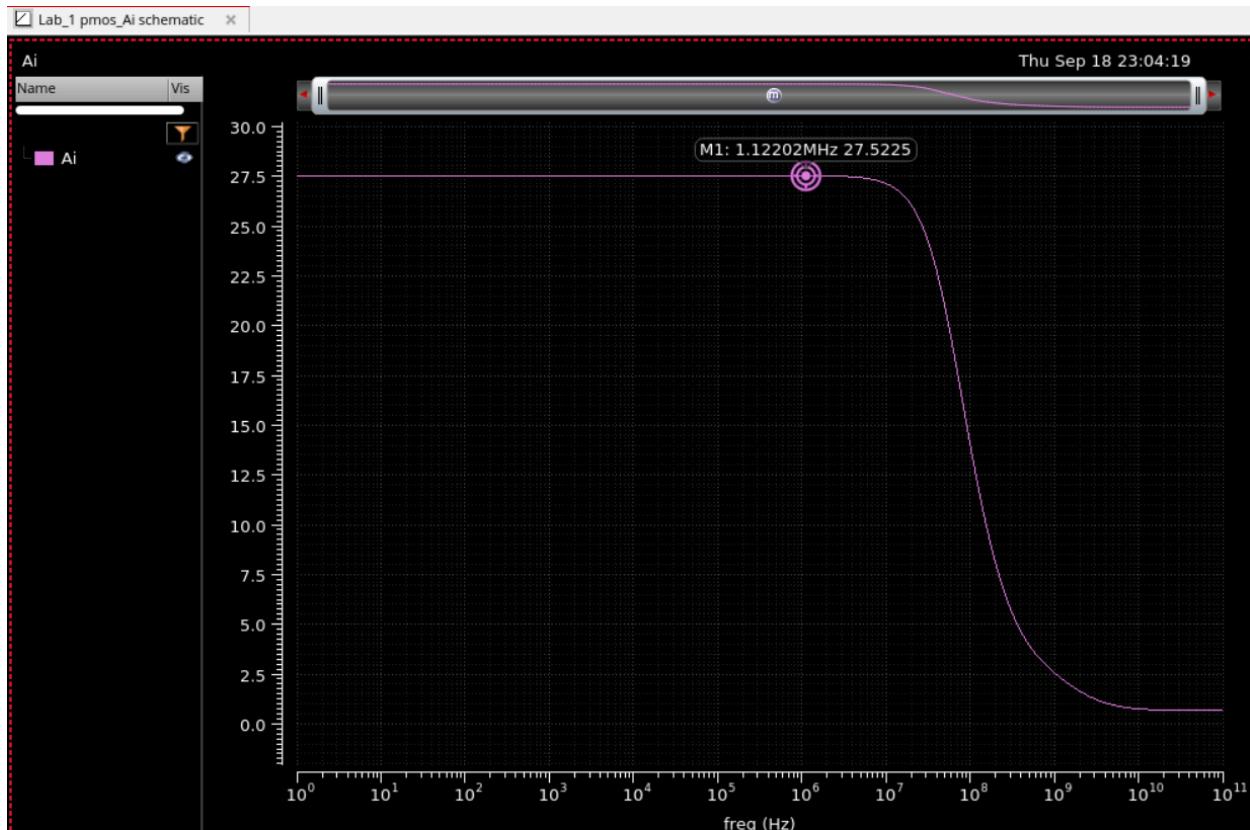
## Condition 4



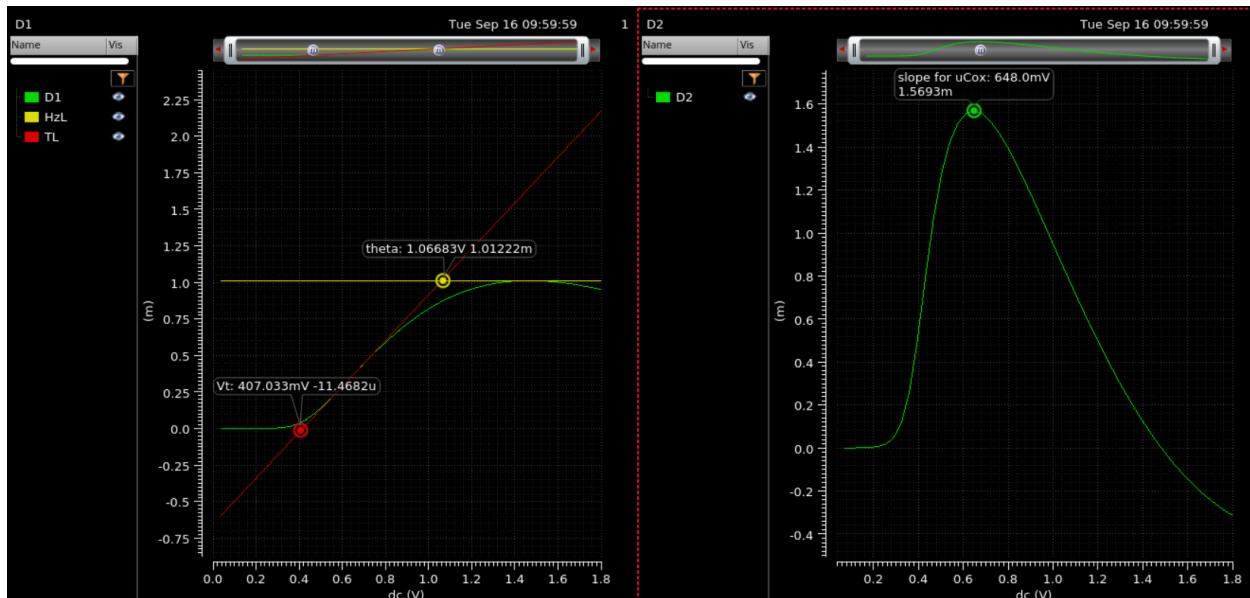


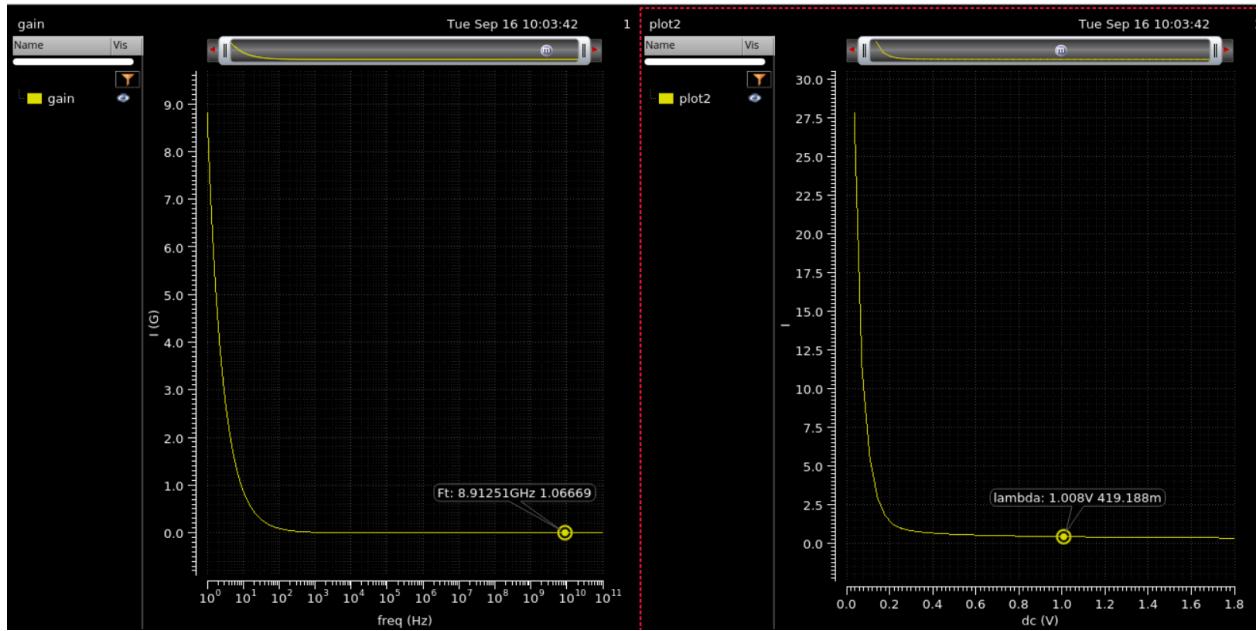
## Condition 5

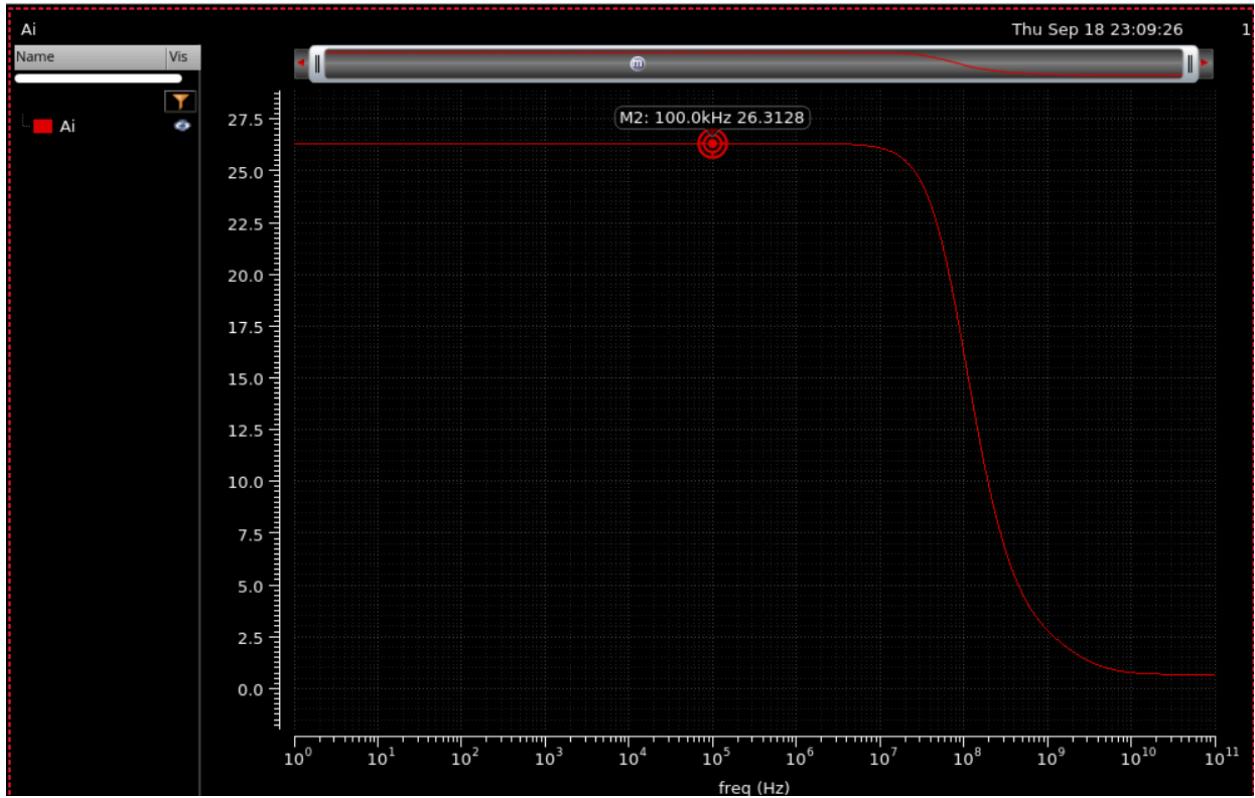




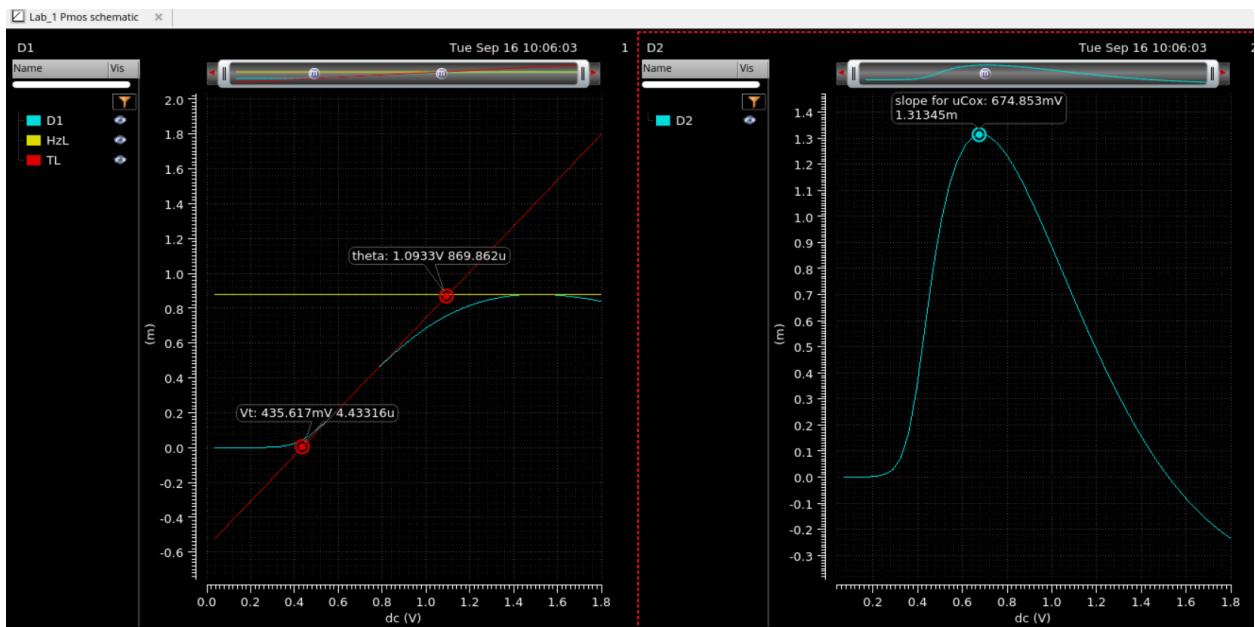
## Condition 6

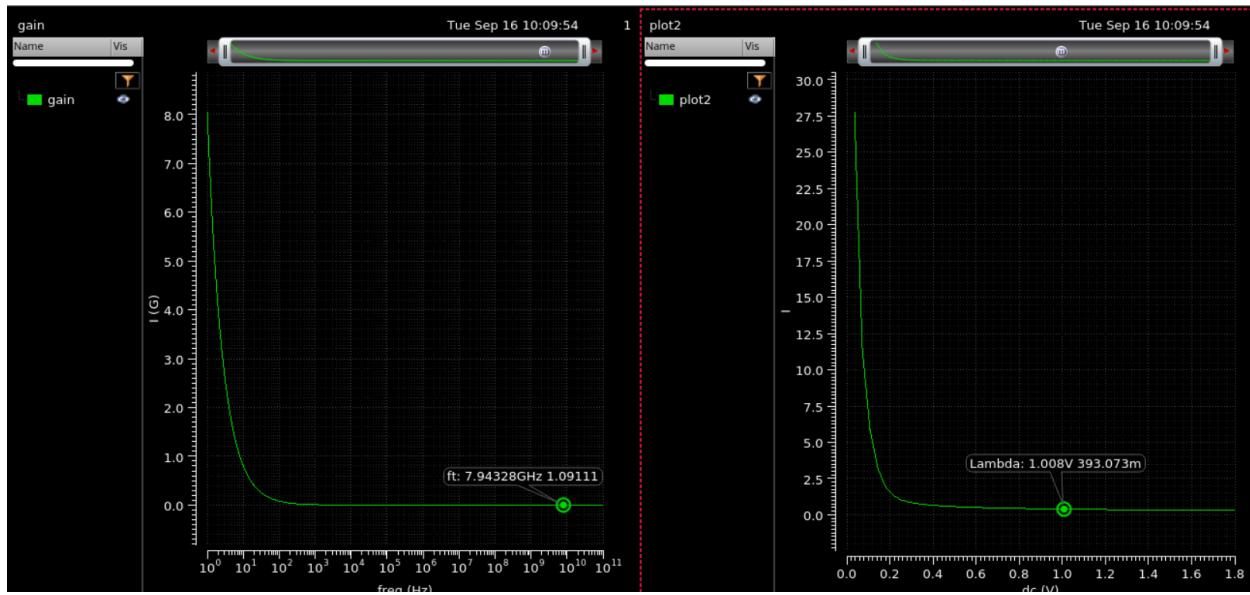


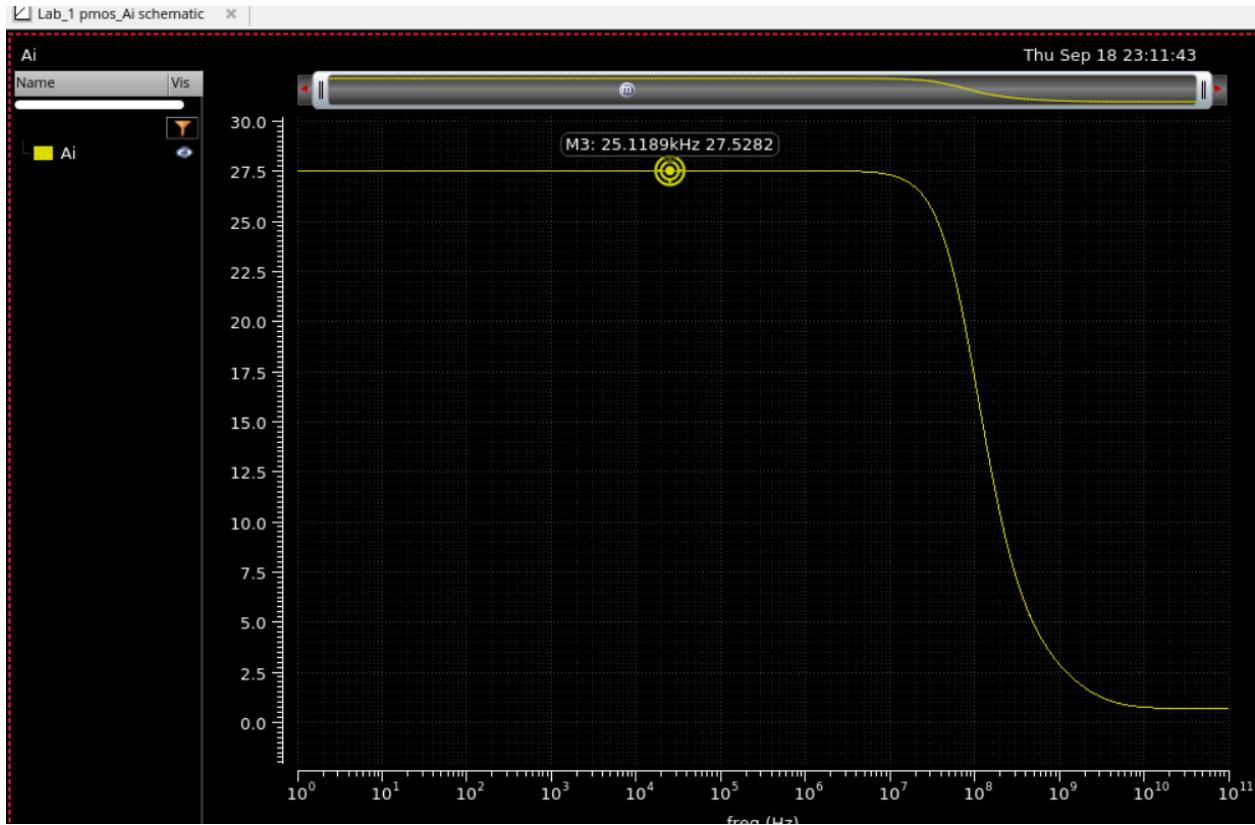




## Condition 7







## Condition 8

