

# ECEN 474/704: Lab 02

## Layout Design, Simulation and Verification in Cadence

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Due date: 2025-09-26

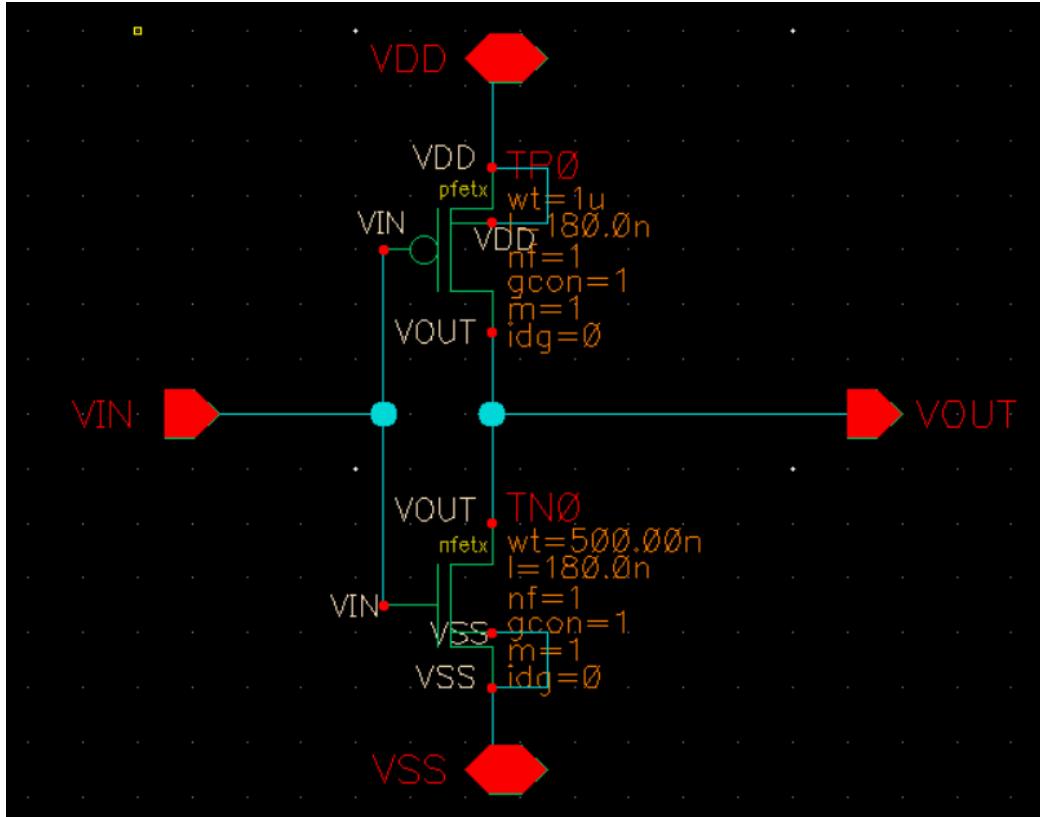
### I. DISCUSSION OF THE LAB AND RESULTS

The point of this lab was less about learning the hardware, and more about the software cadence and the manufacturing process's limitations. Designing transistor layouts such that the selected manufacturing process will be able to guarantee functionality. Therefore learning how to make the layout, verify it and ensure that the layout we design is equivalent to the schematic we based it off of.

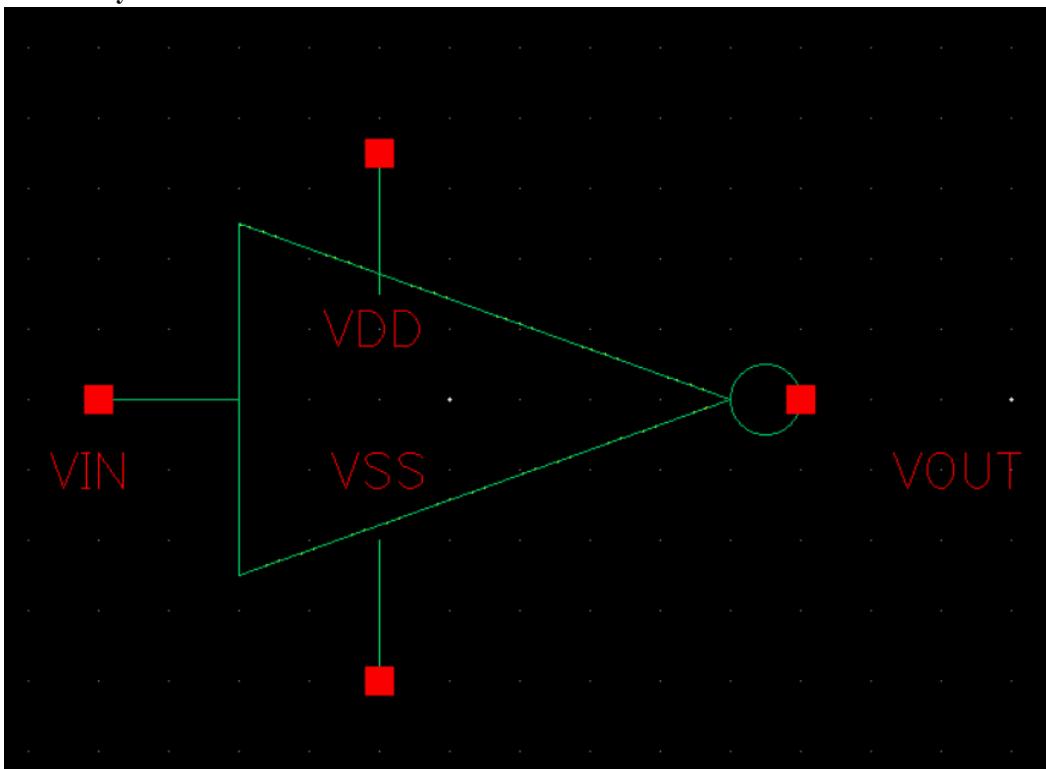
The results showed the layout designed performing slightly worse than the ideal transistor, which is to be expected. You can note that in the rise and fall of the simulations, the layout we designed had a little more "delay" in switching signals. The propagation is most likely due to non-ideal conditions about the layout being performed. However these differences are barely noticeable and will only affect us in higher frequencies when fast mobility is a requirement.

### II. SUB-CIRCUIT AND TEST BENCH SCHEMATICS

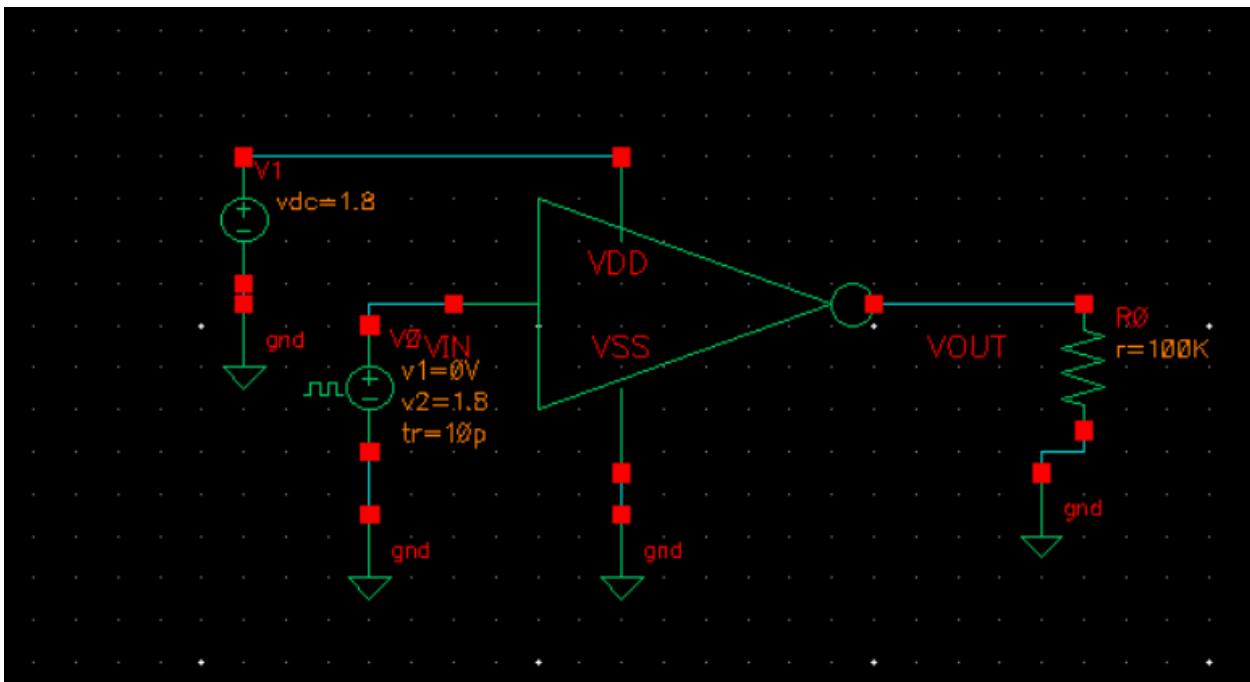
Inverter Schematic



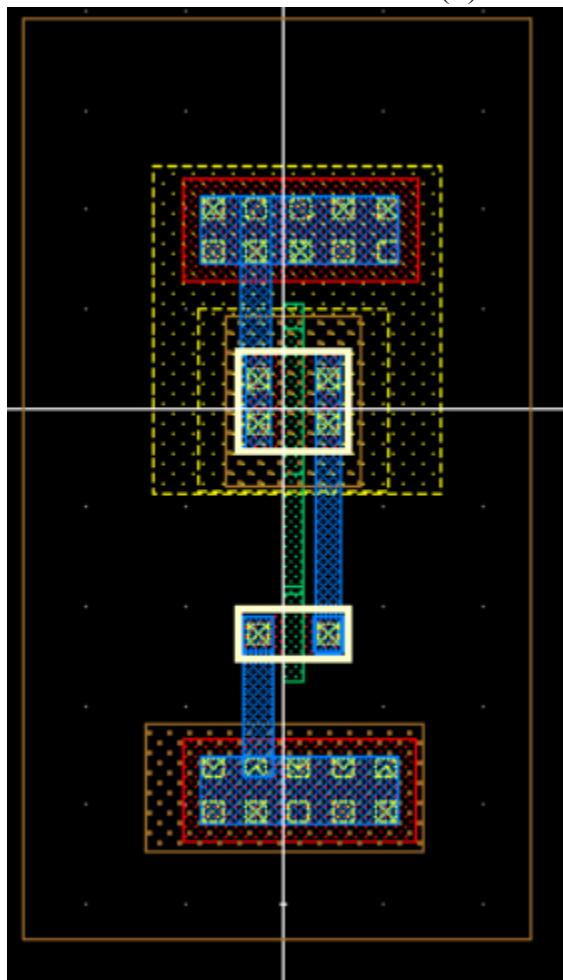
Inverter Symbol



Test bench schematic



### III. LAYOUT(S) AND FLOOR PLAN(S)



#### IV. DRC AND LVS RESULTS

**Calibre - RVE v2024.2\_29.16 : inverter.drc.results**

File View Highlight Tools Window Setup Help

Filter: Show Unresolved inverter, 2 Results (in 2 of 2503 Checks), 2 Waived

Check / Cell	Results
Check GREPDL_RX_minR	1
Check GREPDL_PC_minR	1

Rule File Pathname: [\\_cmhv7sf.drc.cal](#)  
Local PC minimum estimated density with 126 um tiling within (CHIPEDGE, CRACKSTOP), need to be >= 5 %

Calibre Run Completed Successfully -- Results are Valid

**Check GREPDL\_PC\_minR**

File Settings Configurations Help Search Calibre

inverter.lvs.report

```

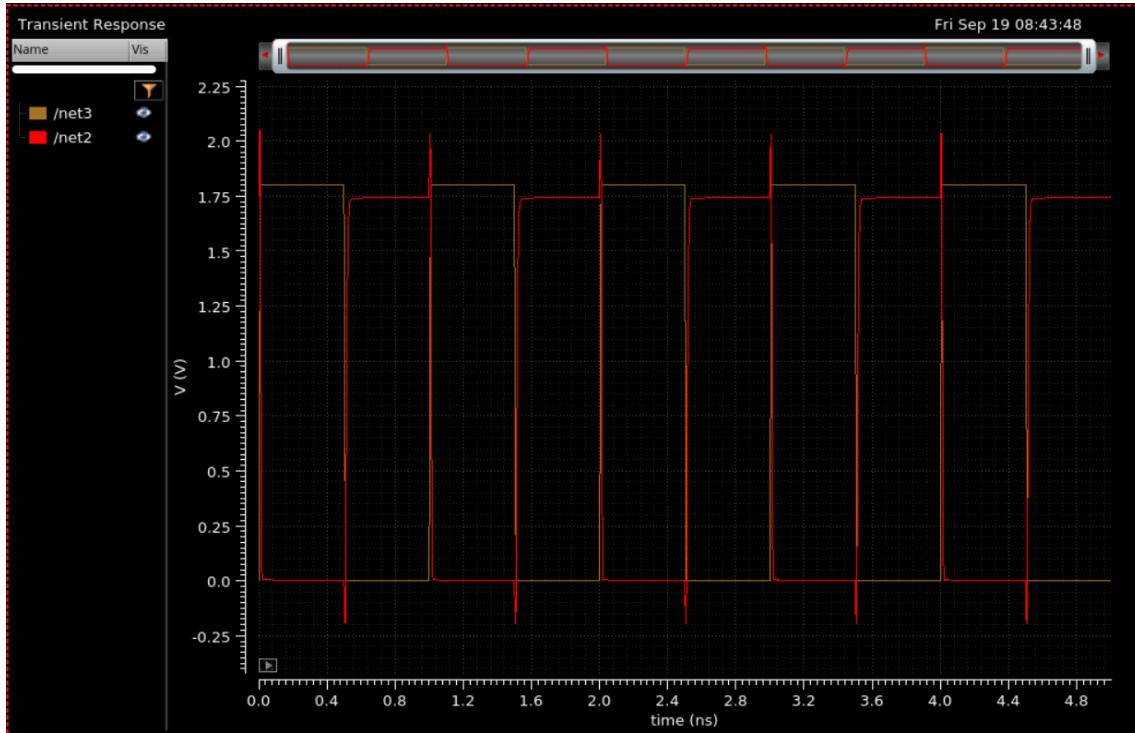
7      ##
8      ##      L V S   R E P O R T      ##
9      ##      ##
10     #####
11
12
13
14 REPORT FILE NAME:      inverter.lvs.report
15 LAYOUT NAME:          inverter.sp ('inverter')
16 SOURCE NAME:          inverter.src.net ('inverter')
17 RULE FILE:            _cmhv7sf.lvs.cal_
18 CREATION TIME:        Fri Sep 19 10:31:42 2025
19 CURRENT DIRECTORY:    /home/ugrads/s/skywalker499/CAL
20 USER NAME:            skywalker499
21 CALIBRE VERSION:      v2024.2_29.16 Thu May 2 07:35:42 PDT 2024
22
23
24
25      OVERALL COMPARISON RESULTS
26
27
28
29      #
30      #      #####      -- -
31      #      #      * *
32      #      #      CORRECT      #      |
33      #      #      #      \_/
34      #
35      #####      #####
36

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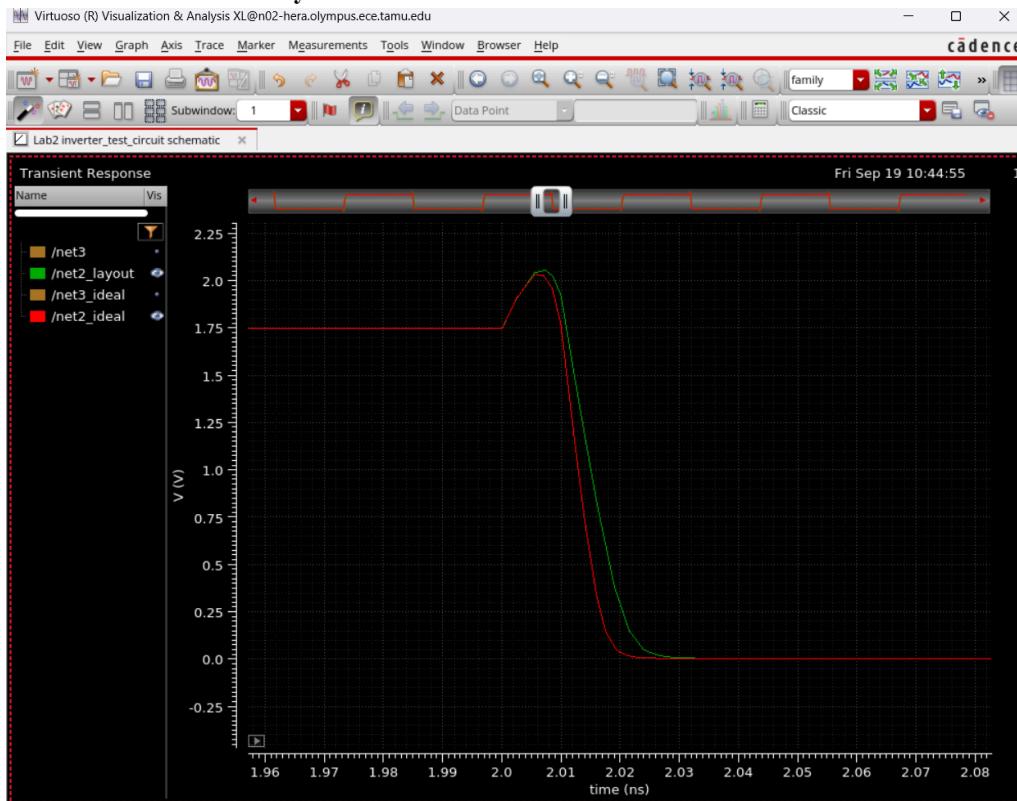
Run LVS  
Show RVE

## VI. SIMULATION RESULTS

Before layout design



### Fall difference between layout and ideal



## Rise difference between layout and ideal

