ECEN 474/704: Lab 02

Layout Design, Simulation and Verification
in Cadence

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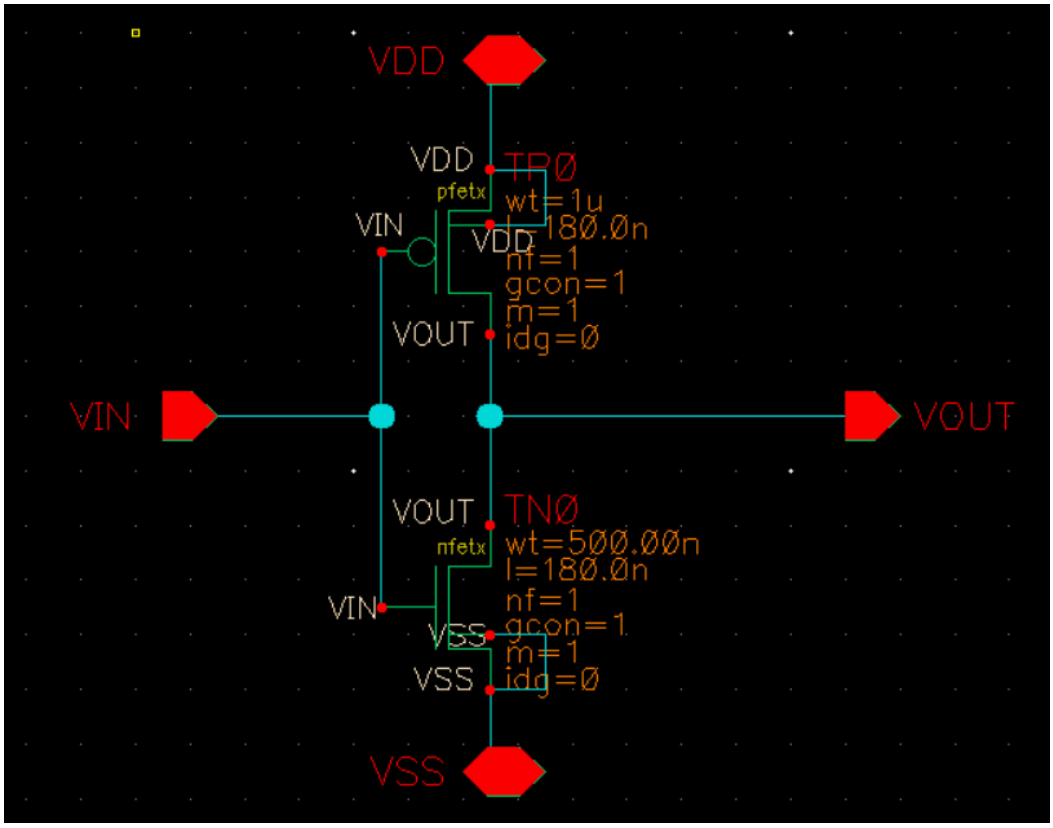
I. DISCUSSION OF THE LAB AND RESULTS

The point of this lab was less about learning the hardware, and more about the software cadence and the manufacturing process's limitations. Designing transistor layouts such that the selected manufacturing process will be able to guarantee functionality. Therefore learning how to make the layout, verify it and ensure that the layout we design is equivalent to the schematic we based it off of.

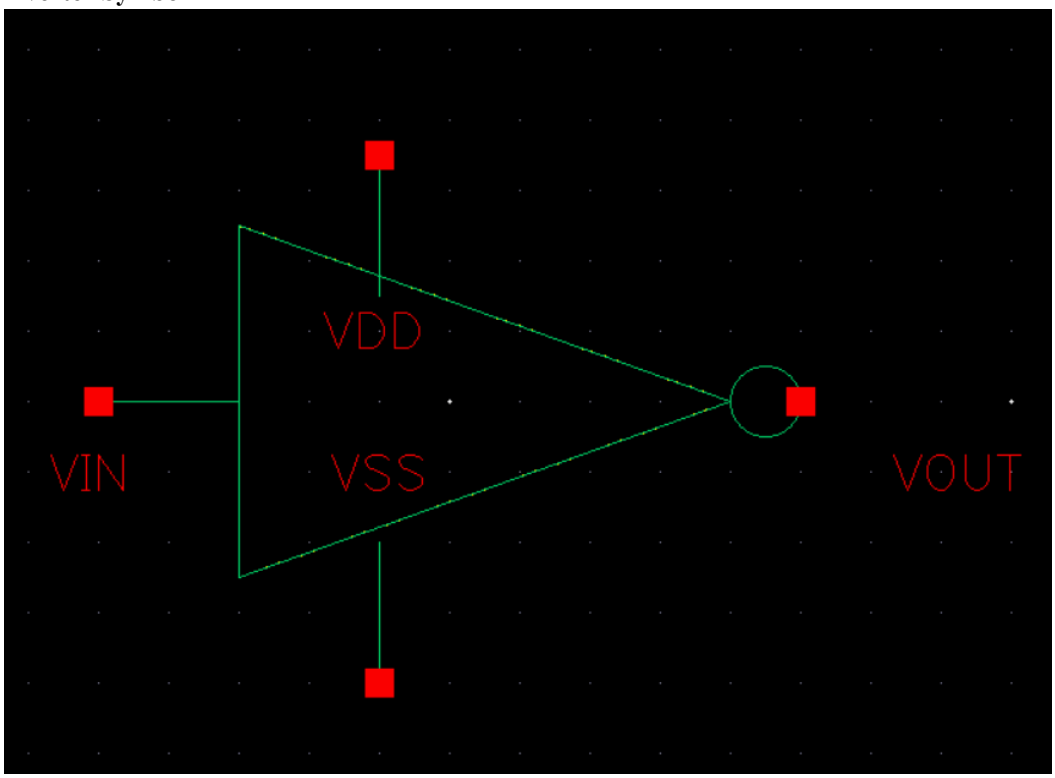
The results showed the layout designed performing slightly worse than the ideal transistor, which is to be expected. You can note that in the rise and fall of the simulations, the layout we designed had a little more "delay" in switching signals. The propagation is most likely due to non-ideal conditions about the layout being performed. However these differences are barely noticeable and will only affect us in higher frequencies when fast mobility is a requirement.

II. SUB-CIRCUIT AND TEST BENCH SCHEMATICS

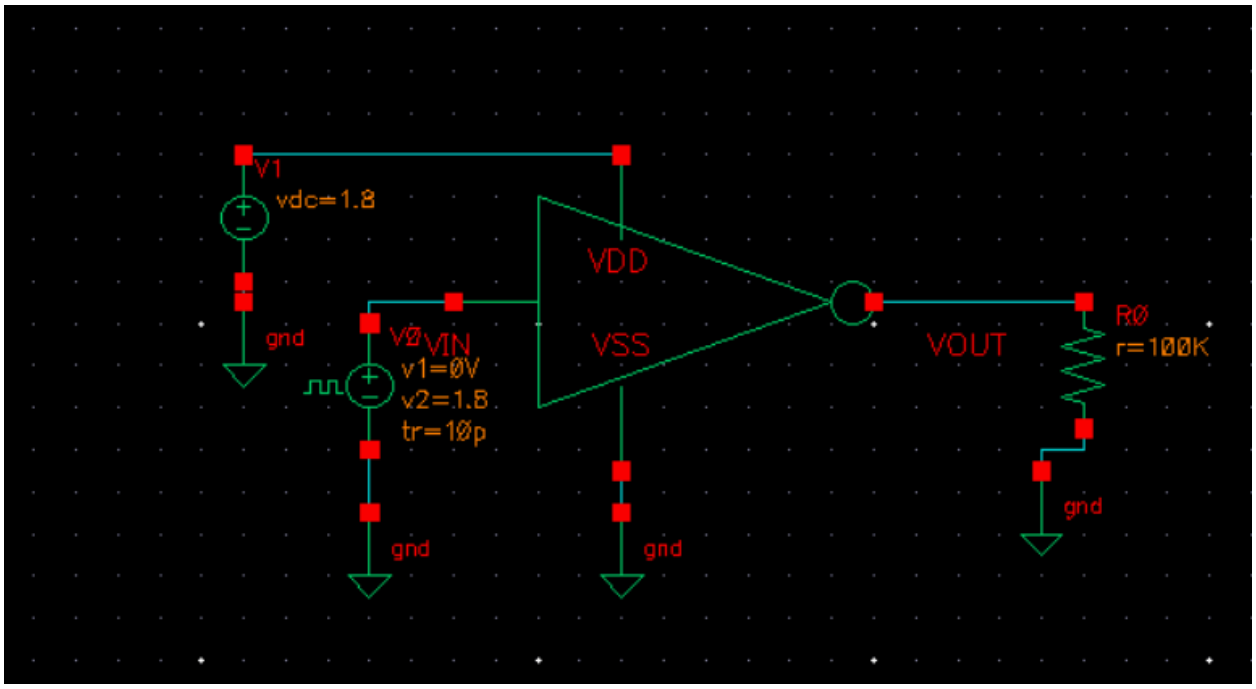
Inverter Schematic



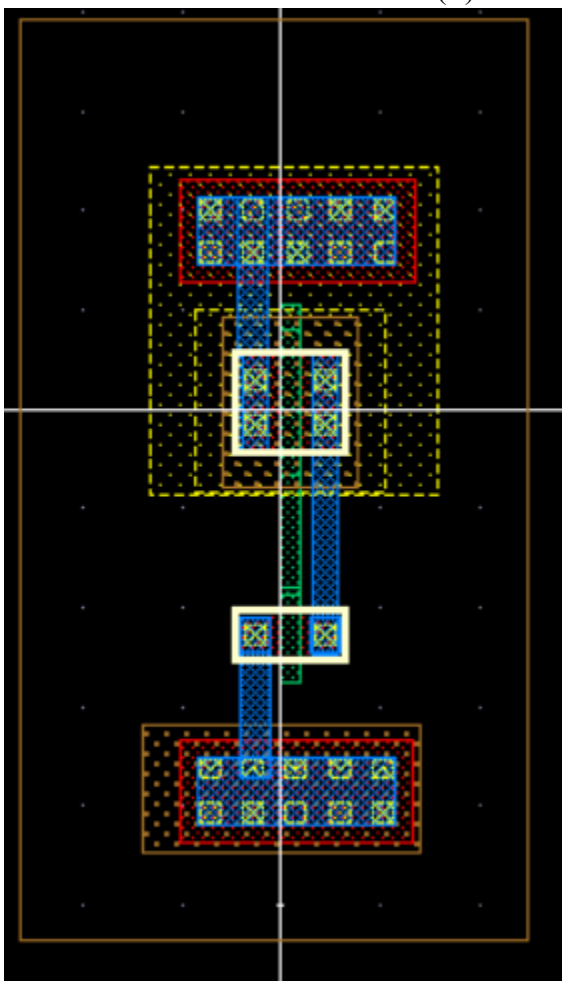
Inverter Symbol



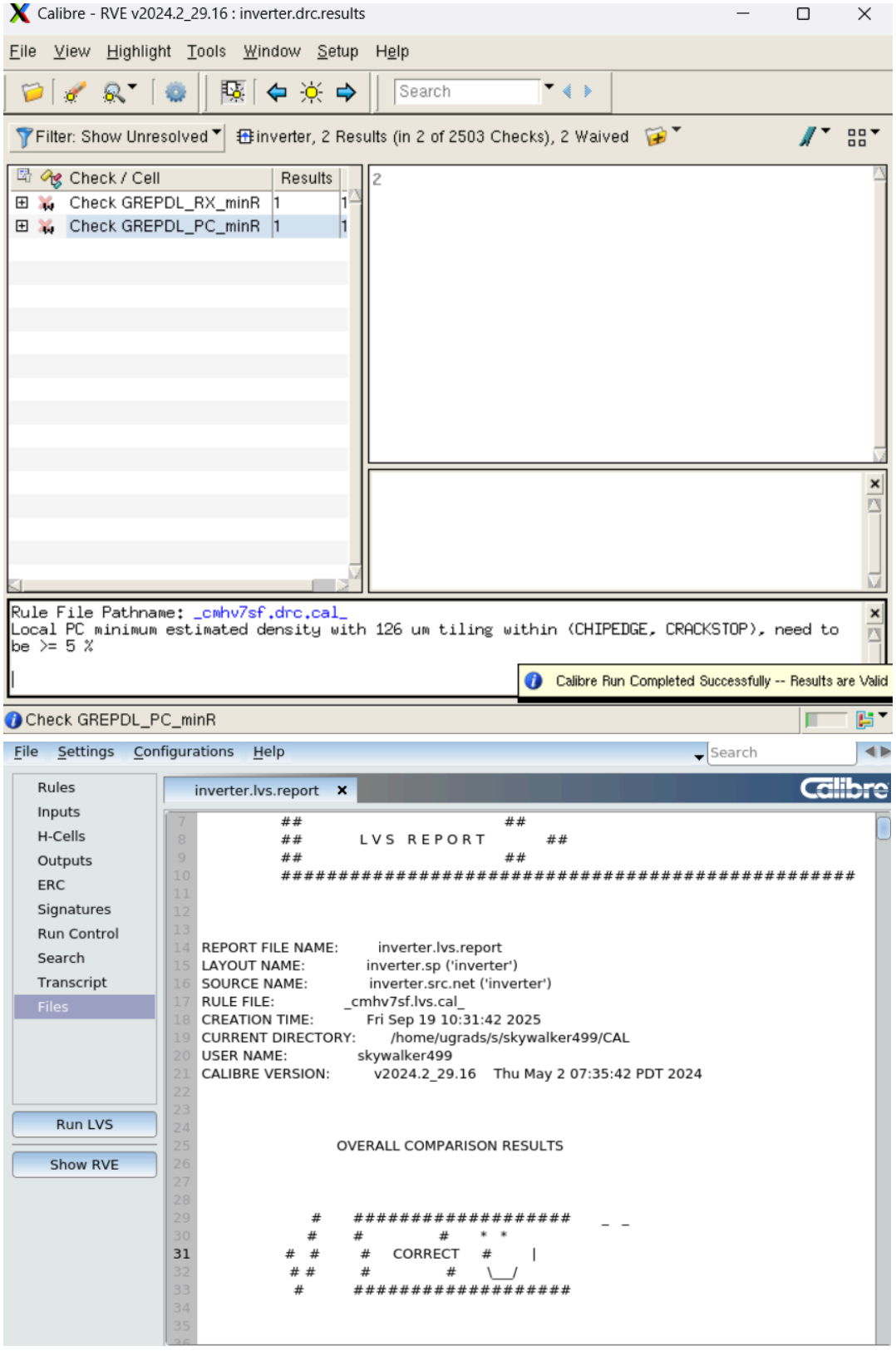
Test bench schematic



III. LAYOUT(S) AND FLOOR PLAN(S)

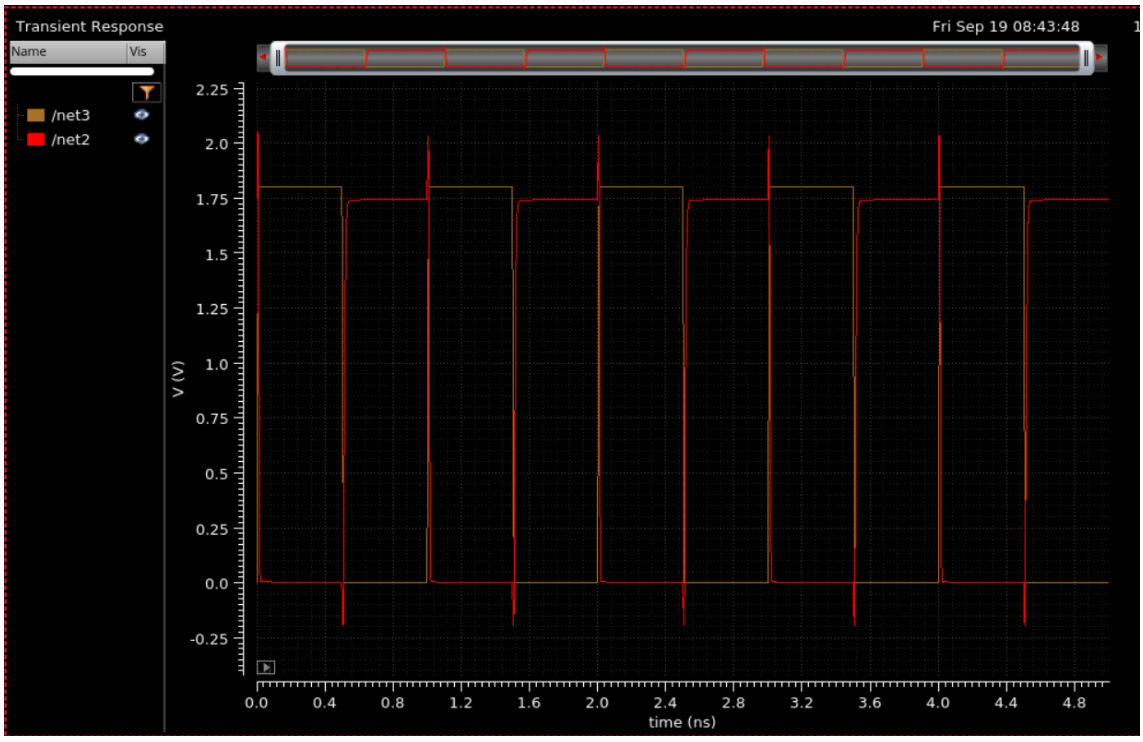


IV. DRC AND LVS RESULTS

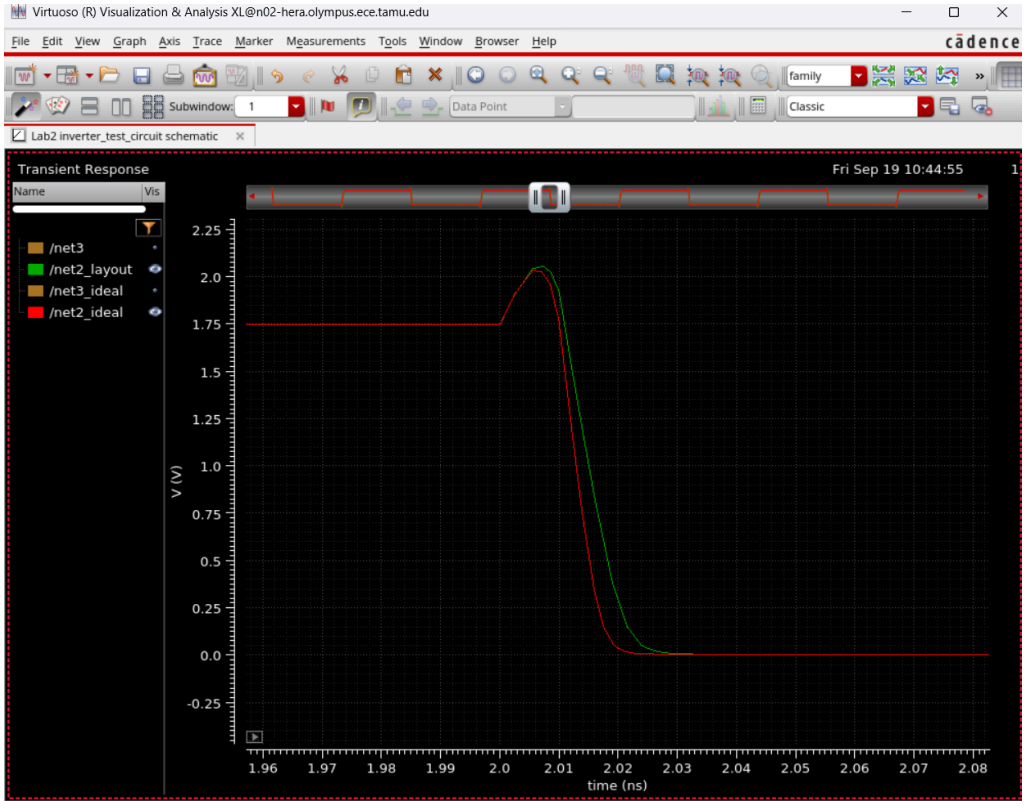


VI. SIMULATION RESULTS

Before layout design



Fall difference between layout and ideal



Rise difference between layout and ideal