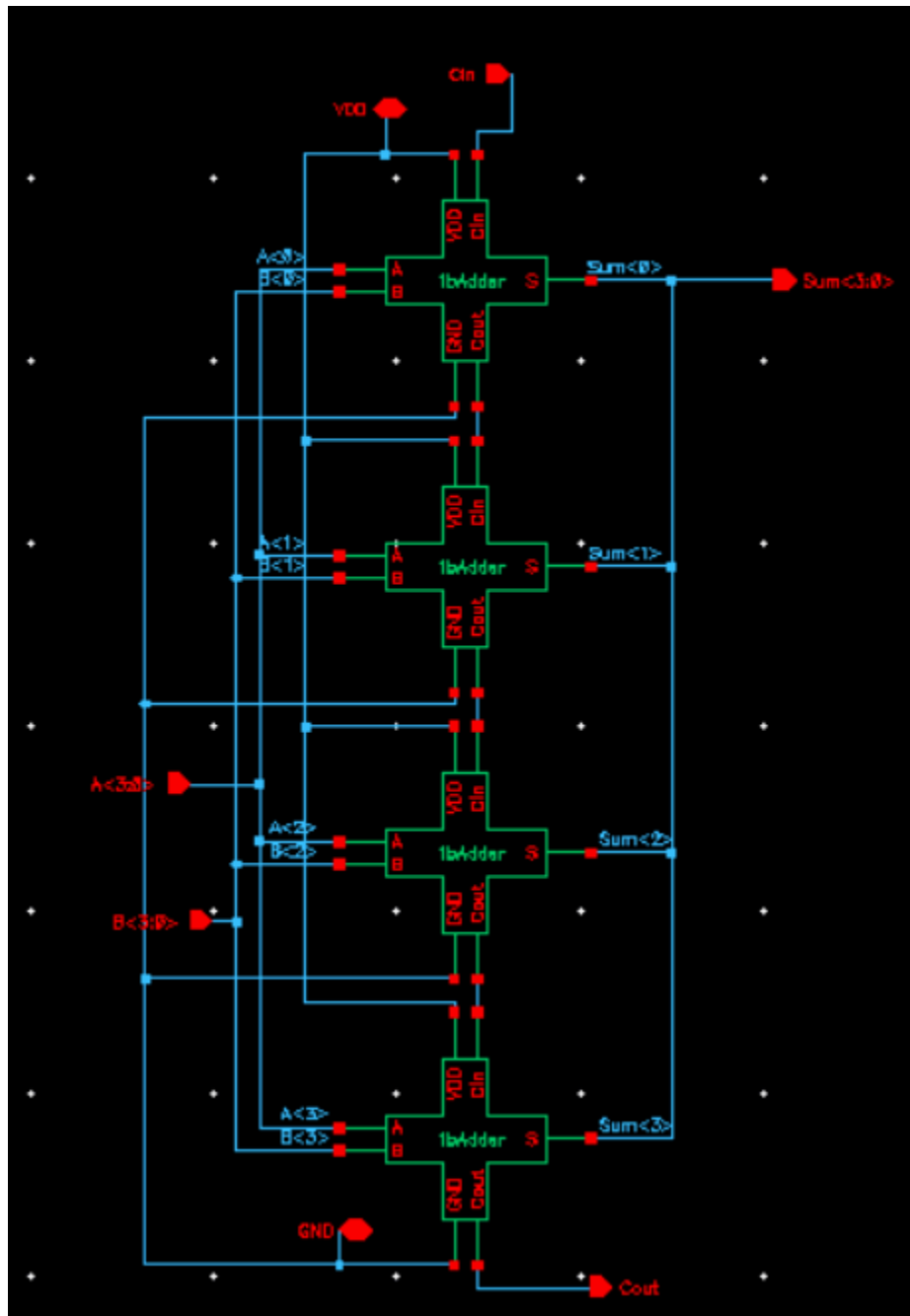
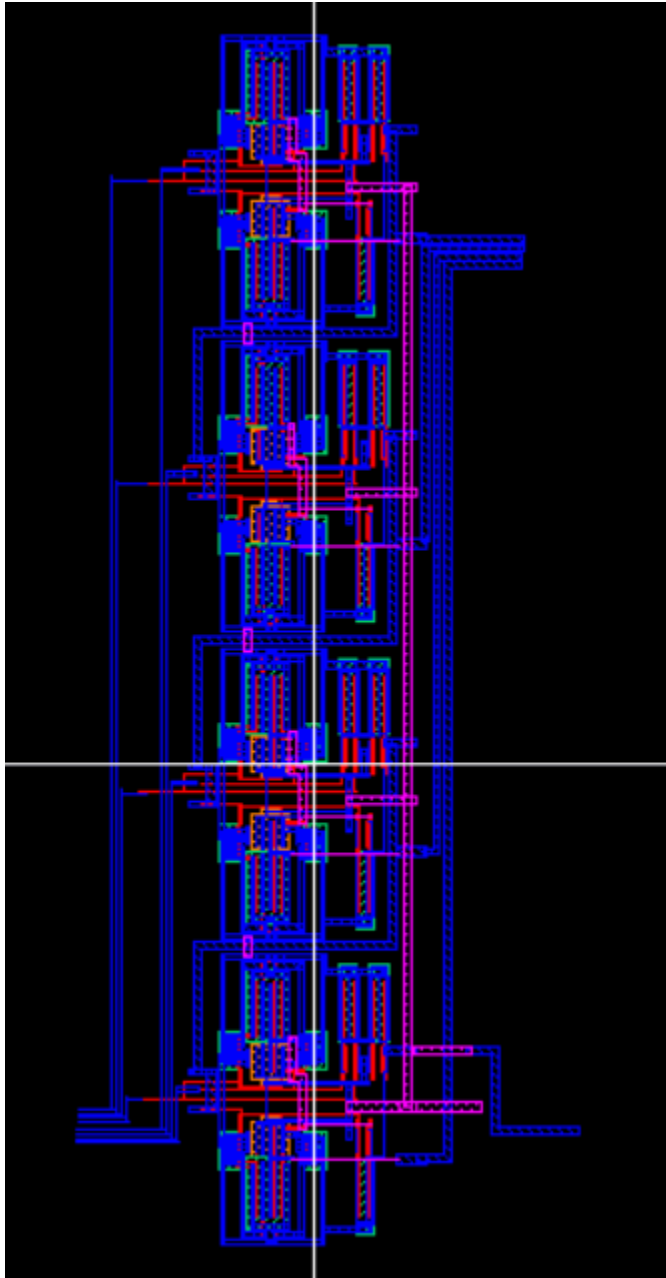


ECEN 454 - Lab 5 Report  
Luke Lopez

# Schematic



## Layout || LVS



Compiling Diva LVS rules...

```
Net-list summary for /home/ugrads/s/skywalker499/454-ECEN/LVS/layout/netlist
count
151      nets
16       terminals
1440     pmos
656      nmos
```

```
Net-list summary for /home/ugrads/s/skywalker499/454-ECEN/LVS/schematic/netlist
count
91       nets
16       terminals
72       pmos
72       nmos
```

Terminal correspondence points

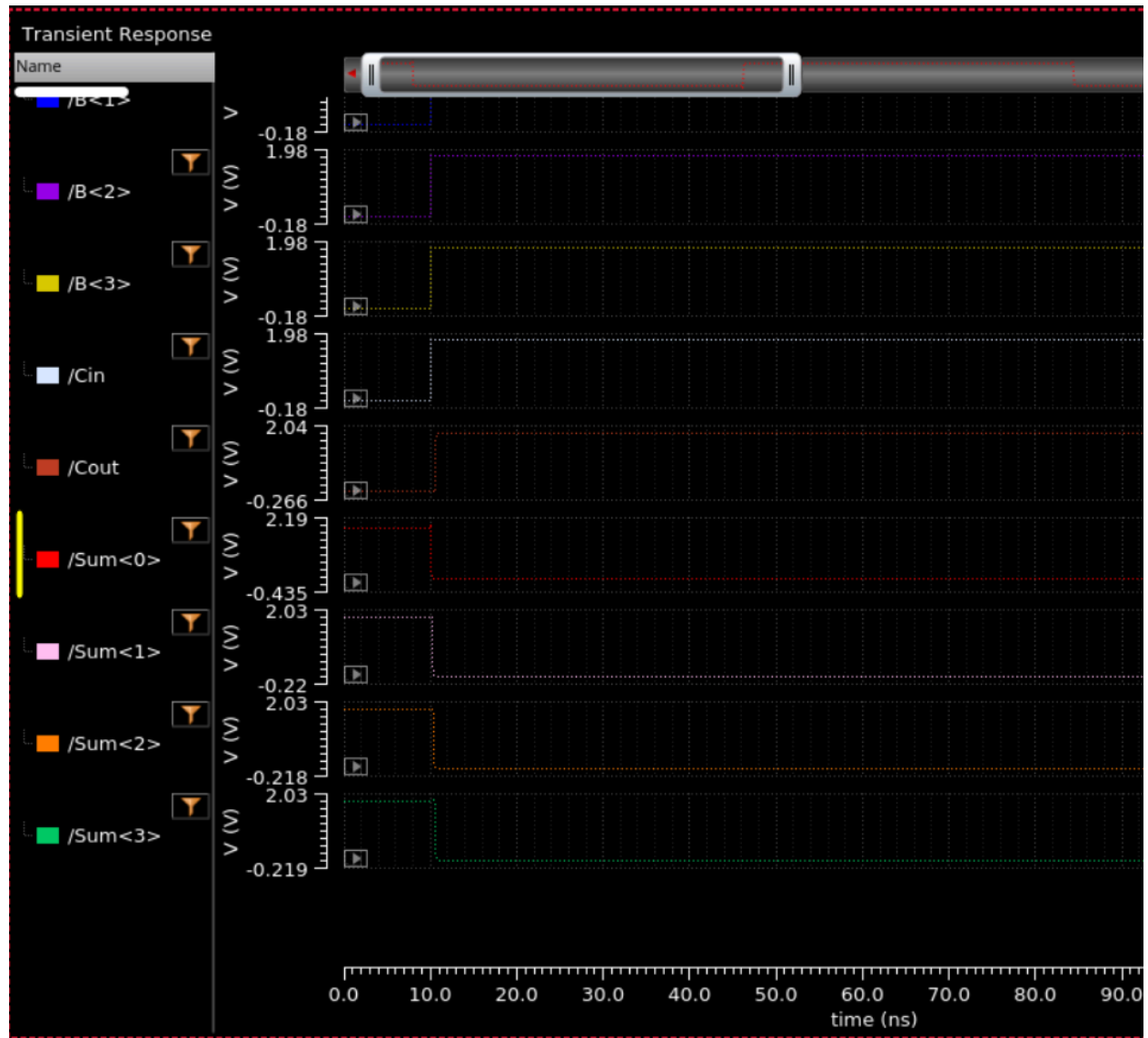
N142	N4	A<0>
N140	N3	A<1>
N137	N6	A<2>
N135	N7	A<3>
N150	N5	B<0>
N147	N0	B<1>
N145	N2	B<2>
N143	N1	B<3>
N144	N8	Cin
N146	N11	Cout
N139	N10	GND
N141	N18	Sum<0>
N138	N17	Sum<1>
N136	N16	Sum<2>
N149	N15	Sum<3>
N148	N9	VDD

Devices in the rules but not in the netlist:  
cap nfet pfet nmos4 pmos4

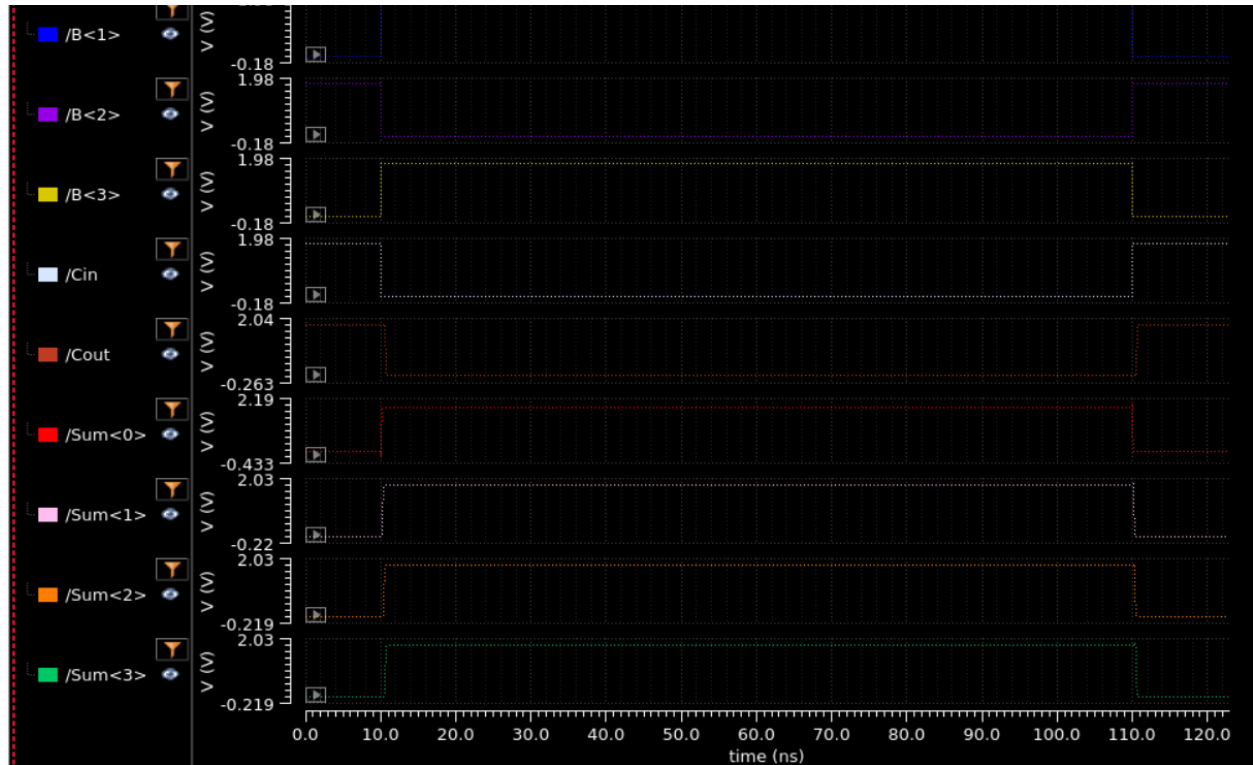
The net-lists match.

# Waveforms

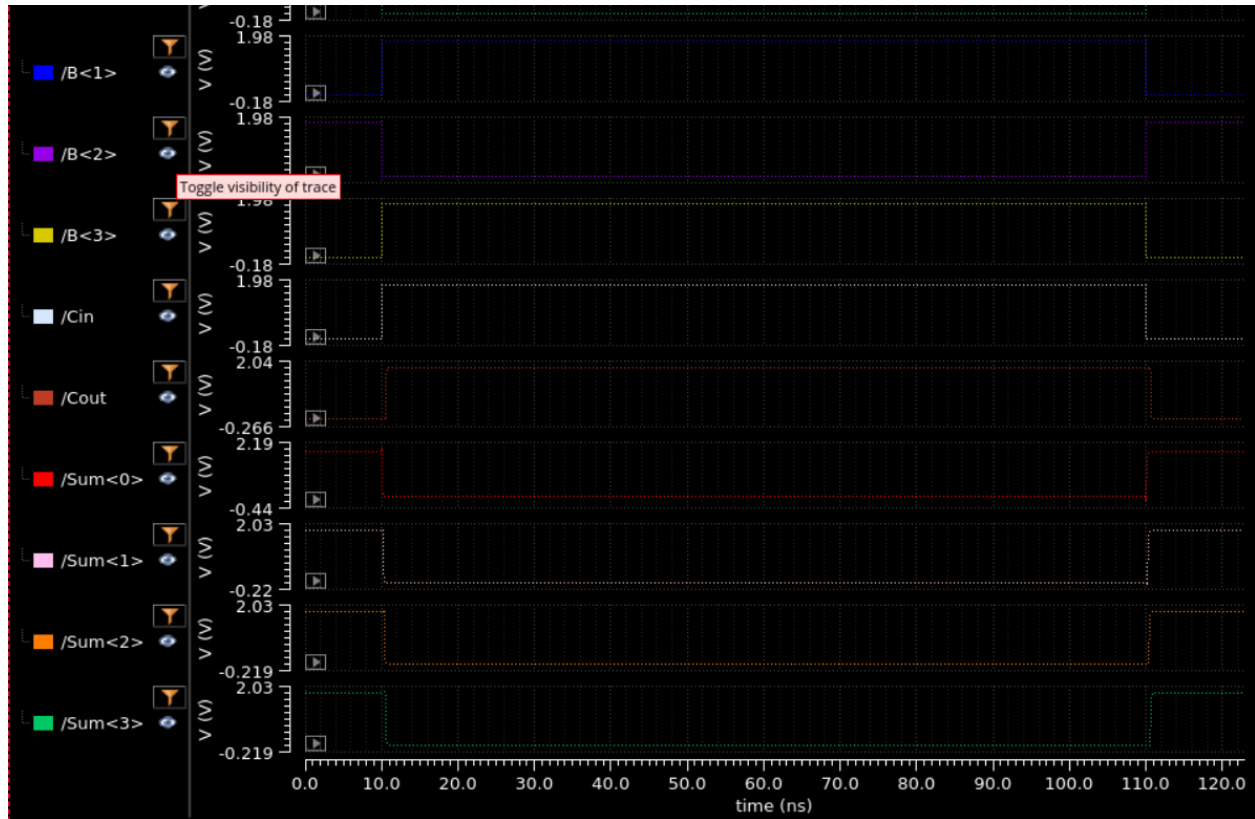
A=0000, B=1111, Carry In=1



A=1010, B=0101, Carry In=0



A=1010, B=0101, Carry In=1



A=1100, B=1000, Carry In=0

## Delays

15	D_Sum0	-64.43p
16	D_Sum<1>	-233.9p
17	D_Sum<2>	-393.3p
18	D_Sum<3>	-552.7p
19	D_Cout	-593.5p

We can see that the delays are linear, this makes sense because the values of the cout needs to ripple through to reach the actual value for its output. Cout being similar to D\_Sum<3> also

makes sense since each of these needed to go through the same number of stages. Cout is only slightly slower since it has to go through 1 extra XOR gate.

## Power

Mode	Power W
• A=0000, B=1111, Carry In=1	1.529u
A=1010, B=0101, Carry In=0	1.103u
A=1010, B=0101, Carry In=1	1.415u
A=1100, B=1000, Carry In=0	1.388u