# Section 9. Watchdog Timer and Power-up Timer

## HIGHLIGHTS

This section of the manual contains the following major topics:

**Note:** This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all PIC32 devices.

Please consult the note at the beginning of the **"Power-Saving Features"** and **"Special Features"** chapters in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

## 9.1 INTRODUCTION

The PIC32 Watchdog Timer (WDT) and Power-up Timer (PWRT) modules are described in this section. Refer to Figure 9-1 for a block diagram of the WDT and PWRT.

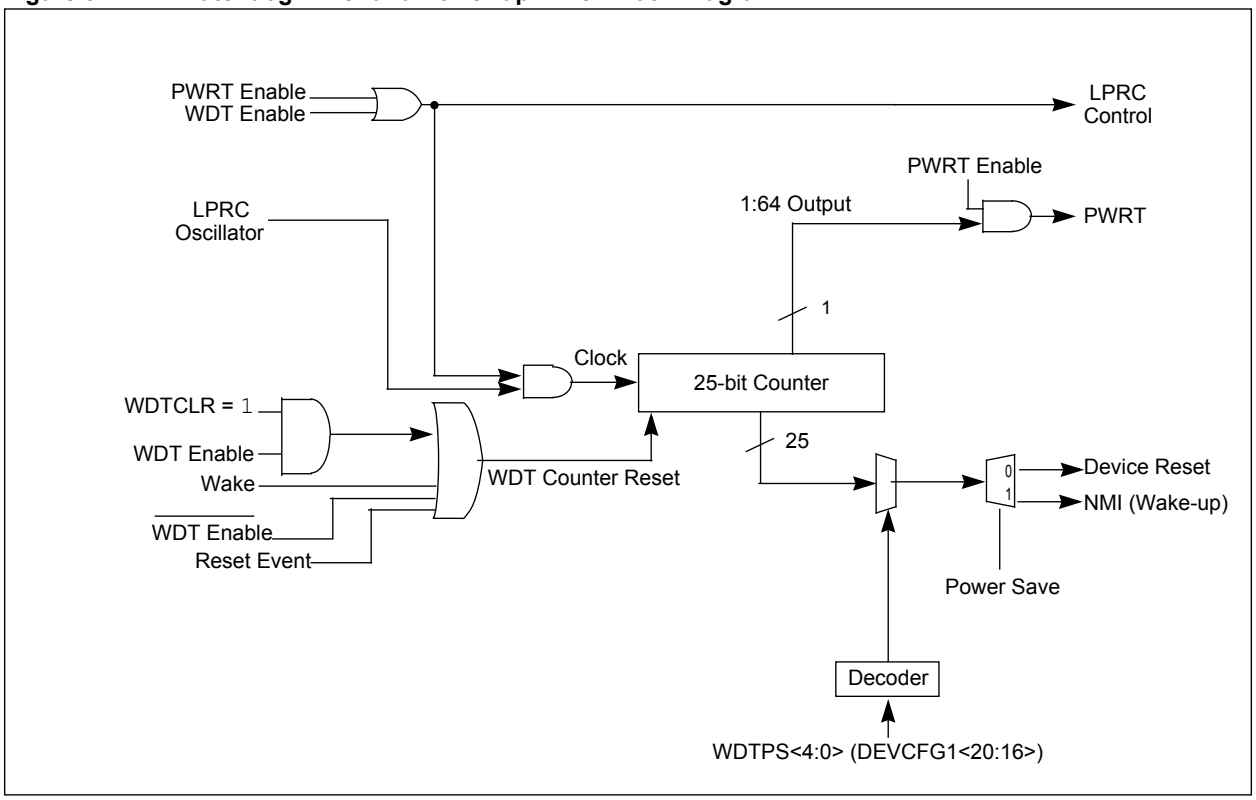
The WDT, when enabled, operates from the internal Low-Power RC (LPRC) Oscillator clock source. The WDT can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The PWRT, when enabled, holds the device in Reset for a 64 millisecond period after the normal Power-on Reset (POR) start-up period is complete. This allows additional time for the Primary Oscillator (POSC) clock source and the power supply to stabilize. Like the WDT, the PWRT also uses the LPRC as its clock source. For more information, refer to Figure 9-1.

Following are some of the key features of the WDT and PWRT modules:

- Configuration or software controlled
- User configurable time-out period
- Can wake the device from Sleep or Idle

**Figure 9-1: Watchdog Timer and Power-up Timer Block Diagram**



## 9.2 WATCHDOG TIMER AND POWER-UP TIMER CONTROL REGISTERS

The WDT and PWRT modules consist of the following Special Function Registers (SFRs):

- **WDTCON: Watchdog Timer Control Register(1,2,3)**
- **RCON: Resets Control Register(1,2,3)**

The following table provides a brief summary of the related WDT module and PWRT module registers. Corresponding registers appear after the summary, followed by a detailed description of each register.

**Table 9-1: Watchdog Timer and Power-up Timer SFR Summary**

| Name | | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| WDTCON(1,2,3) | 31:24 | — | — | — | — | — | — | — | — |
| | 23:16 | — | — | — | — | — | — | — | — |
| | 15:8 | ON | — | — | — | — | — | — | — |
| | 7:0 | — | SWDTPS<4:0> | | | | | — | WDTCLR |
| RCON(1,2,3,4) | 31:24 | — | — | — | — | — | — | — | — |
| | 23:16 | — | — | — | — | — | — | — | — |
| | 15:8 | — | — | — | — | — | — | CM | VREGS |
| | 7:0 | EXTR | SWR | — | WDTO | SLEEP | IDLE | BOR | POR |

**Legend:** — = unimplemented, read as '0'.

**Note 1:** This register has an associated Clear register at an offset of 0x4 bytes. These registers have the same name with CLR appended to the end of the register name (e.g., WDTCONCLR). Writing a '1' to any bit position in the Clear register will clear valid bits in the associated register. Reads from the Clear register should be ignored.

**2:** This register has an associated Set register at an offset of 0x8 bytes. These registers have the same name with SET appended to the end of the register name (e.g., WDTCONSET). Writing a '1' to any bit position in the Set register will set valid bits in the associated register. Reads from the Set register should be ignored.

**3:** This register has an associated Invert register at an offset of 0xC bytes. These registers have the same name with INV appended to the end of the register name (e.g., WDTCONINV). Writing a '1' to any bit position in the Invert register will invert valid bits in the associated register. Reads from the Invert register should be ignored.

**4:** Shaded bit names in this register are not associated with the WDT or PWRT modules.

**Register 9-1: WDTCON: Watchdog Timer Control Register(1,2,3)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 31 | | | | | | | bit 24 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 23 | | | | | | | bit 16 |

| R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| ON(4,5) | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R-x | R-x | R-x | R-x | R-x | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SWDTPS<4:0> | | | | | — | WDTCLR |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | P = Programmable bit | r = Reserved bit |
| U = Unimplemented bit | -n = Bit Value at POR: (‘0’, ‘1’, x = Unknown) | | |

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** Watchdog Timer Enable bit(4,5)
- 1 = Enables the WDT if it is not enabled by the device configuration
- 0 = Disable the WDT if it was enabled in software

bit 14-7 **Unimplemented:** Read as ‘0’

bit 6-2 **SWDTPS<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value from Device Configuration bits
On reset, these bits are set to the values of the WDTPS <4:0> Configuration bits.

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **WDTCLR:** Watchdog Timer Reset bit
- 1 = Writing a ‘1’ will clear the WDT
- 0 = Software cannot force this bit to a ‘0’

**Note 1:** This register has an associated Clear register (WDTCONCLR) at an offset of 0x4 bytes. Writing a ‘1’ to any bit position in the Clear register will clear valid bits in the associated register. Reads from the Clear register should be ignored.

**2:** This register has an associated Set register (WDTCONSET) at an offset of 0x8 bytes. Writing a ‘1’ to any bit position in the Set register will set valid bits in the associated register. Reads from the Set register should be ignored.

**3:** This register has an associated Invert register (WDTCONINV) at an offset of 0xC bytes. Writing a ‘1’ to any bit position in the Invert register will invert valid bits in the associated register. Reads from the Invert register should be ignored.

**4:** A read of this bit will result in a ‘1’ if the WDT is enabled by the device configuration or by software.

**5:** When using the 1:1 PBCLK divisor, the user’s software should not read or write the peripheral’s SFRs in the SYSCLK cycle immediately following the instruction that clears the module’s ON bit.

**Register 9-2: RCON: Resets Control Register(1,2,3)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 31 | | | | | | | bit 24 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 23 | | | | | | | bit 16 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | r-0 | r-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | CM(4) | VREGS(4) |
| bit 15 | | | | | | | bit 8 |

| r-0 | r-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | r-0 | r0 |
|---|---|---|---|---|---|---|---|
| EXTR(4) | SWR(4) | — | WDTO | SLEEP | IDLE | BOR(4) | POR(4) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | P = Programmable bit | r = Reserved bit |
| U = Unimplemented bit | -n = Bit Value at POR: (‘0’, ‘1’, x = Unknown) | | |

bit 31-10 **Unimplemented:** Read as ‘0’

bit 9-6 **Reserved:** Do not use

bit 5 **Unimplemented:** Read as ‘0’

bit 4 **WDTO:** Watchdog Time-out bit
- 1 = A WDT time-out has occurred since either the device was powered up or the WDTO bit was last cleared by software
- 0 = A WDT time-out has not occurred since either the WDTO bit was cleared by software or the device was reset

bit 3 **SLEEP:** Sleep Event bit
- 1 = The device was in Sleep since either the device was powered up or the SLEEP bit was last cleared by software
- 0 = The device was not in Sleep since either the SLEEP bit was cleared by software or the device was reset

bit 2 **IDLE:** Idle Event bit
- 1 = The device has been in Idle mode since either the device was powered up or the IDLE bit was last cleared by software
- 0 = The device has not been in Idle mode since either the IDLE bit was cleared by software or the device was reset

bit 1-0 **Reserved:** Do not use

**Note 1:** This register has an associated Clear register (RCONCLR) at an offset of 0x4 bytes. Writing a ‘1’ to any bit position in the Clear register will clear valid bits in the associated register. Reads from the Clear register should be ignored.

**2:** This register has an associated Set register (RCONSET) at an offset of 0x8 bytes. Writing a ‘1’ to any bit position in the Set register will set valid bits in the associated register. Reads from the Set register should be ignored.

**3:** This register has an associated Invert register (RCONINV) at an offset of 0xC bytes. Writing a ‘1’ to any bit position in the Invert register will invert valid bits in the associated register. Reads from the Invert register should be ignored.

**4:** Shaded bit names in this register are not associated with the WDT or PWRT modules.

## 9.3 OPERATION

If enabled, the WDT will increment until it overflows or “times out”. A WDT time-out will force a device Reset, except during Sleep or Idle modes. To prevent a WDT time-out Reset, the user must periodically clear the WDT by setting the WDTCLR bit (WDTCON<0>).

The WDT module uses the LPRC Oscillator for reliability.

| **Note:** | The LPRC Oscillator is enabled whenever the WDT is enabled. |
|---|---|

### 9.3.1 Enabling and Disabling the WDT

The WDT is enabled or disabled by the device configuration or controlled through software by writing to the WDTCON register.

### 9.3.2 Device Configuration Controlled WDT

If the FWDTEN Configuration bit (DEVCFG1<23>) is set, the WDT is always enabled. The WDT ON control bit (WDTCON<15>) will reflect this by reading a ‘1’. In this mode, the ON bit cannot be cleared in software. This bit will not be cleared by any form of reset. To disable the WDT in this mode, the configuration must be rewritten to the device.

| **Note:** | The default state for the WDT on an unprogrammed device is WDT enabled. |
|---|---|

### 9.3.3 Software Controlled WDT

If the FWDTEN Configuration bit is a ‘0’, the WDT module can be enabled or disabled (the default condition) by software. In this mode, the ON bit (WDTCON<15>) reflects the status of the WDT under software control. A ‘1’ indicates the WDT module is enabled and a ‘0’ indicates it is disabled.

The WDT is enabled in software by setting the WDT ON control bit. The WDT ON control bit is cleared on any device Reset. The bit is not cleared upon a wake from Sleep or exit from Idle mode. The software WDT option allows the user to enable the WDT for critical code segments and disable the WDT during noncritical segments for maximum power savings. This bit can also be used to disable the WDT while the device is awake to eliminate the need for WDT servicing, and then re-enable it before the device is put into Idle or Sleep to wake the device at a later time. Example 9-1 shows the WDT initialization and servicing sample.

**Example 9-1: Sample WDT Initialization and Servicing**

```
//This code fragment assumes the WDT was not enabled by the device configuration
    // The Postscaler value must be set with the device configuration

    WDTCONSET = 0x8000;         // Turn on the WDT

    main
    {
        WDTCONSET = 0x01;       // Service the WDT
        ... User code goes here ...
    }
```

### 9.3.4 WDT Operation in Power-Saving Modes

The WDT, if enabled, will continue operation in Sleep or Idle modes. The WDT module may be used to wake the device from Sleep or Idle mode. When the WDT times out in a power-saving mode, a Non-Maskable Interrupt (NMI) is generated and the WDTO bit (RCON<4>) is set. The NMI vectors execution to the CPU start-up address, but does not reset registers or peripherals. If the device was in Sleep, the SLEEP status bit (RCON<3>) will also be set. If the device was in Idle, the IDLE status bit (RCON<2>) will also be set. These bits allow the start-up code to determine the cause of the wake-up.

### 9.3.5 Time Delays on Wake

There will be a time delay between the WDT event in Sleep and the beginning of code execution. The duration of this delay consists of the start-up time for the oscillator in use and the power-up timer delay, if it is enabled.

Unlike a wake-up from Sleep mode, there are no time delays associated with wake-up from Idle mode. The system clock is running during Idle mode; therefore, no start-up delays are required at wake-up.

### 9.3.6 Resetting the WDT

The WDT is cleared by any of the following:

- On any device Reset
- By a `WDTCONSET = 0x01` or equivalent instruction during normal execution
- Execution of a `DEBUG` command
- Exiting from Idle or Sleep due to an interrupt

**Note:** The WDT is not reset when the device enters a power-saving mode. The WDT module should be serviced prior to entering a power-saving mode.

### 9.3.7 WDT Period Selection

The WDT clock source is the internal LPRC Oscillator, which has a nominal frequency of 32 kHz. This creates a nominal time-out period for the WDT (TWDT) of 1 millisecond when no postscaler is used.

**Note:** The WDT module time-out period is directly related to the frequency of the LPRC Oscillator. The frequency of the LPRC Oscillator will vary as a function of device operating voltage and temperature. Please refer to the specific PIC32 device data sheet for LPRC clock frequency specifications.

### 9.3.8 WDT Postscalers

The WDT has a 5-bit postscaler to create a wide variety of time-out periods. This postscaler provides 1:1 through 1: 1048576 divider ratios. Time-out periods that range between 1 ms and 1048.576 seconds (nominal) can be achieved using the postscaler.

The postscaler settings are selected using the WDTPS bits in the DEVCFG1 Configuration register. The time-out period of the WDT is calculated as follows:

**Equation 9-1: WDT Time-out Period Calculation**

$$WDT\ Period = 1\ ms \bullet 2^{Prescaler}$$

**Table 9-2: WDT Time-out Period versus Postscaler Settings(1,2)**

| WDTPS<4:0> | Postscaler Ratio | Time-out Period |
|---|---|---|
| 00000 | 1:1 | 1 ms |
| 00001 | 1:2 | 2 ms |
| 00010 | 1:4 | 4 ms |
| 00011 | 1:8 | 8 ms |
| 00100 | 1:16 | 16 ms |
| 00101 | 1:32 | 32 ms |
| 00110 | 1:64 | 64 ms |
| 00111 | 1:128 | 128 ms |
| 01000 | 1:256 | 256 ms |
| 01001 | 1:512 | 512 ms |
| 01010 | 1:1024 | 1.024s |
| 01011 | 1:2048 | 2.048s |
| 01100 | 1:4096 | 4.096s |
| 01101 | 1:8192 | 8.192s |
| 01110 | 1:16384 | 16.384s |
| 01111 | 1:32768 | 32.768s |
| 10000 | 1:65536 | 65.536s |
| 10001 | 1:131072 | 131.072s |
| 10010 | 1:262144 | 262.144s |
| 10011 | 1:524288 | 524.288s |
| 10100 | 1:1045876 | 1048.576s |

**Note 1:** All other combinations will result in operation as if the prescaler was set to '10100'.
**2:** The periods listed are based on a 32 kHz (nominal) input clock.

## 9.4 INTERRUPT AND RESET GENERATION

The WDT will cause an NMI or a device Reset when it expires. The power-saving mode of the device determines which event occurs. The PWRT does not generate interrupts or resets.

### 9.4.1 Watchdog Timer Reset

When the WDT module expires and the device is not in Sleep or Idle mode, a device Reset is generated. The CPU code execution jumps to the device reset vector and the registers and peripherals are forced to their reset values.

To detect a WDT Reset, the WDTO bit (RCON<4>), SLEEP bit (RCON<3>) and IDLE bit (WDTCON<2>) must be tested. If the WDTO bit is a '1', the event was due to a WDT time-out. The SLEEP and IDLE bits can then be tested to determine if the WDT event occurred while the device was awake or if it was in Sleep or Idle.

### 9.4.2 Watchdog Timer NMI

When the WDT module expires in Sleep or Idle, a NMI is generated. The NMI causes the CPU code execution to jump to the device reset vector. Although the NMI shares the same vector as a device Reset, registers and peripherals are not reset.

To detect a wake from a power-saving mode by the WDT, the WDTO bit (RCON<4>), SLEEP bit (RCON<3>) and IDLE bit (WDTCON<2>) must be tested. If the WDTO bit is a '1', the event was caused by a WDT time-out. The SLEEP and IDLE bits can then be tested to determine if the WDT event occurred in Sleep or Idle modes.

To cause a WDT time-out in Sleep mode to act like an interrupt, a return from interrupt instruction (`RETFIE`) may be used in the start-up code after the event was determined to be a WDT wake-up. This will cause code execution to continue with the opcode following the `WAIT` instruction that put the device into the power-saving mode. Refer to Example 9-2.

**Example 9-2: Sample Code to Determine the Cause of a WDT Event**

```
// sample code to determine the cause of a WDT event

// Unlock the OSCCON register
SYSKEY = 0x12345678;                        //write invalid key to force lock
SYSKEY = 0xAA996655;                        //write Key1 to SYSKEY
SYSKEY = 0x556699AA;                        //write Key2 to SYSKEY
// OSCCON is now unlocked

OSCCONSET = 0x10;                           // set power save mode to Sleep

// Alternate relock code in 'C'
SYSREG = 0x33333333;
// OSCCON is relocked

    WDTCONSET = 0x8000;                     //Enable WDT

    while (1)
    {
        ... user code ...

        WDTCONSET = 0x01;                   // service the WDT
        asm volatile ( "wait" );            // put device into selected power save mode

        // code execution will resume here after wake

        ... user code ...
    }

// The following code fragment is at the top of the device start-up code

    if ( RCON & 0x18 )
    {
        // The WDT caused a wake from sleep
        asm volatile ( "eret" );            // return from interrupt
    }

    if ( RCON & 0x14 )
    {
        // The WDT caused a wake from idle
        asm volatile ( "eret" );            // return from interrupt
    }

    if ( RCON & 0x10 )
    {
        // WDT timed-out
           (device may have been awake or may have been in sleep/idle mode)
    }
```

### 9.4.3 Determining Device Status When a WDT Event Has Occurred

To detect a WDT Reset, the WDTO bit (RCON<4>), SLEEP bit (RCON<3>), and IDLE bit (WDTCON<2>) must be tested. If the WDTO bit is a '1', the event was due to a WDT time-out. The SLEEP and IDLE bits can then be tested to determine whether the WDT event occurred while the device was awake or if it was in Sleep or Idle mode. The user should clear the WDTO, SLEEP, and IDLE bits in the Interrupt Service Routine (ISR) to allow software to correctly determine the source of a subsequent WDT event.

### 9.4.4 Wake from Power-Saving Mode By a Non-WDT Event

When the device is awakened from a power-saving mode by an interrupt, the WDT is cleared. Practically, this extends the time until the next WDT generated device Reset occurs, so that an unintended WDT event does not occur too soon after the interrupt that woke the device.

## 9.5 I/O PINS

The PWRT is disabled when the internal voltage regulator is enabled. A device without an internal voltage regulator will always have the PWRT enabled. A device with an internal voltage regulator will enable the PWRT when the VREG pin is tied to ground (to disable the regulator).

## 9.6 OPERATION IN DEBUG AND POWER-SAVING MODES

### 9.6.1 WDT Operation in Power-Saving Modes

The WDT can be used to wake the device from Sleep or Idle modes. The WDT continues to operate in power-saving modes. A time-out can then be used to wake the device. This allows the device to remain in Sleep mode until the WDT expires or another interrupt wakes the device.

If the device does not re-enter Sleep or Idle mode following a wake-up, the WDT must be disabled or periodically serviced to prevent a device Reset.

### 9.6.2 WDT Operation in Sleep Mode

The WDT, if enabled, will continue operation in Sleep mode. The WDT may be used to wake the device from Sleep mode. When the WDT times out in Sleep, a NMI is generated and the WDTO bit (RCON<4>) is set. The NMI vectors execution to the CPU start-up address, but does not reset registers or peripherals. The Sleep status bit (RCON<3>) will be set indicating the device was in Sleep mode. These bits allow the start-up code to determine the cause of the wake-up.

### 9.6.3 WDT Operation in Idle Mode

The WDT, if enabled, will continue operation in Idle mode. The WDT may be used to wake the device from Idle mode. When the WDT times out in Idle, a NMI is generated and the WDTO bit (RCON<4>) is set. The NMI vectors execution to the CPU start-up address, but does not reset registers or peripherals. The IDLE status bit (RCON<2>) will be set indicating the device was in Idle mode. These bits allow the start-up code to determine the cause of the wake-up.

### 9.6.4 Time Delays During Wake-up

The delay between a WDT time-out and the beginning of code execution depends on the power-saving mode.

There will be a time delay between the WDT event in Sleep mode and the beginning of code execution. The duration of this delay consists of the start-up time for the oscillator in use and the PWRT delay, if it is enabled.

Unlike a wake-up from Sleep mode, there are no time delays associated with wake-up from Idle mode. The system clock is running during Idle mode; therefore, no start-up delays are required at wake-up.

### 9.6.5 WDT Operation in Debug Mode

The WDT is always frozen and therefore does not time-out in Debug mode.

## 9.7 EFFECTS OF VARIOUS RESETS

Any form of device Reset will clear the WDT. The reset will return the WDTCON register to the default value and the WDT will be disabled unless it is enabled by the device configuration.

| **Note:** | After a device Reset, the WDT ON bit (WDTCON<15>) will reflect the state of the FWDTEN bit (DEVCFG1<23>). |
|---|---|

## 9.8 DESIGN TIPS

***Question 1:*** ***Why does the device reset even though I reset the WDT in my main software loop?***

**Answer:** Make sure that the timing of the software loop that clears the WDTCLR bit (WDTCON<0>) meets the minimum time-out specification of the WDT (not the typical value) to ensure operation at different voltage and temperatures. Also, make sure that interrupt processing time has been accounted for.

***Question 2:*** ***What should my software do before entering Sleep or Idle mode?***

**Answer:** Make sure that the sources intended to wake the device have their IEC bits set. In addition, make sure that the particular source of interrupt has the ability to wake the device. Some sources do not function when the device is in Sleep mode. If the device is to be placed in Idle mode, make sure that the Stop In Idle (SIDL) control bit for each device peripheral is properly set. These control bits determine whether the peripheral will continue operation in Idle mode. See the individual peripheral sections of this manual for details. If the WDT is to be used in Sleep mode, then the WDT should be serviced before entering sleep to provide a complete WDT interval before the device exits Sleep mode.

***Question 3:*** ***How do I tell if the WDT or other peripheral woke the device from Sleep or Idle mode?***

**Answer:** Most interrupts have their own unique vector. The vector is determined by the interrupt source. For interrupts that share a vector, the IFS bits for each enabled interrupt source (that shares the vector) can be polled to determine: a.) the source of the interrupt and b.) the source of the wake-up. If the WDT woke the device, the user's start-up code must check for the WDT time-out event, WDTO bit (RCON<4>), and branch accordingly.

## 9.9 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC32 device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Watchdog Timer and Power-up Timer modules are:

| Title | Application Note # |
|---|---|
| No related application notes at this time. | N/A |

**Note:** Visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC32 family of devices.

## 9.10 REVISION HISTORY

### Revision A (October 2007)

This is the initial released version of this document.

### Revision B (October 2007)

Updated document to remove Confidential status.

### Revision C (April 2008)

Revised status to Preliminary; Revised U-0 to r-x.

### Revision D (June 2008)

Revised Registers 29-1, bit 14; Revised Registers 29-26, 29-27, Footnote; Revised Examples 29-1 and 29-9; Change Reserved bits from “Maintain as” to “Write”; Added Note to ON bit (RTCCON Register).

### Revision E (November 2010)

This revision includes the following changes:

- Sections:
  - Added information to **9.3.6 “Resetting the WDT”**, which states that the Watchdog Timer can be cleared by executing a `DEBUG` command
- Notes:
  - Added a Note at the beginning of the section, which provides information on complementary documentation
  - Added a Note regarding the shaded bit names in Register 9-2
  - Added Notes describing the Clear, Set and Invert registers associated with the WDTCON and RCON registers in Table 9-1
- Registers:
  - Revised the following registers:
    - Register 9-1
    - Register 9-2
  - Removed the following registers:
    - RCONCLR, RCONSET, RCONINV
    - WDTCONCLR, WDTCONSET, WDTCONINV
    - DEVCFG1
- Updated the FWDTPS bit as WDTPS bit throughout the document
- Minor changes to the text and formatting have been incorporated throughout the document

**NOTES:**

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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*Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

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