A Foolproof Guide to the Design and Implement of Circuit Simulator

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Contents

Preface

here i will give a brief introduction and my motivation

Chapter 1

theory

Introduce the theory of circuit simulation, the abstrace and working flow

Chapter 2

Arch

introduce the architure of this project, in a involving manner

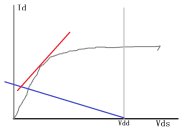

Figure 3.1: Unfold in Linear Region

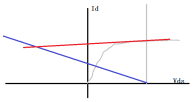

Figure 3.2: Unfold in Saturation Region

Chapter 3

Problem

describe each problem i encountered in detail and how to solve them

3.1 MOSFET Convergence Issus

problem description:
In current model, whether the MOSFET will converge highly depends on the initial state. Under 1.8V Vdd, in most cases encountered, if set the initial of Vgs to 1.8v for nmos and -1.8V for pmos and Vds to 0, the model have no problem of convergence(the test case is pesudo-nmos/pmos inverter, and this setting is essentially set the initial condition to linear region)
however, if set the initial condition to saturation region, (or in the inverter case, set all the value to 0, and after one iteration, it will become in saturation region), the circuit seems never be able to converge. A more detailcheck shows that in iterations, vds will get smaller and smaller(negative). this error are illustrate in the figure below the reason why unfold in saturation region will lead to an Unconvergence Issue is that current mosfet model

can't cover the behavior in the negative Vds plane, and actuall using the model for the positive plane will lead the next iteration to even further, thus result in never ever will converge.

temporary remedy

a way to deal this is to force the Vds out of the negative plane(for pmos, keep it out of positive plane). to do so , ever time doing iteration, if find the vds falls in the negative plane, just set it to 0. This method prove to work out fine.

Appendix A

Math

here is the math needed