Instruction			Extra Info
Description	Abbr	Structure	Register A - H, RAM 0 - 223, I/O 224 - 255
No Operation	NOP	NOP	
Move	MOV	MOV, Dest, Src 1	
Store Memory	STM	STM, MDest, RSrc 1	RAM 0 - 223, I/O 224 - 255
Load Memory	LDM	LDM, RDest, MSrc 1	
Left Shift	LSH	LSH, Dest, Src 1	Shift By 1
Right Shift	RSH	RSH, Dest, Src 1	Shift By 1
Addition	ADD	ADD, Dest, Src 1, Src 2	
Subtraction	SUB	SUB, Dest, Src 1, Src 2	
Increment	INC	INC, Dest, Src 1	
Decrement	DEC	DEC, Dest, Src 1	
Increment Add	IAD	IAD, Dest, Src 1, Src 2	Src 1 + Src 2 + 1
Decrement Sub	DES	DES, Dest, Src 1, Src 2	Src 1 - Src 2 - 1
Bitwise And	AND	AND, Dest, Src 1, Src 2	
Bitwise Or	ORE	ORE, Dest, Src 1, Src 2	
Bitwise Xor	XOR	XOR, Dest, Src 1, Src 2	
Invert A	INV	INV, Dest, Src 1	
Negative A	NEG	NEG, Dest, Src 1	
Immediate	IMM	IMM, Number	Number, 0 - 255
Branch Imm	BRH	BRH, Condition, Number	Number, 0 - 31
Branch Pointer	PNT	PNT, Condition, Src 1	Line, 0 - 31

Conditions / Flags			Extra Info
Description	Abbr	Requirements	Use Abbr In Assembly
Zero	ZERO	None	Z
Not Zero	NZRO	None	!Z
Cout	COUT	None	C
Always	TRUE	None	None
Greater	GRTR	Prev Inst, SUB	!Z, C
Greater Equal	GREQ	Prev Inst, SUB	C
Equal	EQAL	Prev Inst, SUB or XOR	Z
Not Equal	NEQL	Prev Inst, SUB or XOR	!Z