DATA SHEET

GP328525C

ARM926EJ-S Multi-Media Camera w/ PPU SoC Platform

Aug. 27, 2021

Version 1.0

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MULTI-MEDIA CAMERA w/ PPU SoC PLATFORM

1. GENERAL DESCRIPTION

GP328525C, a highly integrated SoC (System-On a Chip) by Generalplus, is a high cost-performance ratio solution for multi-media and video streaming applications. It is developed with a high performance and power efficient ARM's ARM926EJ-S core operating at up to CPU/system 513/171MHz with significant enhancements in image, video processing, and power savings. Other features include DDR memory, GPDLA deep learning accelerator, Chroma key engine, JPEG CODEC engine, TFT-LCD interface, MIPI DSI interface, Display adjustment engine, CMOS sensor interface, MIPI CSI interface, scaling engine, Picture Process Unit (PPU), 16-channel Sound Process Unit (SPU), audio compressor, USB 2.0 OHCI/EHCI, USB 2.0 HS device, etc. GP328525C processor is designed to work with various types of memory card interfaces such as SD and MMC. For more information about its features, please refer to the following section.

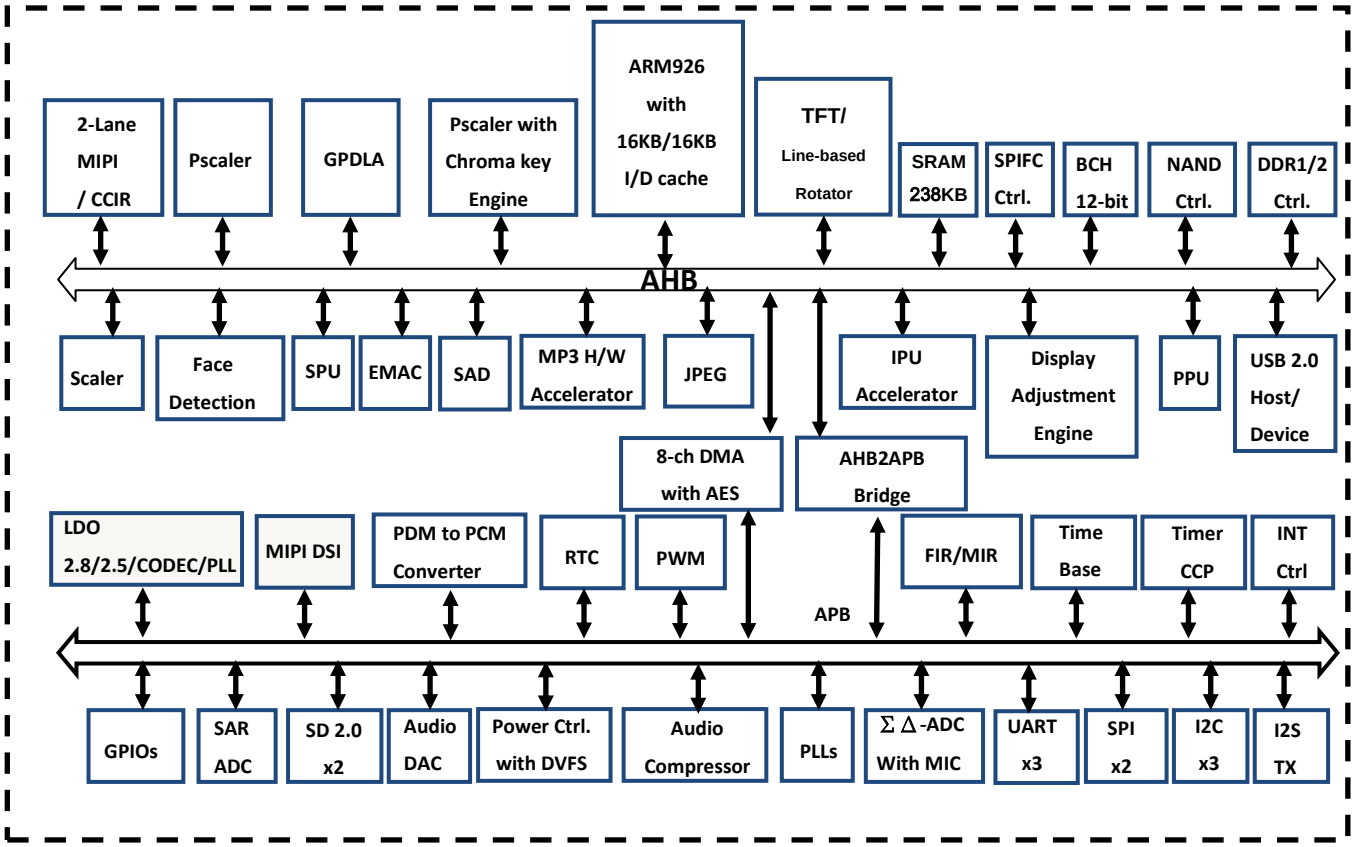
2. FEATURES

- ARM926EJ-S CPU with both 16K-byte I/D-cache, embedded JTAG ICE, and working frequency up to 513MHz
- Up to 238KB SRAM for local data buffer
- Embedded 128Mb DDR SDRAM
- Embedded 2Gb SLC NAND Flash
- GPDLA is a deep learning accelerator which supports various deep neural network models; applications such as object classification, object detection and face detection are all possible and will enrich user experience.
- Chroma key engine with robust mechanism and low bandwidth requirements
- SPI FLASH controller, allowing CPU directly runs program on it. 1-bit/2-bit/4-bit IO mode supported
- Picture Process Unit. (PPU)
  - Four Text layers + 1024 internal Sprites + 4096 extended Sprites
  - Virtual 3D effect for text and sprite
  - QVGA/VGA/D1 and arbitrary size up to 2032x2032 output
  - Line-based or frame-based operation
  - Max. 1024x768 LCD Resolution output
  - Texture mapping with anti-aliasing and bilinear interpolation
  - High precision sprite rotate effect supports up to 256-step (each step 360-degree/256).
  - High precision sprite zoom effect supports up to 256-step adjustment
  - Supports both alpha blending and additive blending
- Sound Process Unit (SPU)
  - 16 hardware PCM/ADPCM channels
  - Dynamic volume compressor
  - MP3 decoder
- Audio compressor engine which enhances audio quality
- JPEG CODEC
  - ISO/IEC 10918-1 baseline JPEG
  - High-speed decoding and encoding with resolution up to 64M pixels
  - Hardware Motion JPEG decoding and encoding (up to 1080p@30fps) for real-time video record and playback application
- Video-in & CMOS sensor interface and CCIR601/CCIR656 CSI standard supported.
- Two/one-lane MIPI CSI input supported
- Face Detection Engine for interactive application
- NAND FLASH controller with ECC and 4/8/12-bit BCH
- Eight-channel DMA controller with AES function
- Mono and 16 gray levels STN-LCD controller
- Rotating engine supports 90/180/270/360/Mirror/Flip function
- Y only rotating engine supports rotate at any angle
- Line-based rotating engine supports panels with different orient with frame buffer without extra bandwidth consumption.
- Two sets of TFT-LCD controller.
  - UPS051 (serial RGB)
  - UPS052 (serial RGB dummy)
  - Parallel RGB (6-6-6, 7-7-7, 8-8-8).
  - I80 (8-bit/16-bit/18-bit system bus) I/F type
  - CCIR601/CCIR656
  - Timing Controller for TFT-LCD drivers
  - Scaling engine inside with programmable up-scaling and down-scaling factor
  - Gamma Table Adjustment(TFT1 Only)
- Up to 4-lane MIPI DSI interface which supports panel resolution up to 1280x720 or 720x1280.
- Display adjustment engine which provides edge enhancement, R/G/B gamma table and auto hue adjustment
- Two sets of PSCAL supporting transform and zoom-in/out image data to the format supported by JPEG/ PPU/ DRAM
- One Y-only PSCAL for face-detection engine
- Image Processing Unit
  - Max. width more than 2048 pixels

  - Address-remap supporting direct addressing and Coordinates addressing
  - Color-remap-only supporting ARGB155 and RGB565
  - Sixteen OP modes supported
  - Support Alpha transform
- Universal Serial Bus (USB) 2.0 high/full speed compliance device and USB OHCI/EHCE host controller with built-in transceiver.
- Watchdog timer
- Real-time clock
- Eight 32-bit timers/counters with PWM output capability.
- Eight-channel quadrature decoder
- Two sets of SD 2.0/MMC interface
- Two sets of SPI (master/slave) interface with data rate up to 24Mbps.
- Three sets of UART (asynchronous serial I/O) or IrDA interface with baud rate up to 1.8432Mbps and 115.2Kbps; smart card interface (ISO7816) supported
- Three sets of I2C controller
- Four sets of I2S input with 24-bit resolution and up to 192KHz sample rate
- Four sets of I2S output with 24-bit resolution and up to 192KHz sample rate
- PDM to PCM converter which supports MEMS microphones with PDM interface
- Embedded Ethernet MAC hardware
- One set hardware SAD (Sum of Absolute Difference) engine
- 90 general programmable I/O ports (GPIO) with pull-high/low control
- Power management
- 1.2V DC2DC Feedback reference voltage out for core logic
- 3.3V to 2.8V~1.8V regulator for sensor's power
- 3.3V to 2.5V~1.8V regulator for DDR memory
- Dedicated 3.3V to 3.0V LDO for audio ADC
- Dedicated 3.3V to 3.0V LDO for PLLs
- Low voltage reset
- RTC with independent power supply
- Power-down mode with low standby current, typically less than 10uA
- Two sets of programmable PLLs frequency from 144MHz to 1188MHz and 72MHz to 594MHz
- 16-bit stereo DAC (2-channel) for audio playback
- 16-bit ADC with MIC for audio recording
- 12-bit SAR ADC with 8 line-in channels and 800KMsps
- MIC with digital AGC (auto gain control)
- LFBGA108 package

Item	Product number	Embedded DDR density	Embedded NAND Flash density
1	GP328525C	128Mb DDR memory	2Gb SLC NAND Flash

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTION

PKG No	Name	Group	Type	Normal Function Description
A1	X32KO	RTC	AO	X'tal 32768Hz output
A2	PWR_ON3	SYSTEM	AI	Power on key input 3
A3	DC2DC_EN	SYSTEM	AO	DC to DC enable output
A4	MICIN_PAD	CODEC ADC	AI	CODEC ADC microphone input
A5	CODEC_V30O	CODEC ADC	P	3.0V Power for CODEC ADC. #3
A6	DAC_V33I	AuDAC	P	3.3V Power for AuDAC/SAR ADC
A7	VOL	AuDAC	AO	Audio DAC left channel output
A8	LINEIN1_PAD	SAR ADC	AI	SAR ADC LINEIN1
A9	IOA7	TFT	IO	TFT D7
A10	IOA6	TFT	IO	TFT D6
A11	IOA3	TFT	IO	TFT D3
B1	RTC_V33	RTC	P	RTC power input
B2	X32KI	RTC	AI	X'tal 32768Hz input
B3	WPB	NAND	I/O	NAND Flash WPB
B4	PWR_ON1	SYSTEM	AI	Power on key input 1
B5	ADVCM	CODEC_ADC	AO	CODEC ADC VREF
B6	VOR	SAR ADC	AO	Audio DAC right channel output
B7	LINEIN0_PAD	SAR ADC	AI	SAR ADC LINEIN0
B8	LINEIN2_PAD	SAR ADC	AI	SAR ADC LINEIN2
B9	IOD1	SPIF	IO	SPI FLASH CLK
B10	IOA5	TFT	IO	TFT D5
B11	IOD4	SPIF	IO	SPI FLASH RX2
C1	IOD10	SD	IO	SD CMD
C2	IOD12	SD	IO	SD DATA3
C3	PWR_ON2	SYSTEM	AI	Power on key input 2
C4	PWR_ON0	SYSTEM	AI	Power on key input 0
C5	AGND	SAR ADC	P	Ground for AuDAC/ADC/SAR ADC
C6	LINEIN3_PAD	SAR ADC	AI	SAR ADC LINEIN3
C7	IOD5	SPIF	IO	SPI FLASH RX3
C8	IOD2	SPIF	IO	SPI FLASH RX0
C9	IOA2	TFT	IO	TFT D2
C10	IOC12	ICE	IO	JTAG TDI
C11	IOC13	ICE	IO	JTAG TDO
D1	IOD13	SD	IO	SD DATA0
D2	IOD11	SD	IO	SD CLK
D3	VSS	Digital Ground	P	Digital ground
D6	DDR_V25O	DDR LDO	P	DDR LDO output#2
D9	IOE0	GPIO	IO	IOE0
D10	IOC14	ICE	IO	JTAG TCK
D11	IOC15	ICE	IO	JTAG TMS
E1	IOC7	MIPI	IO	MIPI0 DATA1P/CSI D9
E2	IOC6	MIPI	IO	MIPI0 DATA1N/CSI D8
E3	RESETB	SYSTEM	I	External RESETB(Low active)
E5	REG_V33I	SYSTEM	P	LDO power input for DDR_REG/REGV28/REGV18

PKG No	Name	Group	Type	Normal Function Description
E6	VSS	Digital Ground	P	Digital Ground
E7	VSS	Digital Ground	P	Digital ground
E9	IOA4	TFT	IO	TFT D4
E10	IOE2	GPIO	IO	IOE2
E11	IOE1	GPIO	IO	IOE1
F1	IOC9	MIPI	IO	MIPI0 CLKP/ CSI CLKO
F2	IOC8	MIPI	IO	MIPI0 CLKN/ CSI CLKI
F3	IOD15	SD	IO	SD DATA2
F4	V33I	IO PWR	P	3.3V IO Power
F5	V12i	CORE PWR	P	1.2V Core Power
F7	VSS	Digital Ground	P	Digital ground
F8	V33I	IO PWR	P	3.3V IO Power
F9	IOA1	TFT	IO	TFT D1
F10	IOD9	SPI	IO	SPI RX
F11	IOE3	GPIO	IO	IOE3
G1	IOC11	MIPI	IO	MIPI0 DATA0P/CSI VSYNC
G2	IOC10	MIPI	IO	MIPI0 DATA0N/CSI HSYNC
G3	IOD14	SD	IO	SD DATA1
G5	DDR_V25I	DDR	P	DDR SSTL2 power input
G6	VSS	Digital Ground	P	Digital ground
G7	V12i	CORE PWR	P	1.2V Core Power
G9	IOA0	TFT	IO	TFT D0
G10	IOD7	SPI	IO	SPI CLK
G11	IOD8	SPI	IO	SPI TX
H1	PLL_V30O	PLL	P	3.0V PLL power[#2]
H2	X12MI_SINGLE	PLL	AI	X'tal 12MHz input
H3	IOA12	GPIO	IO	IOA12
H6	V12i	CORE PWR	P	1.2V Core Power
H9	IOF9	GPIO	IO	IOF9
H10	IOE7	GPIO	IO	IOE7
H11	IOD6	SPI	IO	SPI CSI
J1	IOA10	GPIO	IO	IOA10
J2	IOA11	GPIO	IO	IOA11
J3	IOB3	TFT	IO	TFT CLK
J4	IOA13	GPIO	IO	IOA13
J5	IOA14	GPIO	IO	IOA14
J6	IOA15	GPIO	IO	IOA15
J7	IOF8	GPIO	IO	IOF8
J8	IOB5	UART	IO	UART TX
J9	IOC5	CSI	IO	CSI D6
J10	IOE5	GPIO	IO	IOE5
J11	IOE6	GPIO	IO	IOE6
K1	IOB0	TFT	IO	TFT DE
K2	IOB1	TFT	IO	TFT HSYNC
K3	DP	USB	AIO	USB DP[#4]

PKG No	Name	Group	Type	Normal Function Description
K4	IOB6	CSI	IO	CSI D0
K5	IOF0	GPIO	IO	IOF0
K6	IOF2	GPIO	IO	IOF2
K7	IOF4	GPIO	IO	IOF4
K8	IOF6	GPIO	IO	IOF6
K9	IOC2	CSI	IO	CSI_D4
K10	IOC0	CSI	IO	CSI D2
K11	IOE4	GPIO	IO	IOE4
L1	IOB2	TFT	IO	TFT VSYNC
L2	IOB4	UART	IO	UART RX
L3	DM	USB	AIO	USB DM#4
L4	IOB7	CSI	IO	CSI D1
L5	IOF1	GPIO	IO	IOF1
L6	IOF3	GPIO	IO	IOF3
L7	IOF5	GPIO	IO	IOF6
L8	IOF7	GPIO	IO	IOF7
L9	IOC3	CSI	IO	CSI D5
L10	IOC1	CSI	IO	CSI D3
L11	IOC4	CSI	IO	CSI D7

Note1: AO: Analog Output, AI: Analog Input, AIO: Anaalog IO, P: Power/Ground PAD

Note2: Power source REG33I

Note3: Power source DAC_V33I

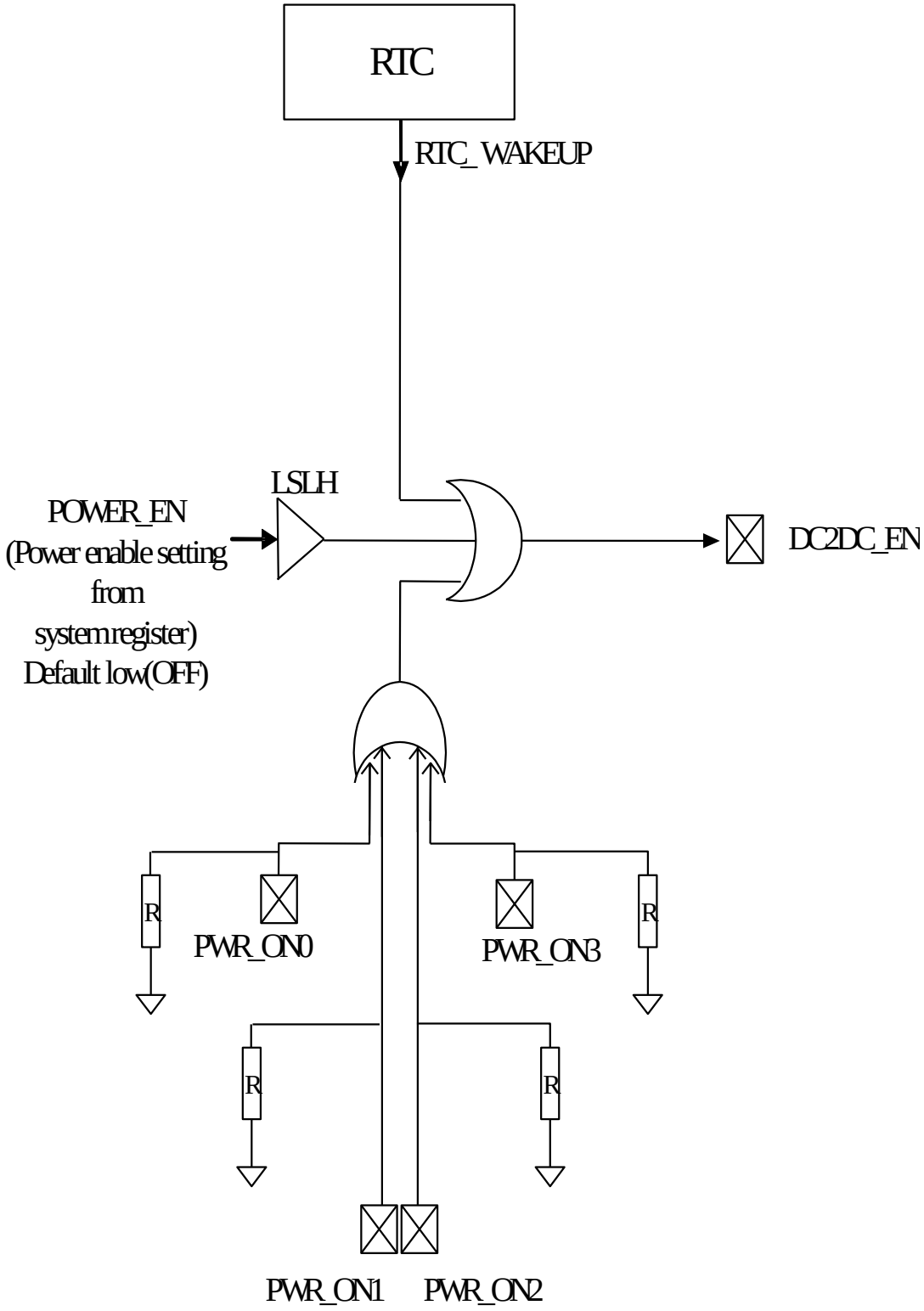
Note4: For compatibility issue, either 32768Hz or 12MHz crystal is required.

4.1. Package Pin Sequence

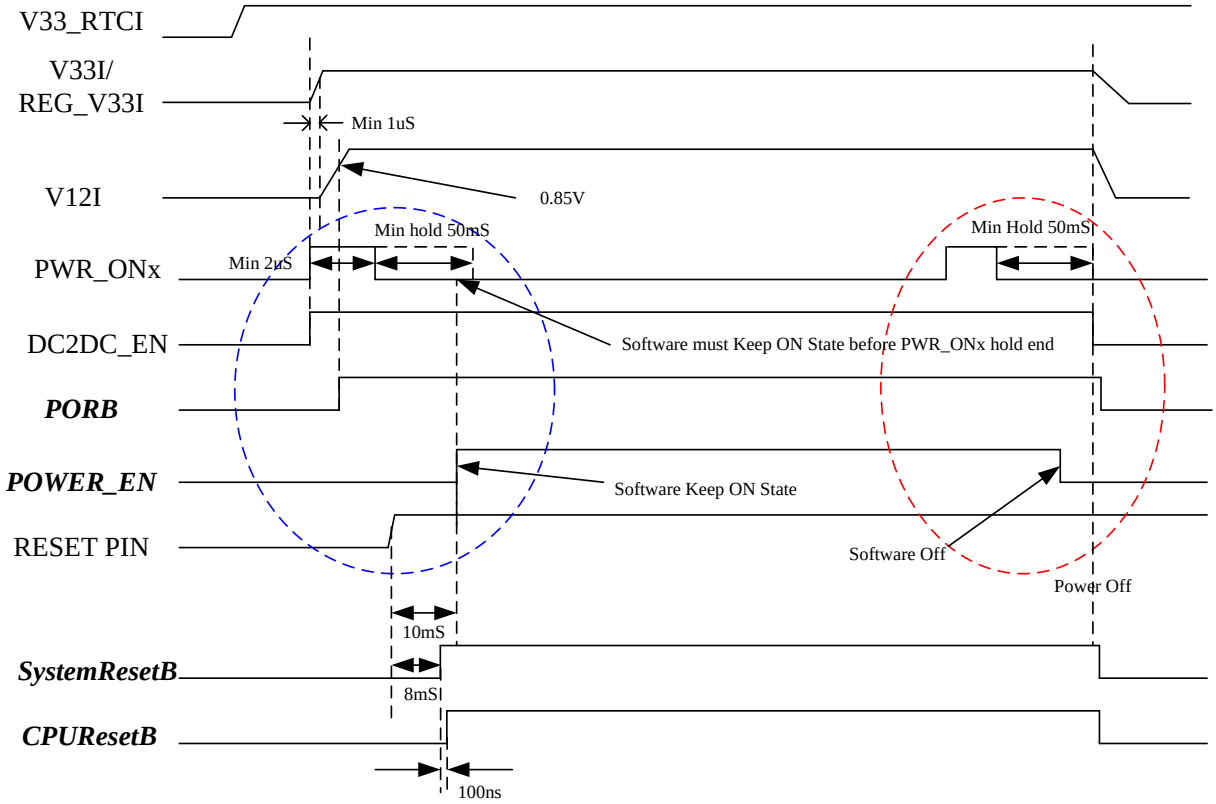
LFBGA108 Package Ball Sequence

	1	2	3	4	5	6	7	8	9	10	11
A	X32KO	PWR_ON3	DC2DC_EN	MICIN_PAD	CODEC_V30O	DAC_V33I	VOL	LINEIN1_PAD	IOA7	IOA6	IOA3
B	RTC_V33	X32KI	WPB	PWR_ON1	ADVCM	VOR	LINEIN0_PAD	LINEIN2_PAD	IOD1	IOA5	IOD4
C	IOD10	IOD12	PWR_ON2	PWR_ON0	AGND	LINEIN3_PAD	IOD5	IOD2	IOA2	IOC12	IOC13
D	IOD13	IOD11	VSS	#N/A	#N/A	DDR_V25O	#N/A	#N/A	IOE0	IOC14	IOC15
E	IOC7	IOC6	RESETB	#N/A	REG_V33I	VSS	VSS	#N/A	IOA4	IOE2	IOE1
F	IOC9	IOC8	IOD15	V33I	V12i	#N/A	VSS	V33I	IOA1	IOD9	IOE3
G	IOC11	IOC10	IOD14	#N/A	DDR_V25I	VSS	V12i	#N/A	IOA0	IOD7	IOD8
H	PLL_V30O	X12MI_SINGLE	IOA12	#N/A	#N/A	V12i	#N/A	#N/A	IOF9	IOE7	IOD6
J	IOA10	IOA11	IOB3	IOA13	IOA14	IOA15	IOF8	IOB5	IOC5	IOE5	IOE6
K	IOB0	IOB1	DP	IOB6	IOF0	IOF2	IOF4	IOF6	IOC2	IOC0	IOE4
L	IOB2	IOB4	DM	IOB7	IOF1	IOF3	IOF5	IOF7	IOC3	IOC1	IOC4

5. POWER MACRO FUNCTION BLOCK



6. POWER SEQUENCE



Note 1. Word in ***Bold and Italic*** means IC internal signal

Note 2. In fast shutdown mode, PWR_Onx min hold time is 3mS

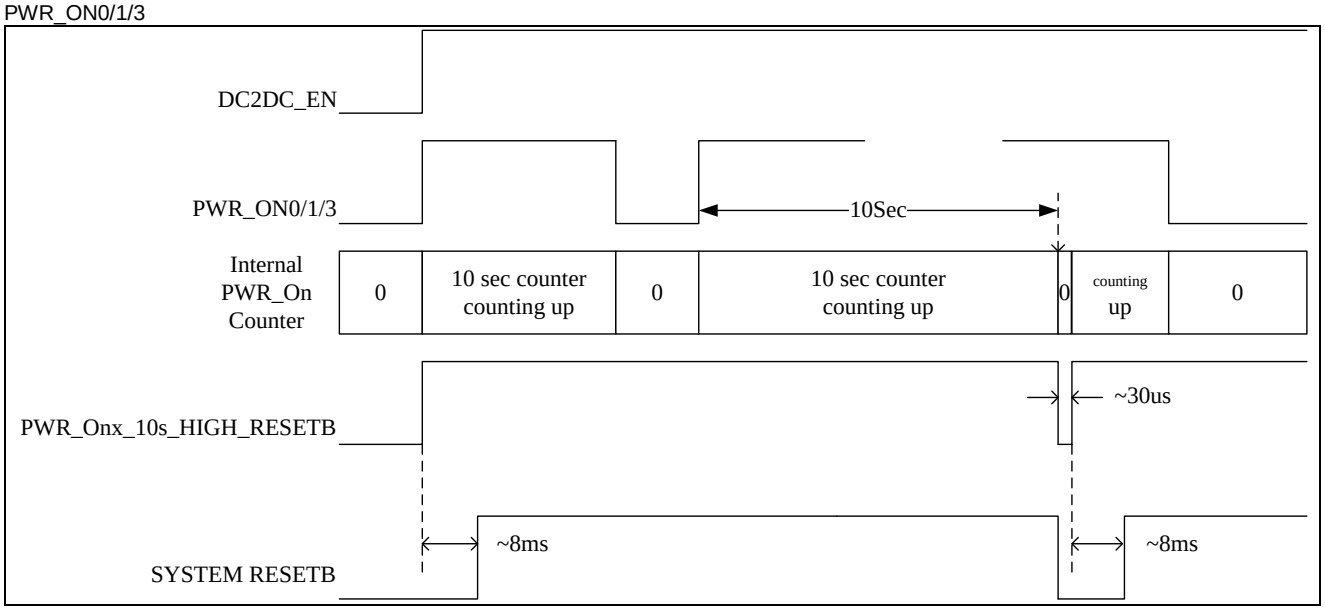
Note 3. PORB will be released after power satisfy all of following conditions,

1. V12I reach 0.85V
2. 2 mS late after REG_V33I reach 1.6V.
3. If user enable LVR and REG_V33I reach selected voltage level.

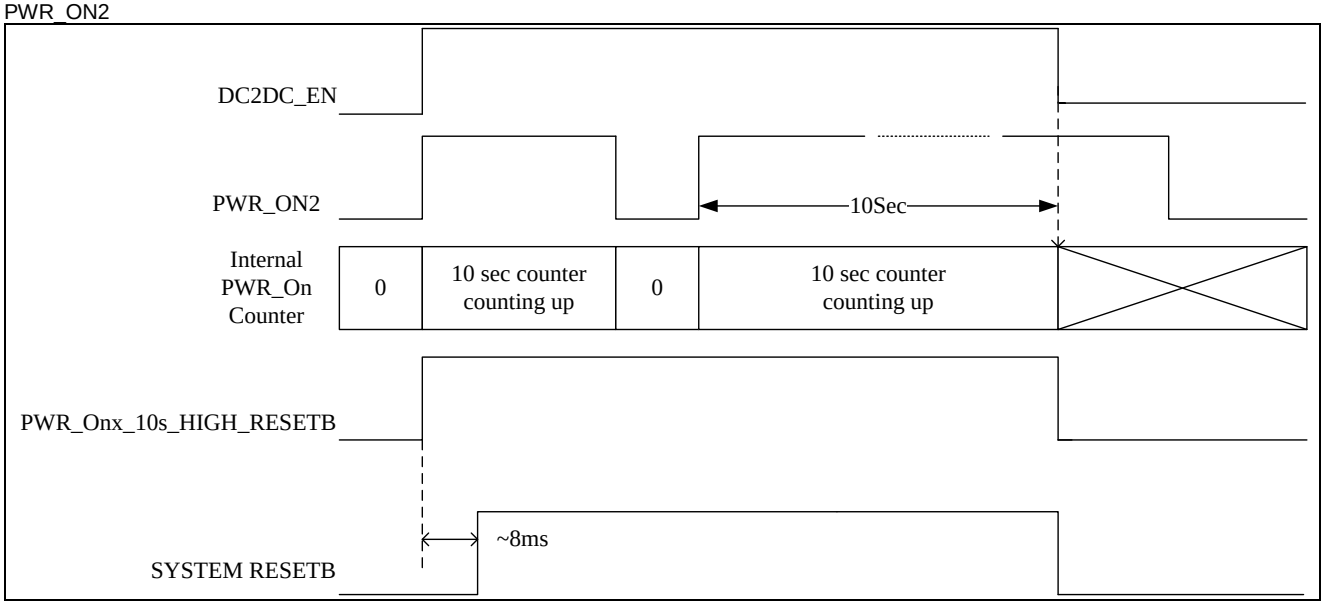
Note 4. During the entire power-on period, V33I must be higher than V12I.

7. POWER-ON KEY LONG PRESS RESET

PWR_ON0/1/3



PWR_ON2



Key No.	Default 10 Sec reset	Wake up system after 1st time power up	High Level active	Rising Edge active
NO0	ON	YES	YES	NO
NO1	OFF	NO	YES	NO
NO2	OFF	YES	NO	YES*1
NO3	OFF	YES	YES	NO

Note: PWR_ON0/1/2 includes a 5us deglitch circuit; PWR_ON2 shall be kept at last 5us for the rising edge detection.

8. ELECTRICAL SPECIFICATIONS

8.1. Absolute Maximum Rating

Rating	Symbol	Value	Unit
Supply Voltage 1	REGV33I	-0.3 to 3.6	V
Supply Voltage 2	RTC_V33I	-0.3 to 3.6	V
Supply Voltage 3	V33I	-0.3 to 3.6	V
Supply Voltage 4	PLL_V30O	-0.3 to 3.6	V
Supply Voltage 5	USB_V33	-0.3 to 3.6	V
Supply Voltage 6	DAC_V33I	-0.3 to 3.6	V
Supply Voltage 7	CODEC_V30O	-0.3 to 3.6	V
Supply Voltage 8	REG_V28O	-0.3 to 3.6	V
Supply Voltage 9	DDR_V25I	-0.3 to 3.6	V
Supply Voltage 10	DDR_V25O	-0.3 to 3.6	V
Supply Voltage 11	V12I	-0.3 to 1.4	V
Input Voltage	V_{IN}	-0.3 to 3.6	V
Operating Temperature	T_A	-20~70	℃
Storage Temperature	T_{STG}	-40 to +150	℃

8.2. DC Characteristics

Characteristic	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Supply Voltage 1	REGV33I	2.7	3.3	3.6	V	-
Supply Voltage 2	RTC_V33I	2.2	3.3	3.6	V	-
Supply Voltage 3	V33I	2.7	3.3	3.6	V	-
Supply Voltage 4	PLL_V30O	2.7	3.3	3.6	V	-
Supply Voltage 5	USB_V33	3.0	3.3	3.6	V	
Supply Voltage 6	DAC_V33I	2.7	3.3	3.6	V	-
Supply Voltage 7	CODEC_V30O	2.7	3.0	3.6	V	-
Supply Voltage 8	REG_V28O	1.35	2.8	3.3	V	-
Supply Voltage 9	DDR_V25I	2.25	2.5	2.75	V	-
Supply Voltage 10	DDR_V25O	2.25	2.5	2.75	V	-
Supply Voltage 11	V12I	1.1	1.2	1.32	V	-
Operating Current Case 1	I_{OP1}	-	164	-	mA	Core power current@ System 171MHz, CPU 513MHz V33=3.3V, V12=1.2V , Sensor(CSI) +PPU+ TFT
Operating Current Case 2	I_{OP2}	-	60	-	mA	Core power current@ System 87MHz, CPU 87MHz, V33=3.3V, V12=1.2V , Sensor(CSI) +PPU+ TFT
Operating Current Case 3	I_{OP3}	-	25	-	mA	Core Power current@ System 24MHz CPU 48MHz V33=3.3V, V12=1.2V DAC decode MP3
Power Down Current	I_{PD}	-	10	-	μA	All power is off except RTC macro

Characteristic	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
						(RTC_V33=3.3V, the others = 0V) X'tal 32K on, IOSC32K off
High Input Voltage	V_{IH}	0.7V33	-	V33	V	-
Low Input Voltage	V_{IL}	VSS	-	0.3V33	V	-
Crystal Frequency 1	-	-	32768	-	Hz	-
Crystal Frequency 2	$F_{CRYSTAL}$	-	12	-	MHz	-
System Clock	F_{SYS}	5461Hz[1]	-	171	MHz	-

Note1: By setting clock divider and changing system clock to SLOW mode (32768Hz).

8.3. GPIO Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Input High Voltage(VIH)	0.55*V33	-	V33	V	-
Input Low Voltage(VIL)	0	-	0.45*V33	V	-
Output High Voltage(VOH)	0.8*V33	-	V33	V	-
Output Low Voltage(VOL)	0	-	0.2*V33	V	
IOA**,IOB***,IOC,IOD,IOE**** Output Driving Current(IOH)	-	15/20	-	mA	V33@3.3V, room temperature
IOA**,IOB***,IOC,IOD,IOE**** Output Sinking Current(IOL)	-	-15/-22	-	mA	V33@3.3V, room temperature
IOA[7:4], IOB[7:4], IOE[11:8], IOF Output Driving Current(IOH)	-	9/16	-	mA	V33@3.3V, room temperature
IOA[7:4], IOB[7:4], IOE[11:8], IOF Output Sinking Current(IOL)	-	-9/-17	-	mA	V33@3.3V, room temperature
Power On Pad0/1/3 High Pulse for Power Enable	5	-/-8	-	us	
Power On Pad2 High Pulse for Power Enable	1	-	-	us	
Power On Pad0/1 Input High Voltage(POVIH)	-	0.7*RTC_V33I	-	V	
Power On Pad2/3 Input High Voltage(POVIH)	1.5	-	-	V	
Power On Pad(PWR_ON0/1) Internal Pull-Down Resistor(POPRPD)	9K	18K	-	Ω	
Power On Pad(PWR_ON2/3) Internal Pull-Down Resistor(POPRPD)	100K	200K	-	Ω	
IOA,IOB,IOC,IOD,IOE,IOF Internal Pull-Up Resistor(RPU)*	40K*0.85	40K	40K*1.15	Ω	V33@3.3V, room temperature
IOA,IOB,IOC,IOD,IOE,IOF Internal Pull-Down Resistor(RPD)*	50K*0.85	50K	50K*1.15	Ω	V33@3.3V, room temperature

*GPIO pull resistor will vary with V33.

**IOA not including IOA[7:4]

***IOB not including IOB[7:4]

****IOE not including IOE[11:8]

8.4. Audio DAC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	16	16	16	Bit	Audio DAC digital input
Full Scale Output Voltage	0.55* DAC_V33I	0.6* DAC_V33I	-	Vp-p	-
THD+N (Fin = 0.997kHz)	0.15	0.10	-	%	Fin=0.997KHz output loading=32 ohm
Dynamic Range	75	79	-	dB	Fin=0.997KHz w/ -60dB output loading=32 ohm
Output Loading	32	-	-	ohm	-
Frequency Response	20	-	19200	Hz	-

8.5. CODEC ADC/MIC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	16	16	16	Bit	CODEC ADC digital output
Input Voltage Range	2.7	-	3.6	V	-
SNR	80	84	-	dB	Boost=0dB, PGA=0dB, filter: 20K LPF + A weighting@V33_DA16=3.3V
THD+N	70	72.8	-	dB	Boost=0dB, PGA=0dB, Fin=0.997KHz, Fs=48kHz @V33_DA16=3.3V
Dynamic Range	80	84.8	-	dB	Boost=0dB, PGA=0dB, filter: 20K LPF + A weighting @V33_DA16=3.3V
MICBIAS	CODEC_V30O * 0.75	2.25	-	V	MICBIAS= V33_AD * 0.75

8.6. SAR ADC Characteristics

Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
SAR ADC Input Voltage Range	VIN_RANGE	2.7	-	3.6	V
Resolution of ADC	RESO	12	12	12	bit
Signal-to-Noise Plus Distortion of ADC from Line in	SINAD (Note 1)	58	58.56	-	dB
Effective Number of Bit	ENOB (Note 2)	9.03	9.44	-	bit
Integral Non-Linearity of ADC	INL	-2	-	2	LSB (Note 3)
Differential Non-Linearity of ADC	DNL	-2	-	2	LSB
No Missing Code		10	11	12	bit
AD Conversion Rate=ADCCLK/20	F_{CONV}	-	534K	800K	Hz(Note4)

Note1: The SINAD testing condition at VINLp-p = 0.8 * DAC_V33I, F_{CONV} = 200KHz, Fin = 1.0KHz Sine waves at DAC_V33I = 3.0V from ADC input.

Note2: ENOB = (SINAD - 1.76) / 6.02.

Note3: LSB means Least Significant Bit (at 12-bit resolution).

Note4: @System CLK 171MHz, ADCCLK = SYSCLK/16.

8.7. DDR Regulator for DDR Characteristics

Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.7	-	3.6	V
Maximum Current Output	IREGO	-	-	100	mA
Output Voltage	VREGO	2.5*0.95	2.5(Note)	2.5*1.05	V
Standby Current	IREGS	-	-	2	uA

Note: The typical regulator output voltage is adjustable through register settings.

8.8. 3.3V-to-2.8V Regulator for Sensor Characteristics

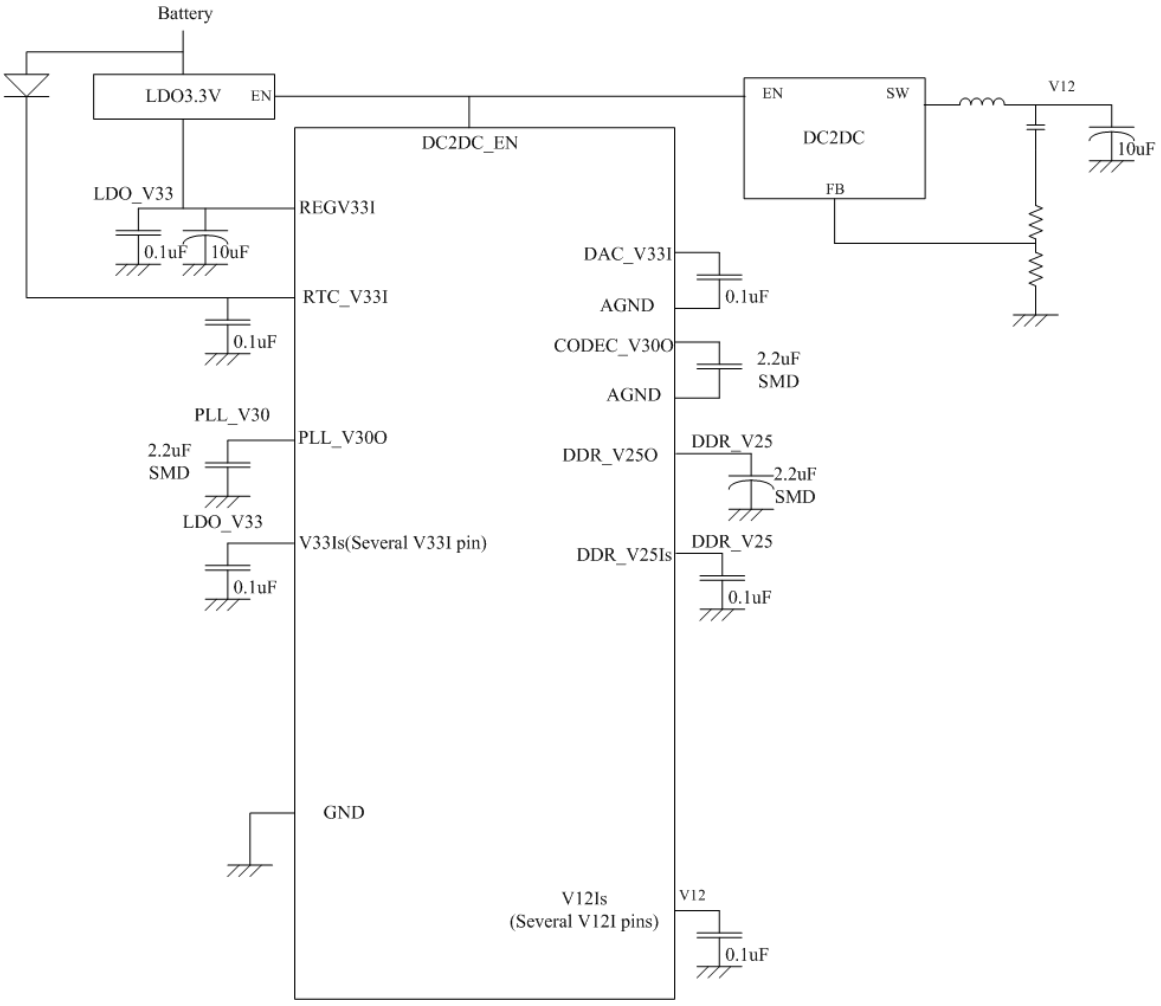
Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	3.0	-	3.6	V
Maximum Current Output	IREGO	-	-	60	mA
Output Voltage	VREGO	2.8*0.95	2.8(Note)	2.8*1.05	V
Standby Current	IREGS	-	-	2	uA

Note: The typical regulator output voltage is adjustable through register settings.

9. RECOMMENDED BOARD LAYOUT

9.1. Power and Ground

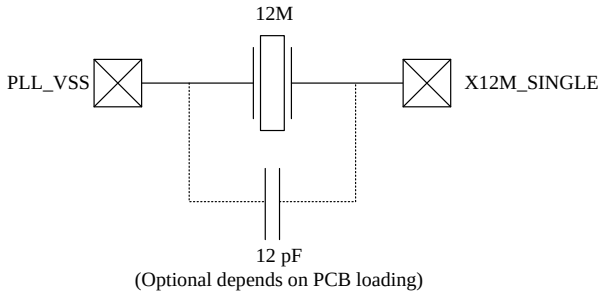
All power and ground pins are connected as in the following diagram for general application. The decoupling capacitor of 0.1μF, 10μF, and 47uF should be connected to each corresponding power pin of IC and 0.1uF capacitor must be placed as close as possible to the power pin. Each V33I/V12I requires one 0.1μF capacitor and must be placed as close as possible to the power pin.



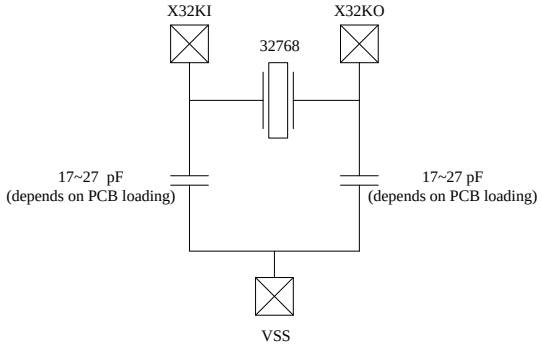
Note1: DC2DC should be located as close as possible to the main chip. If possible, the distance between DC2DC and main chip should be less than 1cm.
Note2: The wire width of FB_ADJ should keep at least 2x wire width; if possible, please shading FB_ADJ.
Note3: DC2DC feedback reference Voltage must be 0.6V because of FB_ADJ feedback 0.6V to DC2DC.

9.2. Crystal and PLL

When 12MHz crystal is applied in the system, please connect the crystal circuit as indicated in the following diagram.



Note*: Please refer to the crystal's application circuit.



A Crystal (32768Hz) may be used for applications that may involve with precise time clock requirement. See the above diagram for more details.

For USB compatibility issue, either 32768Hz or 12M Hz crystal is required.

Note*: Please refer to the crystal's application circuit.

10. PACKAGE/PAD LOCATIONS

10.1. Ordering Information

Product Number	Package Type
GP328525C_XXXX-NnnV-QM02x	LFBGA-108

Note1: Code number is assigned for customer.

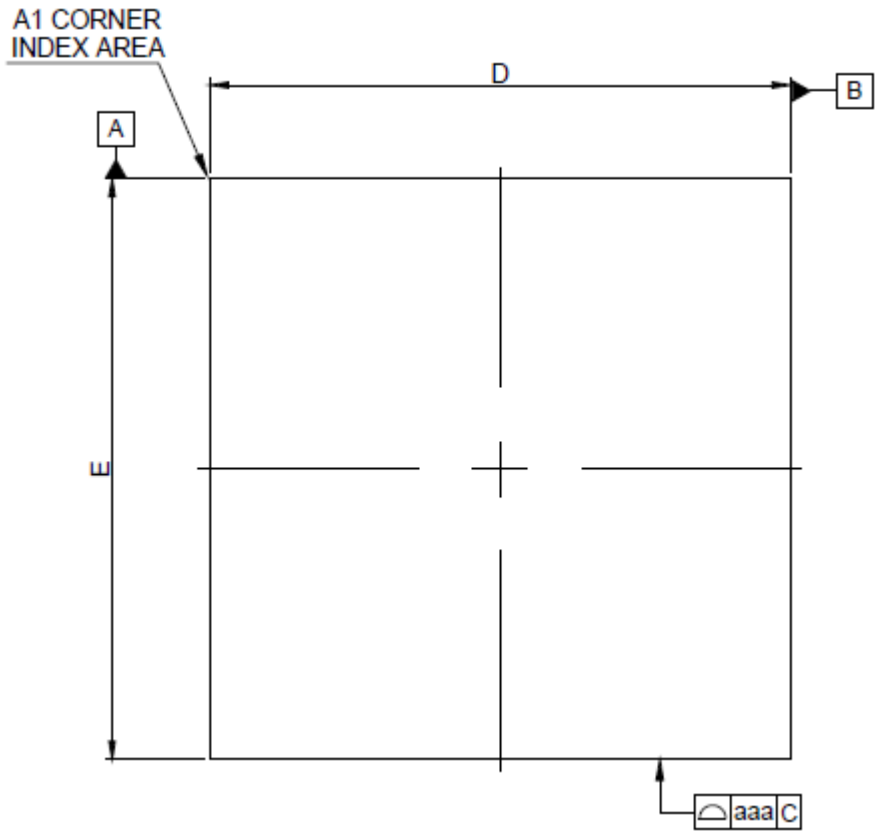
Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

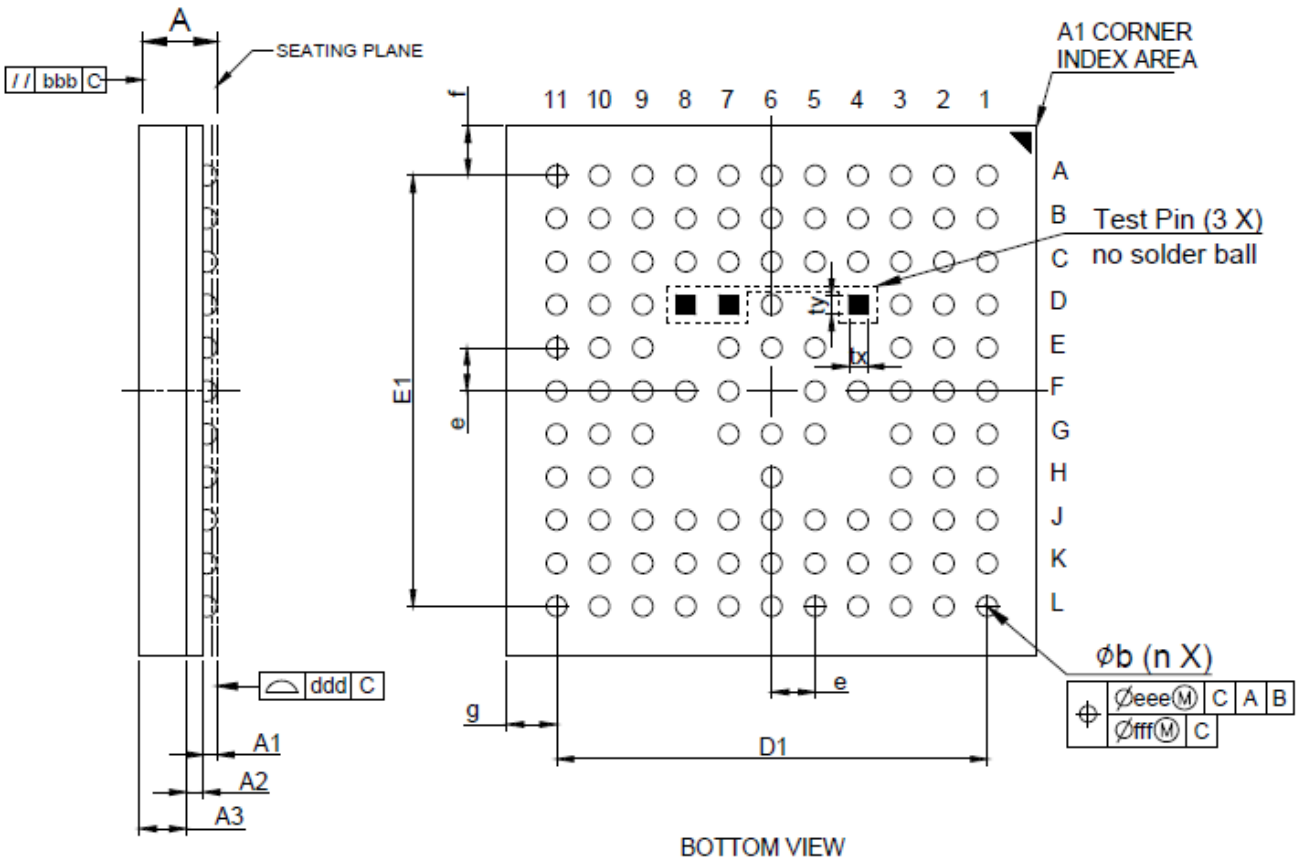
Note3: Package form number (x = 1 - 9, serial number).

Note4: PartNumber_XXXX where "_XXXX" is a 4-digit code, managed by Generalplus, to indicate additional software algorithm(s) or royalty type(s) applied to the product. Same part numbers bearing different codes make no differences in hardware specification.

10.2. Package Information

LFBGA108





TOP VIEW

	Axis	SYMBOL	COMMON DIMENSIONS		
			MIN	NOR	MAX
Total thickness	A		-	1.17	1.40
Stand off	A1		0.16	0.21	0.26
Substrate thickness	A2		0.22	0.26	0.30
Mold thickness	A3		0.70 REF		
Body size	X	D	7.90	8.00	8.10
	Y	E	7.90	8.00	8.10
Ball diameter			0.30		
Ball width		b	0.27	0.32	0.37
Ball Pitch		e	0.65 BSC		
Ball Count		n	108		
Test Pin size	X	tx	0.275		
	Y	ty	0.275		
Edge ball center to center	X	D1	6.50 BSC		
	Y	E1	6.50 BSC		
BODY CENTER TO CENTER BALL	X	g	0.65	0.75	0.85
	Y	f	0.65	0.75	0.85
Package edge tolerance		aaa	0.10		
Mold flatness		bbb	0.10		
Coplananty		ddd	0.10		
Ball offset(package)		eee	0.15		
Ball offset (ball)		fff	0.08		

11. DISCLAIMER

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12. REVISION HISTORY

Date	Revision #	Description	Page
Aug. 27, 2021	1.0	1. Remove “Preliminary”	
		2. Modify LQFP128 to LFBGA108	4
		3. Add Note.4	8
		4. Add USB compatibility issue.	18
		5. Modify package type to LFBGA108	19
		6. Add LFBGA108 package information	20-21
Sep. 24, 2020	0.1	Preliminary version.	23