On the Zero-Crossing Distortion in Single-Phase PFC Converters

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***Abstract*—Input current distortion in the vicinity of input voltage zero crossings of boost single-phase power factor corrected (PFC) ac–dc converters is studied in this paper. Previously known causes for the zero-crossing distortion are reviewed and are shown to be inadequate in explaining the observed input current distortion, especially under high ac line frequencies. A simple linear model is then presented which reveals two previously unknown causes for zero-crossing distortion, namely, the leading phase of the input current and the lack of critical damping in the current loop. Theoretical and practical limitations in reducing the phase lead and increasing the damping factor are discussed. A simple phase compensation technique to reduce the zero-crossing distortion is also presented. Numerical simulation and experimental results are presented to validate the theory.**

***Index Terms*—Crossover distortion, current distortion, cusp distortion, harmonic current, PFC converter modeling, phase shift control, single-phase PFC converters, zero-crossing distortion.**

I. Introduction

THE ADVANCES IN power factor correction (PFC) technology in the past two decades have enabled the development of single-phase ac-dc converters with close to unity input power factor and much less input current distortion than that generated by simple diode rectification circuits. On the other hand, it has been widely observed that the input current of single-phase PFC converters almost always contains some residual distortion, especially in the vicinity of zero crossings of the input voltage. This *zero-crossing distortion* (also referred to as crossover distortion), although never thoroughly analyzed in the literature and not clearly understood by those practicing in the field, has nevertheless been considered a secondary issue for most low- and medium-power applications with 50 or 60-Hz inputs as far as meeting regulatory requirements is concerned.

Recently, there has been a renewed interest in high-performance PFC technologies, fueled by new harmonic current emission limits for airborne equipment set by such regulatory requirements as DO-160D and ISO-1540. Table I summarizes the harmonic current limits defined in DO-160D for single-phase airborne equipment [1]. The stringent harmonic current limits, coupled with the high line frequency (400 Hz) commonly used on commercial jet airplanes, have forced designers to look into all possible sources of input current distortion, most importantly the zero-crossing distortion. To further compound the design challenge, future aircraft will use ac power of variable frequency ranging from 360 Hz to 800 Hz. A clear understanding of the zero-crossing distortion problem is thus crucial for successful application of single-phase PFC techniques in airborne environment.

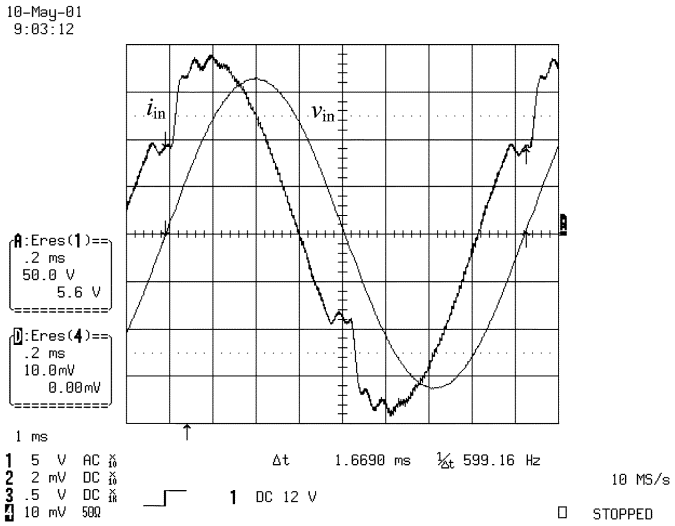

Fig. 1. Input current and voltage waveform of a boost single-phase PFC converter measured with 600-Hz input. The input current contains a capacitive component drawn by a 1.5 μF input filter capacitor at the ac side of the rectifier bridge.

To illustrate the limitations of existing PFC converter design techniques for airborne applications, a boost single-phase PFC converter demo board [2] was measured under different line frequencies. The converter shows almost no visible current distortion when operating from 50–60 Hz input. The distortion level, however, increases significantly when the line frequency is increased to 400 Hz or higher. At 600-Hz input, for example, the input current, shown in Fig. 1, is very distorted and fails to meet the harmonic current limits listed in Table I. It can be clearly seen from Fig. 1 that most of the input current distortion appears around the zero crossings of the input voltage. One may argue that the poor performance may be due to the inappropriate design of the converter for operation under high line frequency. This is, however, not the case, as will be discussed in Section V.

Cusp distortion [3]–[5] and discontinuous conduction mode (DCM) of operation of the boost inductor [6], [7] have been considered the two major causes for the zero-crossing distortion in single-phase PFC converters. The cusp distortion occurs

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TABLE I
DO-160D HARMONIC CURRENT LIMITS FOR SINGLE-PHASE AIRBORNE EQUIPMENT

Harmonic Order	Limits
Odd Non Triplen Harmonics (h = 5, 7, 11, 13, ..., 37)	$I_h = 0.3I_1/h$
Odd Triplen Harmonics (h = 3, 9, 15, 21, ..., 39)	$I_h = 0.15I_1/h$
Even Harmonics (h = 2, and 4)	$I_h = 0.01I_1/h$
Even Harmonics (h = 6, 8, 10, ..., 40)	$I_h = 0.0025I_1$

right after the input voltage crossover where there is very limited voltage across the boost inductor to drive its current up even with the switch closed at all times. As the result, the inductor current may not be able to follow the reference for a short time period after the zero crossing, causing current distortion. In general, using a smaller boost inductor will help to reduce the cusp distortion, but will cause other problems including higher ripple current and more DCM distortion.

Input current distortion due to DCM operation of the boost inductor may occur both before and after the zero crossing. It should be noted that the discontinuous inductor current waveform itself does not necessarily lead to low-frequency input current distortion, especially when the switching frequency is high compared to the line frequency. Rather, it is the lower gain of the power stage (compared to that under continuous conduction mode) that causes a lower current loop gain when the current is discontinuous and deteriorates the input current response. The length of the DCM interval depends on both the power level and the boost inductance value, so the problem is severer when the load is lighter and/or a smaller boost inductor is used. Increasing the boost inductance can shorten the DCM interval and reduce the associated input current distortion, but will cause more cusp distortion.

A close look at the waveform shown in Fig. 1, however, will tell that the cusp distortion and the DCM operation cannot really explain the large zero-crossing distortion appeared in the input current waveform. Specifically, the measured input current appears to be clamped at zero for a time interval prior to the voltage zero crossing, which cannot possibly be caused by DCM operation alone. Additionally, the steep rise of the current after the zero crossing and the subsequent oscillation cannot be explained by either the cusp distortion or the DCM operation.

This paper presents two previously unknown causes for the zero-crossing distortion in single-phase PFC converters employing average current control, namely, the leading-phase effect and the lack of critical damping in the current loop. Both causes are shown to be related to fundamental characteristics of converter dynamics and can be quantified by simple analytical models. They are also shown to be the predominant causes for the zero-crossing distortion, especially when the input line frequency is high compared to the current loop crossover

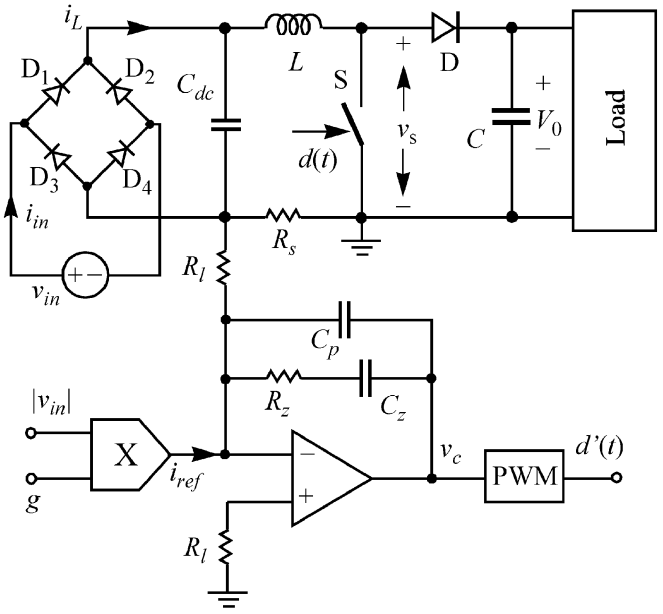

Fig. 2. Boost single-phase PFC converter with average current control. Leading-edge modulation is assumed for the PWM.

frequency. The analytical models from which these effects are predicted also point to possible circuit and control design techniques that can effectively reduce the zero-crossing distortion. Following is a brief outline of the paper.

The next section presents a simple linear model for boost single-phase PFC converter with average current control. Characteristics of the input current transfer function derived from the model are then studied in Section III, pointing to the two new causes for zero-crossing distortion. The analytical models and the analyses are validated by numerical simulation and experimental results in Section IV. Reduction of the zero-crossing distortion through circuit and control design, including adding a phase shift to the reference current, is discussed in Section V along with some experimental results to verify the theory. Applicability of the models to other converter topologies, such as half-bridge and actively clamped SEPIC converters, are briefly discussed in Section VI. Section VII concludes the paper.

II. CURRENT LOOP DYNAMICS AND MODELING

Fig. 2 depicts a typical boost single-phase PFC converter with average current control. The pulse-width modulator is assumed to use leading-edge modulation [2] such that the off-time duty ratio, $d' = 1-d$, of the switch is proportional to the output of the current amplifier, v_c. The inductor current is shown here to be sensed by a resistor; other current sensing methods can also be used, and the model presented in the following is applicable in general. Note that the output voltage loop and the input voltage feedforward loop [3] are not considered here, as they don't interact with the current loop in steady state when properly designed. The circuit diagram also shows a filtering capacitor on the dc side of the diode bridge. This capacitor will be ignored first in the following; its effects on converter performance will be discussed in Section III-C.

The output of the multiplier, which serves as the reference for the boost inductor current, can be expressed as $i_{\rm ref} = g \cdot |v_{\rm in}|$,

where g is a constant under the above assumptions. In steady state and under ideal control, the input (rms) current and power of the converter are related to the parameter g by

$$I_{\rm in} = \frac{gV_{\rm in}R_l}{R_s}, \quad P_{\rm in} = V_{\rm in}I_{\rm in} = \frac{gV_{\rm in}^2R_l}{R_s}. \tag{1}$$

To model the current loop dynamics, we first assume that the PWM carrier signal has a peak-to-peak value equal to V_m, so the gain of the modulator is $1/V_m$. With average current control and the circuit arrangement shown in Fig. 2, the current compensator output, v_c, can be expressed as

$$V_c(s) = \left[R_s i_L - R_l I_{\rm ref}(s)\right] H_c(s) \tag{2}$$

where $H_c(s)$ is the current compensator transfer function

$$H_c(s) = \frac{K_c\left(1+\frac{s}{\omega_z}\right)}{s\left(1+\frac{s}{\omega_p}\right)} \tag{3}$$

$$K_c = \frac{1}{(C_p+C_z)R_l}, \quad \omega_z = \frac{1}{C_zR_z}, \quad \omega_p = \frac{C_p+C_z}{C_pC_zR_z}.$$

Since the modulator can be modeled by a constant gain under average current control [8], the off-time duty ratio of the switch can be expressed as

$$D'(s) = \frac{1}{V_m}\left[R_s I_L(s) - R_l I_{\rm ref}(s)\right] H_c(s). \tag{4}$$

To model the power stage of the converter shown in Fig. 2, we further assume that

1) all components in the circuit are ideal;
2) the boost inductor operates in the continuous conduction mode (CCM) over the entire line cycle;
3) the output voltage V_0 is constant;
4) the sensing resistor, R_s, is small so that it can be ignored when modeling the power stage.

Based on these assumptions, an average model can be written for the boost inductor current, i_L

$$L\frac{di_L}{dt} = |v_{\rm in}| - d'V_0. \tag{5}$$

Next, we will transform (4) and (5) into a model for the input current, $i_{\rm in}$. Since $i_{\rm in} = \mathrm{sgn}(v_{\rm in})\cdot i_L$, (5) can be rearranged to

$$L\frac{di_{\rm in}}{dt} = v_{\rm in} - \mathrm{sgn}(v_{\rm in})\cdot d'V_0. \tag{6}$$

On the other hand, multiplying both sides of (4) by the sign function, $\mathrm{sgn}(v_{\rm in})$, yields

$$\mathrm{sgn}(v_{\rm in})\cdot D'(s) = \frac{1}{V_m}\left[R_s I_{\rm in}(s) - R_l I_{\rm ref}(s)\right] H_c(s). \tag{7}$$

Equations (6) and (7) indicate that the input current dynamics of the boost PFC converter can be represented by the block diagram shown in Fig. 3,[1] from which the following transfer function can be obtained:

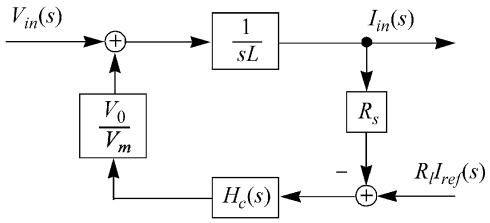

Fig. 3. Block diagram representing the input current dynamics of a boost single-phase PFC converter with average current control.

$$I_{\rm in}(s) = \frac{R_l V_0 V_m^{-1} H_c(s) I_{\rm ref}(s)}{Ls + R_s V_0 V_m^{-1} H_c(s)} + \frac{V_{\rm in}(s)}{Ls + R_s V_0 V_m^{-1} H_c(s)}. \tag{8}$$

Defining

$$\omega_n = \sqrt{\frac{R_s V_0 K_c}{LV_m}}, \quad p(s) = 1 + \frac{s}{\omega_z} + \frac{s^2}{\omega_n^2} \tag{9}$$

and assuming that the effects of the current compensator pole, ω_p, can be ignored in the low-frequency region, i.e.

$$H_c(s) \approx \frac{K_c\left(1+\frac{s}{\omega_z}\right)}{s} \tag{10}$$

we can further simplify (8) as

$$I_{\rm in}(s) = \frac{R_l I_{\rm ref}(s)}{R_s}\cdot\frac{1+\frac{s}{\omega_z}}{p(s)} + \frac{V_{\rm in}(s)}{L\omega_n^2}\cdot\frac{s}{p(s)}. \tag{11}$$

Equation (11) is a key result of this paper. Note that this model is linear, it is a large-signal model since small-signal operation is not assumed in the derivation.

Although leading-edge modulation has been assumed so far, (11) was found to be applicable also under trailing-edge modulation and when a transconductance type amplifier is used for the current compensator. The transfer function will be slightly different when using a conventional current amplifier where the output is offset by the reference, $R_l i_{\rm ref}$, i.e.,

$$V_c(s) = \left[R_l I_{\rm ref}(s) - R_s i_L\right] H_c(s) + R_l I_{\rm ref}(s).$$

In that case, the input current response becomes

$$I_{\rm in}(s) = \frac{R_l I_{\rm ref}(s)}{R_s}\cdot\frac{1+s\left(\frac{1}{\omega_z}+\frac{1}{K_c}\right)}{p(s)} + \frac{V_{\rm in}(s)}{L\omega_n^2}\cdot\frac{s}{p(s)}. \tag{12}$$

As can be seen, the only change of (12) from (11) is the move of the zero in the first term to a lower frequency. This will affect the phase response of the input current and cause more zero-crossing distortion, as will become clear in the next section.

III. Zero–Crossing Distortion

As mentioned in the previous section, the reference signal, $i_{\rm ref}$, for the current loop is generated by scaling down the input voltage by a factor proportional to the output of the voltage compensator, i.e., $i_{\rm ref} = g\cdot v_{\rm in}$. Substituting this relation into (11)

[1] $i_{\rm ref}$ in (7) and Fig. 3 is understood as the reference for the input current, $i_{\rm in}$, instead of the inductor current as in (4) and Fig. 2.

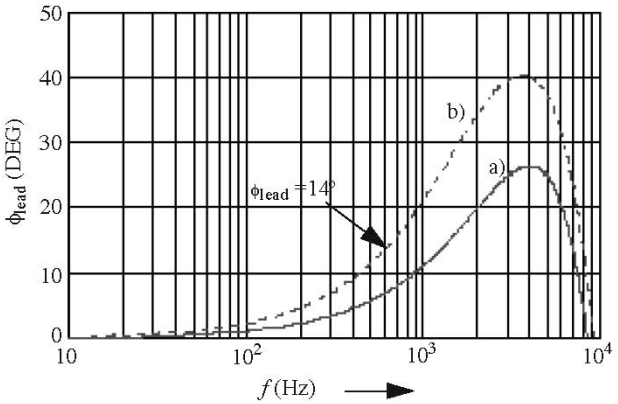

Fig. 4. Phase response of $Q(s)$ as defined in (13) for the example boost single-phase PFC converter with (a) 100-W input power (solid line) and (b) 50-W input power (dashed line).

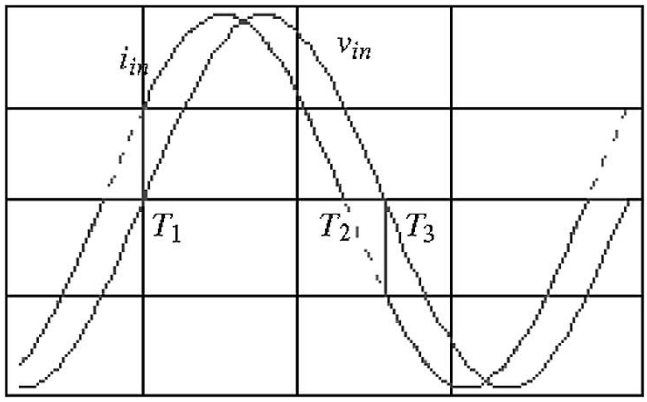

Fig. 5. Input current zero-crossing distortion caused by the diode rectifier bridge when the current has a leading phase. The dashed line represent the theoretical current waveform when the rectifier bridge has bidirectional current capability.

results in the following input current to input voltage transfer function:

$$\frac{I_{\rm in}(s)}{V_{\rm in}(s)} = \frac{gR_l}{R_s} \cdot \frac{1 + s\left(\frac{1}{\omega_z} + \frac{R_s}{gR_lL\omega_n^2}\right)}{p(s)} = \frac{gR_l}{R_s} \cdot Q(s). \quad (13)$$

Equation (13) indicates that the input current has a complex phase and amplitude response. A sinusoidal input current and unity power factor would be achieved if $Q(s) = 1$ holds at the line frequency. However, the following analyses show that this is almost always not the case in practical designs.

A. Phase-Lead and Current Distortion Before Zero Crossing

For typical PFC converter designs, the zero of $Q(s)$ defined in (13) is found to be located at a frequency higher than the line frequency but lower than that of the resonant pole of $Q(s)$, ω_n. This implies a leading phase of the input current relative to the input voltage at the line frequency. As an example, consider again the boost PFC converter described in [2]. The converter has the following parameters (refer to Fig. 2): $L = 1\,\text{mH}$, $V_0 = 385\,\text{V}$, $R_s = 0.25\,\Omega$, $V_m = 4\,\text{V}$, $R_l = 4\,\text{k}\Omega$, $R_z = 12\,\text{k}\Omega$, $C_z = 1.2\,\text{nF}$, and $C_p = 270\,\text{pF}$. The zero of the current compensator, ω_z, is calculated to be $\omega_z = 69\,444\,\text{rad/sec}$, and, according to (9), ω_n is calculated to be 63 971 rad/s. The corresponding phase responses of $Q(s)$ are shown in Fig. 4 for two different cases:

a) $P_{\rm in} = 100\,\text{W}\,(gR_l/R_s = 0.007\,56)$;
b) $P_{\rm in} = 50\,\text{W}\,\backslash,\,(gR_l/R_s = 0.003\,78)$.

As can be seen, $Q(s)$ has an increasing leading phase relative to the input voltage below 8 kHz. The leading phase becomes more significant as the power level decreases. For example, the curve shows that the input current will lead the input voltage by as much as 14° at 600 Hz under 50-W input power.

A leading phase of the input current at the line frequency implies that, within each half line cycle, the input current will reach zero prior to the input voltage zero-crossing point. Consider, for example, the positive half cycle of the line voltage. With reference to Fig. 2 and the waveform in Fig. 5, $i_{\rm in}$ flows through diodes D_1 and D_4 during $[T_1, T_2]$. At T_2, the input current reaches zero and will attempt to reverse its direction due to the leading phase, as indicated by the dashed line in Fig. 5. This would require the conduction of diodes D_2 and D_3. However, D_2 and D_3 are still reverse-biased by the positive input voltage and cannot conduct until T_3. As the result, $i_{\rm in}$ will be clamped at zero for the rest of the half line cycle, as illustrated by the solid line in Fig. 5. The same happens near the end of the negative half cycle of $v_{\rm in}$. The length of the time interval in which $i_{\rm in}$ is clamped to zero is the same in both cases and can be easily determined from (13). Response of the current after the voltage zero crossing, assumed to have a step change in Fig. 5, will be discussed in the next subsection.

The foregoing analysis and the waveform in Fig. 5 indicated that a leading phase of the input current will cause distortion before the zero crossing of the input voltage. The amount of phase lead at the line frequency depends on the location of the zero of $Q(s)$ relative to the line frequency: A large phase lead, hence high zero-crossing distortion, will occur when the line frequency is high and/or the zero of $Q(s)$ is at a low frequency. Note that the zero of $Q(s)$ is a function of both converter and control design as well as the power level, and, in general, moves to higher frequency when current loop crossover frequency increases.

From (12), it can be shown that, under trailing-edge modulation and using a conventional (nontransconductance type) current amplifier, the input current transfer function becomes

$$\frac{I_{\rm in}(s)}{V_{\rm in}(s)} = \frac{gR_l}{R_s} \cdot \frac{1 + s\left(\frac{1}{\omega_z} + \frac{1}{K_c} + \frac{R_s}{gR_lL\omega_n^2}\right)}{p(s)}. \quad (14)$$

Since the zero of (14) is at a lower frequency than that of (13) for a given converter and compensator design, the input current will have more phase lead, hence more zero-crossing distortion. Therefore, use of leading-edge modulation or transconductance type current amplifier can help to reduce zero-crossing distortion in single-phase PFC converters.

B. Damping Factor and Distortion After Zero Crossing

Fig. 5 assumes that the input current undergoes an instantaneous step change right after the voltage zero-crossing. This, however, cannot happen in a real circuit due to dynamics of the input current as described by (13). Instead, the current will

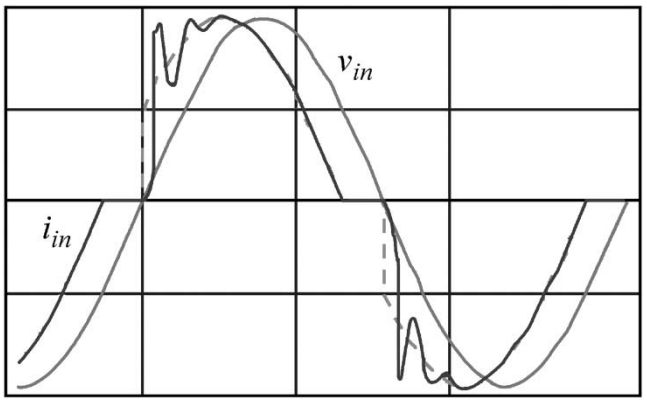

Fig. 6. Input current zero-crossing distortion due to combined effects of phase lead and lack of sufficient damping in the current loop. The dashed line (same as the solid line shown in Fig. 5) corresponds to the current waveform when the current loop is ideal.

follow a trajectory typical of second-order systems, with overshoot and oscillation if the denominator of $Q(s)$ is not critically damped [9]. Note that the damping factor of $p(s)$ is defined by $\zeta = \omega_n/(2\omega_z)$. To determine whether $p(s)$ is critically damped, we note first that the gain of the current loop (see Fig. 3) at the crossover frequency, ω_c, is equal to unity, i.e.,

$$|H_c(j\omega_c)| \cdot \frac{R_s}{V_m} \cdot \frac{V_0}{|j\omega_c|L} = \sqrt{1+\frac{\omega_c^2}{\omega_z^2}} \cdot \frac{R_s V_0 K_c}{\omega_c^2 V_m L} = 1. \quad (15)$$

The current compensator zero, ω_z, is usually placed at the crossover frequency, ω_c [3], in order to maximize the loop gain in the low-frequency region and to ensure a 45° phase margin. Substituting $\omega_z = \omega_c$ into (15) and noting the definition of ω_n in (9), we have

$$\omega_z = 2^{\frac{1}{4}}\omega_n = 1.189\omega_n. \quad (16)$$

Hence, the damping factor of $p(s)$ is $\zeta = \sqrt[4]{2}/2 = 0.42$, which is indeed smaller than the critical damping factor $\sqrt{2}/2 = 0.707$. As such, the current response after the zero crossing will be characterized by overshoot and possibly oscillation, as illustrated by the solid line in Fig. 6. Note that the illustrated waveform closely resembles the measured waveform shown in Fig. 1.

The zero-crossing distortion discussed above is due only to the dynamics of the current loop; other factors such as cusp distortion and DCM operation are not included as they were not considered when deriving the model (11). Also note that the leading phase angle of the input current depends on how close the line frequency is to the zero of $Q(s)$. For a given converter design, the two become closer as the line frequency increases and/or the input power decreases (in which case g is smaller causing the zero of $Q(s)$ to move to a lower frequency.) This provides a quantitative explanation for the increase of crossover distortion with the increase of the line frequency and/or the decrease of input power.

C. Effects of Dc-Side Capacitors

A dc filter capacitor is usually placed between the diode bridge and the boost inductor, as shown in Fig. 2. This capacitor helps to reduce the noise in the rectified line voltage that can otherwise affect the operation of the multiplier. Although this capacitor is usually small, the reactive current it draws adds to the total input current and can cause additional phase lead and more zero-crossing distortion [7], [10]. A simple solution would be to use a $C_{\rm dc}$ that doesn't cause significant reactive current. Since the problem is severer under light load, it is important to select $C_{\rm dc}$ based upon the lower end of input power range. A rule of thumb is to select $C_{\rm dc}$ such that its impedance at the line frequency is in the order of 100 or more times the input impedance of the converter at rated input power. Note that the filter capacitor at the ac side of the rectifier bridge, although also drawing a capacitive current, doesn't cause any current distortion.

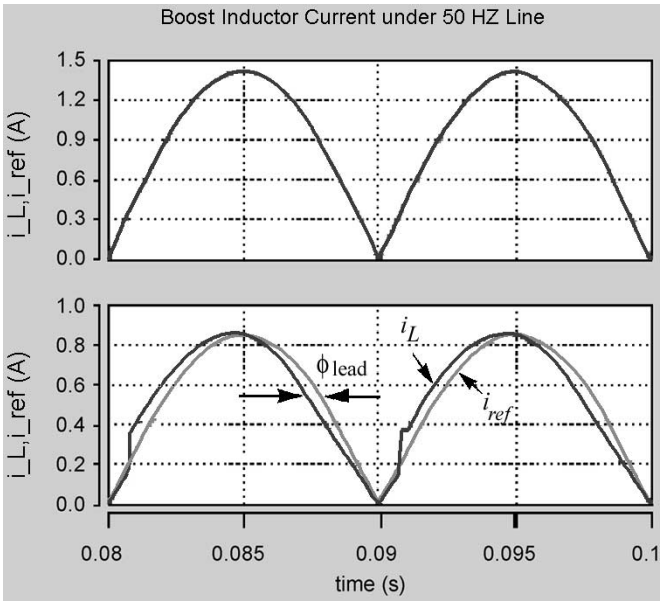

Fig. 7. Simulated boost inductor current waveform of the example boost PFC converter under 50-Hz/115-V input and with different current loop design and output power. Upper traces (a): $\omega_c = \omega_z = 10$ kHz, $P_{\rm in} = 100$ W; Lower traces (b): $\omega_c = \omega_z = 4$ kHz, $P_{\rm in} = 60$ W.

IV. Model Validation

To verify the model and the analyses presented in the previous sections, the boost PFC converter studied in Section III-A was simulated in SABER for operation under various line and load conditions and with different current compensator designs. Since the focus here is on current loop responses, the output voltage feedback loop was kept open in all simulations. For the same reason, the input voltage feedforward path was not included. The model of the converter power stage was built using the unified average PWM switch model presented in [11], which is a large-signal model and is valid for both continuous and discontinuous conduction modes. Use of the average model not only significantly reduces the simulation time and avoids numerical convergence problems, but also allows us to focus on the average current response without the distraction of high-frequency switching ripples.

Fig. 7 shows the simulated boost inductor current waveform in comparison with the reference current under 50 Hz input. The upper traces (a) represent the response when both the compensator zero, ω_z, and the current loop crossover frequency, ω_c, are

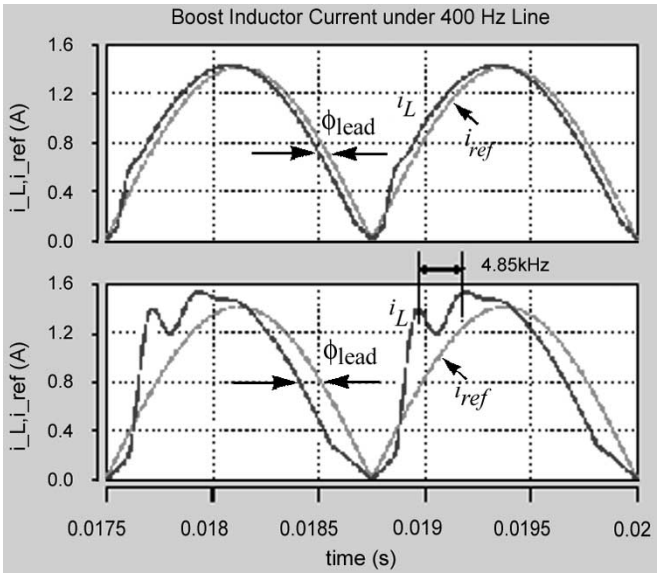

Fig. 8. Simulated responses of the boost PFC converter under 400-Hz/115-V input and with different current loop designs. Upper traces (a): $\omega_c = \omega_z = 10$ kHz; Lower traces (b): $\omega_c = 5.15$ kHz, $\omega_z = 10$ kHz.

at 10 kHz. The input power is about 100 W. The lower traces (b) correspond to a lower input power level (60 W) and a slower current loop, with both ω_z and ω_c at 4 kHz. The damping factor, ζ, is equal to 0.42 in both cases, as explained in the previous section. The leading phase angle of the input current, ϕ_{lead}, at the line frequency was calculated to be 0.85° for the upper traces and 8.8° for the lower traces.

As can be seen, the boost inductor current in Fig. 7(a) contains no visible distortion and is almost identical to the reference. This can be explained by the negligible leading phase angle of the current, which in turn is the result of the relatively wide bandwidth of the current loop and high input power. However, the current in Fig. 7(b) contains significant amount of zero-crossing distortion. The leading phase angle, as indicated in the figure, is found to be very close to the value (8.8°) calculated from (13). The current waveform also resembles that illustrated in Fig. 6, with the exception that, when approaching zero crossings, the simulated current does not follow a sine wave and does not return completely to zero until the input voltage crosses zero. This deviation from the theoretical waveform is caused by the discontinuous conduction mode of the boost inductor near the zero crossing, which was ignored in the derivation of the model. The damping factor is less than the critical value in both cases, which explains the overshoot occurred shortly after the zero crossing in Fig. 7(b). In the case of Fig. 7(a), the lack of critical damping does not cause a visible overshoot because of the negligible phase lead.

Fig. 8 shows the responses of the same converter under 400-Hz input. The upper traces (a) are obtained with the same compensator design as that for Fig. 7(a). However, due to the higher line frequency, the predicted phase lead of the current at the line frequency increases to 6.74°. As can be seen from Fig. 8(a), this relatively large phase lead caused significant zero-crossing distortion in the current. The actual leading phase angle of the current can be measured in the figure and is found to be very close to the predicted value. The overshoot after the zero crossing is similar to that in Fig. 7(b) and is also caused by the lack of critical damping ($\zeta = 0.42$).

The waveform in Fig. 8(b) corresponds to yet another current compensator design, with $\omega_c = 5.15$ kHz and $\omega_z = 10$ kHz. This is not a practically sound design, but serves the purpose of verifying another aspect of the model: With the given values of ω_c and ω_z, the damping factor is calculated to be 0.24. With such a small damping, the current is expected to oscillate for more than one resonant cycle after the zero crossing such that the oscillation frequency can be measured from the simulated waveform. From (9), the oscillation frequency of the current response is calculated to be

$$\omega_b = \omega_n \sqrt{1 - \zeta^2} = 4.85 \text{ kHz}. \tag{17}$$

This is indeed the oscillation frequency of the current after the zero-crossing, as can be seen from the measurement shown in Fig. 8(b). Furthermore, the predicted leading phase of the current is 19.2°, which also correlates closely to the phase lead of the simulated current waveform.

As an experimental verification, the oscillation frequency of the input current with the converter's original compensator design (given in Section III-A) was calculated to be 9.04 kHz. The measured waveform shown in Fig. 1, which was taken under this condition, shows an oscillation after the zero crossing at around 12 kHz, which is close to the predicted value considering possible deviations of component parameters from their theoretical values. Correctness and accuracy of the model as well as the analyses presented in Sections II and III can therefore be concluded.

V. Design for Minimum Distortion

In addition to selecting an appropriate dc-side filter capacitor, the analyses presented in the previous sections also point to other possible solutions to the zero-crossing distortion problem, namely

1) to reduce the amount of phase lead at the line frequency by pushing the zero of $Q(s)$ to higher frequency;
2) to achieve critical damping through appropriate control and/or converter design.

However, there are practical limitations to both approaches. To understand these constraints, we point out first that the crossover frequency, ω_c, of the current loop is usually limited to 1/10–1/5 of the switching frequency by noise and other parasitic effects, and we assume that this limit has already been attained through proper design of the current loop.

To see the constraints on the zero of $Q(s)$ defined in (13), we rewrite it as follows noting that $gV_{\text{in}}R_l = I_{\text{in}}R_s$ holds in steady state

$$\left(\frac{1}{\omega_z} + \frac{R_s}{gR_lL\omega_n^2}\right)^{-1} = \left(\frac{1}{\omega_z} + \frac{V_{\text{in}}}{I_{\text{in}}} \cdot \frac{V_m}{R_sV_oK_c}\right)^{-1}. \tag{18}$$

As mentioned before, ω_z is usually placed at the crossover frequency to maximize current loop gain and to ensure loop stability. With ω_c already at its practical limit, as assumed before, moving the zero of $Q(s)$ to a higher frequency by increasing ω_z would result in less phase margin. On the other hand, the second

term in (18) is related to current loop gain, hence cannot be reduced without increasing the crossover frequency.

It is neither possible to increase the damping factor without negatively affecting the current loop gain and overall control performance: The damping factor can be increased by either increasing ω_n or by decreasing ω_z. The former requires increasing the current loop gain and the crossover frequency, which is not feasible if the loop has already been optimized for maximum bandwidth; the latter will reduce the loop gain at low frequencies, which is not desirable for overall current response.

The foregoing discussion indicates that the leading phase of the input current and the lack of critical damping is inherent in boost single-phase PFC converters, and that reducing the phase lead or increasing the damping factor by modification of current compensator design may negatively affect overall input current response. Note that our discussion has been based on the assumption that the current loop has been properly designed such that the loop gain and bandwidth cannot be further increased without losing stability margin; any design that doesn't meet this assumption will not only suffer from the crossover distortion problem discussed here, but will also have poor overall current response, including possibly distortion over the entire line cycle.

Since (13) was derived based on $i_{\rm ref} = g \cdot v_{\rm in}$, the leading phase of $i_{\rm in}$ relative to $v_{\rm in}$ can also be viewed as a leading phase between $i_{\rm in}$ and $i_{\rm ref}$. Therefore, intuitively, the leading phase between $i_{\rm in}$ and $v_{\rm in}$ can be reduced by adding a phase delay between $i_{\rm ref}$ and $v_{\rm in}$. To determine the necessary amount of phase delay for $i_{\rm ref}$, we assume that $I_{\rm ref}(s) = gV_{\rm in}(s)P(s)$, where $P(s)$ is unknown. Substituting this into (11) yields

$$\frac{I_{\rm in}(s)}{V_{\rm in}(s)} = \frac{gR_l}{R_s} \cdot \frac{P(s) \cdot \left(1 + \frac{s}{\omega_z}\right) + \frac{s}{gR_l R_s^{-1} L\omega_n^2}}{p(s)}. \tag{19}$$

Hence, in order for $i_{\rm in}$ to be in-phase with $v_{\rm in}$, $P(s)$ has to take the following constraint:

$$P(s) = \frac{1 + s\left(\frac{1}{\omega_z} - \frac{1}{gR_l R_s^{-1} L\omega_n^2}\right) + \frac{s^2}{\omega_n^2}}{1 + \frac{s}{\omega_z}}. \tag{20}$$

As can be seen, this transfer function is dependent of the input power as represented by g. Therefore, its realization would require an adaptive filter and is best implemented using digital devices. A simplified version of it, as

$$P(s) \approx \frac{1}{1 + \frac{s}{\omega_z}} \tag{21}$$

can be used instead for analog implementation. This can be implemented by simply adding a capacitor, $C_{\rm d}$, to the input of the multiplier, as shown in Fig. 9 for two different multiplier designs (voltage or current input). The phase shift caused by $P(s)$ will compensator for the intrinsic phase lead of the current loop, thereby eliminating the associated zero-crossing distortion. Note that the added capacitor, $C_{\rm d}$, also helps to reduce the high-frequency noise, providing additional noise immunity for the control circuitry. A similar circuit was used in [12] as a means to reduce dipping of the input impedance.

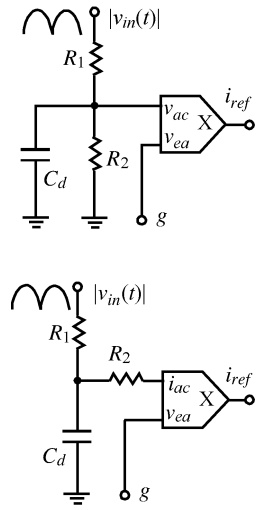

Fig. 9. Implementation of a phase delay in the reference current generation circuit by adding a capacitor to the input of the multiplier. Upper: multiplier input is a voltage. Lower: multiplier input is a current.

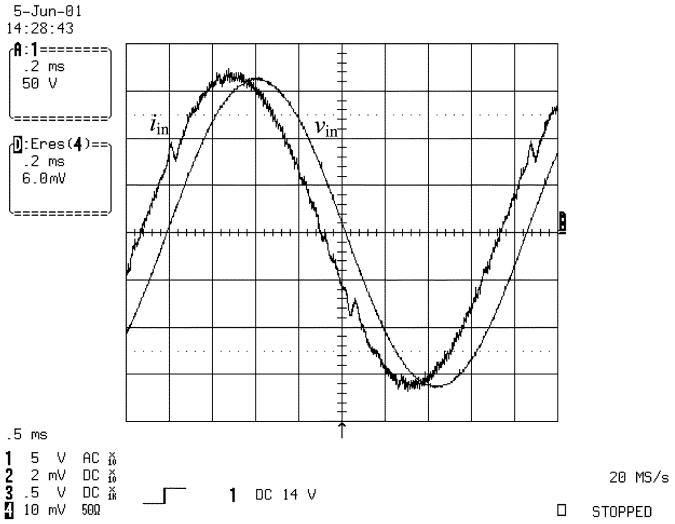

Fig. 10. Input current and voltage waveform of the example boost single-phase PFC converter with phase delay and a 30 nF dc-side capacitor, measured at 600 Hz line frequency.

The phase delay method was applied to the example boost converter studied before. To reduce the additional phase lead due to the dc-side capacitor, its capacitance is reduced from the original 0.47 μF used in [2] to 30 nF. The input current of the converter was then measured at different line frequencies. Fig. 10 shows the results at 600-Hz line. As can be seen, significant reduction in the zero-crossing distortion has been achieved compared to the measurement shown in Fig. 1 for the original design. The remaining phase displacement between the input current and voltage is due to the input filter capacitor of the converter.

VI. Application to Other Topologies

Although the analyses presented so far were for the boost topology, the results are found to be applicable to other topologies as well. As an example, the phase delay control method was applied to a transformer-isolated single-phase PFC converter

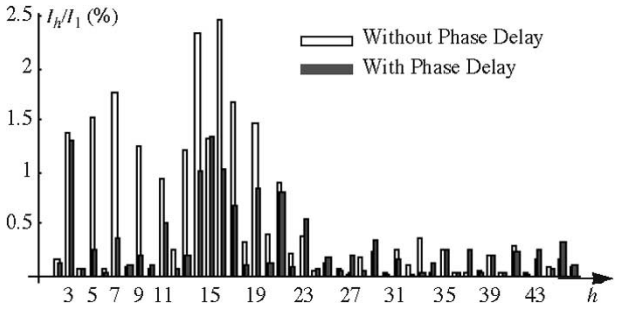

Fig. 11. Input current harmonics of an actively clamped SEPIC PFC converter with transformer isolation.

based on the actively clamped SEPIC topology [13]. Fig. 11 compares the input current spectrum of the converter before and after the phase delay was added. It clearly shows the effects of the added phase delay in reducing input current harmonics.

The models presented in Section II are also applicable to single-phase PFC converters using half-bridge or full-bridge boost topologies [14]. However, these topologies have bi-directional current capabilities, which allows the input current to be out of phase with the input voltage. Therefore, the leading phase of the input current will not cause zero-crossing distortion in these converters, and will only affect the displacement factor of the fundamental component.

VII. Conclusion

A simple mathematical model of boost single-phase PFC converters with average current control was presented. The model reveals some previously unknown characteristics of the input current such as phase lead and overshoot due to the lack of critical damping. These characteristics are demonstrated to be intrinsic in the converter design and responsible for the input current zero-crossing distortion, especially under high line frequencies. A phase delay technique was proposed to compensate for the phase lead, which was proven to be effective in reducing the zero-crossing distortion.

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