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Double Voltage Rectification Modulation for Bidirectional DC/DC Resonant Converters for Wide Voltage Range Operation

Sheng Zong, Guoxing Fan, Xiaobo Yang

***Abstract* –It is difficult to achieve wide voltage range for full-bridge-based bidirectional resonant DC/DC converter due to the large resonant current caused by the small magnetizing inductance. A half-bridge modulation was proposed to extend the output voltage range by offering an additional step-down voltage step of 0.5 normalized gain. But in backward operation, the converter cannot provide the 2-times step-up voltage gain to match the forward 0.5 step-down voltage gain, which disables the converter to truly work bidirectionally with large voltage range. This paper proposes a double voltage rectification (DVR) modulation on the rectification side to achieve twice of the voltage gain for the backward direction to effectively widen the operation voltage range, which matches the ratio of the two DC port voltages where the half-bridge modulation is used in the forward direction. In the DVR modulation, the operation of the input-side resonant tank is the same as that of the conventional modulation. The switches on the input side still turn on with zero voltage switching (ZVS), and the body diodes on the rectification side still turn off with zero current switching (ZCS). Moreover, the turning-on and -off of the MOSFETs on the rectification side are also ZVS, which causes no additional losses and guarantees high frequency operation. The rotational operation of the rectification-side switches improves the thermal balance condition, enlarging the power capacity and improving the reliability of the converter. A smooth transition method between the two modulations is also proposed, which still guarantees ZVS turning-on for the rectification-side switches. The symmetrical CLLLC resonant converter is taken as an example to illustrate the operation principle and features of the proposed modulation. And other bidirectional resonant converters for the DVR modulation are also presented. Finally, a 3kW bidirectional CLLLC resonant converter prototype with 100-kHz resonant frequency is built to verify the proposed modulation.**

***Index Terms* – Bidirectional resonant converter, voltage double rectification, passive rectification, wide voltage range.**

I. INTRODUCTION

LLC resonant converter has become one of the most widespread DC/DC converters for many applications, such as server power supply, LED driver, micro-inverter, and battery charger [1-4]. The advantages include zero voltage switching (ZVS) turn-on for all primary switches, zero current switching (ZCS) turn-off for all secondary rectification diodes, galvanic isolation, simple topology and easy control method. The bidirectional LLC resonant converter and its variants inherit the features of the unidirectional LLC converter, and become the promising candidates for bidirectional DC/DC conversion applications, such as the interface of energy storage devices in the microgrid and distributed power generation system [5-6].

The basic bidirectional LLC resonant converter is formed just by replacing the rectification diodes in the unidirectional LLC converter with active switches [7-8]. But the equivalent model in the backward direction is equivalent to the LC series resonant converter, and thus the AC gain is less than 1, which makes it difficult to achieve enough voltage range. An LC resonant converter is proposed in [9-10], but the soft switching cannot be ensured over the whole operation range. The CLLC resonant converter is proposed in [11] by adding an additional resonant capacitor on the secondary side. But the parameter design requires too many iterations to optimize. Ref [12] proposed a bidirectional LCL resonant converter. Phase shift modulation is used and ZVS can be lost when the duty cycle is small. In [13], an extra inductor is added across the midpoints of the primary-side full bridge to achieve symmetrical output characteristics in the two directions. But additional conduction loss is caused by the extra inductor, and the converter parameter inconsistency can cause non-zero voltage-second product on the inductor causing magnetic saturation. The symmetrical bidirectional CLLLC resonant converter is proposed in [14-17], which has the same output characteristics in the two directions. The conversion gain and design method are similar to the conventional LLC resonant converter.

One of the main limitations of the LLC resonant converter and the bidirectional CLLLC resonant converter is wide voltage range operation, because a very small magnetizing inductance is usually required which causes high conduction losses. However, wide voltage operation is essential to many applications such as telecom power supply, micro-inverter, and interface for battery or super-capacitor in microgrids. A parameter design method for wide output voltage range is analyzed in [18]. But the parasitic parameters are difficult to be determined before design and the operation voltage range extension is still strictly limited. In order to reduce the size of the DC-link capacitor in the server power supply, an auxiliary circuit is added to change the equivalent magnetizing inductance to extend the input voltage range during hold-up time [19]. But additional components require extra footprints and cost. A major type of wide-voltage-range LLC resonant converters are structure reconfigurable converters. Ref [20-21] proposed two LLC resonant converters with a variable resonant

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capacitor and a variable transformer respectively to widen the operation voltage range. The secondary side can also be reconfigurable to double or halve the conversion gain [22-23]. But the additional active switches for the reconfigurable structure cause extra loss, size and cost. Another major means to achieve wide output voltage range is based on variable modulation, which usually does not need additional components. Phase shift plus switching frequency changing is used in [24]. But the ZVS condition depends on voltage gain and power, and can be lost when the equivalent duty cycle is small. Moreover, the abovementioned methods of wide voltage operation are all intended for unidirectional LLC resonant converter, and can barely be used for bidirectional resonant converters. In [25-26], along with changing the switching frequency, full-bridge and half-bridge modulations can be both used to provide two voltage steps, which ensures the realization of ZVS and does not require additional components. But both the modulations can not achieve high step-up voltage gain to interface with low input voltage. Therefore, when the output voltage decreases to a very low level, though the converter can still operate by using half-bridge modulation in the forward direction, the converter is not able to achieve high step-up gain to work backward. Thus wide voltage range cannot be truly realized for bidirectional operation.

In this paper, a double voltage rectification modulation (DVR) is proposed to provide step-up voltage step for bidirectional resonant converters, which extends the operation voltage range in both directions. The proposed modulation requires no extra components, and the soft switching condition is still ensured for all the switches of the bidirectional converter, which ensures the high efficiency and low cost for the converter. The introduction of the proposed modulation is provided in Section II. The operation of the modulation on the symmetrical bidirectional CLLLC resonant converter is elaborated in Section III. The performance and features of the proposed modulation are analyzed in Section IV. The prototype of the bidirectional resonant converter is built and the experimental results are shown in Section V. Finally, Section VI gives the conclusion.

II. Conventional and Proposed Modulations

The symmetrical full bridge bidirectional CLLLC resonant converter has the same voltage gains in the two directions [22], and thus is suitable for wide operation range in both the directions, as shown in Fig. 1.

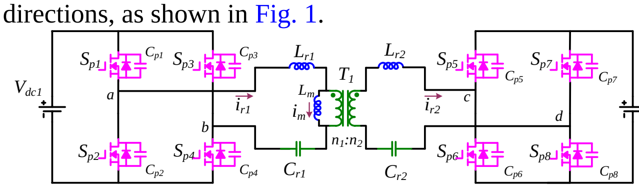


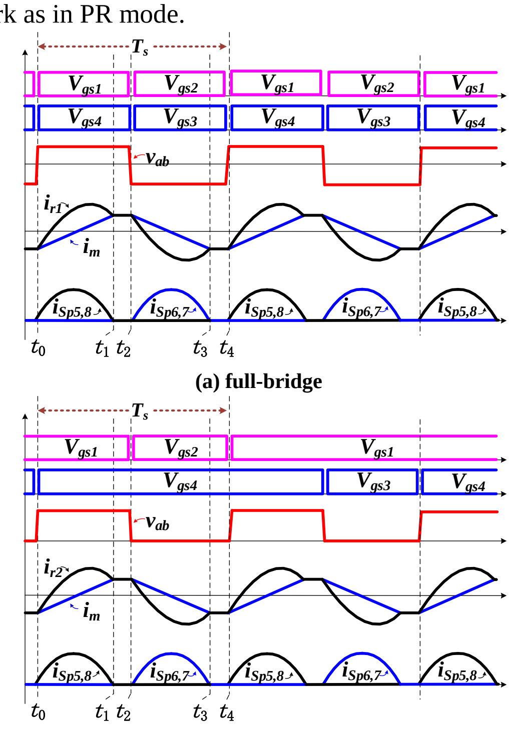
Fig. 1 Symmetrical bidirectional resonant converter

V_{dc1} and V_{dc2} are the voltages of the two DC ports. Since the converter is usually connected between a DC bus and energy storage device (ESD) such as a supercapacitor or battery, V_{dc1} is assumed to be connected to the DC bus whose voltage is relatively fixed, and V_{dc2} is assumed to be connected to the ESD with a wide operation voltage range. The converter is defined to work in forward direction when power is transferred from V_{dc1} to V_{dc2}, and in backward direction if power is transferred from V_{dc2} to V_{dc1}. C_{p1}~C_{p8} are the output capacitances of the four switches respectively. C_{p1}~C_{p4} are all equal to C_{pdc1}, and C_{p5}~C_{p8} are all equal to C_{pdc2}. L_{r1}, L_{r2}, C_{r1}, C_{r2} and L_m are the resonant inductors, resonant capacitors, and transformer magnetizing inductor, respectively. T_1 is the high-frequency transformer with the turn ratio $N=n_1/n_2$. In order to achieve symmetrical gain curves, the resonant components meet the following relations:

$$L_{r1} = N^2 L_{r2} \tag{1}$$

$$C_{r1} = \frac{C_{r2}}{N^2} \tag{2}$$

The conventional modulation for the full bridge resonant converter is only changing the switching frequency. Because all the four switches on the primary side have 0.5 duty cycle and turn on and off in a diagonal pattern, it can be called full-bridge (FB) modulation, as shown in Fig.2(a). V_{gs1} ~ V_{gs4} and V_{gs5} ~ V_{gs8} are the gate signals of the switches on the both sides, respectively. The secondary switches are all kept turned off when working in the forward direction, and only the body diodes work, which is named passive rectification (PR). v_{ab} and v_{cd} are the voltages across the midpoints of the full bridges on V_{dc1} and V_{dc2} sides, respectively. i_{r1}, i_{r2} are the resonant currents. i_m is the magnetizing current of the transformer on V_{dc1} side. i_{sp5} ~ i_{sp8} are the currents through S_{p5} to S_{p8}. In [21], in order to achieve low output voltage and narrow the switching frequency range, the half bridge modulation (HB) is proposed on the switches on the primary side to halve the output voltage, as shown in Fig.2(b). In HB modulation, the output side switches also work as in PR mode.



(a) full-bridge

(b) half-bridge

Fig. 2 Modulations in forward direction

The output curves of the FB and HB modulations in the forward direction are shown in Fig.3(a). G_{AC_F} is the AC voltage gain in the forward direction regardless of the turn ratio of the transformer. f_{sw} is the switching frequency, and f_r is the

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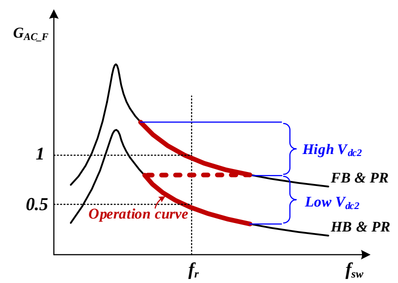
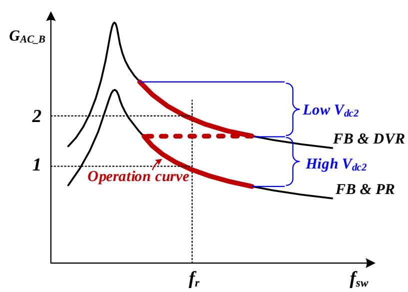
resonant frequency of the converter. The voltage gains of the two modulations should be designed to have an overlap range to cover the whole voltage range.

In the backward direction, V_{dc2} becomes the input voltage. When V_{dc2} is high, FB modulation and PR can also be applied to the V_{dc2} and V_{dc1} sides, respectively, which corresponds to the range of V_{dc2} where FB modulation is used in the forward direction. But when V_{dc2} becomes much lower, neither FB nor HB modulation can provide high enough step-up gain to feed power to V_{dc1}. In this paper, a double voltage rectification (DVR) modulation is proposed on the rectification side to double the output voltage to provide a step-up voltage gain, which just corresponds to the range of V_{dc2} where the HB modulation is used in the forward direction, as shown in Fig.3(b). Meantime, FB is still used on V_{dc2}-side full bridge in order to maximize the voltage gain. With the proposed DVR modulation, the bidirectional resonant converter is fully enabled to work with wide voltage range in both the directions.



(a) FB and HB modulations with PR in forward direction



(b) FB modulation with PR and DVR inbackward direction

Fig. 3 AC gains

III. Operation of DVR Modulation

In the proposed DVR modulation, when the converter works in the backward direction, the full bridge on V_{dc2} side still works in the FB pattern, and the operations of the resonant tanks are almost the same as that in [10]. On V_{dc1} side, instead of bipolar operation, v_{ab} is unipolar by switching S_{p1} and S_{p4}, stepping between zero and V_{dc1}. The voltage of C_{r1} has a DC bias of 0.5V_{dc1} to block saturation of T_1 and L_{r1}. The turning on and off of S_{p1} and S_{p4} are all ZVS, which causes no additional losses and enables high frequency operation.

Similar to the conventional modulation, the converter still has two resonant frequencies with the DVR modulation, which are

$$f_r = \frac{1}{2\pi\sqrt{L_{r1}\cdot C_{r1}}} = \frac{1}{2\pi\sqrt{L_{r2}\cdot C_{r2}}} \quad (1)$$

$$f_m = \frac{1}{2\pi\sqrt{(L_{r1}+L_m)\cdot C_{r1}}} \quad (2)$$

When the switching frequency is below f_r, ZCS is achieved for the rectifier-side diodes, while ZCS can be lost if $f_{sw} > f_r$. At f_r, the resonant tank achieves unity gain regardless the transformer turn ratio.

A. *Below fr*

The key operational voltage and current waveforms of the DVR modulation in the backward direction when $f_{sw} < f_r$ are shown in Fig.4, and the corresponding equivalent circuits in all the stages are displayed in Fig.5. i_{sp1} ~ i_{sp4} are the currents through S_{p1} to S_{p4}. The positive directions of i_{r1}, i_{r2} and i_m are marked by the corresponding arrows in Fig.1, and the real current flow directions are indicated in Fig.5. There are 10 operational stages in a complete switching cycle T_{2s}.

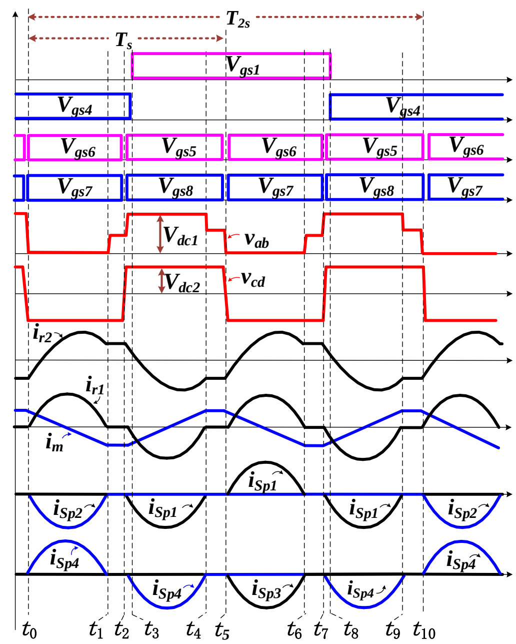


Fig. 4 Operational waveforms of DVR modulation when $f_{sw} < f_r$

Stage 1 [t_0, t_1]: As S_{p6} and S_{p7} turn on at t_0, v_{cd} becomes negative, and the resonant tank is powered by the input voltage V_{dc2}. Resonance begins among L_{r1}, L_{r2}, C_{r1} and C_{r2}. i_{r2} increases in a sinusoidal manner at the resonant frequency f_r. The voltage across L_m is almost constant, and thus i_m rises linearly. Because S_{p4} is already turned on, i_{r1} flows through S_{p4} and the body diode of S_{p2}, clamping v_{cd} to zero. Because the voltage across C_{r1} has a DC bias of 0.5V_{dc1}, the operation of the resonant tank is similar to conventional CLLLC converter. The power is transferred to C_{r1} as the buffer during this stage.

Stage 2 [t_1, t_2]: Once the absolute values of i_{r2}/N and i_m become equal, i_{r1} decreases to zero, and the body diode of S_{p2} turns off with ZCS. During this stage, no power is transferred to the V_{dc1} side, and resonance occurs among C_{r2}, L_{r2} and L_m at the resonant frequency f_m. Because L_m is usually much larger than L_{r2}, f_m is far lower than f_r, and i_{r2} barely changes in this stage.

Stage 3 [t_2, t_3]: When S_{p6} and S_{p7} turn off at t_2, i_{r2} keeps flowing due to the inductive equivalent input impedance and v_{cd} flips to positive. Therefore, S_{p5} and S_{p8} turn on with ZVS. The operation in the deadtime is not shown here. On V_{dc1} side, i_{r1} starts rising from zero, charging C_{p2} and discharging C_{p1}.

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Because C_{p1} and C_{p2} are much smaller than C_{r1} and C_{r2}, the resonant period T_{dc1rec} during this interval is determined by C_{p1} and C_{p2}, as shown below

$$T_{dc1rec} = \frac{1}{2\pi\sqrt{2C_{pdc1}\cdot(L_{r1}+N^2L_{r2})}} \tag{3}$$

This stage is intended for ZVS realization of S_{p1} and S_{p4}. The duration of this stage must be long enough to fully discharge C_{p1} before turning on S_{p1}, which will be analyzed in detail in Section IV B(1).

Stage 4 [t_3, t_4]: After C_{p1} is discharged completely, S_{p1} turns on with ZVS. Since i_{r1} already flows reversely through S_{p4}, S_{p4} also turns off with ZVS. Therefore, ZVS is achieved for both turning on and off of S_{p1} and S_{p4}. The active switching on the rectification side of DVR modulation causes no additional losses compared to the conventional passive diode rectifier. L_m quits resonance, and the resonance starts at f_r. i_{r1} flows through S_{p1} and S_{p4} reversely, transferring power to V_{dc1}.

Stage 5 [t_4, t_5]: This stage is similar to Stage 2. i_{r1} becomes zero, the body diode of S_{p4} turns off with ZCS, and no power is transferred to the V_{dc1}. The resonant tank resonates at f_m.

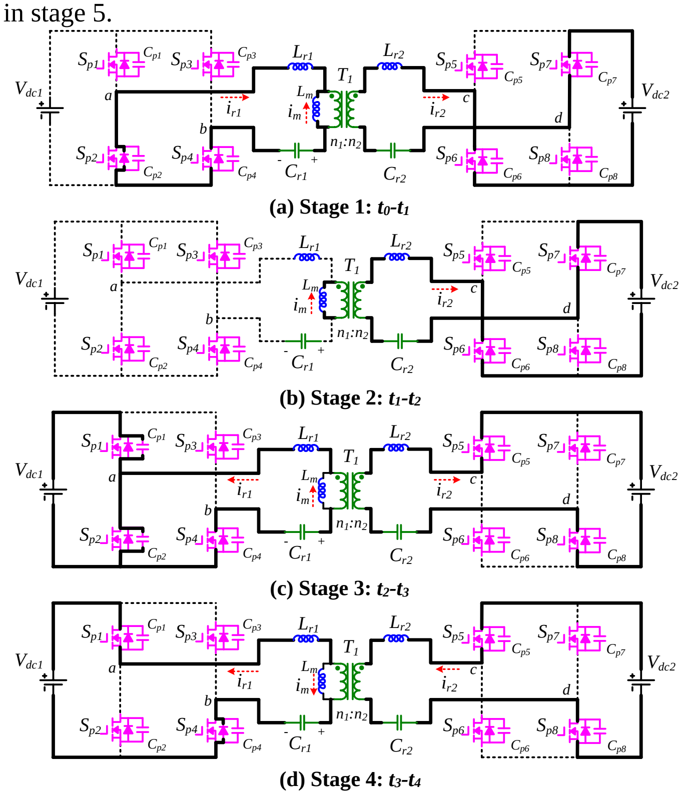
Stage 6 [t_5, t_6]: When v_{cd} flips to negative, i_{r1} starts flowing through S_{p1} and the body diode of S_{p3}, clamping v_{ab} to zero. The operation is similar to that in stage 1.

Stage 7 [t_6, t_7]: The stage begins when i_{r1} decreases to zero, and the operation is similar to stage 2.

Stage 8 [t_7, t_8]: The operation in this stage is the same to stage 3, except that C_{p3} is charged and C_{p4} is discharged, instead of C_{p1} and C_{p2}.

Stage 9 [t_8, t_9]: After C_{p4} is discharged completely, i_{r1} starts flowing reversely through S_{p1} and S_{p4}. Thus ZVS is achieved for both turning-off of S_{p1} and turning-on of S_{p4}.

Stage 10 [t_9, t_{10}]: the operation in this stage is the same as that in stage 5.

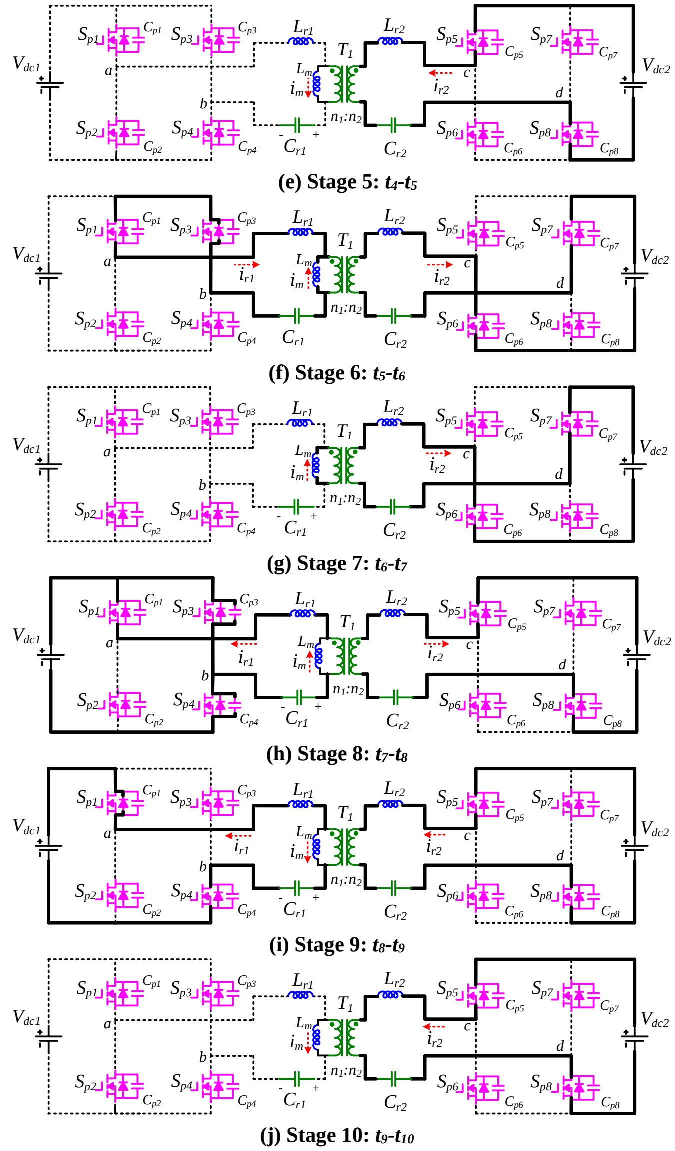


(a) Stage 1: t_0-t_1

(b) Stage 2: t_1-t_2

(c) Stage 3: t_2-t_3

(d) Stage 4: t_3-t_4



(e) Stage 5: t_4-t_5

(f) Stage 6: t_5-t_6

(g) Stage 7: t_6-t_7

(h) Stage 8: t_7-t_8

(i) Stage 9: t_8-t_9

(j) Stage 10: t_9-t_{10}

Fig. 5 Equivalent circuits of DVR modulation when $f_{sw} < f_r$

v_{ab} is controlled to step between zero and V_{dc1} in a switching cycle, doubling V_{dc1} compared to conventional PR operation, while inflicting a DC bias of $0.5V_{dc1}$ on C_{r1}. As described above, $v_{ab} = V_{dc1}$ when i_{r1} flows through S_{p1} and S_{p4} reversely. There are two ways to clamp v_{ab} to 0: the first is conducting S_{p1} and S_{p3} in stage 1, and the second is conducting S_{p2} and S_{p4} in stage 6. The two paths are applied alternately in the proposed DVR modulation to distribute losses more evenly to reduce temperature rise. Therefore, the switching frequency of S_{p1} and S_{p4} is half of f_{sw}.

B. Above f_r

The operational waveforms of DVR modulation when $f_{sw} > f_r$ are shown in Fig. 6, and there are eight operational stages in a complete cycle T_{2s}. The operation is similar to that when $f_{sw} < f_r$. The switches on the V_{dc2} side still work with the FB modulation, while on V_{dc1} side S_{p1} and S_{p4} are turned on and off alternately at $0.5f_{sw}$. The operations in stage 1 [t_0, t_1] and 3 [t_2, t_3] are the same as those in stage 1 and 4 of below-f_r range in Fig.4.

The main difference compared to below-f_r range is that i_{r1} lags v_{cd} when $f_{sw} > f_r$. The switching of S_{p1} and S_{p4} has to be

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delayed much longer than below-f_r range to ensure ZVS turning-on and turning-off of S_{p1} and S_{p4}. The equivalent circuits during the interval between the switching of the two sides are indicated in Stage 2 [t_1, t_2] and Stage 6 [t_5, t_6], as shown in Fig.7. The delay time will be analyzed in detail in Section IV B(2).

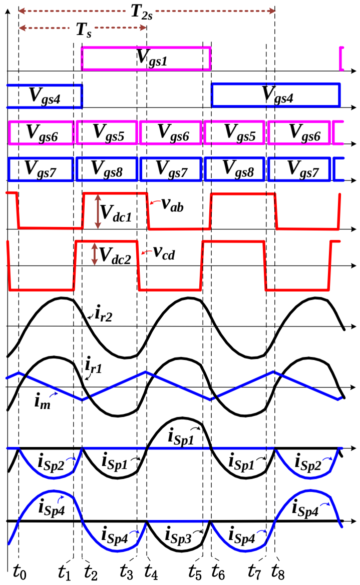
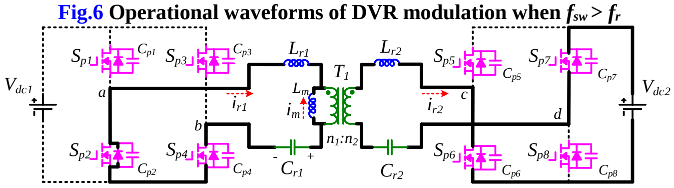
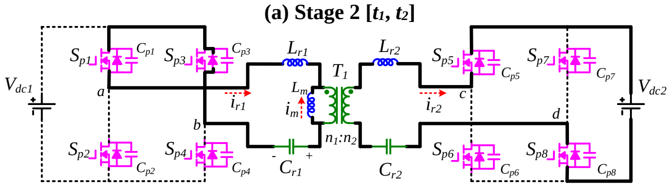


Fig.6 Operational waveforms of DVR modulation when $f_{sw} > f_r$



(a) Stage 2 [t_1, t_2]



(b) Stage 6 [t_5, t_6]

Fig.7 Equivalent circuits of Stage 2 and 6 of above-f_r range

IV. Converter Performance Analysis

A. Output Characteristics

1) Gain and power rating

The first harmonic analysis (FHA) is used to calculate the voltage gain of the converter. The model reflected on V_{dc1} side is shown in Fig.8. $0.5V_{dc1ac}$ and V_{dc2ac} are the first harmonic components of v_{ab} and v_{cd}, respectively. The gain of the converter is the ratio of V_{dc1ac} and V_{dc2ac}. R_{eq} is the equivalent load. Compared to PR, the equivalent voltage across R_{eq} halves, and i_{r1} doubles. Therefore, R_{eq} is only 1/4 of that with the conventional PR:

$$R_{eq\_DVR} = \frac{2}{\pi^2}\frac{V_{dc1}^{\ 2}}{P} \tag{4}$$

where P is the output power of the converter.

The first harmonic transfer function from V_{dc2} to V_{dc1} is

$$G_{dc2-1\_DVR} = 2N\frac{\omega L_m R_{eq\_DVR}}{(\omega L_m R_{eq\_DVR} + \omega L_{r1} R_{eq\_DVR} - \frac{R_{eq\_DVR}}{\omega C_{r1}}) + i(2\omega^2 L_{r1} L_m + \omega^2 L_{r1}^{\ 2} + \frac{1}{\omega^2 C_{r1}^{\ 2}} - 2\frac{L_{r1}}{C_{r1}} - 2\frac{L_m}{C_{r1}})} \tag{5}$$

Thus the absolute value $|G_{dc2\text{-}1\_DVR}|$ is the voltage gain with the proposed DVR modulation.

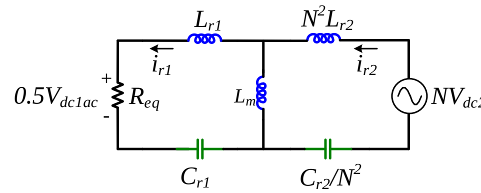


Fig.8 FHA model reflected on V_{dc1} side

For clear comparison, the equivalent load in PR mode is expressed as (6), the first harmonic transfer function from V_{dc2} to V_{dc1} is as shown in (7). With examination of (5) and (7), $|G_{dc2\text{-}1\_DVR}|$ is nearly twice of $|G_{dc2\text{-}1\_PR}|$ at the same frequency, besides that the different equivalent loads slightly affect the output curves.

$$R_{eq\_PR} = \frac{8}{\pi^2}\frac{V_{dc1}^{\ 2}}{P} \tag{6}$$

$$G_{dc2-1\_PR} = N\frac{\omega L_m R_{eq\_PR}}{(\omega L_m R_{eq\_PR} + \omega L_{r1} R_{eq\_PR} - \frac{R_{eq\_PR}}{\omega C_{r1}}) + i(2\omega^2 L_{r1} L_m + \omega^2 L_{r1}^{\ 2} + \frac{1}{\omega^2 C_{r1}^{\ 2}} - 2\frac{L_{r1}}{C_{r1}} - 2\frac{L_m}{C_{r1}})} \tag{7}$$

The normalized gain curves for PR and DVR modes are plotted in Fig. 9, based on the prototype parameters listed in Section V. f_n is the normalized switching frequency defined as f_{sw}/f_r. The gain of DVR mode is almost twice of that of PR mode over the whole frequency range, as analyzed above. For wide voltage range applications, the combination of the proposed DVR mode and PR mode can narrow the switching frequency range effectively, while increasing the conversion efficiency.

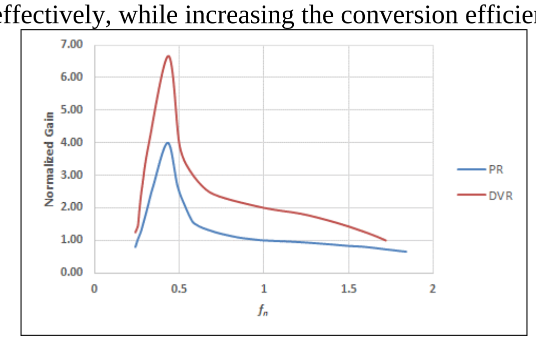


Fig.9 Normalized backward and forward voltage gain allocation

In terms of the maximum transmission power for the DVR modulation, it is limited by the current ratings of V_{dc2}-side switches, i.e. the thermal limit of V_{dc2}-side switches. The maximum current drawn from and fed into V_{dc2} are fixed. When V_{dc2} drops, the transmission power becomes lower. Therefore, the power in DVR mode is lower than that in PR mode. This feature is suitable for battery storage application, since the maximum charging or discharging current is fixed for a battery.

2) Gain range allocation

Another problem is to determine the voltage boundary between PR and DVR modes. Over the whole output voltage range, the DVR mode covers the higher part of the voltage gain, and the lower gain is still provided by the conventional PR mode, as shown in Fig. 10. g_{dh} and g_{dl} are the highest and lowest gains for DVR mode, and g_{ph} and g_{pl} are the highest and lowest

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gains for PR mode. In order to ensure the whole range is considered,

$$g_{ph} \geq g_{dl} \quad (8)$$

Because HB mode in the forward direction is corresponding to DVR mode in backward direction, when V_{dc1} is between g_{dh} and g_{dl} , the forward voltage gain of HB mode is from $1/g_{dl}$ to $1/g_{dh}$. It is the same with PR and FB modes.

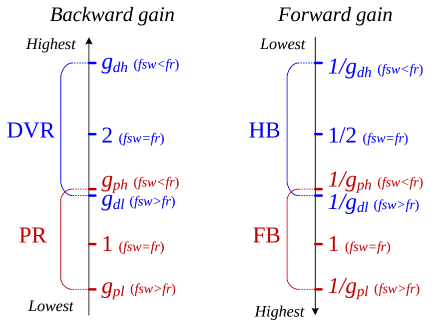

Fig.10 Normalized backward and forward voltage gain allocation

It is assumed M_{max} is the highest voltage gain of PR mode, at which f_{sw} reaches its lowest value, and

$$g_{ph} = M_{max} \quad (9)$$

Since the equivalent resonant tanks on the primary and secondary sides are the same, the gain curves are the same regardless of the multipliers of 2 or 0.5 for different modes. Thus the highest gain in HB mode is

$$1/g_{dl} = 0.5M_{max}. \quad (10)$$

From (8) ~ (10), $M_{max} \geq 1.414$. Thus it is required that the maximum voltage gain of the converter in FB mode is at least 1.414. In order to narrow the switching frequency range, M_{max}=1.414. Therefore $g_{dl} = g_{ph} = 1.414$, which is the transition point between the PR and DVR modes.

Since the voltage gains of DVR mode are just almost twice of that of PR mode, $g_{dh} = 2.828$, and $g_{pl} = 0.707$. Therefore, it is required that the minimum gain of FB mode is at most 0.707. Similarly, in forward direction, the lowest and highest gains of FB are also 0.707 and 1.414, and the gain range of HB mode is from 0.353 to 0.707. The whole gain range in the backward direction is from 0.707 to 2.828, which is a 1:4 voltage range.

In a word, in order to achieve seamless voltage gain change between PR and DVR modes, the gain of the resonant tank is required to cover at least the range of 0.707 ~ 1.414. Given this resonant tank design, the whole gain range for the proposed modulation is around 1:4 which is defined as the ratio of the lowest and the highest output voltage. If the required voltage gain range is narrower than 1:4, the designer can arrange the gain range into the DVR and PR range, as long as the two resonant points are included for higher efficiency. If the required voltage gain range for the target application is wider than 1:4, the gain range of the resonant tank should be designed to be wider than 0.707~1.414, while the transition voltage point does not change.

B. Soft Switching Condition

1) Below f_r

When the switching frequency f_{sw} is lower than the resonant frequency f_r, the switching of S_{p1} and S_{p4} have to be later than the primary switches to ensure ZVS turning-on. The circuit model reflected on the primary side during Stage 3 in Section IIIA is shown in Fig.11. Because L_m is much larger than L_{r1} and L_{r2}, the effect of L_m can be ignored in this stage. Therefore, the model can be seen as a LC resonance circuit with zero initial inductor current. i_{r1} needs to charge C_{p2} and discharge C_{p1} simultaneously, so the equivalent capacitance for i_{r1} is $2C_{pdc1}$ whose voltage is designated as v_{cpdc1}. At the end of Stage 2, v_{cd} is $-N{\cdot}V_{dc2}$, and the voltages of C_{r1} and C_{r2} are V_{cr1_s23} and V_{cr2_s23}, respectively. v_{cpdc1} at the end of Stage 2 is

$$v_{cpdc1\_s2} = -NV_{dc2} + V_{cr1\_s23} + NV_{cr2\_s23} \quad (11)$$

At the beginning of Stage 3, v_{cd} becomes $+N{\cdot}V_{dc2}$. C_{r1} and C_{r2} are much larger than C_{pdc1}, so V_{cr1_s23} and V_{cr2_s23} are almost constant during Stage 3. v_{cpdc1} during stage 3 is expressed as

$$v_{cpdc1}(t) = NV_{dc2} + V_{cr1\_s23} + NV_{cr2\_s23} + 2NV_{dc2}\sin[\omega(t-t_2)-\frac{\pi}{2}] \quad (12)$$

$$\omega = \frac{1}{\sqrt{2C_{pdc1}(L_{r1}+N^2L_{r2})}} \quad (13)$$

At the end of Stage 3, v_{cpdc1} rises to V_{dc1}. So the duration t_{23} of Stage 3 in Fig.4 is

$$t_{23} = \sqrt{2C_{pdc1}(L_{r1}+N^2L_{r2})}\cdot[\frac{\pi}{2}+\arcsin(\frac{V_{dc1}-V_{cr1\_s23}-NV_{cr2\_s23}}{2NV_{dc2}}-\frac{1}{2})] \quad (14)$$

V_{cr1_s23} has $0.5V_{dc1}$ DC bias. V_{cr2} and the AC component of V_{cr1} are both positive during stage 3, and are higher as the load becomes heavier. Considering the worst case when the load is extremely light, and V_{cr2} and the AC component of V_{cr1} are zero,

$$t_{23\max} = \sqrt{2C_{pdc1}(L_{r1}+N^2L_{r2})}\cdot[\frac{\pi}{2}+\arcsin(\frac{V_{dc1}}{4NV_{dc2}}-\frac{1}{2})] \quad (15)$$

Therefore, regardless of the load, t_{23max} can be applied to generate the gates of S_{p1} and S_{p4} to ensure ZVS turning-on when $f_{sw} < f_r$, which is easy to implement by digital or even analog control.

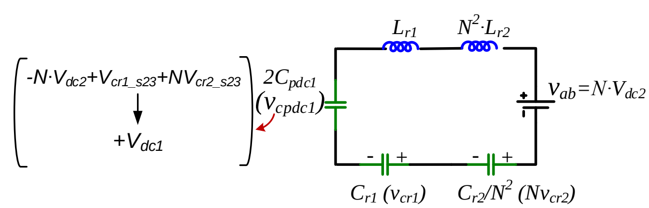

Fig.11 Circuit model of Stage 3 when $f_{sw} < f_r$

2) Above f_r

When $f_{sw} > f_r$, i_{r1} lags v_{cd}, and thus the switching on V_{dc1} side must delay a certain phase to guarantee i_{r1} flipping direction. FHA model in Fig.8 can be used to calculate the phase difference between i_{r1} and v_{cd}. Since i_{r1} is in phase with V_{dc1ac}, the phase difference between i_{r1} and v_{cd} is the same as that between V_{dc1ac} and V_{dc2ac}. Therefore, the angle of $G_{dc2\text{-}1}$ is the phase delay required to ensure ZVS of S_{p1} and S_{p4}. Thus the durations of stages 2 and 6 in Fig.6 are

$$t_{12} = t_{56} = \frac{1}{f_{sw}}\frac{\arg(G_{dc2-1})}{2\pi} \quad (16)$$

where $\arg(G_{dc2\text{-}1})$ is the argument of $G_{dc2\text{-}1}$ in radians.

Although the time delay for ZVS of S_{p1} and S_{p4} can be obtained by (16), the FHA model is not precise enough when f_{sw} is far away from f_r. It is recommended to double check the value by software simulation and give a margin at the same time.

C. Modulation transition

A smooth transition between the DVR and the conventional PR on the output side is key to the safe operation of the

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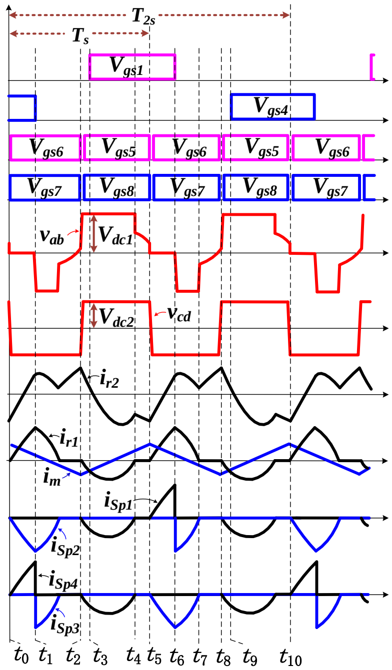
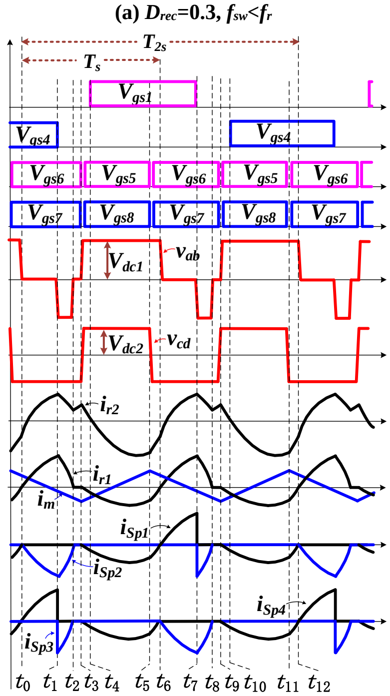
converter and the load which can be sensitive to the supply voltage fluctuation. One major difference between PR and DVR is the DC voltage bias on the resonant capacitor C_{r1}. If the modulations are switched abruptly, the DC voltage bias of C_{r1} would not be built up for the new modulation immediately, and thus a large surge resonant current can occur on both sides, affecting the reliability of the converter badly. Also, the abrupt switch between the modulations causes voltage dip or spike on the output during the transition, which is harmful to the load.



(a) D_{rec}=0.3, f_{sw}<f_r



(b) D_{rec}=0.4, f_{sw}>f_r

Fig.12 Operational waveforms during modulation transitions

A smooth transition method is proposed in this paper: the duty cycle D_{rec} of the rectification-side switches changes gradually, while the output voltage is regulated at the same time by adjusting the switching frequency. For instance, when V_{dc2} decreases, the required voltage gain increases to enter the overlapping range of PR and DVR, PR can be switched to DVR, and thus D_{rec} is needed to change from zero to 0.5. When $D_{rec}<0.25$, the rectification side works in synchronous rectification pattern, the DC bias voltage of C_{r1} is still zero. When $0.5>D_{rec}>0.25$, the DC bias voltage of C_{r1} is equal to $(2D_{rec}-0.5)V_{dc1}$. There is no surge current with D_{rec} gradually changing. Meantime, the switching frequency increases gradually to keep the voltage gain unchanged, which is controlled by the voltage feedback loop. Thus the modulation changes smoothly with no surge current or overvoltage. The operation is similar when the modulation is switched from DVR to PR.

The operation waveforms during modulation transitions are shown in Fig.12. The waveforms in below-f_r range is shown in Fig. 12(a). Between t_2 and t_5, the converter operates for a complete half resonant cycle, which is similar to that in normal operation. But in the other half switching period between t_5 and t_8, due to the early turning-off of the output-side switch, i_{r1} is forced to decrease to zero and enters discontinuous state. The operation in above-f_r range in Fig. 12(b) is similar except that i_{r1} is forced to decrease by the commutation on the input side in the first half switching period, which happens between t_3 and t_5. During the whole transition in both the below-f_r and above-f_r ranges, ZVS turning-on is realized for both the V_{dc2}-side and V_{dc1}-side switches, and ZCS turn-off is achieved for the body diodes of V_{dc1}-side switches. That guarantees device safety as well as high efficiency and low temperature rise during transition. Since ZVS turn-off is lost for the switches on V_{dc1} side, it is recommended to finish transition in a short time.

D. *Other topologies for DVR*

If a resonant capacitor is connected in the resonant tank on V_{dc1} side to block the DC bias voltage of v_{ab}, DVR modulation can be used to extend the voltage range, which is similar to the requirement of HB modulation. Therefore, other than the CLLLC resonant converter, the proposed DVR modulation can also be used on other bidirectional resonant topologies, such as LLC and CLLC resonant converters [8].

V. EXPERIMENTAL VERIFICATIONS

A 3kW bidirectional CLLLC converter prototype is established to verify the theoretical analysis. The specifications of the prototype are listed in Table I. V_{dc1} is fixed at 400V to simulate a DC bus, while V_{dc2} floats from 150V to 400V. The transformer turn ratio is 1:1, so V_{dc2} at the resonant frequency in PR and DVR modes are 400V and 200V, respectively. V_{dc2} range in the DVR mode is from 150V to 300V, and the conventional PR mode is adopted when V_{dc2} is from 270V to 400V. The overlapped V_{dc2} range is 270V-300V, and the transition between DVR and PR happens at around 280V, which complies with the analysis in Section IV A. The resonant frequency is 100kHz, and the switching frequency floats between 65kHz and 200kHz to regulate the output voltage. Throughout the whole voltage range, the V_{dc2}-port output current I_{dc2} is limited at the nominal current 8A, due to the thermal stress of switches.

TABLE I. PROTOTYPE SPECIFICATIONS

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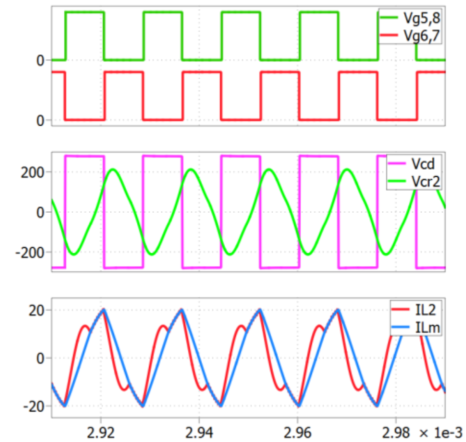
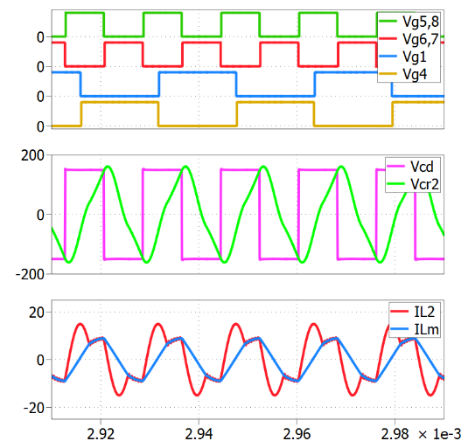
Parameters	Values
V_{dc1}	400 V
V_{dc2} range/ rated	150~400V / 400V
P_{out} (Rated output power)	3.2kW
I_{dc2}	8A
f_{sw}	65~200 kHz
f_r	100 kHz
N (Turns ratio n_1/n_2)	1/1
L_m	64 μH
L_{r1}, L_{r2}	10.2 μH
C_{r1} ,C_{r2}	225 nF
L_{lk1} (V_{dc1}-side leakage inductor)	1.1 μH
L_{e1} (V_{dc1}-side external inductor)	9.1 μH
L_{lk2} (V_{dc2}-side leakage inductor)	3.9 μH
L_{e2} (V_{dc2}-side external inductor)	6.3 μH
S_{p1} ~ S_{p8}	IPW65R041CFD

In order to illustrate the advantages of the proposed DVR modulation, simulations using PLECS are implemented, as shown in Fig. 13. As analyzed in Section IV A, 280V V_{dc2} is the transition point of DVR and PR modes. Since the highest resonant current occurs at the lowest switching frequency point in either mode, 280V-400V conversion with PR mode and 150V-400V conversion with DVR mode are shown in Fig. 13(a) and (b). In comparison, the 150V-400V conversion with PR mode in the conventional solution is shown in Fig.13(c). In the proposed hybrid modulation solution, the resonant current for DVR mode is much lower than PR mode. Thus the highest resonant current for the proposed hybrid solution occurs at 280-400V conversion with PR mode at 63kHz, whose RMS value is 12.9A. The RMS value of the highest resonant current in the conventional PR operation is 16A at 48kHz, which is 25% higher than the proposed solution. That means higher loss on the switches and larger sizes of the inductors and transformer. The peak transformer magnetizing current of the proposed solution is 20A, which is lower than 25A for that of the conventional solution. Thus the core size and losses are further reduced. Moreover, the RMS voltage of V_{cr2} for the proposed solution is 142V, much lower than 239V for that of the conventional solution, which reduces the capacitor size and cost.

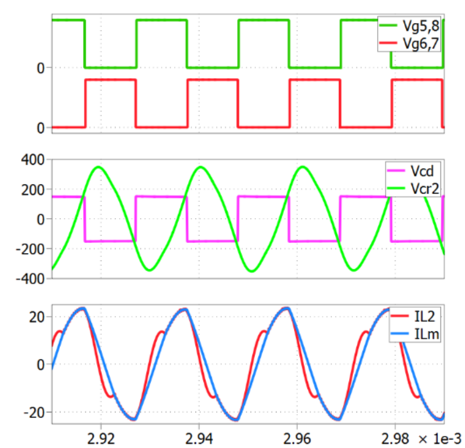
To give a thorough comparison between the two modulations, the RMS values of the resonant current i_{r2} under different V_{dc2} with 8A input current are summarized in Fig.14. When V_{dc2} is below 280V, the proposed DVR mode is applied for the proposed hybrid modulation scheme. The resonant current is lower than the counterpart in the conventional PR scheme. When V_{dc2} is higher than 280V, PR mode is used in both schemes, so the results are the same. Over the whole input voltage range, the highest i_{r2} of the proposed hybrid modulation scheme is at the around 280V, and is much lower than that of the conventional modulation. Therefore, the proposed DVR modulation offers a high efficiency, high power density and low cost solution for wide voltage range applications.



(a) 280V-400V with PR operation in the proposed hybrid solution



(b) 150V-400V with DVR operation in the proposed hybrid solution



(c) 150V-400V with conventional solely PR mode operation

Fig.13 Simulation waveforms of conventional and proposed solutions

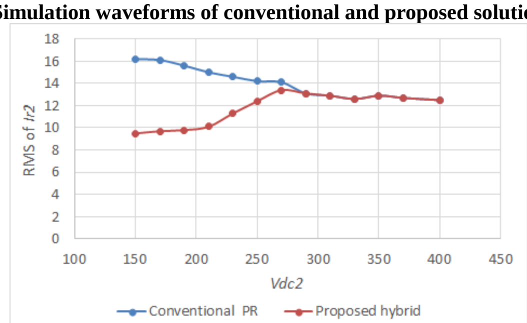


Fig.14 i_{r2} values under different V_{dc2} by simulation

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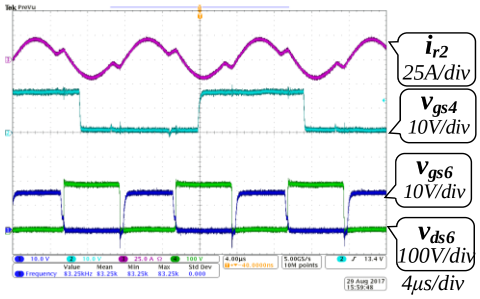
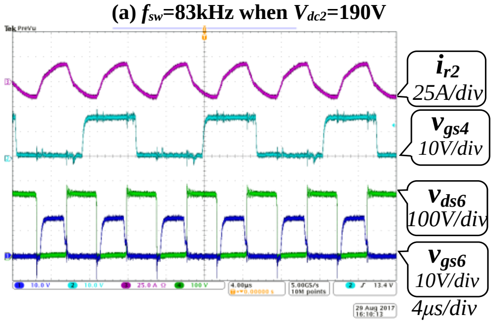
Because the proposed DVR modulation is applied on the backward operation, the waveforms below are captured when the power is transmitted from V_{dc2} to V_{dc1}. The switching waveforms of S_{p6} on V_{dc2} side with the DVR modulation when $f_{sw}<f_r$ and $f_{sw}>f_r$ are shown in Fig. 15. ZVS turning on is achieved for the input-side switches over the whole range due to the inductive input impedance of the resonant tank, which is the same as the conventional modulation.



(a) f_{sw}=83kHz when V_{dc2}=190V

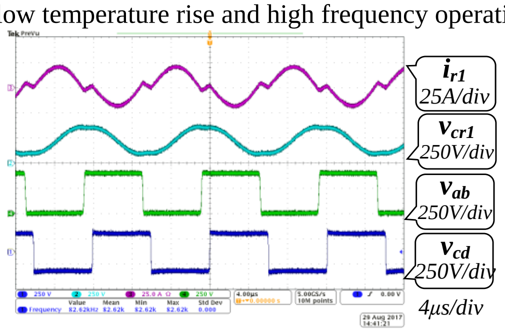


(b) f_{sw}=159kHz when V_{dc2}=250V

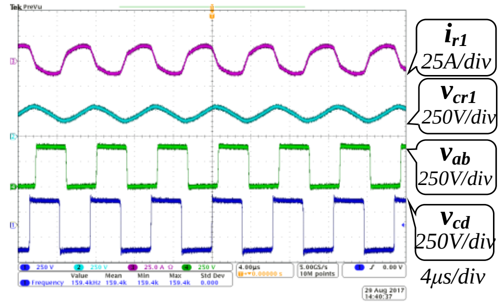
Fig. 15 Switching waveforms of S_{p6} in backward direction

v_{ab}, v_{cd}, i_{r1}, the voltage of the resonant capacitor C_{r1} are shown in Fig. 16. The switching frequency of the output-side switches is half of that of the input-side switches. v_{cr1} has $0.5V_{dc1}$ DC bias voltage. But the resonant capacitor is usually made of an array of high voltage film capacitors to overcome the thermal stress caused by the large AC high-frequency resonant current. The DC breakdown voltage of the resonant capacitor is much higher than the AC peak voltage plus the DC bias voltage. Therefore, the additional DC bias voltage does not cause extra cost on the capacitor. On the other hand, similar to the conventional modulations, ZCS turn off for the body diodes of the output-side switches is also achieved when $f_{sw}\leq f_r$.

The switching waveforms of S_{p4} on the rectification side are shown in Fig.17. Because both of turning-on and -off happen while the switch works in synchronous rectification mode, ZVS on and off are both achieved. Thus the switching of rectification-side switches does not cause any extra loss, ensuring low temperature rise and high frequency operation.

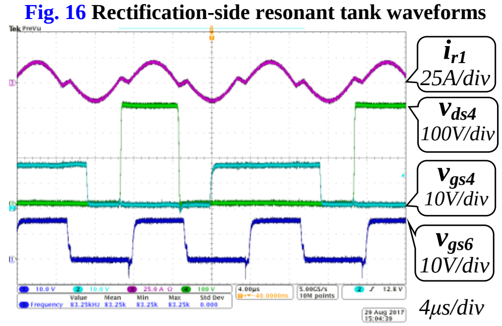


(a) f_{sw}=83kHz when V_{dc2}=190V

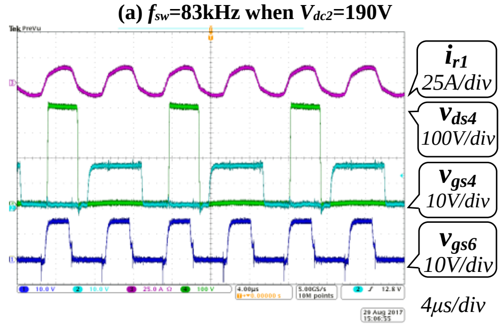


(b) f_{sw}=159kHz when V_{dc2}=250V

Fig. 16 Rectification-side resonant tank waveforms

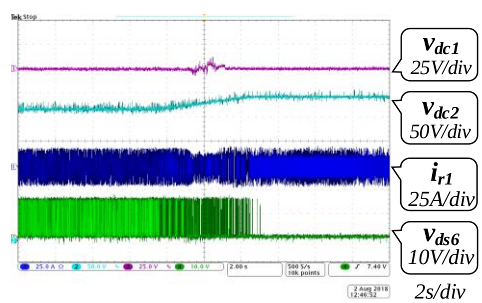


(a) f_{sw}=83kHz when V_{dc2}=190V

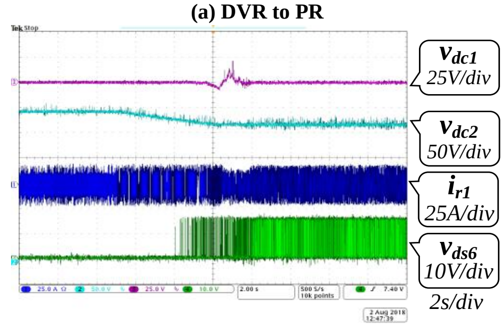


(b) f_{sw}=159kHz when V_{dc2}=250V

Fig. 17 Switching waveforms of S_{p4}



(a) DVR to PR



(b) PR to DVR

Fig. 18 Transition between PR and proposed DVR

The transition between PR and DVR is triggered when V_{dc2} is equal to 280V, which are shown in Fig. 18. The transition process from DVR to PR is captured when V_{dc2} is

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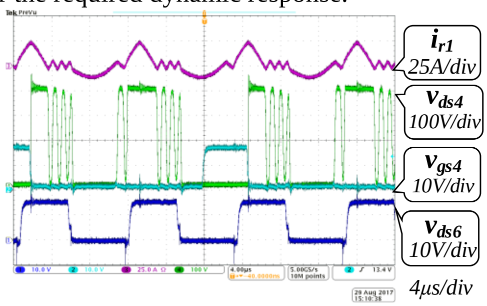
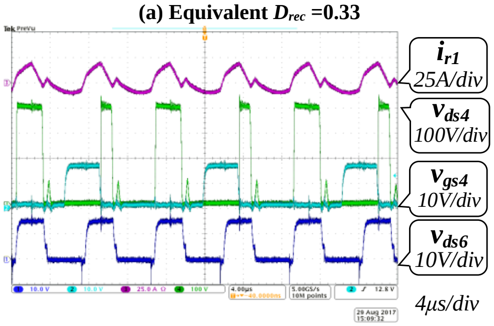
raised from 270V to 290V, as shown in Fig. 18(a). And the reverse process is tested when V_{dc2} is reduced from 290V to 270V, as shown in Fig. 18(b). Because the voltage of V_{dc1} is too large to show with 25V/div scale and DC coupling, 400V offset is set when capturing the waveforms. Due to the gradual change of D_{rec} and real-time voltage regulation by changing f_{sw}, the output voltage V_{dc1} has only 10V overvoltage or voltage dip which is around 2.5% of the nominal voltage, and there is no surge current in the resonant tank during the transition. Since the bidirectional converter is usually to connect to supercapacitor or battery, the proposed transition scheme is enough for the required dynamic response.



(a) Equivalent D_{rec} =0.33



(b) Equivalent D_{rec}=0.43

Fig. 19 Switching waveforms during transition

The switching waveforms during transition between PR and DVR are shown in Fig.19. With different D_{rec}, the rectification-side switches still turn on with ZVS which ensures the safe operation of switches and low temperature rise.

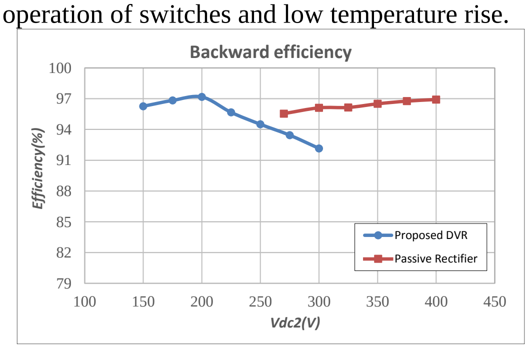


Fig. 20 Experimental efficiency of PR and DVR in backward direction

The measured efficiencies of the converter with PR and the proposed DVR modulations at nominal input current are both shown in Fig. 20. Since the components on the primary and secondary sides are almost the same, only the efficiency of the backward operation is measured. The peak efficiencies are above 97% for the both PR and DVR modulations due to the relatively small resonant current compared to conventional modulation. For the DVR operation at around 200V V_{dc2}, the conduction loss is almost the same as PR, while the output power is lower. But the voltage across the transformer halves, which largely reduces the core loss. Thus the efficiency of DVR at the resonant frequency point is almost as high as that of PR mode. From 200V to 300V in DVR mode, the switching frequency increases rapidly from 100kHz to around 200kHz, leading to significant increase of transformer core loss and MOSFET turn-off losses. Thus the efficiency has a clear drop over this range.

VI. Conclusion

In this paper, a double voltage rectification (DVR) modulation is proposed to extend the voltage range for bidirectional resonant converters by provide a step-up voltage gain step, especially for the backward direction operation. Wide voltage range can be achieved in both directions with this modulation. Similar to the conventional modulation, the switches on the input side still turn on with ZVS, and the body diodes on the rectification side still turn off with ZCS. Moreover, the turning-on and -off of the MOSFETs on the rectification side are also ZVS, which causes no additional losses and guarantees high frequency operation. A smooth transition method is also proposed to suppress surge current and voltage fluctuation along with ZVS on rectification side. Finally, a 3kW bidirectional CLLLC resonant converter prototype with 100-kHz resonant frequency is built to demonstrate that the proposed double voltage rectification modulation is an effective modulation for wide-voltage-range bidirectional DC/DC resonant converter.

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