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Design of GaN-based MHz Totem-pole PFC Rectifier

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***Abstract*—The totem-pole bridgeless power factor correction (PFC) rectifier has recently been recognized as a promising front-end candidate for applications like servers and telecommunication power supplies. This paper begins with a discussion of the advantages of using emerging high-voltage gallium-nitride (GaN) devices in totem-pole PFC rectifiers rather than traditional PFC rectifiers. Critical-mode operation is used in the totem-pole PFC rectifier in order to achieve both high frequency and high efficiency. Then several high-frequency issues and detailed design considerations are introduced, including extending zero-voltage-switching (ZVS) operation for the entire line-cycle; a variable on-time strategy for zero-crossing distortion suppression; and interleaving control for ripple current cancellation. The volume reduction of differential-mode (DM) electro-magnetic interference (EMI) filters is also presented, which benefits greatly from MHz high-frequency operation and multi-phase interleaving. Finally, a dual-phase interleaved GaN-based MHz totem-pole PFC rectifier is demonstrated with 99% peak efficiency and 220 W/in^3 power density.**

***Index Terms*— GaN, totem-pole PFC, MHz, CRM, ZVS, interleaving**

I. Introduction

With the advent of 600 V gallium-nitride (GaN) power semiconductor devices, the totem-pole bridgeless power factor correction (PFC) rectifier, which was a nearly abandoned topology, has suddenly become a popular solution for applications like front-end converters in server and telecommunication power supplies. This is mostly attributed to the significant performance improvement of the GaN high-electron-mobility transistor (HEMT) compared to the silicon (Si) metal–oxide–semiconductor field-effect transistor (MOSFET), particularly its better figure-of-merit and significantly smaller body diode reverse-recovery effect.

The benefits of the GaN-based hard-switching totem-pole PFC rectifier is demonstrated in recent literature [1-6]. As the reverse-recovery charge of the GaN HEMT is much smaller than that of the Si MOSFET, hard-switching operation in totem-pole bridge configuration is practical. By limiting the switching frequency to be around or below 100 kHz, the efficiency could be above 98% for a 1 kW level single-phase PFC rectifier. Even though the simple topology and high efficiency are attractive, the system-level benefit is limited because the switching frequency is still similar to that of Si-based PFC rectifiers.

Previous studies show soft switching truly benefits the cascode GaN HEMT [7-10]. As the cascode GaN HEMT has high turn-on loss and extremely small turn-off loss due to the current-source turn-off mechanism [8], critical mode (CRM) operation is very suitable. A GaN-based critical mode (CRM) boost PFC rectifier has been demonstrated which exhibits the high-frequency capability of the GaN HEMT and shows it has significant benefits, as the volume of both the boost inductor and the DM filter are dramatically reduced [11, 12].

With a similar system-level vision, the cascode GaN HEMT is applied in the totem-pole PFC rectifier while pushing the operating frequency to above 1 MHz [13-15]. Several important issues, which are less significant at low frequencies, are emphasized at high frequencies, and corresponding solutions are proposed and experimentally verified.

To address these issues, the advantages of the totem-pole PFC rectifier are summarized at first, while the differences between hard-switching and soft-switching and between the Si MOSFET and the GaN HEMT are illustrated in Section II. After that, detailed design considerations are presented in Section III, including ZVS extension to solve the problem of switching loss caused by non-ZVS valley switching; variable on-time control to improve the power factor, particularly the zero-crossing distortion caused by traditional constant on-time control; and interleaving control to cancel the input current ripple. The volume of the DM filter is reduced significantly by pushing the operating frequency to several MHz and increasing the use of multi-phase interleaving. Section IV is a summary with hardware prototype and experimental results.

II. Topology Comparison Between the Totem-pole Bridgeless PFC Rectifier and the Dual-boost Bridgeless PFC Rectifier

The bridgeless PFC rectifier has clear advantages [16, 17] because it eliminates the diode rectifier bridge so that the conduction loss of the power semiconductor devices is reduced. Among different boost-type bridgeless PFC rectifiers, the dual-boost bridgeless PFC rectifier is popular in industry products because it has less conduction loss than boost PFC rectifiers; lower common-mode (CM) noise compared to conventional bridgeless boost PFC rectifiers; and only a low-side gate driver, rather than the high-side floating gate driver required by other rectifiers. However, in

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terms of topology, the totem-pole PFC rectifier is even simpler than the dual-boost bridgeless PFC rectifier. Performing a side-by-side comparison using Fig. 1 and Table I, we see that the totem-pole PFC rectifier eliminates the usage of the silicon-carbide (SiC) Schottky diode and requires only four switches and one inductor. Therefore it is the most simplified topology among the boost-type bridgeless PFC rectifiers.

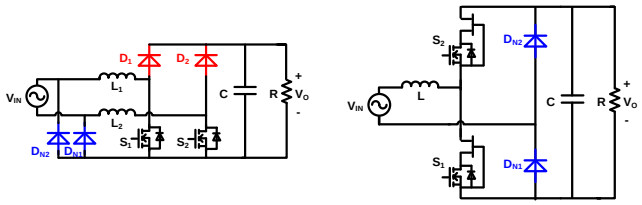

Fig. 1. Comparison between (a) Dual-boost bridgeless PFC rectifier and (b) Totem-pole bridgeless PFC rectifier

TABLE I
Component count of dual-boost bridgeless PFC rectifier and totem-pole bridgeless PFC rectifier

	Dual-boost PFC	Totem-pole PFC
Active switch	2 (S_1/S_2)	2 (S_1/S_2)
SiC Schottky diode	2 (D_1/D_2)	0
Rectifier diode	2 (D_{N1}/D_{N2})	2 (D_{N1}/D_{N2})
Total switch count	6	4
Inductor count	2	1

Even though the topology of the totem-pole PFC rectifier is very simple, it is seldom used due to significant drawbacks that cannot be overcome by using a Si MOSFET. If used with continuous-current mode (CCM) hard-switching operation, it can hardly work because there is tremendous turn-on loss and parasitic ringing due to the reverse-recovery effect of the anti-parallel body diode. Use of the CRM totem-pole PFC has been reported in literature [18-21], and although the previous issue is alleviated by ZCS turn-off of the body diode and ZVS turn-on of the control switch, the increased current ripple still leads to higher conduction loss and higher turn-off loss. So the Si-based CRM mode totem-pole PFC rectifier is usually limited to applications that use low frequencies and a low power level.

The high-voltage GaN HEMT is able to extend the application of the totem-pole PFC rectifier. The significantly reduced reverse-recovery charge of the cascode GaN HEMT makes CCM operation practical within a certain frequency range (e.g. 50 kHz or 100 kHz). Furthermore, the turn-off loss of the cascode GaN HEMT is extremely small, so with CRM operation the switching frequency is able to be pushed to above 1 MHz while achieving good efficiency.

Fig. 2 shows the switching loss distribution of several GaN device samples. The switching loss are tested under similar double-pulse tester setup discussed in [8, 9]. The PCB layout has minimized power loop and driving loop to achieve low parasitic inductance. 0 Ω external gate driving resistor is used to achieve fast possible switching transition speed. The energy stored in the output junction capacitor (E_{OSS}) is calculated according to turve tracer tested C_{OSS}-V_{DS} curve. For the testing results, the E_{OSS} is included in E_{off}. However, the E_{OSS} is actually dumped during turn-on transition. Therefore E_{OSS} is subtracted from E_{off} and added to E_{on} in the date post-process to reflect more accurate switching loss distribution.

Fig. 2 exhibits that for both e-GaN and cascode GaN the turn-on loss is significantly larger than the turn off loss. The major reason is reverse recovery charge or junction capacitor charge induced high current spike during turn-on transition. In addition, when the E_{off} part is enlarged, the dashed green curve shows that the cascode GaN has small and relative flat turn off loss. It has clear advantage if it operates at high turn-off current. The insight of this phenomenon is already illustrated in [8, 9] which is a unique current-source turn off mechanism brought by cascode structure.

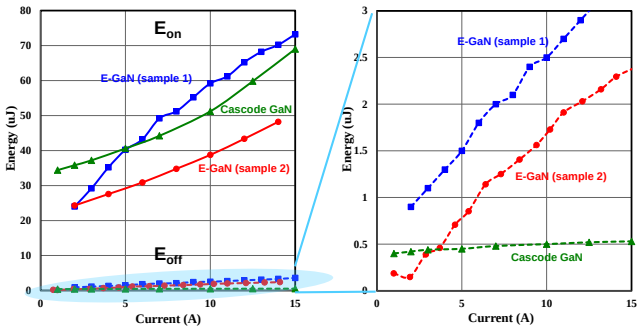

Fig. 2. Measured switching loss distribution of different GaN device samples

When traditional design approach applied to GaN-based totem-pole PFC operating at CCM hard switching condition, the significantly large turn-on loss is the bottle neck to pursue high frequency with reasonable efficiency target. As demonstrated in [1, 6], 99% efficiency is achieved at 50 kHz or 100 kHz but there is very limited system level benefits compared to Si-based design.

Based on the tested switching characteristic of GaN devices, soft switching is preferred in order to dramatically increase the switching frequency without efficiency reduction. Simple CRM soft switching operation is adopted which demonstrates superior advantages in [7-10]. Furthermore, a MHz CRM boost PFC rectifier was demonstrated with 98% peak efficiency. Hence the MHz totem-pole PFC is also designed in CRM and the following sections focus on detailed design considerations.

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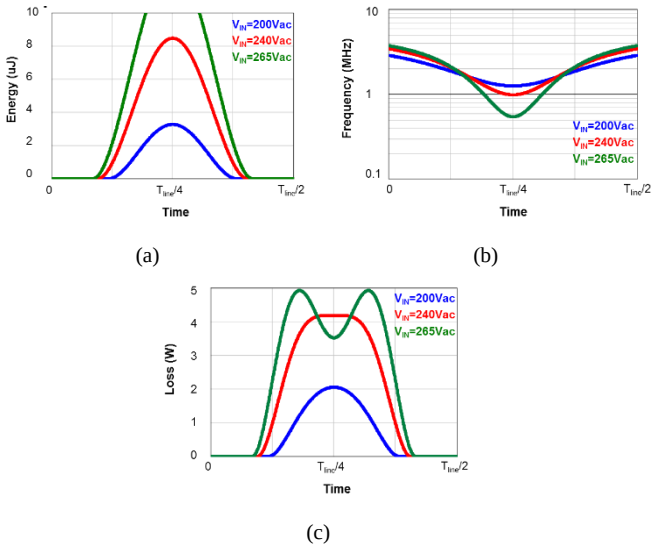
III. Detailed Design Considerations of GaN-based MHz Totem-pole PFC Rectifier

A. Valley switching and ZVS extension

The CRM PFC rectifier utilizes the resonance between the inductor and the device junction capacitors to achieve ZVS or valley-switching. For boost-type CRM PFC rectifiers, ZVS can be achieved only when the input voltage is lower than one-half of the output voltage, assuming a negligible damping effect, which is often true with good design and limited resonant cycles. Thus when the input voltage is higher than one-half of the output voltage, the drain-source voltage can only resonate to a valley point which is equal to ($2V_{in}$-V_o), so ($0.5CV^2$) loss occurs at the following turn-on instant.

The non-ZVS energy of each valley point switch is calculated at each operating point of a half-line cycle according to (1). Then the non-ZVS loss in a half-line cycle is also derived as the product of non-ZVS energy and the switching frequency according to (2). The final step is to average the line-cycles so that the line-cycle averaged non-ZVS loss at different input voltages is calculated according to (3). Fig. 3 illustrates the calculation process.



(a) (b)

(c)

Fig. 3. Calculation process of non-ZVS loss (a) Non-ZVS energy distribution; (b) Frequency distribution; and (c) Non-ZVS loss distribution

$$E_{oss}(V_{in}, t) = \begin{cases} 0 & (V_{in} \le 0.5V_o) \\ 0.5C_{OSS}(2\sqrt{2}V_{in}\sin\omega t - V_o)^2 & (V_{in} > 0.5V_o) \end{cases} \quad (1)$$

$$P_{oss}(V_{in}, t) = \begin{cases} 0 & (V_{in} \le 0.5V_o) \\ 0.5C_{OSS}\left(2\sqrt{2}V_{in}\sin\omega t - V_o\right)^2 f_s(V_{in}, t) & (V_{in} > 0.5V_o) \end{cases} \quad (2)$$

$$P_{oss\_ave}(V_{in}) = \frac{[\int_t^{t+T_{line}} 0.5C_{OSS}(2\sqrt{2}V_{in}\sin\omega t - V_o)^2 f_s(V_{in}, t)]}{T_{line}} \quad (3)$$

As this loss is directly related to the switching frequency, when the frequency is pushed to the multi-MHz level, the non-ZVS loss is significant and dominant in the total converter loss, as shown in Fig. 4.

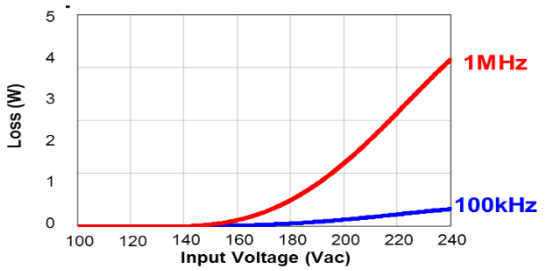


Fig. 4. Line-cycle averaged non-ZVS loss vs. input voltage

In order to solve this issue, the ZVS extension strategy explained in [18-21] is used. The concept is to modify the operation from CRM to quasi-square-wave (QSW) mode. Hence instead of turning off the synchronous rectifier (SR) right before the inductor current crosses zero, a short delay time is purposely added so that there is enough initial energy stored in the inductor to help achieve ZVS after the SR is turned off.

The control of the ZVS extension is critical because if there is too much extra SR on-time, then there would be more circulating energy, increased current ripple and increased conduction loss; on the other hand, if there is not enough SR extra on-time, then ZVS cannot be achieved. To ensure an accurate calculation, a trajectory analysis (Fig. 5) is used which clearly illustrates the resonant status for CRM and QSW modes.

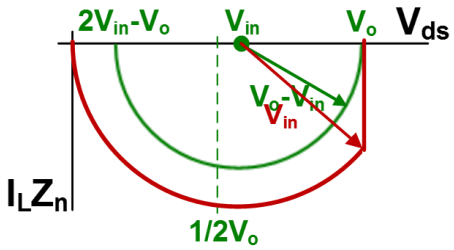


Fig. 5. Trajectory of resonance for CRM and QSW operations

According to the trajectory, the minimum required negative current to achieve ZVS is calculated as (4). Then the required extra SR conduction time is further calculated with (5) in order to achieve the desired negative current. The calculation results are illustrated in Fig. 6. Within the two dashed lines is the non-ZVS zone, which requires ZVS extension control.

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$$i_{min}(t) = \frac{\sqrt{[2V_{in}(t)-V_o]V_o}}{\sqrt{L/2C_{oss(tr)}}} \quad (4)$$

$$t_{SR\_extra}(t) = \frac{L\sqrt{[2V_{in}(t)-V_o]V_o}}{[V_o-V_{in}(t)]\sqrt{L/2C_{oss(tr)}}} \quad (5)$$

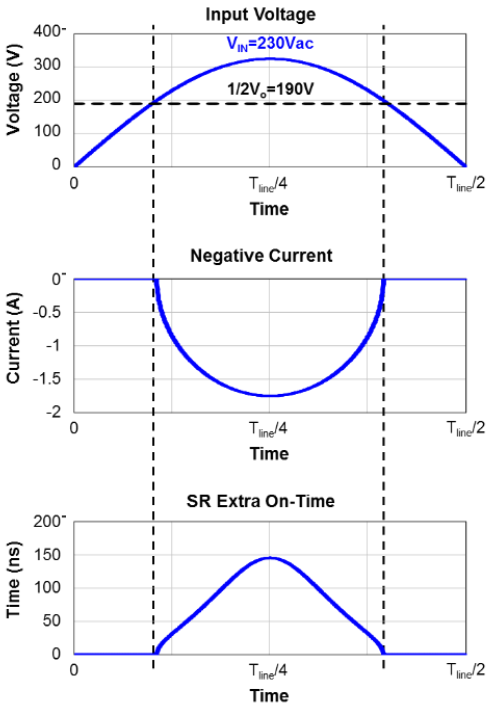
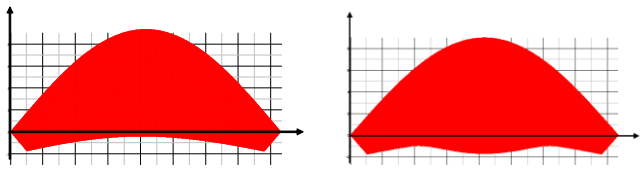


Fig. 6. Minimum negative current and SR extra on-time in half-line cycle to achieve ZVS extension

To further explore this ZVS extension control method, Fig. 7 shows the simulated half-line cycle inductor current without and with ZVS extension, while the experimental waveforms (Fig. 8 and Fig. 9) with entire line-cycle ZVS validates the ZVS extension strategy. The saved switching loss is significant because the total efficiency is increased by 0.3% to 1% from full load to half load, which is shown in Section IV.



(a) (b)

Fig. 7. Half-line cycle inductor current simulation waveforms (a) Non-ZVS and (b) With ZVS extension

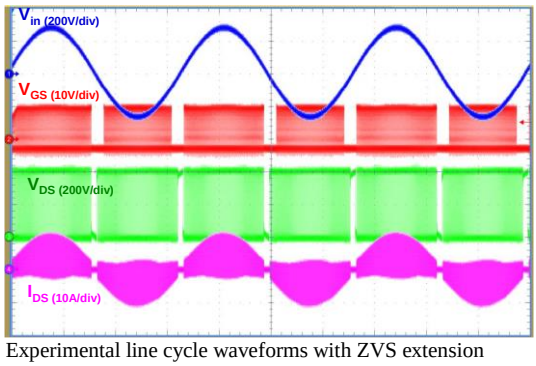
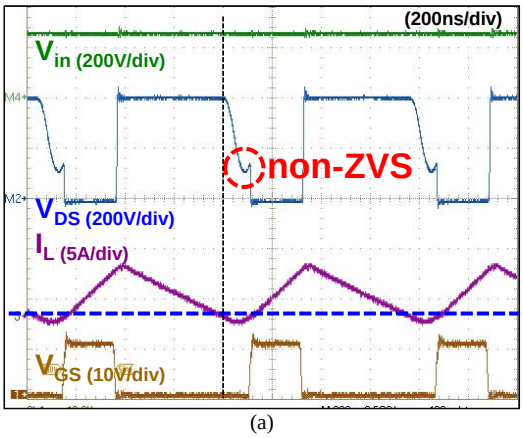
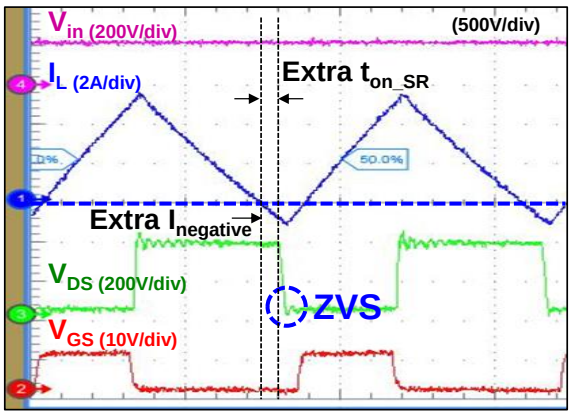


Fig. 8. Experimental line cycle waveforms with ZVS extension



(a)



(b)

Fig. 9. Experimental waveform comparison of (a) Non-ZVS operation and (b) ZVS achieved after ZVS extension

B. Zero-crossing distortion and variable on-time control

The second high-frequency issue is related to the power quality and harmonics emission. Ideally, the CRM-mode PFC offers unity power factor with voltage mode (constant on-time) control. Since the on-time is constant, the envelope of the inductor peak current follows the shape of the input voltage. Then, if ignoring the negative current, the peak current of the inductor is always twice the average current, which means the input current always follows the shape of the input voltage. However, when the frequency is increased

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to the MHz range, the negative current during the resonant period is not negligible; thus there is a notable difference between the shape of the peak inductor current and the average inductor current. In addition, there is also a non-energy transfer time around the time the line voltage crosses zero in which the average inductor current is zero. Both of these lead to increased harmonics and a poor power factor, as shown in Fig. 10 and Fig. 11.

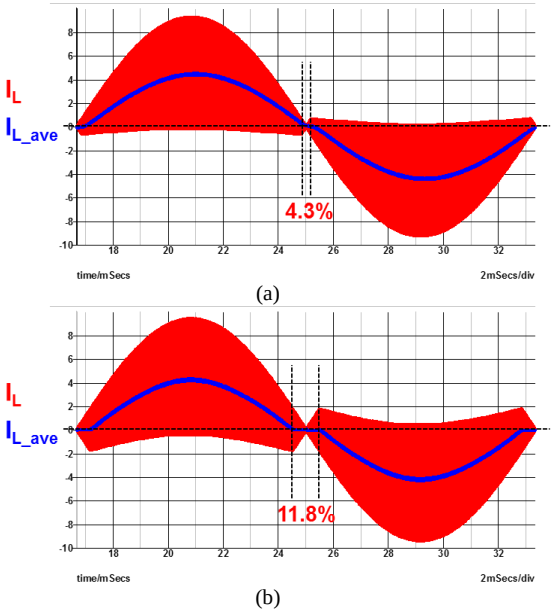

Fig. 10. Frequency impact on power factor and harmonics (a) 100 kHz constant on-time CRM PFC and (b) 1 MHz constant on-time CRM PFC

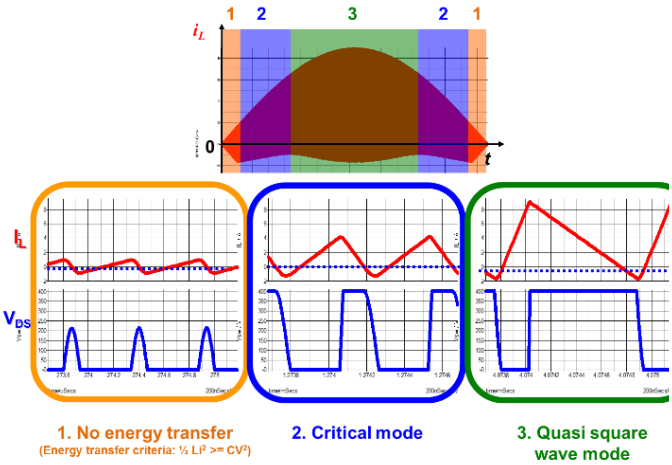

Fig. 11. Three operation modes in half-line cycle with voltage-mode constant on-time operation

Variable on-time control is introduced in [22]. A similar concept is used in this paper but with improved and more accurate implementation by using digital control in order to solve the problems of increased harmonics and a poor power factor. The concept is illustrated in Fig. 12. By increasing the on time near the zero crossing, the input current is again able to achieve good power factor. Fig. 13 shows the experimental verification.

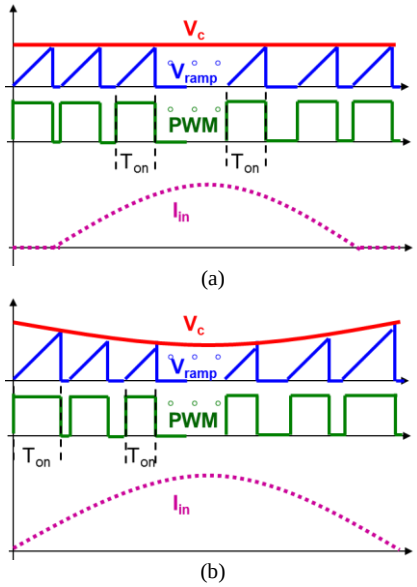

Fig. 12. Concept diagram of CRM PFC with (a) Constant on-time control and (b) Variable on-time control

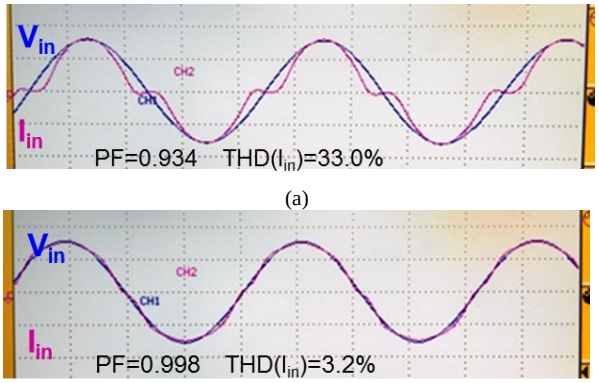

Fig. 13. Experimental verification (a) Constant on-time control and (b) Variable on-time control

The calculation of variable on-time involves massive mathematical work. Different implementations are possible with trade-offs between accuracy and use of microcontroller unit (MCU) resources. A real-time calculation method is practical but requires a high-end MCU, which increases the total cost of the system. Instead, using a look-up table (LUT) is an alternative solution that preloads several tables for different input and output conditions.

An analytical model is built to accurately calculate the required on-time for each operating point in a half-line cycle [23]. Fig. 14 shows the two operation modes and corresponding trajectories in a switch cycle, in which Zn is the characteristic impedance in the resonance, as shown in (6). Since the output junction capacitor (C_{OSS}) has non-linear characteristics and is a function of voltage, a time-

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equivalent output junction capacitor ($C_{OSS(tr)}$) is used to calculate resonant time and impedance. The control switch on-state is defined as the starting point of State I. After State I, all the remaining statuses are determined in Mode 1, critical-mode operation, and Mode 2, quasi square-wave mode operation. As the trajectory is unique with a given circuit design and input/output parameters like V_{in} and V_o, then the instantaneous current in every switch cycle can be derived as a function of on-time. So the average current can also be derived in a further step. After that, the average current is equal to a sinusoidal reference so that the on-time distribution in a half-line cycle can be calculated as the required variable on-time table to achieve unity power factor.

$$Zn = \sqrt{\frac{L}{2Coss(tr)}} \tag{6}$$

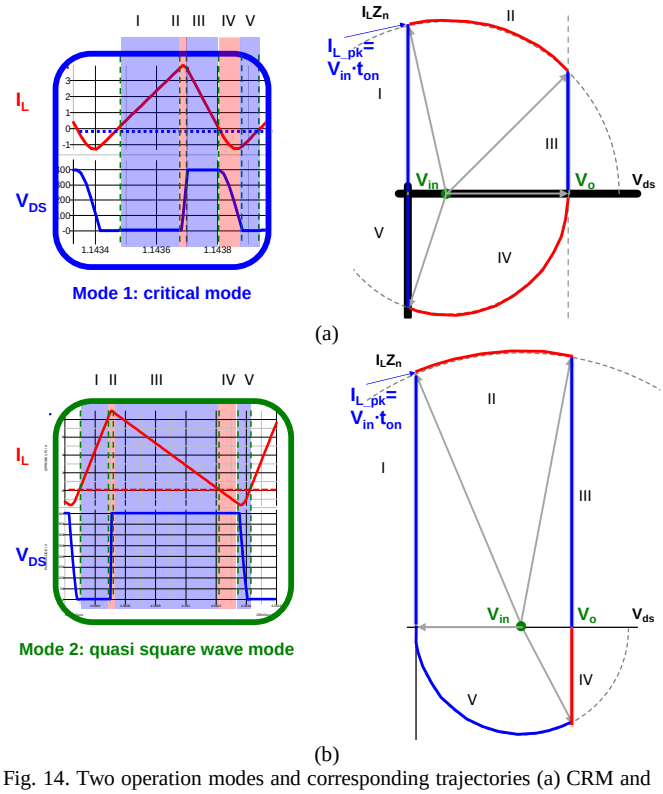

Fig. 14. Two operation modes and corresponding trajectories (a) CRM and (b) QSW

C. Dual-phase interleaving and ripple cancellation

Another drawback of the CRM PFC rectifier is the high current ripple, which leads to not only higher conduction loss but also higher DM noise than the CCM PFC rectifier. To deal with this issue, a two-phase interleaving structure is used to effectively reduce the DM noise by taking advantage of the ripple cancellation effect. Fig. 15 shows the preferred 2-phase interleaved totem-pole PFC topology.

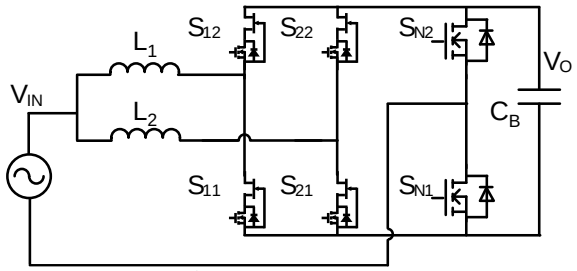

Fig. 15. Circuit diagram of two-phase interleaved totem-pole PFC with cascode GaN devices

The impacts of high-frequency current on the DM filter are shown in Fig. 16 and Fig. 17. By pushing the frequency 10 times higher, the volume of the DM filter is reduced at least 50% and a simple one-stage filter is sufficient to suppress the noise to be below the EMI standard. By making use of good interleaving, the volume is reduced by another 50%. Thus in total, the DM filter is just one-quarter of the size of a 100 kHz DM filter. Further analysis regarding EMI filter design for this MHz totem-pole PFC is included in [12].

Interleaving control is very critical to achieving good interleaving and maintaining a small enough phase error. The waveforms in Fig. 18 show that good interleaving is achieved. Therefore even though the current ripple in each phase is always more than two times higher than the average phase input current, the total input current ripple is significantly reduced by interleaving. The interleaving control is usually not an issue for frequencies below 100 kHz, but it becomes a challenge for multi-MHz variable-frequency CRM PFCs. Issues related to MHz-level high-frequency interleaving control and digital implementation are addressed in [15].

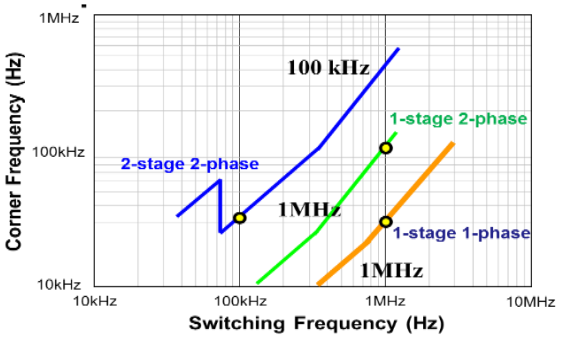

Fig. 16. Switching frequency impact on DM filter corner frequency

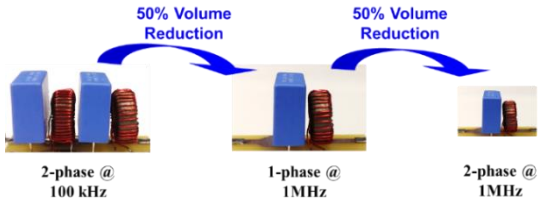

Fig. 17. DM filters for 100 kHz and 1 MHz totem-pole PFC rectifier

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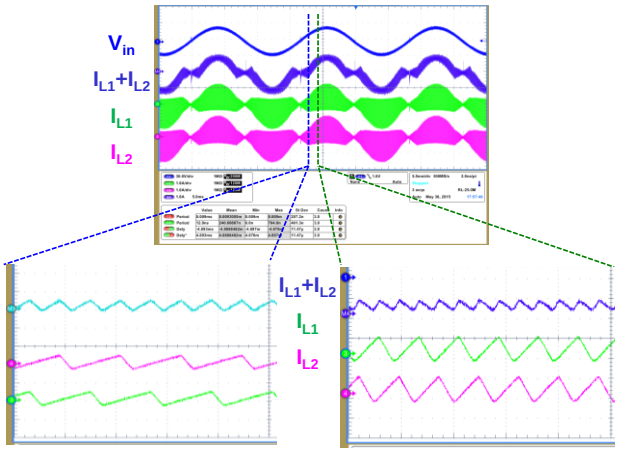

Fig. 18. Ripple cancellation effect with two-phase interleaving

D. Digital control implementation

As no commercial CRM PFC controller currently supports multi-MHz operation, it is quite a challenge to implement the MHz CRM totem-pole PFC and all the functions mentioned above. An MCU-based digital control is used that balances the tradeoffs between performance and cost. The system diagram with MCU-based control implementation is shown in Fig. 19.

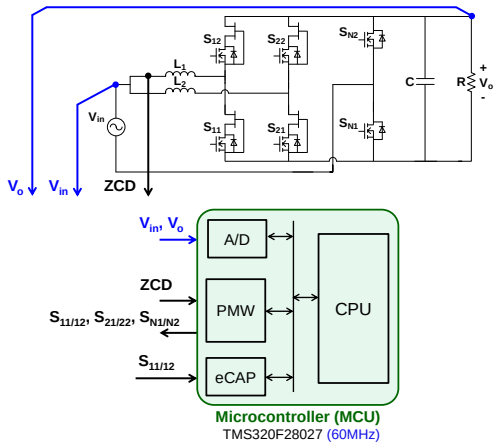

Fig. 19. System architecture with MCU-based digital control implementation

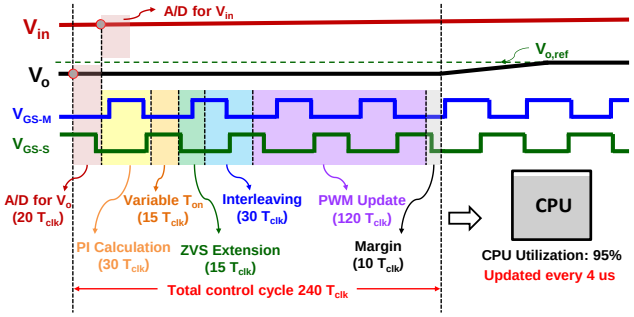

Fig. 20. MCU control implementation sequence (V_{GS-M} and V_{GS-S} are the gate driving signal of the control switch of the master phase and the slave phase respectively)

Fig. 20 shows the sequence of different functions. One control cycle takes close to 240 digital clock cycles which equals to 4 us when it is implemented by the 60 MHz clock frequency MCU. 95% CPU resources are utilized within the 4 us.

IV. Experimental Results and Summary

The prototype of the dual-phase interleaved totem-pole PFC is shown in Fig. 21. The power rating is 1.2 kW and the power density achieved by this prototype is around 220 W/in^3. The DC-link capacitors are not included with the PFC because the capacitors are used to handle double-line frequency ripple and to meet hold-up time requirements, so while the capacitances are closely related to the design of the DC-DC stage, they do not benefit from the high-frequency operation of the PFC.

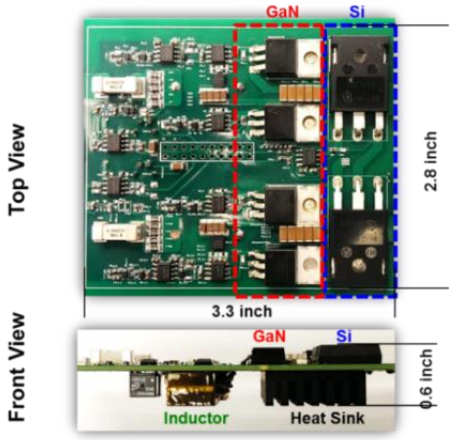

Fig. 21. Prototype of two-phase interleaved 1.2 kW MHz totem-pole PFC

In this design, S_{11}, S_{12}, S_{21}, and S_{22} are cascode GaN (TPH3006PS) operating at high frequency while S_{N1} and S_{N2} are Si MOSFETs (IPW65R019C7) switching at line frequency. S_{11} and S_{12} form phase 1 while S_{21} and S_{22} form phase 2. In positive line cycle when the input voltage is positive, S_{N1} is always on and S_{N2} is always off; then for each phase the bottom switch is the control switch and the top switch is operating as synchronous rectifier. In negative line cycle, the functions of two switches in a half bridge are swapped therefore the topology has symmetric characteristic. S_{N1} and S_{N2} are also considered as line frequency synchronous rectifier with lower conduction loss and better control of negative current to realize ZVS of all high frequency control switches. The two phases usually operate with 180-degree phase shift to have ripple cancellation benefit for the total input current.

The inductor design follows the guideline presented in [24]. The shape of the magnetic core is ER23/4/13. The magnetic material is Mn-Zn ferrite P61 from ACME which is designed for 1-6 MHz applications with low core loss

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property. The winding is 12 turns of litz wire (250/46). About 1 mm air gap is added in the middle of all three legs.

ZCD is another critical issue in hardware design. DCR derived inductor current sensing method is not applicable since the common mode voltage across the inductor is too large. Sensing resistor in series with bottom switch doesn't work in negative line cycle. Sensing resistor in the return path is good for single phase topology but not applicable for multiphase topology with interleaving. Current transformer (CT) method is applicable but each cascode GaN needs one CT series connected. The bulky CT will make the critical power loop very large thus significant switching loss and parasitic ringing can be induced which are major drawbacks. Finally, the ZCD sensing method proposed in [28] is adopted, which is good for interleaved topology, no side impact on power loop, and relative simple implementation. 60 mΩ resistor is connected in series between the AC input and inductor of phase-1. High speed comparator ADCMP601 is used to sense the polarity of phase-1 inductor current. High speed digital isolator ADUM1100 is applied to transfer the floating ZCD signal to the controller. Isolated auxiliary power supply MEU1S0505ZC provides power to the comparator and the primary side of the digital isolator.

Digital isolator ADUM1100 and high speed current booster FAN3122 are adopted to design the gate driver. Boot-strap power supply structure is used for the high-side driver. Similar design guideline discussed in [29] is considered to avoid dv/dt and di/dt related noise issues.

Fig. 22 is the tested single phase efficiency at $230V_{ac}$ input and $400V_{dc}$ output condition. It is close to 99% with ZVS extension strategy. The efficiency and THD in this paper are measured based by YOKOGAWA PZ4000 power analyzer.

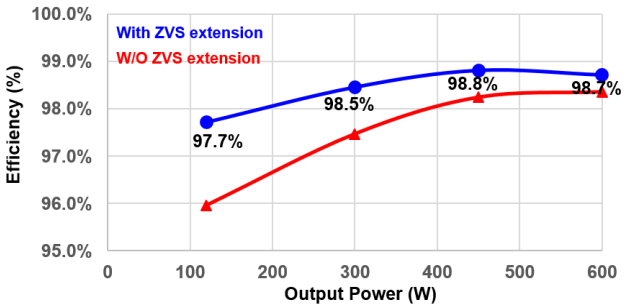

Fig. 22. Measured single-phase efficiency with ZVS extension to reduce non-ZVS loss

Fig. 23 further shows the loss breakdown at full load condition. Without ZVS extension, the non-ZVS loss is the highest loss bar. After ZVS extension is implemented, the non-ZVS loss is almost eliminated with very small increase on other loss bars. As a result, the efficiency is improved from the red curve to the blue curve. There is 0.3% efficiency improvement at full load point and 1.8% efficiency improvement at 20% light load point. This is because the switching frequency becomes higher from heavy load to light load. Thus the impact of ZVS extension is becoming more significant.

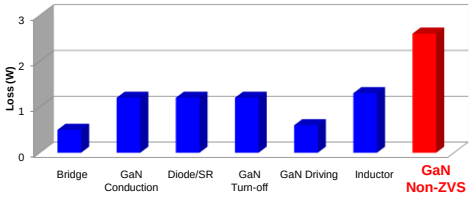

Fig. 23. Loss breakdown at full load condition without ZVS extension

Fig. 24 is the measured total harmonic distortion at different load. Constant on-time has significant diction around line cycle zero crossing thus the THD is much higher than the limit. Variable on-time is effectively reduce the THD to below the red line. On the other hand, variable on-time can also reduce the switching frequency over a line cycle. Fig. 25 further compares the switching frequency distribution between constant on-time and variable on-time.

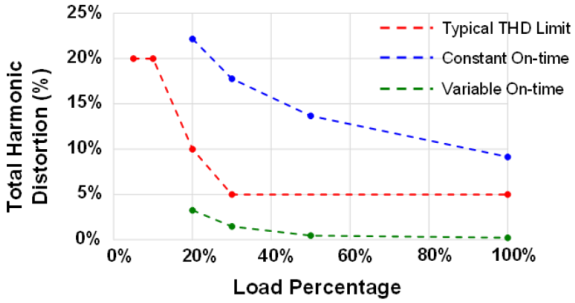

Fig. 24. THD reduction with variable on-time control

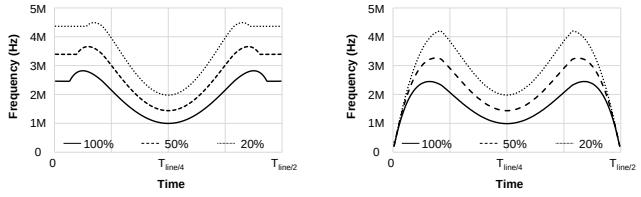

Fig. 25. Frequency distribution with different loading for (a) constant on-time operation and (b) variable on-time operation

The discrete cascode GaN HEMT has a capacitor mismatch issue [10] which causes extra loss. With the solution proposed here, a full-bridge GaN module [25-27] is built with better performance, smaller volume, and improved thermal dissipation capability than existing cascode GaN HEMTs. This design will be applied in the next version totem-pole PFC hardware design so that both efficiency and power density can be further improved.

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DISCLAIMER

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