**Cascode Voltage Switch Logic**

* Cascode Voltage Switch Logic (CVSL) seeks the benefits of ratioed circuits without the static power consumption.
* It uses both true and complementary input signals and computes both true and complementary outputs using a pair of nMOS pulldown networks.
* The pulldown network f implements the logic function as in a static CMOS gate, while f uses inverted inputs feeding transistors arranged in the conduction complement.
* For any given input pattern, one of the pulldown networks will be ON and the other OFF.
* The pulldown network that is ON will pull that output low.
* This low output turns ON the pMOS transistor to pull the opposite output high.
* When the opposite output rises, the other pMOS transistor turns OFF so no static power dissipation occurs. Figure 9.20(b) shows a CVSL AND/NAND gate.
* Observe how the pulldown networks are complementary, with parallel transistors in one and series in the other. Figure 9.20(c) shows a 4-input XOR gate.
* The pulldown networks share A and A transistors to reduce the transistor count by two. Sharing is often possible in complex functions, and systematic methods exist to design shared networks.
* CVSL has a potential speed advantage because all of the logic is performed with nMOS transistors, thus reducing the input capacitance.
* As in pseudo-nMOS, the size of the pMOS transistor is important. It fights the pulldown network, so a large pMOS transistor will slow the falling transition.
* Unlike pseudo-nMOS, the feedback tends to turn off the pMOS, so the outputs will settle eventually to a legal logic level.
* A small pMOS transistor is slow at pulling the complementary output high. In addition, the CVSL gate requires both the low- and high-going transitions, adding more delay.
* Contention current during the switching period also increases power consumption.
* Pseudo-nMOS worked well for wide NOR structures.
* Unfortunately, CVSL also requires the complement, a slow tall NAND structure. Therefore, CVSL is poorly suited to general NAND and NOR logic.
* Even for symmetric structures like XORs, it tends to be slower than static CMOS, as well as more power-hungry.
* However, the ideas behind CVSL help us understand dual-rail domino and complementary pass-transistor logic discussed in later sections.

