Wi-FLIP: A Wireless Smart Camera Based on a Focal-plane Low-power Image Processor

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Abstract—This paper presents *Wi-FLIP*, a vision-enabled WSN node resulting from the integration of *FLIP-Q*, a prototype vision chip, and *Imote2*, a commercial WSN platform. In *Wi-FLIP*, image processing is not only constrained to the digital domain like in conventional architectures. Instead, its image sensor — the *FLIP-Q* prototype — incorporates pixel-level processing elements (PEs) implemented by analog circuitry. These PEs are interconnected, rendering a massively parallel SIMD-based focal-plane array. Low-level image processing tasks fit very well into this processing scheme. They feature a heavy computational load composed of pixel-wise repetitive operations which can be realized in parallel with moderate accuracy. In such circumstances, analog circuitry, not very precise but faster and more area- and power-efficient than its digital counterpart, has been extensively reported to achieve better performance. The *Wi-FLIP*'s image sensor does not therefore output raw but pre-processed images that make the subsequent digital processing much lighter. The energy cost of such pre-processing is really low — 5.6mW for the worst-case scenario. As a result, for the configuration where the *Imote2*'s processor works at minimum clock frequency, the maximum power consumed by our prototype represents only the 5.2% of the whole system power consumption. This percentage gets even lower as the clock frequency increases. We report experimental results for different algorithms, image resolutions and clock frequencies. The main drawback of this first version of *Wi-FLIP* is the low frame rate reachable due to the non-standard GPIO-based *FLIPQ*-to-*Imote2* interface.

I. INTRODUCTION

Wireless Sensor Networks (WSNs) can be considered one of the basic building blocks for *ubiquitous computing* [1], the so-called third generation of computing systems. Tiny low-cost autonomous sensor nodes endowed with processing and communication capabilities constitute their backbone. The potential of application of WSNs has been jointly growing with the sensing capabilities incorporated to the nodes. Currently, most of these capabilities are related to scalar physical magnitudes like temperature, humidity or barometric pressure. However, a new possibility has begun to be explored recently by the research community: multimedia sensing [2]. Specifically, the incorporation of vision results of great interest because of its impact on the field of surveillance systems [3].

The implementation of vision hardware at WSN nodes is not a trivial issue at all. The visual stimulus implies to handle a massive flow of multidimensional information. This information could be simply transmitted for remote processing, but it would dramatically affect the scalability and bandwidth of the network. Alternatively, the node itself could deal with the image flow by taking advantage of its processing capabilities. In this case, the nature of such processing is greatly influenced by energy constraints. Conventional processing architectures make use of an image sensor that simply delivers a serialized raw digital data flow to be processed by a DSP. This is not very suitable when it comes to early vision tasks, that is, low-level image processing [4]. These tasks feature a very heavy, though regular, computational flow in which all pixels are equally processed at every step. Therefore, few instructions applied to all pixels define the corresponding task. Additionally, the result of the computations associated with each pixel is usually independent from the result of the computations over the rest. This means that each pixel can be processed in parallel with the rest without distorting the outcome. And finally, a moderate accuracy (6-7 bits) suffices for this outcome in most cases. This enables the physical implementation of low-level tasks by means of analog circuitry, not very precise but realizing exactly the same processing than its digital counterpart in a faster and more area- and power-efficient way.

The possibility of integrating photosensors with processing hardware in CMOS technologies has opened the door for exploiting these characteristics of early vision. Better performance is thus achieved by massively parallel focal-plane arrays based on the Single Instruction Multiple Data (SIMD) paradigm [5]–[7]. In these arrays, locally interconnected pixel-level analog PEs carry out, concurrently with photosensing, low-level image processing. All the PEs execute the same instruction in parallel but applied to different data. As a result, a pre-processed image flow is delivered, alleviating the computational load of subsequent digital stages. The performance of the system is improved not only because of the energy efficiency of the focal-plane processing. Also the clock frequency and memory accesses are significantly reduced as the digital processor does not have to realize now a great deal of repetitive operations over a serialized data flow. While the ratio 'power consumption'/'computational power' of the arrays reported are really competitive, their total power consumption is still high. Specially, if we think in terms of the strict power budgets demanded by WSN nodes. Recently, we have reported a prototype chip designed ad-hoc for ultra

low-power applications [8]. This chip, called *FLIP-Q*, consists of a SIMD-based focal-plane array implementing a subset of processing primitives intended to deliver a very reduced data flow. Vision-enabled WSN nodes found in the literature carry out data reduction along different processing stages for the sake of low power consumption. However, most of them do not include specific hardware for it. In this paper, after reviewing related work, we present *Wi-FLIP*, the system resulting from the integration of *FLIP-Q* and *Imote2*, a WSN platform commercialized by MEMSIC Corp. From a general point of view, it could be said that *Wi-FLIP* is a vision-enabled WSN node whose image sensor does not simply capture and digitize images. It can be also programmed to efficiently perform early vision tasks whose outcome is a simplified, less data, though elaborated, content-aware, version of the scene being surveyed.

II. RELATED WORK

Different approaches other than the conventional Imager-Memory-DSP scheme have been reported to incorporate vision capabilities into WSN nodes. The wireless smart vision node in [9] is mostly oriented to applications within the field of distributed intelligent surveillance. The core of the system is a 32-bit ARM7 processor that controls the radio module as well as two kilopixel imagers and a VGA camera. One of the kilopixel imager is continuously polling for moving objects entering its field of view. Once one or possibly more objects have been detected, basic stereo vision of the two kilopixel imagers yields the distance to the object. This information allows to calculate and extract only the region of interest containing the object within the VGA camera's image plane. *WiCa* [10] represents the first attempt to exploit the inherent parallelism of early vision tasks. This platform includes *Xetal-II* [11], a high-performance digital co-processor designed ad-hoc for frame-based real-time video analysis. This co-processor contains 320 digital processing elements which work in parallel to reach a measured peak performance of 107GOPS with a power consumption of 600mW. In addition to *Xetal-II*, *WiCa* includes a general-purpose processor, implemented on a CPLD, for control and medium- and high-level image processing. For radio communication, an external module is connected to *WiCa*. The *EyeRIS*[TM]-based platform reported in [12] takes further than *WiCa* the adaptation of the architecture to the characteristics of visual processing. The vision capabilities of this WSN node are provided by *EyeRIS*[TM] v1.2 [13], a general-purpose programmable autonomous vision system. This system employs an architecture in which image processing is carried out by two hierarchical stages. In a first stage, an array of 176×144 sensing-processing cells, called *Q-Eye*, realizes different kind of early vision tasks at the very focal plane very efficiently. The accuracy of these operations is moderate (6-7 bits), but enough for the subsequent 32-bit RISC digital processor, which constitutes the second processing stage. This processor performs higher abstraction tasks by making use of pre-processed images coming from the sensor-processor. The wireless communication is managed by a com-

mercial WSN node interconnected with the *EyeRIS*[TM] system. As a whole, this platform exhibits a computational power of 250GOPS with a power consumption of 4mW/GOPS. This figure improves the 5.6mW/GOPS of *Xetal-II*. However, its total power consumption, 1.5W, is still too high to achieve long node lifetime in real deployments of WSNs.

III. *Wi-FLIP*: SYSTEM DESCRIPTION

The philosophy behind *Wi-FLIP* is to efficiently endow WSN nodes with vision by making the most of an ad-hoc transistor-level design of a smart image sensor. Unlike *Q-Eye*, the smart imager of the *EyeRIS*[TM] system, the objective is not to implement a very extensive catalog of focal-plane processing primitives. Instead, only a reduced subset is considered in order to make the circuitry more compact and simpler and thereby lowering the area and power consumption. The primitives comprising this subset must meet two conditions. First, an ultra low-power VLSI implementation must be feasible. And second, such implementation must admit a high degree of programmability in such a way that the scene representation can be simplified to a user-defined extent. The design of the *FLIP-Q* prototype is based on the grounds of these requirements. We can summarize its processing capabilities as follows:

- *Progressive spatial filtering and correlated subsampling*. This primitive enables image analysis on different spatial frequencies and permits scale space and Gaussian pyramid generation.
- *Fully-programmable multiresolution scene representation*. Different resolutions can be obtained by grouping pixels in rectangular-shape size-variant user-defined blocks. Foveated images are also possible.
- *Reduced kernel filtering*. Images can be pre-processed in order to simplify the subsequent application of convolution kernels meeting a certain structure, e.g. the Sobel operator.
- *Block-wise energy-based scene representation*. This primitive, combined with progressive spatial filtering, allows to efficiently segment spatially-repetitive patterns and high contrast zones at different scales within the scene.

In *Wi-FLIP*, this chip is integrated with *Imote2*, a platform gathering certain features that make it appropriate for such integration. First of all, it contains the 32-bit ARM5 Marvell PXA271 XScale® processor, whose frequency can vary from 13MHz up to 416MHz with dynamic voltage scaling. This means an enormous flexibility when it comes to adjust the power consumption of the system in function of the timing requirements of the artifical vision application considered. Additionally, the amount of memory available, 256kB SRAM, 32MB SDRAM and 32MB FLASH, suffices for image processing algorithms of low/medium complexity, suitable for WSN environments. Finally, thanks to its dense pinout, *Imote2* can carry out the control of *FLIP-Q* as well as retrieve the simplified scene representations it generates. Table I summarizes the main operating parameters of *Imote2* provided by the vendor. The figures related to power consumption have

Supply voltage	
USB voltage	5V
Battery voltage	3.2V - 4.5V
Power consumption	
Current draw in deep sleep mode	390μA
Current draw in active mode (clock speed: 13MHz, radio off)	31mA
Current draw in active mode (clock speed: 13MHz, radio on)	44mA
Current draw in active mode (clock speed: 104MHz, radio on)	66mA
Radio	
Frequency band (ISM)	2400MHz - 2483.5MHz
Data rate	250kbps
Tx power	-24dBm - 0dBm
Rx sensitivity	-94dBm

TABLE I
SUMMARY OF THE MAIN OPERATING PARAMETERS OF *Imote2*.

Fig. 1.   *Wi-FLIP*: a vision-enabled node for wireless applications.

been confirmed during the experimental tests of *Wi-FLIP*. They correspond to a basic configuration where the minimum possible number of PXA271's modules are active. These figures are given in terms of current consumption, what results very useful to rapidly estimate the lifetime of the batteries. Note that, for the configuration where the PXA271 processor works at minimum clock speed, i.e. 13MHz, the maximum current consumed by our prototype, 1.7mA, represents only the 5.2% of the whole system current consumption, 32.7mA.

The *FLIPQ*-to-*Imote2* interconnection has been carefully realized according to the number of PXA271's GPIOs available. Specifically, there are 34 GPIOs which can be accessed through a 40-pin connector. Only the strictly necessary logic to enable the processing primitives implemented by the prototype and retrieve the corresponding outcome is mapped into these GPIOs. Those signals included in the prototype for test purposes are dismissed. In order to carry out this GPIO-based interconnection and supply power and biasing to *FLIP-Q*, a 2-layer PCB has been designed and fabricated. Potentiometers are used to adjust the biasing signals in this first version of *Wi-FLIP*. Two snapshots of the resulting vision-enabled WSN node are shown in Fig. 1.

IV. *Wi-FLIP* PROGRAMMING

In order to realize any experimental test with the *Wi-FLIP* platform, we must write the corresponding program, compile it and download it into the PXA271 processor. As this processor runs *TinyOS*, the prescribed programming language is *nesC*. Thus, we have used the widely known *cygwin* environment to cross-compile *nesC* code and download the resulting native code into the processor via USB. All the applications developed follow the same previous steps before starting the execution of any algorithm:
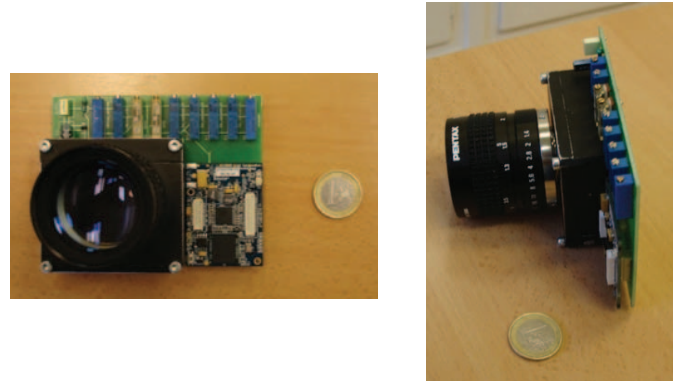
1) *Frequency change* (if necessary): The clock speed of the processor is adjusted according to the timing requirements. The default value is 13MHz. The rest of possibilities are 104MHz, 156MHz, 208MHz, 312MHz and 416MHz.
2) *Voltage level adjustment*: The high level of all the pins associated with signals controlling the operation of *FLIP-Q* must be set to 3.3V. This is a mandatory step as the default value is 2.7V.
3) *Configure pins*: The GPIO pins must be configured as input or output depending on the signal mapped into each one.
4) *Configure timers*: Two timers must be at least configured in order to implement the electronic global shutter for *FLIP-Q*.
5) *Configure and activate the required PXA271's modules*: These modules are a PWM for the *FLIP-Q*'s ADC clock, an internal clock if the energy-based scene representation is to be obtained and a UART and/or the radio if the results are going to be output (see below).

Keep in mind that the biasing signals must be also manually adjusted through the potentiometers before executing any code.

Regarding the outcome of *Wi-FLIP*, we have implemented two different ways of retrieving it. The first option is through the commercially available *Imote2 Interface Board*. This board, which can be stacked onto *Imote2* thanks to its compatible set of connectors, maps a USB port into 2 serial ports corresponding to 2 PXA271's UARTs. We can thus send out a stream of bytes comprising the result of the processing by using any of these UARTs. The second option, slower, is via radio. In this case, we make use of the MIB520 base station, also commercially available, that picks up the radio signal coming from *Wi-FLIP* and maps it into a USB connection. We have also used *cygwin* to cross-compile *nesC* code for the base station.

V. EXPERIMENTAL TESTS

The first tests programmed in *Wi-FLIP* consisted of capturing a frame, applying one of the different primitives implemented by *FLIP-Q* and outputting the resulting image. We

thus corroborated the correct operation of the system. An example of the multiresolution scene representation primitive is depicted in Fig. 2.
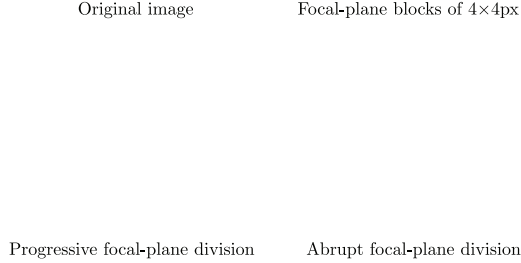
Original image   Focal-plane blocks of 4×4px

Progressive focal-plane division   Abrupt focal-plane division

Fig. 2.   Example of multiresolution representation in *Wi-FLIP*.

A. Exposure time control algorithm

Once the basic operation of *Wi-FLIP* was checked out, we addressed the programming of more elaborated tasks commonly needed for vision applications. As a first approach to such tasks, we have implemented an algorithm which adapts the exposure time, T_{exp}, to the characteristics of the scene at the moment. Operating in photocurrent integration mode, the voltage V_{ij} representing the value of each pixel depends on T_{exp}. Thus, for the same power of incident light over the sensor surface, a larger or smaller value of T_{exp} will result respectively in a larger or smaller excursion of V_{ij} from the reset voltage. If T_{exp} is not correctly set, we will obtain too dark or too bright images. A simple mechanism to adjust T_{exp} is to force that the mean value of the image:

$$\overline{V} = \frac{1}{MN} \sum_{i=1}^{M} \sum_{j=1}^{N} V_{ij} \qquad (1)$$

falls around the middle point of the nominal pixel voltage swing, V_{mid}. In this way, we make sure that most of the pixels are neither over-exposed nor under-exposed according to the current conditions of the scene. Let us define $\overline{T}_{exp}$ as the exposure time achieving this. The algorithm works with five prescribed parameters, namely: $T_{exp_{MIN}}$ and $T_{exp_{MAX}}$ defining the range of possible exposure times, i.e. $\overline{T}_{exp} \in [T_{exp_{MIN}}, T_{exp_{MAX}}]$, V_L and V_H defining the interval which must contain $\overline{V}$, that is $\overline{V} \in [V_L, V_H]$ with $V_{mid} = (V_L + V_H)/2$, and ΔT_{MAX}, which defines the maximum variation of T_{exp} during the search of $\overline{T}_{exp}$. The flowchart is depicted in Fig. 3. Flags F_{inc} and F_{dec} permit to determine when the coarse search increasing or decreasing T_{exp} by ΔT_{MAX} must stop. Then, a finer adjustment starts. During this stage, the variable k doubles after every step of

adjustment, thus speeding up greatly the process of search. But the key operation endowing the algorithm with great efficiency is the computation of $\overline{V}$. This computation is ready just after finishing the period of photointegration without energy cost thanks to the charge redistribution network available at the focal plane. In other words, no extra time and no extra energy are required to obtain $\overline{V}$ apart from the time and energy associated with the image capture.

Concerning the performance of *Wi-FLIP* when running the algorithm, the reachable frame rate will significantly depend on the light conditions of the scene as well as the clock speed of the PXA271 processor. The clock speed will also have a decisive influence on the power consumption of the system. Table II presents some results for different resolutions and clock frequencies. The frame rate is averaged along a sequence composed of 50 frames for each case. The parameters of the algorithm were set as follows: $[T_{exp_{MIN}}, T_{exp_{MAX}}] = [1ms, 1000ms]$, $[V_L, V_H] = [1.9V, 2.1V]$ and $\Delta T_{MAX} = 128ms$. Values of $\overline{T}_{exp}$ ranging from around 200ms to 400ms were obtained. The maximum frame rate reachable is therefore around 5fps. As a measure of the low computational cost associated with the algorithm, we also provide next some figures related to an image capture loop where exposure time adaptation is only realized at the beginning. All the images composing the sequence are therefore captured by applying the initially calculated exposure time. In such a case, the frame rates for full, half and quarter resolution with a clock speed of 13MHz are, respectively, 0.02, 0.09 and 0.29. If the clock speed is set to 416MHz, the frame rates are 0.26, 0.88 and 2.1 respectively. This means that the execution of the algorithm is not the cause of the low frame rates reached. Indeed, the bottleneck preventing *Wi-FLIP* from achieving higher frame rates is the control of the A/D conversion at *FLIP-Q* by *Imote2*. This control, that is not standard and must be therefore programmed step by step in *nesC*, is mostly supported by GPIOs featuring very slow switching. Furthermore, the software overhead introduced by *TinyOS* also plays an important role. As a consequence, a great deal of clock cycles are wasted during the conversion. For instance, the frame conversion for full, half and quarter resolution at maximum clock speed, i. e. 416MHz, takes respectively 3.9s, 1s and 0.3s. It is therefore mandatory for future versions of *FLIP-Q* either the incorporation of internal digital logic realizing efficiently the ADC control or the implementation of a standard interface that speeds up this task, like for example the Quick Capture Interface provided by the PXA271 processor.

B. Edge detection algorithm

Another operation typically needed for artificial vision applications is edge detection. This operation can be realized through Difference of Gaussians (DoG). In our case, the difference between a non-filtered image and a Gaussian-filtered version of that same image will be computed. We can afford this simplification because of the low noise associated to the frames captured by *FLIP-Q*, what enables the possibility of skipping the application of a first Gaussian filter
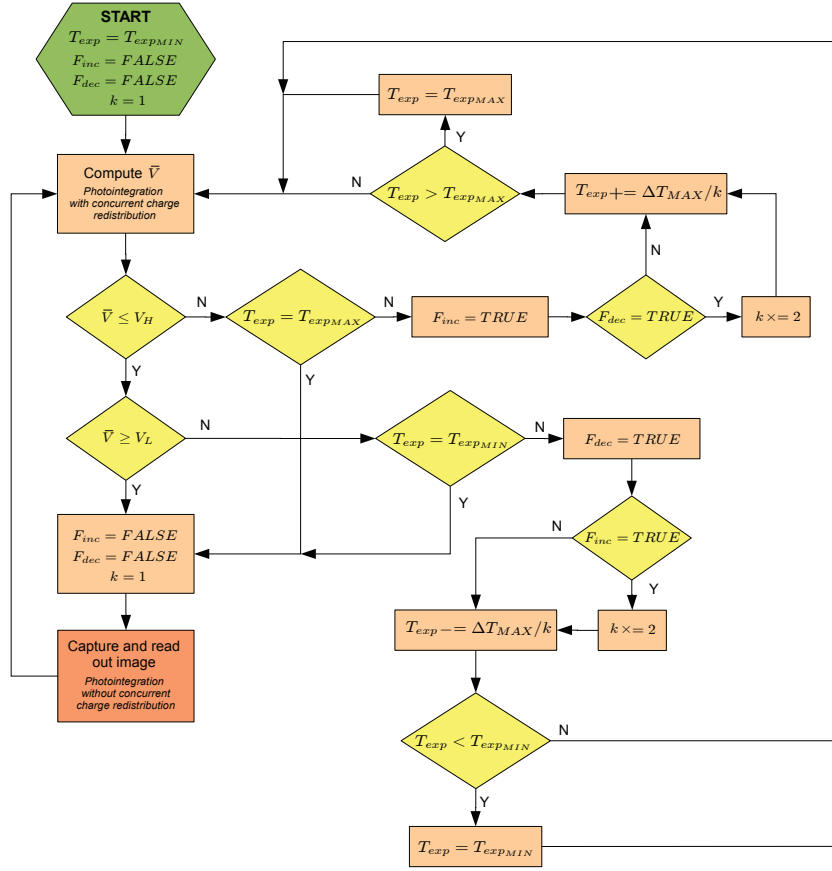
Fig. 3. Flowchart of the exposure control algorithm.

Resolution (px)	Clock frequency (MHz)	Frame rate	Power consumption (mA)
Full 176×144	13	0.02	38.4
	104	0.1	66.9
	208	0.18	105.5
	416	0.23	152.2
Half 88×72	13	0.08	38.1
	104	0.33	65.8
	208	0.62	105.6
	416	0.78	152.2
Quarter 44×36	13	0.28	38.2
	104	1	65.6
	208	1.55	105.2
	416	1.78	152.1

TABLE II
PERFORMANCE OF *Wi-FLIP* WHEN RUNNING THE EXPOSURE TIME CONTROL ALGORITHM.

non-filtered image and the filtered image is calculated by the PXA271 processor. Table III summarizes the results obtained for the same resolutions and clock frequencies considered for the exposure time control algorithm. The scene surveyed is also the same. Two full-resolution edge filtered images obtained as just described are depicted in Fig. 4.

Resolution (px)	Clock frequency (MHz)	Frame rate	Power consumption (mA)
Full 176×144	13	0.01	38.8
	104	0.05	67.8
	208	0.08	107.8
	416	0.1	155.6
Half 88×72	13	0.04	38.7
	104	0.15	67.1
	208	0.22	105.7
	416	0.25	153.3
Quarter 44×36	13	0.12	38.1
	104	0.41	67.5
	208	0.55	105.9
	416	0.59	153.1

TABLE III
PERFORMANCE OF *Wi-FLIP* WHEN RUNNING THE EDGE DETECTION ALGORITHM.

to eliminate high-frequency noise. The algorithm developed firstly performs an adaptation of the exposure time as above explained and then the original image is captured and stored. Subsequently, a focal-plane Gaussian filter is applied over this original image and the result is also stored. Finally, the absolute value of the pixel difference between the original
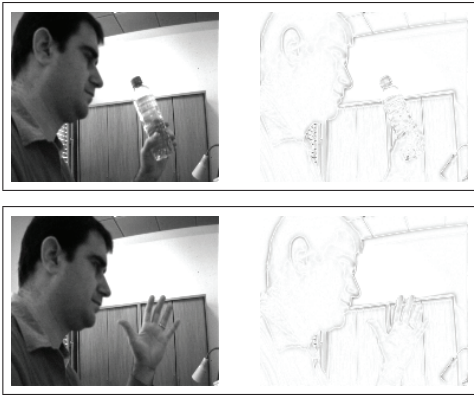
Fig. 4. Two frames after running the edge detection algorithm.

C. Smoke detection algorithm

Finally, we have implemented in *Wi-FLIP* a vision algorithm intended to detect smoke in early stages of a forest fire [14], [15]. This algorithm tries to segment candidate regions to contain smoke which are subsequently analyzed in terms of their propagation speed, clustering ratio and growth rate. It runs at 1fps and works with quarter-resolution images. Under these conditions, the PXA271 processor must be set to 416MHz, what is translated into a power consumption of around 155mA. When an alarm is triggered, full-resolution images are sent via radio every 15s. We present next results corresponding to tests carried out in a natural scenario by using commercial pyrotechnics as smoke generators. No false alarm was triggered during eight sequences of smoke generation. The detection was successful for five of these sequences. For the rest, smoke did not enter the field of view of *FLIP-Q* enough to be detected before the pyrotechnic material burnt out. For a real fire, smoke is steadily spreading and therefore it should be eventually detected. In Fig. 5, some frames captured by a commercial camcorder and the corresponding smoke segmentation realized by *Wi-FLIP* are shown. The last image corresponds to the first alarm image sent via radio.

Fig. 5. Smoke segmentation and alarm image from *Wi-FLIP*.

VI. Conclusions

To our best knowledge, *Wi-FLIP* is the first vision-enabled mote reported which integrates a prototype focal-plane image sensor-processor designed ad-hoc for the very strict power budgets inherent to WSNs. This sensor-processor, called *FLIP-Q*, can deliver different reduced representations of the scene obtained at ultra low energy cost by means of analog circuitry concurrent with photosensing. For the worst-case configuration, the power consumption of *FLIP-Q* represents only the 5.2% of the whole power consumption of *Wi-FLIP*. Currently, the main weakness of this mote is its low throughput. The future work will focus on improving this aspect as well as on addressing new applications in addition to the early detection of forest fires presented here.

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