LPC4088 Timer Interrupts

CM0506 Small Embedded Systems

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Seminar 5

Here the module begins to separate from EN0572. The programming structure will make extensive use of interrupts to handle events, along-side a *main-loop* handling polling and time consuming actions.

Note: *No Operating System*

GitHub

The repository on GitHub has several branches illustrating different aspects of timers.
To get the repository

```
$ git clone https://github.com/dr-alun-moon/timers
$ cd timers
```

Then checkout each example.

`single-timer`	A single timer flashing a single LED
`dual-timers`	Two timers at different rates for two LEDs
`duty-cycle`	LED with a short on and longer off
`multiple-timers`	Complex flashing pattern

Timers and Interrupts

Attention can be turned to the Timers and corresponding interrupts. These can be used to trigger periodic events in some fashion. The LPC4088 has four timers, each of which operate in the same way. See pages 7–11 for details of how the processor's internals work.

Timer Init

The code used for initialising a timer. Most of these have the required values, some are changed for different uses.

```
LPC_SC->PCONP |= (1UL << 1);
LPC_TIM0->TCR = 0;
LPC_TIM0->PR = 59999;
LPC_TIM0->CTCR = 0;
LPC_TIM0->MR0 = period_ms - 1;
LPC_TIM0->MCR = 0x03UL;
timer0UserDefinedHandler = handler;
LPC_TIM0->IR = 0x3F;
```

```
NVIC_EnableIRQ(TIMER0_IRQn);
LPC_TIM0->TCR |= (1UL << 0);
```

A line-by-line discussion of the values used follows. Table 539 on page 691 of the User manual [NXP, 2014] is a good summary of the register functions.

```
LPC_SC->PCONP |= (1UL << 1);
```

The PCONP register controls power to the peripheral devices. Bit 1 is the power supply for Timer-0 (see [NXP, 2014, Table 14, pg.30])

```
LPC_TIM0->TCR = 0;
```

The Timer control register [NXP, 2014, 24.6.2] switches the timer on and off. Disabling the timer while configuring it is important for correct behaviour to occur.

```
LPC_TIM0->PR = 59999;
```

The prescale register [NXP, 2014, 24.6.4] controls the rate at which the Timer ticks. The Timer counts one tick for each (PR+1) ticks of the peripheral clock (60 MHz). Setting the value to 59999 makes the timer count for every 60000 ticks of the Peripheral clock, or $60000 \times 60\,\text{MHz} = 1\,\text{ms}$.

```
LPC_TIM0->CTCR = 0;
```

The count-control-register [NXP, 2014, 24.6.11] selects whether the system is used as a clock (Peripheral Clock) or a counter. By setting it to 0 we are using the device as a counter.

```
LPC_TIM0->MR0 = period_ms - 1;
```

Match Register 0, is one of the 4 Match Registers for the timer [NXP, 2014, 24.6.7]. An interrupt occurs every (MR+1) ticks of the Timer. Since we have make the clock tick once every 1 ms, we just need the period in ms minus 1.

```
LPC_TIM0->MCR = 0x03UL;
```

The Match Control Register [NXP, 2014, 24.6.6] determines what actions occur, when the timer count (CR) equals one of the match registers (MRn). Setting bit 0 causes an interrupt to be generated, setting bit 1 causes a timer reset.

```
timer0UserDefinedHandler = handler;
```

This saves a user defined function for use in the ISR.

```
LPC_TIM0->IR = 0x3F;
```

The Interrupt Register [NXP, 2014, 24.6.1] indicates which interrupt has occurred. Writing 1s to this register resets the corresponding interrupt.

```
NVIC_EnableIRQ(TIMER0_IRQn);
```

Enables the timer-0 interrupts (see [NXP, 2014, Chapter 5].

```
LPC_TIM0->TCR |= (1UL << 0);
```

The Timer control register [NXP, 2014, 24.6.2] switches the timer on and off. Setting bit 0 enables the timer, *note* bit 1 is kept clear.

ISR

The Interrupt-Service-Routine is show below.

```
void TIMER0_IRQHandler(void) {
        timer0UserDefinedHandler();
        LPC_TIM0->IR |= (1UL << 0);
}
```

The first line calls the function stored from the Timer init function. The second line writes a 1 to bit 0 resetting the interrupt. If this bit is *not* reset, then no further interrupts can occur.

The Timing Diagram for timer interrupts is shown in table 1. It is shown for a hypothetical case with the prescale register set to 2 (PR=2) and the match register 1 (MR*n*=1).

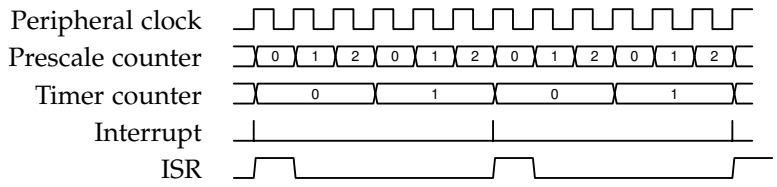

Table 1: Timing diagram

Simple Flashing

Example 1.2 just flashes one LED in a simple fashion.

```
$ git clone https://github.com/dr-alun-moon/timers
$ cd timers
$ git checkout single-timer
```

Exercise 1: Add a second LED

Add code to use a second timer (Timer-1) to flash a second LED at a different rate.
Take care copying the code for TIMER0, it is easy to miss an occurance of a 0 that needs changing to a 1.

Solution

A solution is in Git

```
$ git checkout dual-timers
```

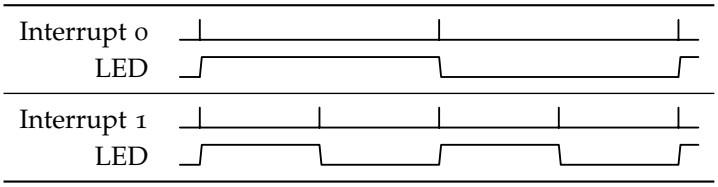

Table 2: Timing diagram for two LEDs

A possible timing diagram is shown in table 2, assuming the LED state is toggled in each ISR.

Question?

The code for TIMER0 and TIMER1 is very nearly identical (They should be the timer hardware on the silicon is identical.)
Is there an easy way to parameterise the function so that we could have something like.

```
init_timer(0, rate, period, handler);
```

Multiple Interrupts

EACH TIMER CAN HAVE UP TO 4 INTERRUPTS. Generated by each of the 4 match registers. One will have to be configured to reset the timer, which gives the timer period (time between interrupts). The other three will have values less than the timer period to cause interrupts at (up to) 3 points within the timer period. The Match Control Register [NXP, 2014, 24.6.6], has bits to enable the interrupts for each of the match registers.

These share the same interrupt routine. The interrupt handler will have to interrogate the Interript Register (IR) [NXP, 2014, 24.6.1] to determine which match register caused the interrupt.

Setting up MR1

TO SET UP AN INTERRUPT ON MR1. We need to write a value into it, and set the appropriate flag in the MCR. The value needs to be a fraction of the value in MR0, or else the interrupt will never occur. A fraction can be passed to `timer0Init` as a `float`, and then used to multiply MR0. Bit 3 in the match control register needs to be set to enable the interrupt. Finally the interrupt handler needs to test the interrupt register (IR) to see which match register caused the interrupt.

A 20% duty cycle means that the LED is on for the first 20% of the flashing period.

Exercise 2: LED1 on a 20% duty cycle

The code in branch ex.1.3 has been modified to set up timer-0 to flash one LED on a 20% duty cycle.

```
$ git clone https://github.com/dr-alun-moon/timers
$ cd timers
$ git checkout duty-cycle
```

Examine `main.c`, `timer.c`, and `timer.h` to check how the changes have been made.

1. Add similar changes to enable a second match register on Timer-1
2. Flash another LED with an 80% duty cycle

Question 1

Are there any behaviours that would need:

- 3 interrupts per Timer?
- 4 interrupts per Timer?

Question 2

How could you stop timer-0 after 4 flashes?
hint take a look at the `multiple-timers` branch.

References

Cortex-M4 Devices, Generic User Guide. ARM, 2010.

LPC4088 Experiment Base Board rev A. Embedded Artists, September 2014a.

LPC4088 Quickstart Board rev B. Embedded Artists, August 2014b.

UM10562 LPC408x/407x User manual. NXP, rev. 3 edition, March 2014.

Timer Behavior

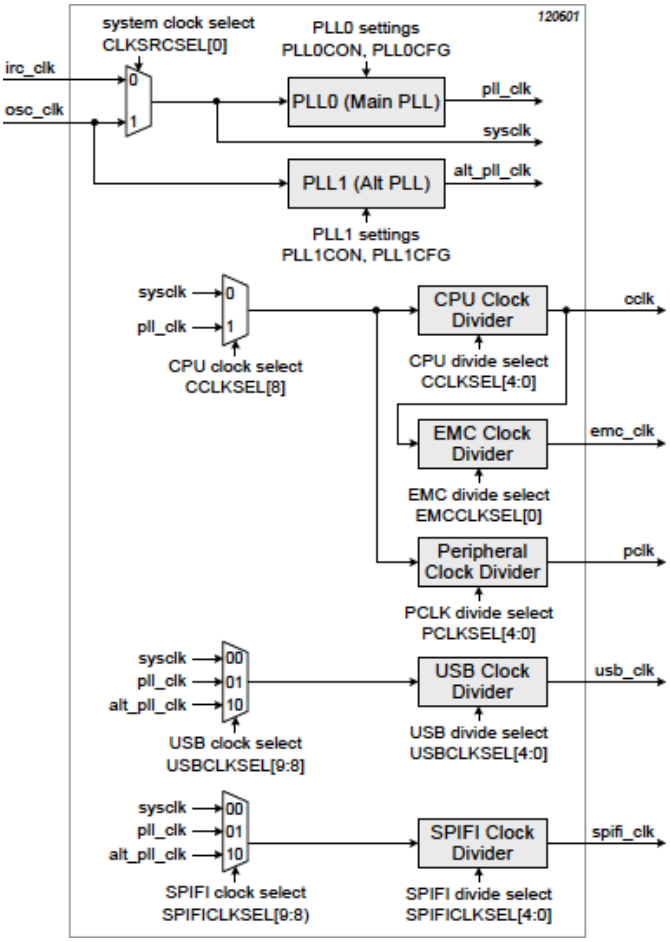

Figure 1: Clock generation

Figure 1 from [NXP, 2014, pg. 21] shows the various clock generation circuits. fFigure 2 [Emb, 2014b, sheet 2] shows the external crystal used as the external oscillator.

The PLL (Phase Locked Loop) is used to boost the input clock signal to higher frequencies.

The Register `PLL0CFG` controls the behaviour of the PLL [NXP, 2014, sec 3.10.4]. In the startup files `system_LPC407x_8x177x_8x.c` and `system_LPC407x_8x177x_8x.h` the values for the PLL and timers are defined. (see [NXP, 2014, table 47] for mapping register values to M and P)

```
#define PLL0CFG_Val           0x00000009
```

Quantity		Source	Value	
M	PLL multiplier	`PLL0CFG` bits 4:0	10	
P	PLL divider	`PLL0CFG` bits 6:5	1	
f_{in}	input frequency	external crystal	12	MHz

Table 3: Values for PLL

The output frequency of the PLL is given by

$$f_{\text{out}} = M f_{\text{in}} \tag{1}$$

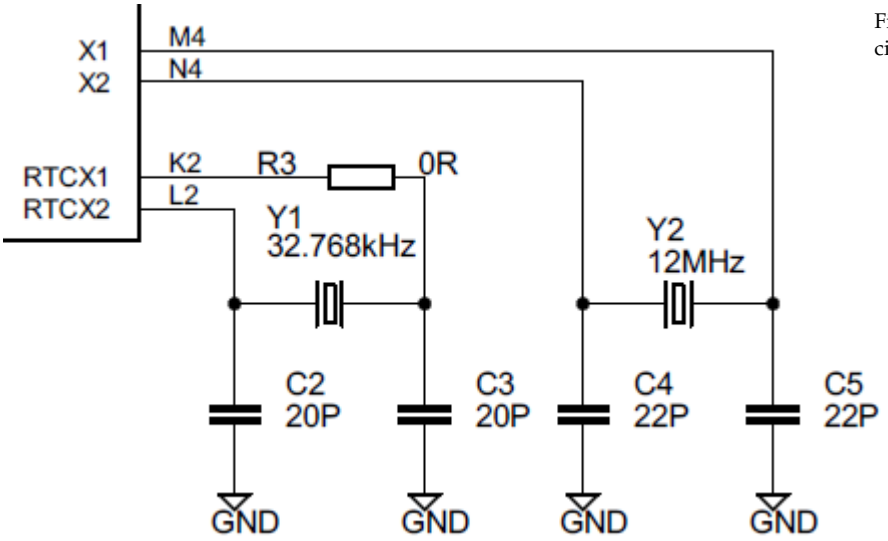

Figure 2: Quickstart board Crystal circuit

The current controlled oscillator (internal to the PLL) has a frequency of

$$f_{CCO} = 2MPf_{in} \tag{2}$$

Putting the values into these we get

crystal	12	MHz
f_{in}	12	MHz
f_{out}	120	MHz
f_{CCO}	240	MHz

Table 4: Clock and oscilator values

CPU Clock

The output from the PLL is selected as the CPU clock frequency by the `CCLKSEL` register, which also defines the divider value in bits 4:0 [NXP, 2014, Table 20, sec3.3.3.2].

```
#define CCLKSEL_Val             0x00000101
```

The CPU clock divider is 1, so the PLL ouput is used directly as the clock signal This 120 MHz frequency is made available from `system_LPC407x_8x_177x_8x.c` line 368 as `SystemCoreClock`.

Peripheral Clock

The Peripheral Clock signal drives most of the on chip peripherals. The register `PCLKSEL` [NXP, 2014, sectin 3.3.3.5, table 23] controls the divider value to use

```
#define PCLKSEL_Val             0x00000002
```

This gives the divider value as 2. The peripheral clock is therefore 60 MHz. This frequency is made available from `system_LPC407x_8x_177x_8x.c` line 369 as `PeripheralClock`.

SysTick

The SysTick timer is driven by the 120 MHz CPU clock signal. The timers uses a 24bit count down timer, the reset value is loaded from `STRELOAD`. Given 24 bits can hold a maximum value of $2^{24} - 1$ or

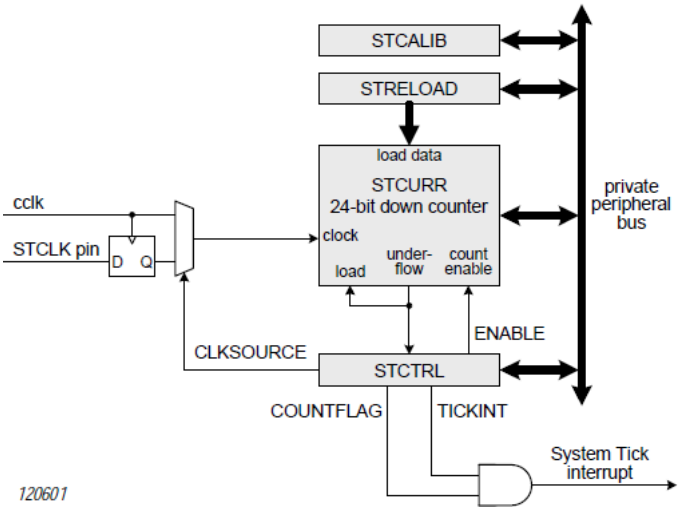

Figure 3: SysTick timer circuit

16 777 215 we get a maximum SysTick period of 2^{24} CPU ticks of 0.139 810 s

$$\frac{16777216}{120000000} = 0.139810$$

Conversely the minimum period is 8 ns! The Cortex M4 User Guide [ARM, 2010] has a good description of the SysTick timer operation.

Timer 0/1/2/3

The timers are covered in [NXP, 2014, Chapter 24]. Figure 4 shows the timer circuit. The peripheral clock signal drives the timer through the prescale counter.

Operation – prescale and count

Timer Counter (TC), Prescale Register (PR) and prescale counter (PC). The 32 bit TC is incremented every PR+1 cycles of PCLK. Prescale Register. When the Prescale Counter (PC) is equal to this value, the next clock increments the TC and clears the PC. Prescale Counter. The 32 bit PC is a counter which is incremented to the value stored in PR. When the value in PR is reached, the TC is incremented and the PC is cleared.

The prescale register therefore is used to scale the CPU clock down to give the timer clock tick.

The timer register, counts up on each tick from the prescaler. When it reaches the value in one of the match registers, the timer reacts acording to the values in the match control register.

So the relevent relations are shown in table 5. A simple scheme is to set the prescaler to 59999 (divide by 60000). This makes the

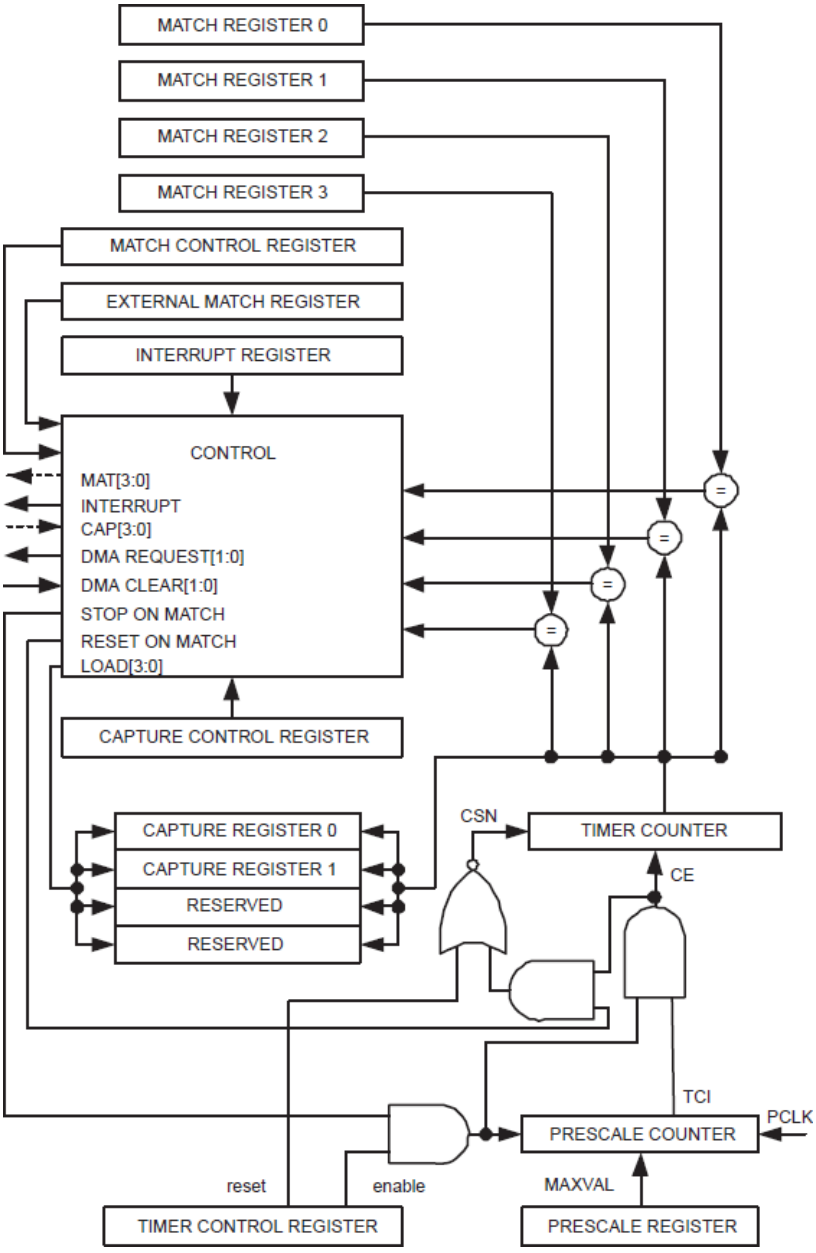

Figure 4: Timer circuit

Timer clock tick at a 1 ms rate. The value written into the match register is just the period in ms minus 1.

Alternatively the prescale value can be just 59, which makes the timer tick every 1 µs

Peripheral Clock rate	f_P	60 MHz
Prescale Register	PR	
Timer tick rate	$f_T = \frac{f_P}{\text{PR}+1}$	
Match Register	MR	
Interupt tick rate	$\frac{f_T}{\text{MR}+1}$	

Table 5: Timer relationships

The highest rate the timer can run at is one interrupt every tick of the Peripheral Clock 60 MHz or once every 16.7 ns. With the prescaler to 0 (divide by 1), the timer interrupt can occur at a maximum of every 2^{32} ticks, or 71.6 s

$$\frac{2^{32}}{60 \times 10^6} = 71.6$$

With the prescaler and the match register set to their maximum values, an interrupt occurs every 307 445 734 561 s or 9749 years!