# MCM6830017 MIKBUG/ MINIBUG ROM

## 1.0 SYSTEMS OVERVIEW

The MIKBUG/MINIBUG ROM provides the user with three separate firmware ppoggrams to interface with asserial asynchronous ((startssopp)) data a communications where it is the user with a serial asynchronous.

- 1) MIKBUG Rew. 99
- 2) MINIBUG Rew. 44
- 3) Test Pattern

The map of the programs is shown in Figure 11-11.

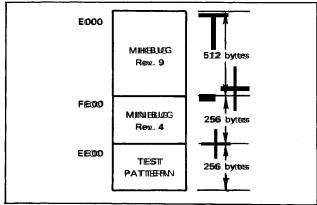


FIGURE 1-1. MIKBUG/MINBBUG ROM Memory Map

## NOTE

All enables for the ROM are active high.

## 2.0 FEATURES

The more important factures of these programs are:

## MIKBUG Rev. 9

- A. Memory Loadler
- B. Print Registers of Target Program
- C. Primt/Punch Dump
- D. Memory Change
- E. Go to Target Programm
- F. Operatesswith PIA for the Panallel to Serial II neef face
- G. Restart/NMI/SWI Internunt Weetoors

### MINIBUG Rev. 4

- A. Memory Loader
- B. Memory Change
- C. Print Registers of Target Program
- D. Go to Target Program
- E. Assumes a UARTI for the Panallel to-Senial Interface

#### 3.0 HARDWARE CONFIGURATION

### 3.1 MIKBUG Hardware

The MIKBUG/MINIBUG ROM is intended from sewith the MC6800 Microprocessing Unitiman M6800 Microprocessing unitimated in Higgure 3-1. As shown, all of the enable inputs a chighlevels and the address line A000 mppin 15 is grounded. The MIKBUG Firmware in this ROM uses addresses E000 through E1FF. The ROM should be connected into a system so that its two top MIKBUG Himmware addresses also will respond to addresses FFFE and FFFE. This is required for the system to restart properly. The reshould not be any devices in the system attalhigheraddress than this ROM achidesesses. Figure 3-2 depicts a memory map for a system suspicion MIKBUG Firmware and Higure 3-33 depicts this system is block diagram.

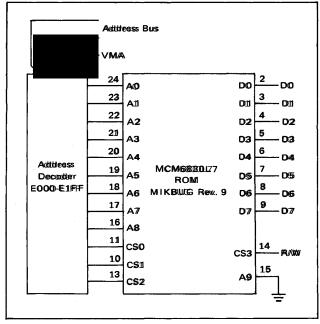


FIGURE 3-1. MCM6830L77 MIKEBUG ROM Schematic

The MIKBUG Firmwame operatess with an MIG6820 Peripheral Interface Adappete (PAA) as shown im Figure 334. The MC14536 device is used as the interface thine. This timer's interval is set by adjusting the 500 kolumnessistor and monitoring the output signal on pim 13 of the MC14536 device. The zero level of the timing pulses should be 9.1 ms

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