Am9112

256 x 4 Static RAM

DISTINCTIVE CHARACTERISTICS

- Low operating power dissipation
  125 mW typ.; 290 mW maximum — standard power
  100 mW typ.; 175 mW maximum — low power
- High noise immunity — full 400 mV
- Uniform switching characteristics — access times insensitive to supply variations, address patterns and data patterns
- Bus-oriented I/O data
- Zero address, setup and hold times guaranteed for simpler timing
- Direct plug-in replacement for 2112 type devices

GENERAL DESCRIPTION

The Am9112/Am91L12 series of products are high-performance, low-power, 1024-bit, static read/write random-access memories. They offer a range of speeds and power dissipations including versions as fast as 200 ns and as low as 100 mW typical.

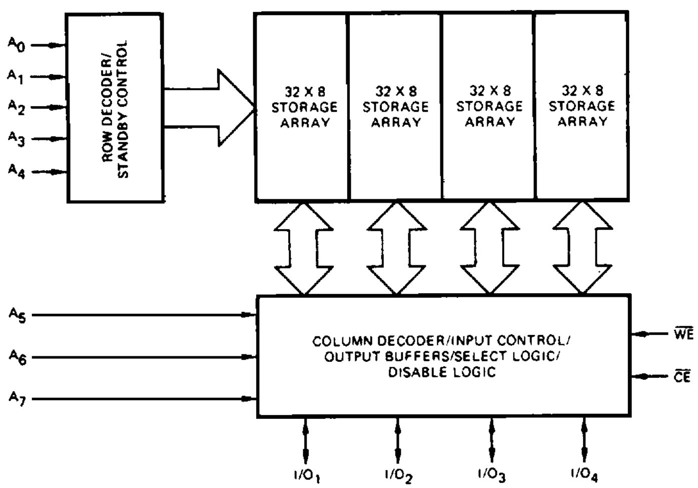
Each memory is implemented as 256 words by 4 bits per word. This organization allows efficient design of small memory systems and permits finer resolution of incremental memory word size relative to 1024 by 1 devices. The output and input data signals are internally bussed together and share 4 common I/O pins. This feature keeps the package size small and provides a simplified interface to bus-oriented systems.

The Am9112/Am91L12 memories may be operated in a DC standby mode for reductions of as much as 84% of the normal operating power dissipation. Though the memory cannot be operated, data can be retained in the storage cells with a power supply as low as 1.5 volts. The Am91L12 versions offer reduced power during normal operating conditions as well as even lower dissipation in standby mode.

The eight Address inputs are decoded to select 1 of 256 locations within the memory. The Chip Enable input acts as a high-order address in multiple chip systems. It also controls the write amplifier and the output buffers in conjunction with the Write Enable input. When $\overline{CE}$ is LOW and $\overline{WE}$ is HIGH, the write amplifiers are disabled, the output buffers are enabled, and the memory will execute a read cycle. When $\overline{CE}$ is LOW and $\overline{WE}$ is LOW, the write amplifiers are enabled, the output buffers are disabled, and the memory will execute a write cycle. When $\overline{CE}$ is HIGH, both the write amplifiers and the output buffers are disabled.

These memories are fully static and require no refresh operations or sense amplifiers or clocks. All input and output voltage levels are identical to standard TTL specifications, including the power supply.

BLOCK DIAGRAM



BD000250

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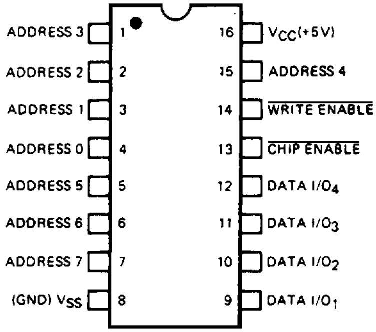
CONNECTION DIAGRAM
Top View



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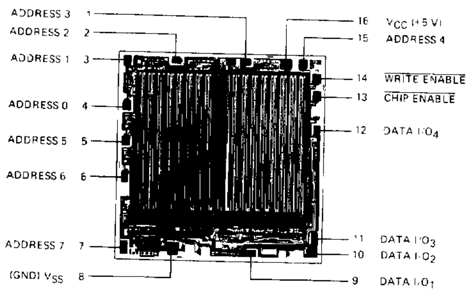
Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT



Die Size 0.132" x 0.131"

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ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

AM9112 A P C _

E. OPTIONAL PROCESSING
Blank = Standard processing

D. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

C. PACKAGE TYPE
P = 16-Pin Plastic DIP (PD 016)
D = 16-Pin Ceramic DIP (CD 016)

B. SPEED OPTION
A = 500 ns
B = 400 ns
C = 300 ns
D = 250 ns

A. DEVICE NUMBER/DESCRIPTION
Am9112
256 x 4 Static RAM
Am91L12 = Low-Power Version

Valid Combinations	
AM9112A	PC, DC
AM9112B	
AM9112C	
AM9112D	
AM91L12A	
AM91L12B	
AM91L12C	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**

B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish

AM9112 A /B V A

E. LEAD FINISH
A = Hot Solder DIP

D. PACKAGE TYPE
V = 16-Pin Ceramic DIP (CD 016)

C. DEVICE CLASS
/B = Class B

B. SPEED OPTION
A = 500 ns
B = 400 ns
C = 300 ns

A. DEVICE NUMBER/DESCRIPTION
Am9112
256 x 4 Static RAM
Am91L12 = Low-Power Version

Valid Combinations	
AM9112A	/BVA
AM9112B	
AM9112C	
AM91L12A	
AM91L12B	
AM91L12C	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Temperature Range**
B. Package Type
C. Device Number
D. Speed Option

___ P 2112 A-2

D. SPEED OPTION
Blank = 1000 ns
A-4 = 400 ns
A = 300 ns
A-2 = 250 ns

C. DEVICE NUMBER/DESCRIPTION
2112
256 x 4 Static RAM

B. PACKAGE TYPE
P = 16-Pin Plastic DIP (PD 016)
C = 16-Pin Ceramic DIP (CD 016)

A. TEMPERATURE RANGE
Blank = Commercial (0 to +70°C)

Valid Combinations		
P, C	2112	A-4, A, A-2

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$A_0 - A_7$ Addresses (Input)
The 8-bit field presented at the address inputs selects one of the 256 memory locations to be read from — or written into — via the Data Input/Output lines.

$I/O_1 - I/O_4$ Data Input/Output Lines (Input/Output)
If $\overline{WE}$ is LOW, the data represented on the Data I/O lines can be written into the selected memory location. If $\overline{WE}$ is HIGH, the Data I/O lines represent the data read from the selected memory location.

$\overline{CE}$ Chip Enable (Input, Active LOW)
Read and Write cycles can be executed only when $\overline{CE}$ is LOW.

$\overline{WE}$ Write Enable (Input, Active LOW)
Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

FUNCTIONAL DESCRIPTION

Applications

These memory products provide all of the advantages of AMD's other static N-channel memory circuits: +5 only power supply, all TTL interface, no clocks, no sensing, no refreshing, military temperature range available, low-power versions available, high speed, high output drive, etc. In addition, the Am9112 series features a 256 x 4 organization with common pins used for both Data In and Data Out signals.

This bussed I/O approach keeps the package pin count low, allowing the design of higher density memory systems. It also provides a direct interface to bus-oriented systems, eliminating bussing logic that could otherwise be required. Most microprocessor systems, for example, transfer information on a bidirectional data bus. The Am9112 memories can connect directly to such a processor since the common I/O pins act as a bidirectional data bus.

If the chip is enabled ($\overline{CE}$ LOW) and the memory is in the Read state ($\overline{WE}$ HIGH), the output buffers will be turned on and will be driving data on the I/O bus lines. If the external system tries to drive the bus with data, there may be contention for control of the data lines and large current surges can result. Since the condition can occur at the beginning of a write cycle, it is important that incoming data to be written not be entered until the output buffers have been turned off.

These operational suggestions for write cycles may be of some help for memory system designs:

1. For systems where $\overline{CE}$ is always LOW or is derived directly from addresses and so is LOW for the whole cycle, make sure t_{WP} is at least t_{DW} + t_{DF} and delay the input data until t_{DF} following the falling edge of $\overline{WE}$. With zero address set-up and hold times, it will often be convenient to make $\overline{WE}$ a cycle-width level ($t_{WP} = t_{WC}$) so that the only subcycle timing required is the delay of the input data.
2. For systems where $\overline{CE}$ is HIGH for at least t_{DF} preceeding the falling edge of $\overline{WE}$, t_{WP} may assume the minimum specified value. When $\overline{CE}$ is HIGH for t_{DF} before the start of the cycle, then no other subcycle timing is required and $\overline{WE}$ and data-in may be cycle-width levels.
3. Notice that because both $\overline{CE}$ and $\overline{WE}$ must be LOW to cause a write to take place, either signal can be used to determine the effective write pulse. Thus, $\overline{WE}$ could be a level with $\overline{CE}$ becoming the write timing signal. In such a case, the data set-up and hold times are specified with respect to the rising edge of $\overline{CE}$. The value of the data set-up time remains the same and the value of the data hold time should change to a minimum of 25 ns.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature .... −65 to +150°C
Ambient Temperature with
Power Applied .... −55 to +125°C
Supply Voltage .... −0.5 V to +7.0 V
DC Voltage Applied to Outputs .... −0.5 V to +7.0 V
DC Layout Voltage .... −0.5 V to +7.0 V
Power Description .... 1.0 W
DC Output Current .... 20 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Temperature .... 0 to +70°C
Supply Voltage .... +4.75 V to +5.25 V

Military (M) Devices*
Temperature .... −55 to +125°C
Supply Voltage .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at $T_C = +25°C$, $+125°C$, and $-55°C$.

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			C Devices Min.	C Devices Max.	M Devices Min.	M Devices Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $I_{OH} = -200\ \mu A$			2.4		2.2		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 3.2 mA				0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage				−0.5	0.8	−0.5	0.8	V
I_{LI}	Input Load Current	V_{CC} = Max., $0\ V \leq V_{IN} \leq V_{CC}$				10		10	μA
I_{IO}	I/O Leakage Current	$V = CE = V_{IH}$	$V_O = V_{CC}$			5		10	μA
			V_O = 0.4 V			−10		−10	
I_{CC}	Power Supply Current	Data Out Open V_{CC} = Max. $V_{IN} = V_{CC}$	T_A = 25°C	9112A/B		50		50	mA
				9112C/D/E		55		55	
				91L12A/B		31		31	
				91L12C/D/E		34		34	
			T_A = 0°C (Note 3)	9112A/B		55			
				9112C/D/E		60			
				91L12A/B		33			
				91L12C/D/E		36			
			T_A = −55°C	9112A/B				60	
				9112C/D/E				65	
				91L12A/B				37	
				91L12C/D/E				40	
C_{IN}	Input Capacitance	V_{IN} = 0 V, T_A = 25°C, f = 1 MHz (Note 3)				9		9	pF
C_O	Output Capacitance	V_O = 0 V, T_A = 25°C, f = 1 MHz (Note 3)				12		11	

Notes: See notes following Switching Characteristics table.

STANDBY OPERATING CONDITIONS over temperature range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ.	Max.	Units
V_{PD}	V_{CC} in Standby Mode				1.5			
I_{PD}	I_{CC} in Standby Mode	T_A = 0°C All Inputs = V_{PD}	V_{PD} = 1.5 V	Am91L12		11	25	mA
				Am9112		13	31	
			V_{PD} = 2.0 V	Am91L12		13	31	
				Am9112		17	41	
		T_A = −55°C All Inputs = V_{PD}	V_{PD} = 1.5 V	Am91L12		11	28	mA
				Am9112		13	34	
			V_{PD} = 2.0 V	Am91L12		13	34	
				Am9112		17	46	
dv/dt	Rate of Change of V_{CC}						1.0	V/μs
t_R	Standby Recovery Time				t_{RC}			ns
t_{CP}	Chip Deselect Time				0			ns
V_{CES}	$\overline{CE}$ Bias in Standby				V_{PD}			Volts

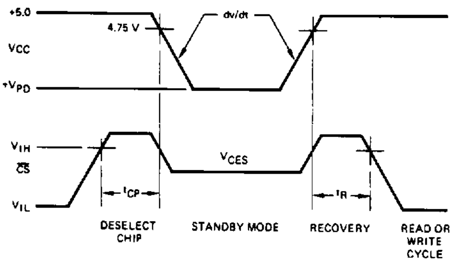
*See the last page of this spec for Group A Subgroup Testing information.

Power-Down Standby Operation

The Am9112/Am91L12 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering V_{CC} to around 1.5 – 2.0 volts (see table and graph). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

To ensure that the output of the device is in a high-impedance OFF state during standby, the chip select should be held at V_{IH} or V_{CES} during the entire standby cycle.

TYPICAL DC and AC CHARACTERISTICS



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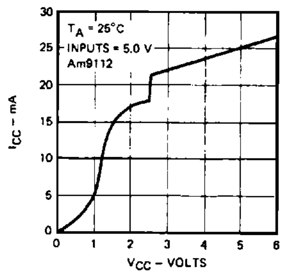
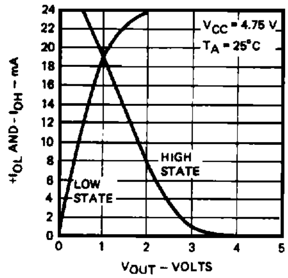
Typical Power Supply Current Versus Voltage



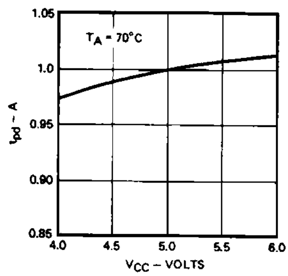
OP000460

Typical Output Current Versus Voltage



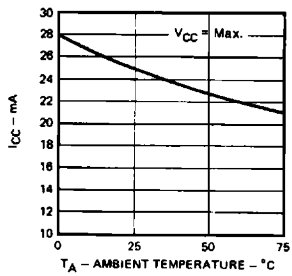
OP001060

Access Time Versus V_{CC} Normalized to V_{CC} = +5.0 Volts



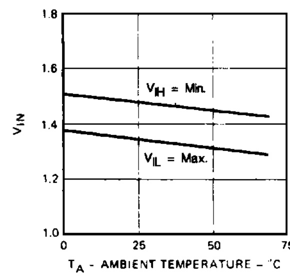
OP000100

Typical Power Supply Current Versus Ambient Temperature



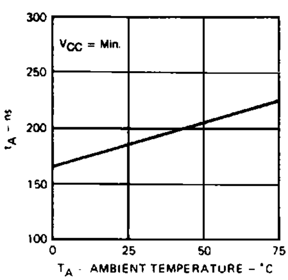
OP001070

Typical V_{IN} Limits Versus Ambient Temperature



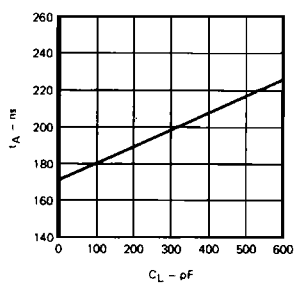
OP001030

Typical t_A Versus Ambient Temperature



OP001040

Typical t_A Versus C_L



OP001050

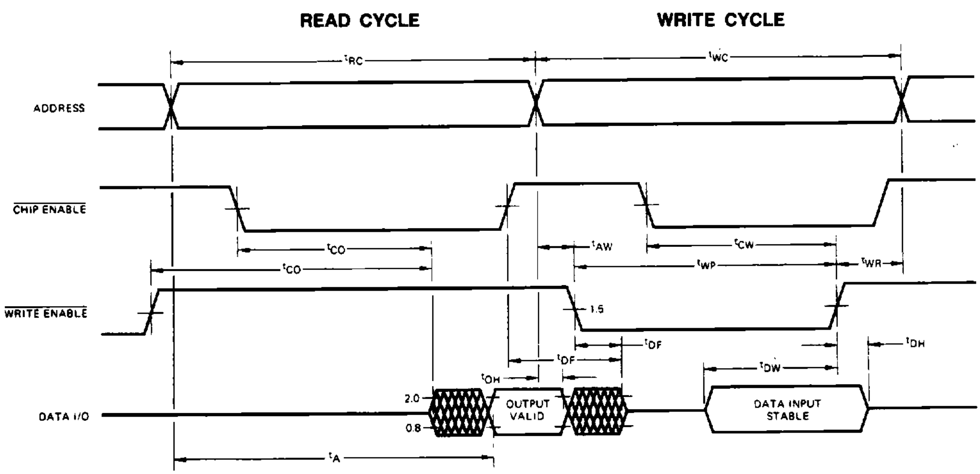
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 4)*

No.	Parameter Symbol	Parameter Description	Am9112A Am91L12A Min.	Am9112A Am91L12A Max.	Am9112B Am91L12B Min.	Am9112B Am91L12B Max.	Am9112C Am91L12C Min.	Am9112C Am91L12C Max.	Am9112D Min.	Am9112D Max.	Units
1	t_{RC}	Read Cycle Time	500		400		300		250		ns
2	t_A	Access Time		500		400		300		250	ns
3	t_{CO}	Output Enabled to Output ON Delay (Note 5)	5.0	175	5.0	150	5.0	125	5.0	100	ns
4	t_{OH}	Previous Read Data Valid with Respect to Address Change	40		40		40		30		ns
5	t_{DF}	Output Disabled to Output OFF Delay (Note 6)	5.0	125	5.0	100	5.0	100	5 0	75	ns
6	t_{WC}	Write Cycle Time	500		400		300		250		ns
7	t_{AW}	Address Setup Time	20		20		20		20		ns
8	t_{WR}	Address Hold Time	0		0		0		0		ns
9	t_{WP}	Write Pulse Width (Note 7)	225		200		175		150		ns
10	t_{CW}	Chip Enable Setup Time	175		150		125		100		ns
11	t_{DW}	Input Data Setup Time	150		125		100		85		ns
12	t_{DH}	Input Data Hold Time (Note 8)	15		15		15		15		ns

Notes:
1. Absolute maximum ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, ambient temperature is defined as the stabilized case temperature.
3. Guaranteed by characterization data. Data will be updated upon any process or design change which affects this parameter.
4. Test conditions assume signal transition times of 10 ns or less. Output load equals 1 TTL gate +100 pF. Input signal timing reference level = 1.5 V, with input pulse levels of 0 to 3.0 V. Data output timing reference levels = 0.8 and 2.0 V.
5. Output is enabled and t_{CO} commences only with both $\overline{CE}$ LOW and $\overline{WE}$ HIGH.
6. Output is disabled and t_{DF} defined from either the rising edge of $\overline{CE}$ or the falling edge of $\overline{WE}$.
7. Minimum t_{WP} is valid when $\overline{CE}$ has been HIGH at least t_{DF} before $\overline{WE}$ goes LOW. Otherwise $t_{WP(Min)} = t_{DW(Min.)} + t_{DF(Min.)}$.
8. When $\overline{WE}$ goes HIGH at the end of the write cycle, it will be possible to turn on the output buffers if $\overline{CE}$ is still LOW. The data out will be the same as the data just written and so will not conflict with input data that may still be on the I/O bus.
9. See Functional Description section of this specification.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS (Note 9)



WF000610

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{LI}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC}	1, 2, 3
V_{PD}	1, 2, 3
I_{PD}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	t_{RC}	7, 8, 9, 10, 11
2	t_A	7, 8, 9, 10, 11
3	t_{CO}	7, 8, 9, 10, 11
4	t_{OH}	7, 8, 9, 10, 11
5	t_{DF}	7, 8, 9, 10, 11
6	t_{WC}	7, 8, 9, 10, 11
7	t_{AW}	7, 8, 9, 10, 11
8	t_{WR}	7, 8, 9, 10, 11
9	t_{WP}	7, 8, 9, 10, 11
10	t_{CW}	7, 8, 9, 10, 11
11	t_{DW}	7, 8, 9, 10, 11
12	t_{DH}	7, 8, 9, 10, 11

4

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.