Design and Test of Novel Computing System for Low Earth Orbit

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Overview

Advances in computing over the last 60 years [1] have led to the widespread use of systems such as neural networks and other machine learning architectures to solve a variety of problems. As algorithms grow in complexity, addressing issues such as feature reconstruction [2], autonomous driving, and various other areas, the hardware requirements grow, with algorithms using more power for more intensive computations. This is inherently a problem for space based systems due to power constraints, and the harsh environment in low earth orbit with respect to ionizing radiation and temperature swing.

Work in this poster shows the design and test of a system to be deployed as a technology demonstration on board the UGA Multi-view Onboard Computational Imager (MOCI) satellite [3]. The system, called the Core GPU Interface (CORGI), serves to integrate a Nvidia TX2i Graphics Processing Unit (GPU), with the satellite imaging payload in order to perform feature reconstruction in orbit. A successful demonstration of this technology would offer a low cost reusable high performance computing platform for any LEO system, which is useful due the low system life expectancy caused by the harsh environment described above.

Circuit Design

The system as deployed in the MOCI satellite serves to integrate the imaging payload with the on board computer via the Universal Asynchronous Receive/Transmit (UART) interface. After carrying out the feature reconstruction operation the data is sent to the OBC to be sent to the ground.

The board interfaces with the camera system via two USB 3.0 connections capable of at most 5 gigabit/sec speeds, allowing for quick and efficient file transfer. The board also carries a JTAG interface for debug, an SD slot for applications requiring mass storage, or possibly an external file system. We also provide the user with a DisplayPort connection for development work, alongside with a redundant USB 2.0 micro-b connector allowing for easy flashing, debug, or file transfer while the camera system is integrated with the board. An image of the routed printed circuit board can be seen below in Figure 1.

It should be noted that USB as well as DisplayPort are high speed differential pair signals, meaning they use two traces to send data. This is done for noise immunity [4]. The requirements impedance control are strictly adhered to in this design with USB requiring 45 Ω single ended and 90 Ω differential impedance, and DisplayPort requiring 50 Ω and 100 Ω single ended and differential impedance respectively. Trace impedance is assumed lossless (i.e no V=IR drop) and is therefore entirely dependent on the trace capacitance (ground plane and atmospheric coupling) as well as the trace inductance. The impedance (voltage to current ratio) can be computed via finite element field solvers, or by approximations. We elect to use the approximation given by Wheeler's equation for a micro-strip transmission line over a constant dielectric [5].

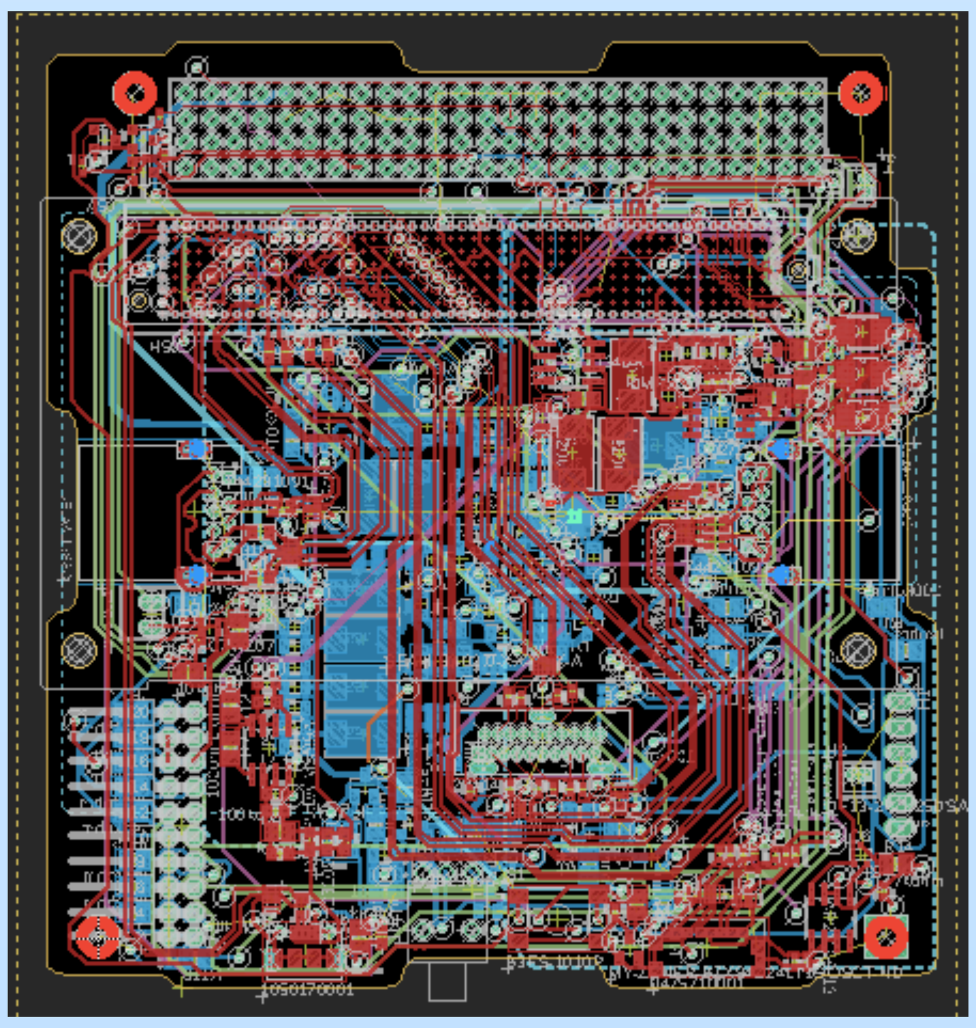

Figure 1: Routed PCB.

Test and Characterization

The PCB (Figure 2) was manufactured and assembled by Advanced Assembly, and was tested in house. Early problems with this revision were encountered. Initially the 12 volt power rail to the GPU was just energized, caused by a faulty P type switch having its Gate/Drain terminals shorted. Rework proved to be impossible, so the part was removed. Upon the GPU receiving a steady 12 volts the was no observable consistent power draw. This was caused by a faulty power switch, which was removed.

We then observe "dirty power", an oscillating 12 volt signal at the power supply. Powering the board via a wall adapter solved this issue. We then observe a constant 100mA draw upon the 12 volt rail, measured by an integrated current sensor on a daughter board, which can be seen in Figure 2. This implies some circuitry in the TX2i has been powered on. Forcing the device into reset by grounding the reset pin causes a current spike of a 600mA consistently, as well as significant heat dissipation from the TX2i. This implies the TX2i is being held in reset by the CORGI, and this can be solved by allowing the user access to all reset signals, instead of obscuring them in the board. A final revision with these fixes implemented is due to arrive and be tested by late April 2021.

Figure 2: Assembled PCB with Integrated Daughter Board

Conclusion

The work presented here shows a design close to completion that will fly on the MOCI satellite in Q2 2022. Future work when design is completed shall include benchmarking algorithmic performance and data transfer rates, applying thermal stress to simulate in orbit conditions, and then benchmarking algorithmic performance and data rates under thermal load.

References

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