

## Overview

The Space Environment Research and Validation of Accelerated LAN (SERVAL) processing focuses on the use of a fully integrated System On Chip (SoC), Field Programmable Gate Array (FPGA), and Graphics Processing Unit (GPU) board. It will act as the flight computer and on satellite processing unit for future satellites by implementing cutting edge interface technology like Local Area Network communication and PCIe to create an accelerated graphics processing stack utilizing the Nvidia Jetson TX2i/Xavier. This technology is used to connect the GPU stack using the USB 3.1 interface 1Gb LAN connection. While the GPU handles the processing of the payload, the Zynq Ultrascale+ will handle the rest of the satellite's functions such as mode tracking and communicating with the rest of the components on the satellite. The second key portion of this project is the modularity that will be designed into the board. There will be the ability to swap out processors, storage, RAM, and GPU using System On a Module (SOM) with the same connectors.

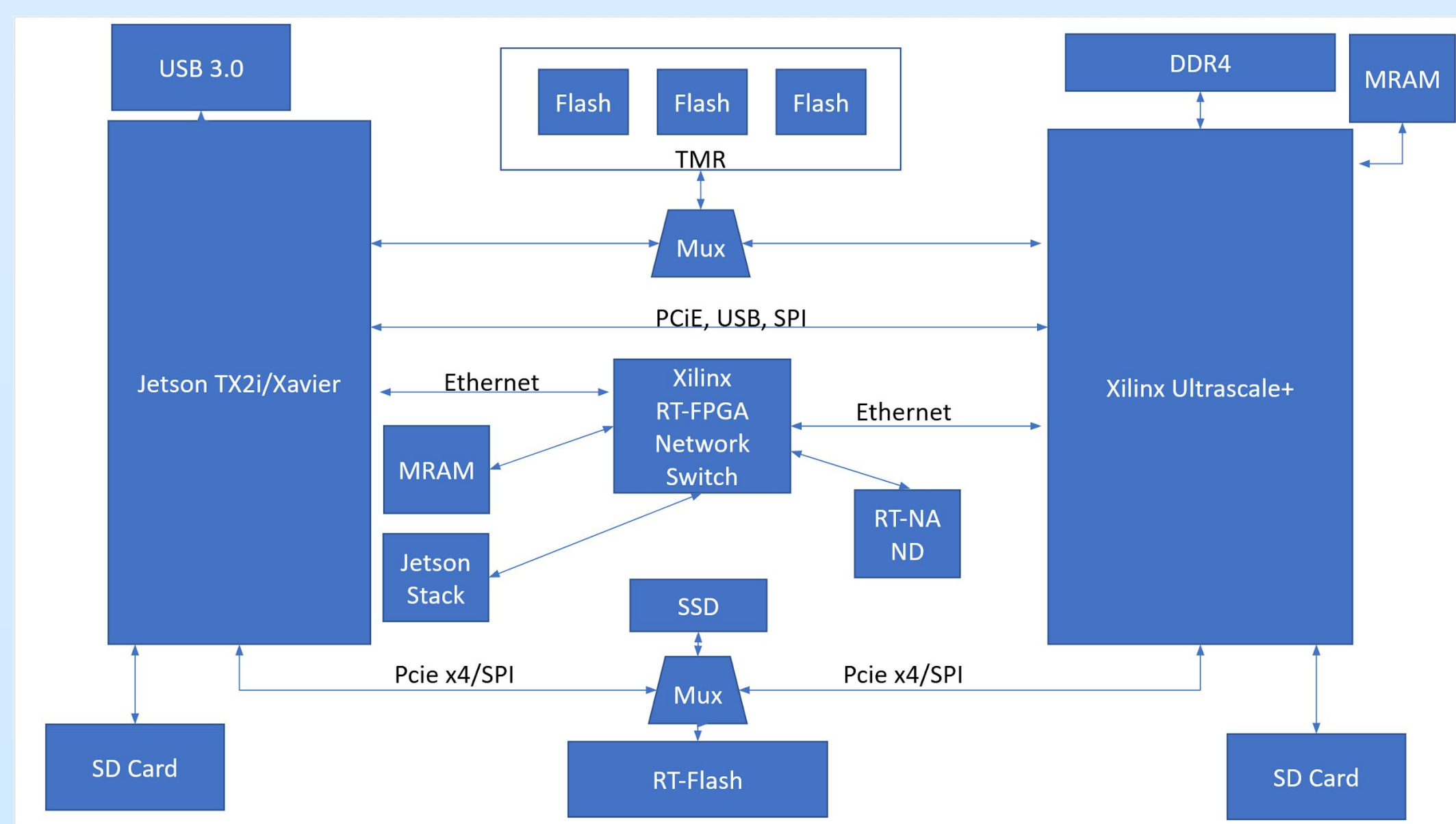


Figure 1: Block Diagram of SERVAL

## Expandable Processing Stack with LAN Communication

- This design contains carrier level Ethernet whose data link and physical layer protocol are described by the IEEE 802.3.
- This will enable each board to act as a separate compute node which can directly interact with any nodes on the network.
- They are connected through a radiation tolerant network switch
- They will also have the ability to communicate over USB 3.1 if the Xavier is the main processing unit.
- The goal is to have a max of 8 Jetson units in one stack.

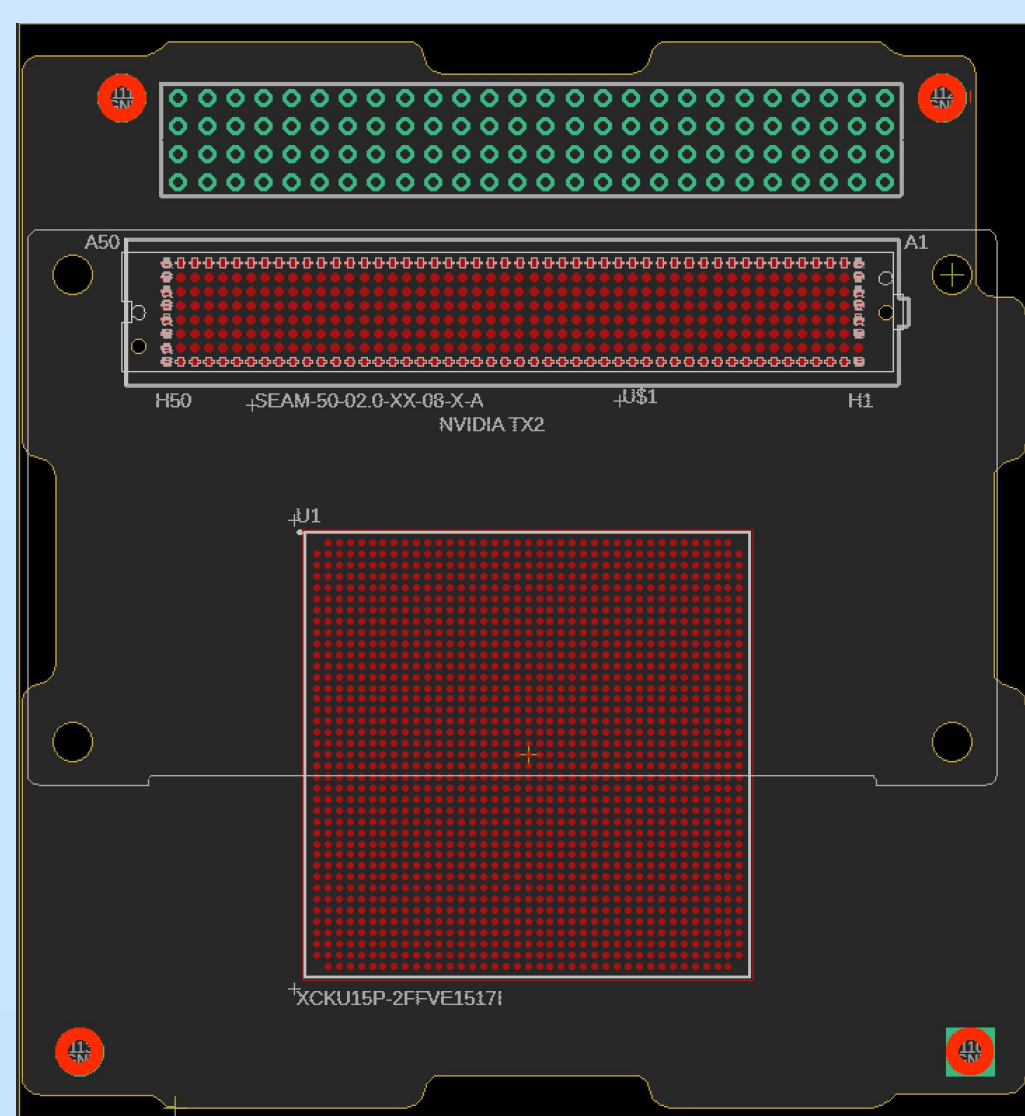


Figure 2: SERVAL Board v1

## Applications

- Designed for numerous Cubesat applications
- Can be used as an FPGA development board
- IOT
- Robotics

## Modular Design for Increased Versatility

Project SERVAL will implement a modular design that works in tandem with a multiprocessing design. The two onboard processors are the TX2i and the Xilinx Zynq Ultrascale+. These two can be swapped out from similar processors in each respective company (i.e. the Jetson Xavier or the RF-SOC version of the Zynq UltraScale+).

The reason for the modular design is for people to have more versatility with the board. There will be potential to scale Project SERVAL in a multitude of ways:

- ❖ The permanent memory can be changed according to the mission requirements
- ❖ RAM can be swapped out as well as different types of RAM
- ❖ Peripherals can be chosen for the mission's needs like adding USB, Ethernet, GPIO header, SPI, etc.

The RF-SOC version of the Ultrascale+ allows for Project SERVAL to be expanded with the capabilities of a software defined radio. The goal of this project is to eventually have an All-in-One board that can completely control the satellite while also handle advanced data processing.

## Radiation Environment and Mitigation

In Low Earth Orbit or LEO, the radiation levels are still near a minimal unless it is a polar orbit. Due to this fact, many satellites have been able to send non-radiation tested components into space and still get results. This can be accomplished due to the thickness of the shielding the electronics have to protect it from radiation. In Figure 4, the graph shows the amount of radiation experienced by multiple satellites in different orbits, and the thickness of the shielding in specific parts. As shown above, about 400 microns of shielding should be enough protection for any Low Earth Orbit satellites. In addition to shielding, project SERVAL will have triple memory redundancy to reduce the rate at which the memory in corrupted. This will be implemented in two different ways:

- On a software level on a large SSD
- On a hardware level using NAND chips and a comparator to select the least corrupted memory set.

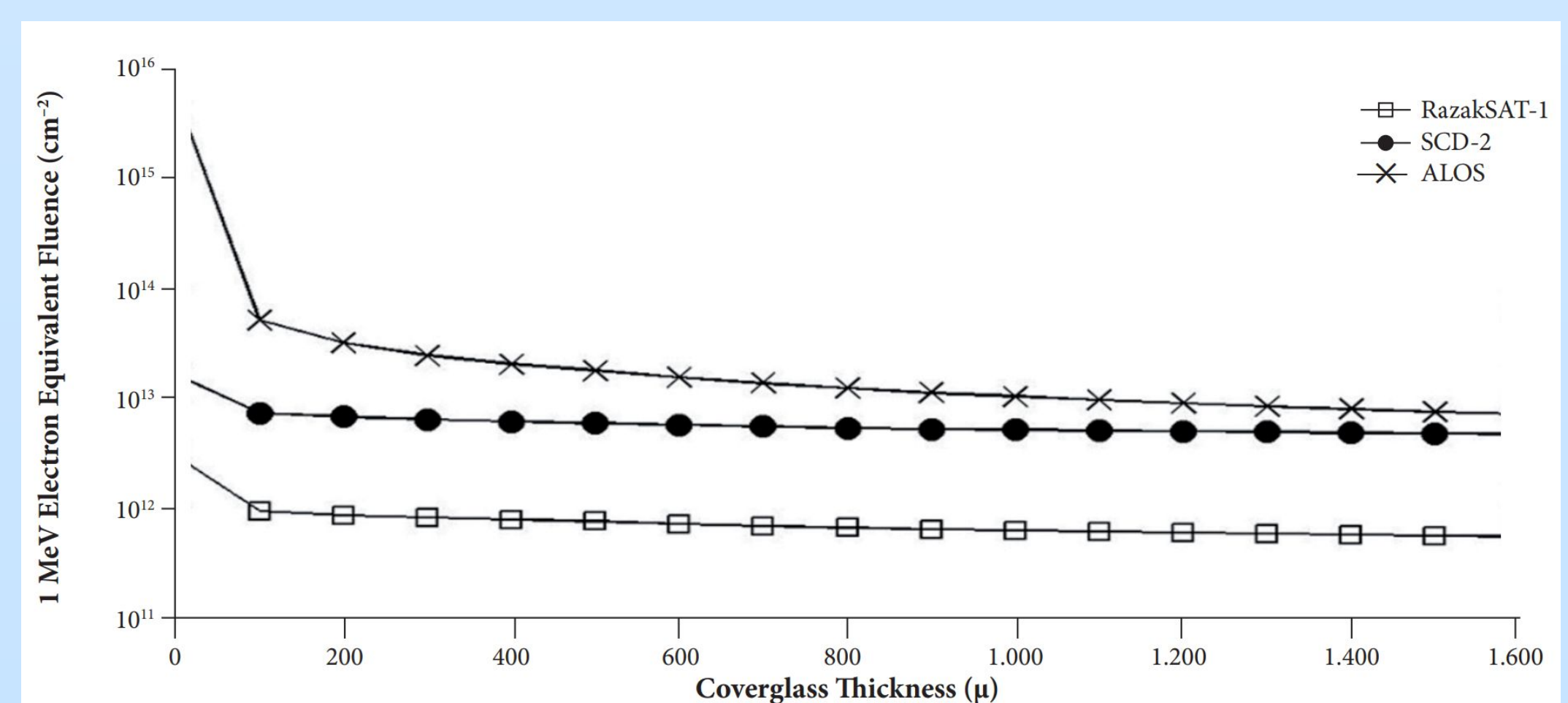


Figure 3: Radiation relative to casing thickness (Suparta 2015).

## References

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4. J. R. D. L. C. Alexandria Lin, "Implementing Fault Tolerance and Radiation Hardening on a Commercial Off The Shelf Accelerated Computing Processor in Space," Athens, 2018.