CSSE2010/7201 - Introduction to Computer Systems

Assignment 1: Digital Logic Design

Semester 1, 2025

Due: **Thursday, 17 April 2025, 4:00PM AEST** via Blackboard submission

Part A - Combinational Logic Synthesis Task [12 Marks]

Last digit of 8-digit student number	Definition of the function $F = f(X, Y, Z)$
0-1	$F = 1$ if the unsigned number given by $XYZ \in \{0, 3, 4, 6, 7\}$
2-3	$F = 1$ if the unsigned number given by $XYZ \in \{1, 2, 4, 5, 6\}$
4-5	$F = 1$ if the unsigned number given by $XYZ \in \{0, 1, 3, 6, 7\}$
6-7	$F = 1$ if the unsigned number given by $XYZ \in \{2, 3, 4, 5, 7\}$
8-9	$F = 1$ if the unsigned number given by $XYZ \in \{1, 3, 4, 5, 6\}$

1. Provide a truth table for the function $F = f(X, Y, Z)$. [1 mark]

Given my student number is 48030504
we know:

$F = 1$ when $XYZ \in \{0, 1, 3, 6, 7\}$

Thus:

X	Y	Z	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

2. Provide the unsimplified **sum-of-product (SOP)** Boolean expression for F, where each product term contains exactly three literals (variables). [1 mark]

Taking the sum-of-products for XYZ combinations for which F=1 we find:

$$\bar{X}\bar{Y}\bar{Z} + \bar{X}\bar{Y}Z + \bar{X}YZ + X\bar{Y}\bar{Z} + XYZ = F$$

3. Provide the most simplified **SOP** expression for F, where each product term contains less than three literals (variables). [2 marks]

$\bar{X}\bar{Y}\bar{Z} + \bar{X}\bar{Y}Z + \bar{X}YZ + XY\bar{Z} + XYZ = F$

$\bar{X}\bar{Y}(\bar{Z}+Z) + YZ(\bar{X}+X) + XY\bar{Z}$

$\bar{X}\bar{Y} + YZ + XY\bar{Z} + XYZ$ ← Note still equivalent as XYZ results in F = 1

$\bar{X}\bar{Y} + YZ + XY(\bar{Z}+Z)$

$F = \bar{X}\bar{Y} + YZ + XY$

4. Provide a simplified non-SOP expression for F by following further simplifications to your SOP expression in step 3, such as allowing XOR/XNOR operations. [1 marks]

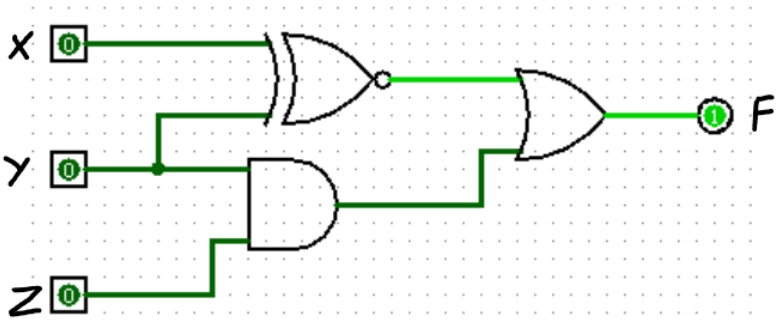
We notice that $\bar{X}\bar{Y} + XY = \overline{X \oplus Y}$

Thus:

$F = YZ + \overline{X \oplus Y}$

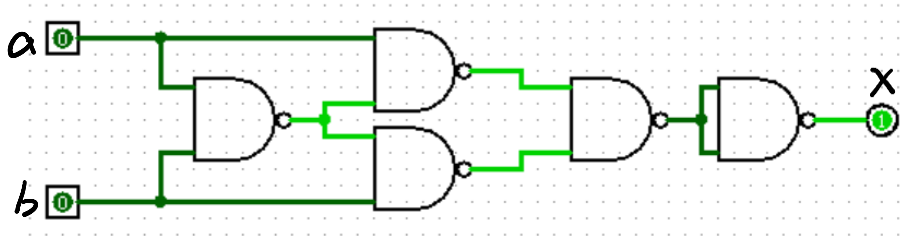
5. Provide a logic diagram[2] to show how F can be implemented with **2-input NAND gates only** with possible simplifications to reduce the gate count. [2 marks]

$F = YZ + \overline{X \oplus Y}$ Can be implemented as the "or" of a YZ "and" with a X-Y xnor gate as shown:



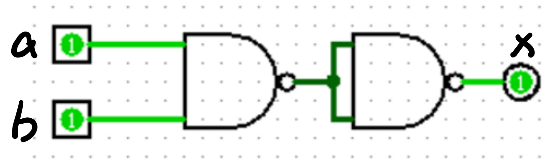
We understand that each of these gates can be constructed as NAND gate configurations. Modeling using logisim, it is demonstrated that the following circuits were NAND gate equivalents

XNOR Gate:



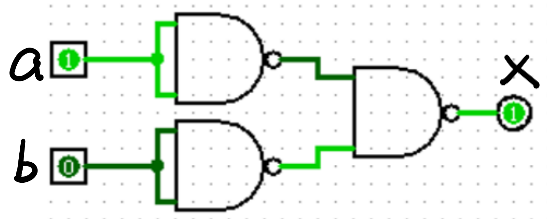
a	b	x
0	0	1
0	1	0
1	0	0
1	1	1

AND Gate



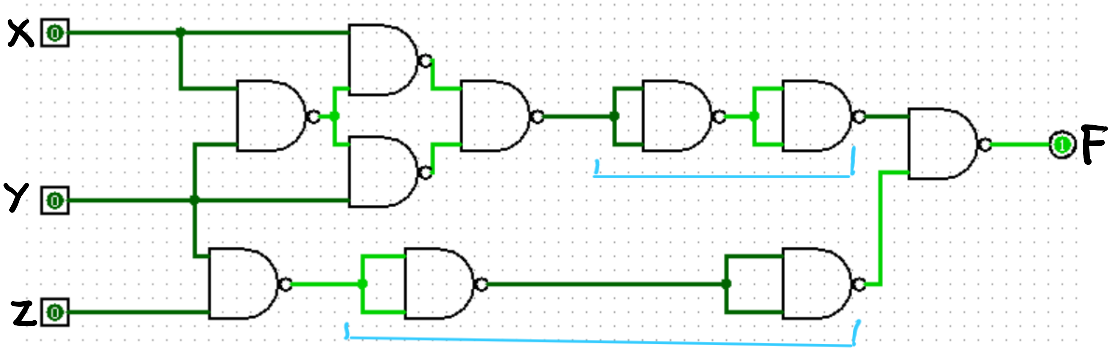
a	b	x
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate:

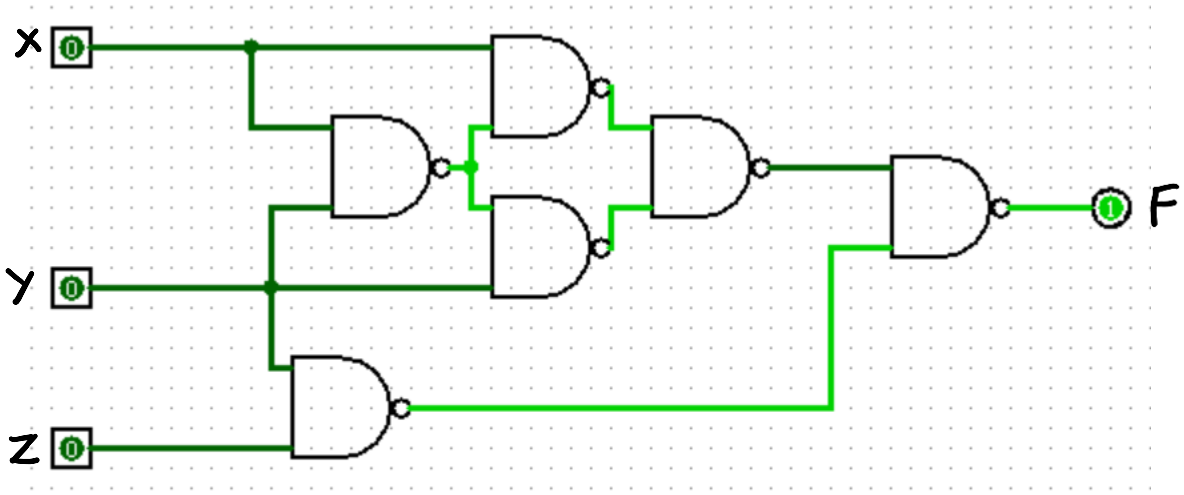


a	b	x
0	0	0
0	1	1
1	0	1
1	1	1

Substituting these into the circuit we find.

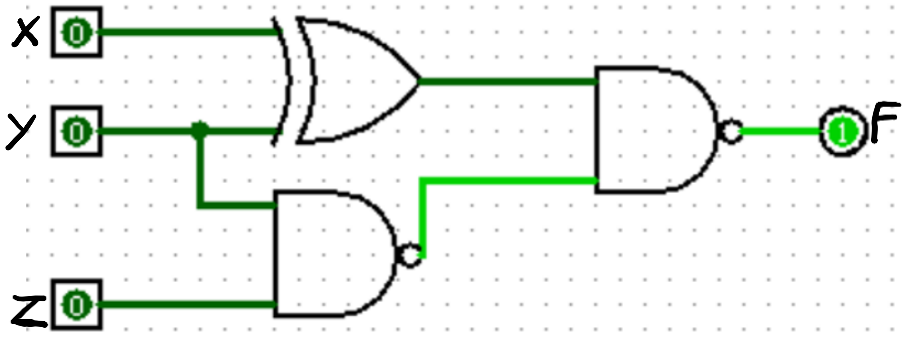


Taking note of the double NAND inverters we can simplify by removing them:

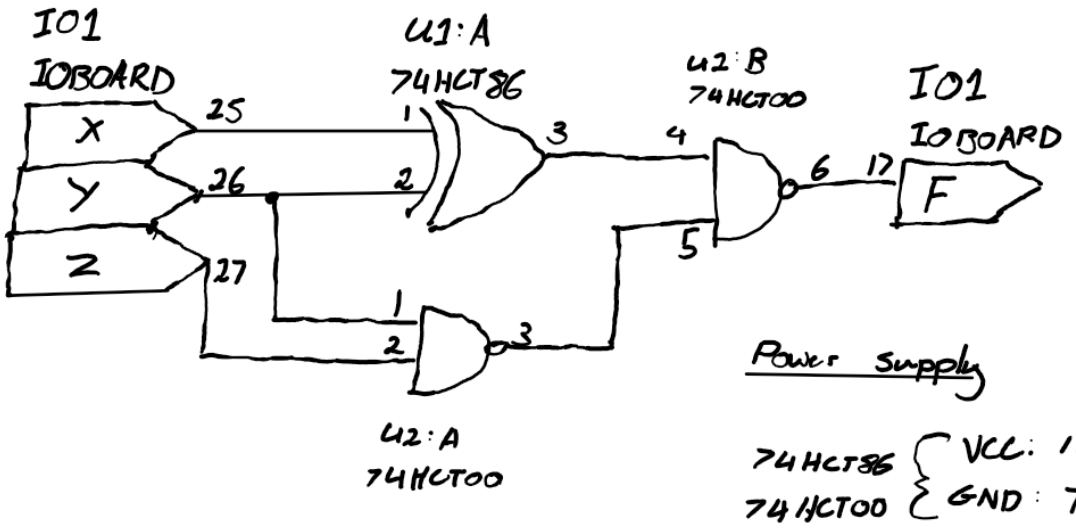


6. Based on different implementation options for F corresponding to steps (3)-(5), select the best option that minimises the required number of logic ICs and provide a circuit schematic diagram[3] with your selected option. Your answer must contain a quantitative justification for your choice of implementation. You can only assume the presence of logic ICs provided in your lab kit, which are also indicated in the device pinout document on the course Blackboard site. [3 marks]

Given each Gate IC provided in the lab kit contain four logic gates, we understand that it will take a minimum of two ICs to perform the F truth table. As is evident the simplified circuit identifies a NAND Gate XOR equivalent in the top left. Replacing this with the 74HCT86 XOR Gate IC leaves only two NAND Gates which are maintained within the 74HCT100 IC. Thus, we are left with the minimum two ICs to form the circuit:



a	b	c	x
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



7. Using a logic diagram, show how F can be implemented with one 4:1 multiplexer and NOT gates (if required) only. [2 marks]

Using the truth table we can identify some key trends:

a	b	c	x
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

When $XY = 00$, $F = 1$. Thus the first input is $\bar{Y}$ or $\bar{X}$.

When $XY = 01$, $F = Z$. Thus the second input is Z

When $XY = 10$, $F = 0$. Thus the third input is Y

When $XY = 11$, $F = 1$. Thus the fourth input is X or Y

This leaves us with the 4:1 mux: