

AIC HW2

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Part I – Common Source Amplifier:

(a) Design this circuit to achieve the requirements:

$$\left\{ \begin{array}{l} \text{under TT corner, } 25^\circ\text{C } L=2\mu\text{m} \\ V_{TH} \approx 0.35\text{V} \\ \mu_n C_{ox} \approx 305.025 \times 10^{-6} \end{array} \right\} \text{ (from hspice)}$$

$$1. |A_v| = |g_m R_D| > 3 \Rightarrow \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) R_D > 3 \\ \Rightarrow \frac{W}{L} R_D > 17.882\text{ k}$$

$$2. V_{out} = 0.9 = V_{DD} - I_D R_D = 1.8 - I_D R_D = 0.9 \Rightarrow I_D R_D = 0.9\text{ V} \\ \Rightarrow \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 R_D = 0.9 \\ \Rightarrow \frac{W}{L} R_D = 19.507\text{ k}$$

$$3. V_{GS} - V_{TH} = 0.9 - 0.35 = 0.55 > 0 \Rightarrow \text{MOS is on} \\ V_{DS} = 0.8 > V_{GS} - V_{TH} = 0.55 \Rightarrow \text{MOS is in sat.}$$

$$\Rightarrow \text{take } \frac{W}{L} = 1 \Rightarrow R_D = 19.507\text{ k}\Omega \Rightarrow \text{take } R_D = 24\text{ k}\Omega$$

∵ 有 r_o 的並聯且 V_{TH} 比 0.35 大

第 1 次測試:

Design parameter: $W/L = 1$, $L = 2\mu\text{m}$, $R_D = 24\text{ k}\Omega$

A_v	-2.9635(V/V)	g_m	$128.31\mu\Omega^{-1}$
V_{out}	917.42 mV	V_{th}	0.354 V
I_D	$36.77\mu\text{A}$	beta	302.60μ
		$\mu_n C_{ox}$	302.60μ

觀察與微調:

如同先前預估的一樣 V_{th} 確實提高了一些，然而 V_{out} 已超過許多，依照 $V_{out} = V_{DD} - I_D R_D$ ，若將 R_D 提高將可以壓低 V_{out} ，且提高 R_D 可以稍增加 Gain，試算：

$$V_{out} = 0.9 = V_{DD} - I_D R_D \Rightarrow I_D R_D = 0.9 \Rightarrow R_D = \frac{0.9}{36.77\mu\text{A}} = 24.47\text{ k}\Omega$$

試取 $R_D = 24.5\text{ k}\Omega$ 。

第 2 次測試:

Design parameter: $W/L = 1$, $L = 2 \mu m$, $R_D = 24.5 k\Omega$

Av	-3.019 (V/V)	gm	$128.22 \mu \Omega^{-1}$
V_{out}	899.74 mV	V_{th}	0.354 V
I_D	$36.74 \mu A$	beta	302.59μ
		$\mu_n C_{ox}$	302.59μ

觀察與微調:

已達到所求的規格 $V_{out} = 0.9 \pm 9mV$ 、 $Av > 3$

發現:

1. 調整 R_D 對 V_{th} 影響不大，因未影響到 V_{SB}
2. 調整 R_D 對 $\mu_n C_{ox}$ 影響不大。
3. 調整 R_D 對 g_m 影響不大。
4. 調整 R_D 對 I_D 影響不大。

(b) show that M1 operates in saturation region:

```
***** operating point status is all simulation time is 0.
node =voltage node =voltage node =voltage
+0:vdd = 1.8000 0:vin = 900.0000m 0:vout = 899.7492m
```

```
**** mosfets
subckt
element 0:mmn
model 0:n_18.1
region Saturation
id 36.7449u
ibs -8.172e-21
ibd -192.3942a
vgs 900.0000m
vds 899.7492m
vbs 0.
vth 354.9676m
vdsat 437.2468m
vod 545.0324m
beta 302.5989u
gam_eff 507.4470m
gm 128.2272u
gds 1.6488u
gmb 23.5457u
cdtot 2.7239f
cgtot 26.8185f
cstot 28.8267f
cbtot 10.5346f
cgs 24.4208f
cgd 707.5863a
```

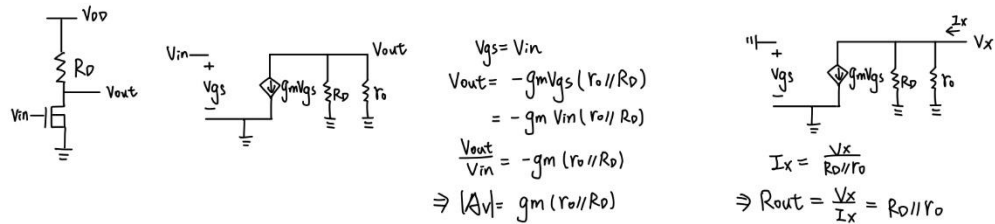
(c) print out:

- (1) the small signal gain from V_{in} to V_{out}
- (2) the output impedance

```
****      small-signal transfer characteristics

v(vout)/vin      = -3.0191
input resistance at vin      = 1.000e+20
output resistance at v(vout) = 23.5489k
```

(d) hand-calculation:



$$V_{out} = V_{DD} - I_D R_D = 1.8 - 36.7449 \times 10^{-6} \times 24500 = 0.89975 \text{ V}$$

$$r_o = \frac{1}{g_{ds}} = \frac{1}{1.6488 \mu} = 606501.698 \Omega$$

$$A_v = g_m (r_o \parallel R_D) = 128.227 \times 10^{-6} \times \left(\frac{1}{\frac{1}{606501.698} + \frac{1}{24500}} \right) = 3.0195 (\%)$$

$$R_{out} = (r_o \parallel R_D) = \left(\frac{1}{\frac{1}{606501.698} + \frac{1}{24500}} \right) = 23.5487 \text{ k}\Omega$$

(e) error rate and the error comes from:

AC gain error:

$$\text{error rate} = \frac{\text{simulation-hand}}{\text{hand}} * 100\% = \frac{3.0191 - 3.0195}{3.0195} * 100\% = -0.013\%$$

output impedance error:

$$\text{error rate} = \frac{\text{simulation-hand}}{\text{hand}} * 100\% = \frac{23.5489\text{k} - 23.5487\text{k}}{23.5487\text{k}} * 100\% = 0.00084\%$$

V_{out} 與 Gain 的誤差小到可以忽略，推測誤差來源可能僅是單純計算上取值所產生的，應該未有其他 Non-ideal Effect 影響，也可推測公式為正確。

(f) table:

	Specification	simulation	hand-calculation
V_{DD}		1.8V	
$V_{in,DC}$		0.9V	
M_1 (W/L, m)	—	2 μm / 2 μm	ratio: 1 m=1
R_D	< 50k Ω	24.5 k Ω	
$V_{out,DC}$	0.9V \pm 1%	899.748 mV	899.750 mV
gain $ A_v $	> 3V/V	3.0191 %	3.0195 %
output impedance	—	23.5489 k Ω	23.5487 k Ω
I_D	—	36.7449 μA	—

Part II – Common Gate:

(a) Design this circuit to achieve the requirements:

$$\left\{ \begin{array}{l} \text{under TT corner, } 25^{\circ}\text{C } L=1\mu\text{m} \\ V_{TH} \approx 0.39\text{V} \\ \mu_n C_{ox} \approx 311.0321 \times 10^{-6} \end{array} \right\} \text{ (from hspice)}$$

$$I_D R_D = 0.9 \Rightarrow \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 R_D = 0.9 \Rightarrow \frac{W}{L} R_D (V_B - 0.89)^2 = 5787.183... \text{ (a)}$$

$$A_v = g_m R_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) R_D > 9 \Rightarrow \frac{W}{L} R_D (V_B - 0.89) > 28.935\text{k} \text{ (b)}$$

$$V_{GS} - V_{TH} = V_B - 0.89 > 0 \Rightarrow V_B > 0.89 \text{ for MOS on}$$

$$V_{DS} > V_{GS} - V_{TH} \Rightarrow V_{out} - V_{in} > V_B - V_{in} - V_{TH} \Rightarrow V_B < V_{out} + V_{TH} = 1.29\text{V for MOS SAT.}$$

\Rightarrow choose $V_B = 1\text{V}$ s.t. (a)(b) 有交集

$$(a) \Rightarrow \frac{W}{L} R_D = 478.279\text{k} \quad (b) \Rightarrow \frac{W}{L} R_D > 263.045\text{k}$$

$$\text{Take } R_D = 90\text{k}\Omega \Rightarrow \frac{W}{L} = 5.3142$$

第 1 次測試:

Design parameter: $W/L = 5.3$, $L = 1\mu\text{m}$, $R_D = 90\text{k}\Omega$

A_v	10.8829 (V/V)	g_m	$156.316\mu\Omega^{-1}$
V_{out}	733.1321 mV	V_{th}	0.389 V
I_D	11.854 μA	beta	1.6491 m
		$\mu_n C_{ox}$	311.151 μ

觀察與微調:

V_{th} 、 $\mu_n C_{ox}$ 與預估的值差不多，然而 V_{out} 還離 0.9V 差很遠，觀察 V_{out} 和 A_v 的公式:

$$A_v = g_m R_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) R_D$$

$$V_{out} = V_{DD} - \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 R_D$$

可以發現如果要提高 V_{out} 的值有兩個做法，可以升高 V_{th} 的值、降低 W/L 的值或是降低 R_D 的值，然而我發現如果升高 L (降低 W/L 的值)，雖然會使得 V_{th} 降低使得 V_{out} 升高，然而 $\mu_n C_{ox}$ 降低的比例更多使得 A_v 大幅下降，所以我打算只調整 R_D 的值，這樣就不太會影響 $\mu_n C_{ox}$ 和 I_D 。

故試取 $R_D = 75\text{k}\Omega$ 。

第 2 次測試:

Design parameter: $W/L = 5.3$, $L = 1 \mu m$, $R_D = 75 k\Omega$

Av	10.5226 (V/V)	gm	$161.386 \mu \Omega^{-1}$
V_{out}	881.3894 mV	V_{th}	0.388 V
I_D	$12.2481 \mu A$	beta	1.6491μ
		$\mu_n C_{ox}$	311.151μ

觀察與微調:

如同先前預估的一樣調整 R_D 的值，不太會影響 $\mu_n C_{ox}$ 和 I_D ，然而 V_{out} 離目標差一點，依照 $V_{out} = V_{DD} - I_D R_D$ ，試算：

$$V_{out} = 0.9 = V_{DD} - I_D R_D \Rightarrow I_D R_D = 0.9 \Rightarrow R_D = \frac{0.9}{12.2481 \mu A} = 73.48 k\Omega$$

試取 $R_D = 73.5 k\Omega$ 。

第 3 次測試:

Design parameter: $W/L = 5.3$, $L = 1 \mu m$, $R_D = 73.5 k\Omega$

Av	10.3906 (V/V)	gm	$161.758 \mu \Omega^{-1}$
V_{out}	897.2135 mV	V_{th}	0.388 V
I_D	$12.2828 \mu A$	beta	1.6491μ
		$\mu_n C_{ox}$	311.151μ

觀察與微調:

已達到所求的規格 $V_{out} = 0.9 \pm 9mV$ 、 $Av > 0.9$

發現:

1. 調整 R_D 對 V_{th} 影響不大，因未影響到 V_{SB}
2. 調整 R_D 對 $\mu_n C_{ox}$ 影響不大。
3. 調整 R_D 對 g_m 影響不大。
4. 調整 R_D 對 I_D 影響不大。

(b) show that M1 operates in saturation region:

```
***** operating point status is all simulation time is 0.
node =voltage node =voltage node =voltage
+0:vb = 1.0000 0:vdd = 1.8000 0:vin = 500.0000m
+0:vout = 897.2135m

**** mosfets

subckt
element 0:mmn
model 0:n 18.1
region Saturation
id 12.2828u
ibs -2.153e-21
ibd -177.3759a
vgs 500.0000m
vds 397.2135m
vbs 0.
vth 388.6071m
vdsat 124.8095m
vod 111.3929m
beta 1.6491m
gam_eff 507.4460m
gm 161.7582u
gds 2.1701u
gmb 32.7743u
cdtot 7.6098f
cgtot 36.2225f
cstot 40.5861f
cbtot 20.3416f
cgs 31.4655f
cgd 1.9063f
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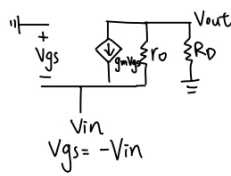
(c) print out:

- (1) the small signal gain from Vin to Vout
- (2) the input impedance
- (3) the output impedance

```
**** small-signal transfer characteristics

v(vout)/vin = 10.3906
input resistance at vin = 7.0737k
output resistance at v(vout) = 63.3901k
```

(d) hand-calculation, error rate and the error comes from:



$$\frac{V_{in} - V_{out}}{r_o} - g_m V_{gs} = \frac{V_{out}}{R_D}$$

$$\Rightarrow R_D(V_{in} - V_{out} + g_m r_o V_{in}) = V_{out} \cdot r_o$$

$$\Rightarrow V_{in} \cdot R_D (1 + g_m r_o) = V_{out} (R_D + r_o)$$

$$\Rightarrow A_v = \frac{V_{out}}{V_{in}} = \frac{R_D (1 + g_m r_o)}{R_D + r_o}$$

$$V_{out} = V_{DD} - I_D R_D = 1.8 - 12.2828 \times 10^{-6} \times 73500 = 0.897214V$$

$$r_o = \frac{1}{g_{ds}} = \frac{1}{2.1701\mu} = 460808.26 \Omega$$

$$A_v = \frac{R_D (1 + g_m r_o)}{R_D + r_o} = \frac{73500 (1 + 161.7582\mu \times 460808.26)}{460808.26 + 73500} = 10.3913$$

$$R_{out} = (r_o \parallel R_D) = \left(\frac{1}{\frac{1}{460808.26} + \frac{1}{73500}} \right) = 63.3893 k\Omega$$

$$R_{in} = \frac{R_D + r_o}{1 + g_m r_o} = 7.0732 k\Omega$$

AC gain error:

$$\text{error rate} = \frac{\text{simulation-hand}}{\text{hand}} * 100\% = \frac{10.3906 - 10.3913}{10.3913} * 100\% = -0.0067\%$$

output impedance error:

$$\text{error rate} = \frac{\text{simulation-hand}}{\text{hand}} * 100\% = \frac{63.3901k - 63.3893k}{63.3893k} * 100\% = 0.0013\%$$

input impedance error:

$$\text{error rate} = \frac{\text{simulation-hand}}{\text{hand}} * 100\% = \frac{7.0737k - 7.0732k}{7.0732k} * 100\% = 0.007\%$$

$V_{out,DC}$ error:

$$\text{error rate} = \frac{\text{simulation-hand}}{\text{hand}} * 100\% = \frac{897.2135m - 897.214m}{897.214m} * 100\% = -0.00005\%$$

V_{out} 、Gain 與 output input impedance 的誤差小到可以忽略，推測誤差來源可能僅是單純計算上取值所產生的，應該未有其他 Non-ideal Effect 影響，也可推測公式為正確。

(e) table:

	Specification	simulation	hand-calculation
V_{DD}	1.8V		
$V_{in,DC}$	0.5V		
M_2 (W/L, m)	—	5.3 μ m/1 μ m ratio=5.3 m=1	
R_D	< 100k Ω	73.5 k Ω	
$V_{out,DC}$	0.9V \pm 1%	897.2135mV	897.2140mV
gain $ A_v $	> 9V/V	10.3906 %	10.3913 %
input impedance	—	7.0737 k Ω	7.0732 k Ω
output impedance	—	63.3901 k Ω	63.3893 k Ω
I_D	—	12.2828 μ A	—

Part III – Source Follower:

(a) Design this circuit to achieve the requirements:

$$\left\{ \begin{array}{l} \text{under TT corner, } 25^\circ\text{C } L=2\mu\text{m} \\ V_{TH} \approx 0.35\text{V} \\ \mu_n C_{ox} \approx 304.967 \times 10^{-6} \end{array} \right\} \text{ (from hspice)}$$

$$1. V_{out} = I_D R_S = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 R_S = 0.9 \Rightarrow \frac{1}{2} \times 304.967 \times 10^{-6} \times \frac{W}{L} (0.6 - 0.35)^2 R_S = 0.9$$

$$\Rightarrow \frac{W}{L} R_S = 94.436\text{k}$$

$$2. A_v = \frac{g_m R_S}{1 + g_m R_S} > 0.75 \Rightarrow g_m R_S > 0.75 + 0.75 g_m R_S \Rightarrow g_m R_S > 3 \Rightarrow \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) R_S > 3$$

$$\Rightarrow \frac{W}{L} R_S > 39.348\text{k}$$

$$\text{I take } \frac{W}{L} = 1.5 \quad R_S = 63\text{k}\Omega$$

第 1 次測試:

Design parameter: $W/L = 1.5$, $L = 2\mu\text{m}$, $R_S = 63\text{k}\Omega$

A_v	853.67m(V/V)	g_m	$98.016\mu\Omega^{-1}$
V_{out}	885.121 mV	V_{th}	0.352 V
I_D	14.05 μA	beta	457.291 μ
		$\mu_n C_{ox}$	304.861 μ

觀察與微調:

V_{th} 、 $\mu_n C_{ox}$ 與預估的值差不多，然而 V_{out} 還沒滿足條件，觀察 V_{out} 和 A_v 的公式:

$$A_v = \frac{R_S}{\frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})} + R_S}$$

$$V_{out} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 R_S$$

可以發現如果要提高 V_{out} 的值有兩個做法，可以降低 V_{th} 的值或是升高 R_S 的值，我們可以發現， V_{out} 對 V_{th} 是一個平方關係式，而 A_v 對 V_{th} 是近似一個線性關係，但影響又不會像 V_{out} 一樣那麼直接且大，所以如果降低 V_{th} 應該可以有效地降低 V_{out} 而不去降低太多 A_v ，在 HW1 時，我們知道當 L 增加時，因為 short channel effect 的關係， V_{th} 會下降，故試取 $L = 2.5\mu\text{m}$ 。

第 2 次測試:

Design parameter: $W/L = 1.5$ ， $L = 2.5\mu\text{m}$ ， $R_S = 63\text{k}\Omega$

A_v	854.44 m(V/V)	g_m	$98.19\mu\Omega^{-1}$
V_{out}	891.128 mV	V_{th}	0.343 V
I_D	14.14 μA	beta	455.61 μ
		$\mu_n C_{ox}$	303.74 μ

觀察與微調:

已達到所求的規格 $V_{out} = 0.9 \pm 9\text{mV}$ 、 $A_v > 0.75$

發現:

1. 調整 R_s 對 V_{th} 、 $\mu_n C_{ox}$ 、 g_m 、 I_D 影響不大。
2. 調整 W/L 對 g_m 、 I_D 影響較大，對 V_{th} 、 $\mu_n C_{ox}$ 的影響不大。
3. 調整 L 對 V_{th} 、 $\mu_n C_{ox}$ 的影響較大，對 g_m 、 I_D 影響不大。

(b) show that M1 operates in saturation region:

```
***** operating point status is all simulation time is 0.
node =voltage node =voltage node =voltage
+0:vdd = 1.8000 0:vin = 1.5000 0:vout = 891.1284m

**** mosfets

subckt
element 0:mmn
model 0:n_18.1
region Saturation
id 14.1449u
ibs -2.646e-21
ibd -306.5143a
vgs 608.8716m
vds 908.8716m
vbs 0.
vth 343.2443m
vdsat 227.5742m
vod 265.6273m
beta 455.6168u
gam_eff 507.4461m
gm 98.1906u
gds 852.3227n
gmb 18.7049u
cdtot 4.9251f
cgtot 62.5877f
cstot 66.3900f
cbtot 23.3332f
cgs 56.5278f
cgd 1.2746f
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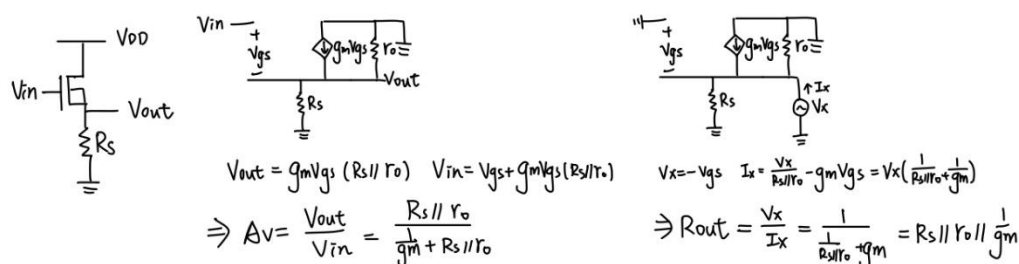
(c) print out:

- (1) the small signal gain from V_{in} to V_{out}
- (2) the output impedance

```
*** small-signal transfer characteristics

v(vout)/vin = 854.4481m
input resistance at vin = 1.000e+20
output resistance at v(vout) = 8.7025k
```

(d) hand-calculation, error rate and the error comes from:



$$V_{out} = I_D R_s = 14.1449 \times 10^{-6} \cdot 63 \times 10^3 = 0.891129 \text{ V}$$

$$g_m = 98.1906 \mu$$

$$r_o = \frac{1}{g_{ds}} = \frac{1}{852.3221 \text{ n}} = 1173264.539 \Omega$$

$$A_v = \frac{r_o \parallel R_s}{\frac{1}{g_m} + r_o \parallel R_s} = \frac{\left(\frac{1}{1173264.539} + \frac{1}{63000} \right)}{\frac{1}{98.1906 \mu} + \left(\frac{1}{1173264.539} + \frac{1}{63000} \right)} = 0.8544558 (\%)$$

$$R_{out} = (r_o \parallel R_s \parallel \frac{1}{g_m}) = 8.7020 \text{ k}\Omega$$

AC gain error:

$$\text{error rate} = \frac{\text{simulation-hand}}{\text{hand}} * 100\% = \frac{0.8544481 - 0.8544558}{0.8544558} * 100\% = -0.0009\%$$

output impedance error:

$$\text{error rate} = \frac{\text{simulation-hand}}{\text{hand}} * 100\% = \frac{8.7025 \text{ k} - 8.7020 \text{ k}}{8.7020 \text{ k}} * 100\% = 0.0057\%$$

$V_{out,DC}$ error:

$$\text{error rate} = \frac{\text{simulation-hand}}{\text{hand}} * 100\% = \frac{0.891128 - 0.891129}{0.891129} * 100\% = -0.00011\%$$

V_{out} 、Gain 與 output impedance 的誤差小到可以忽略，推測誤差來源可能僅是單純計算上取值所產生的，應該未有其他 Non-ideal Effect 影響，也可推測公式為正確。

(e) table:

	Specification	simulation	hand-calculation
V_{DD}	1.8V		
$V_{in,DC}$	1.5V		
M_3 (W/L, m)	—	3.75 μm / 2.5 μm ratio: 1.5 $m=1$	
R_S	< 80k Ω	63k Ω	
$V_{out,DC}$	0.9V \pm 1%	891.128mV	891.129mV
gain $ A_v $	> 0.75V/V	0.8544481 $\%$	0.8544558 $\%$
output impedance	—	8.7025k Ω	8.7020k Ω
I_D	—	14.1449 μA	—