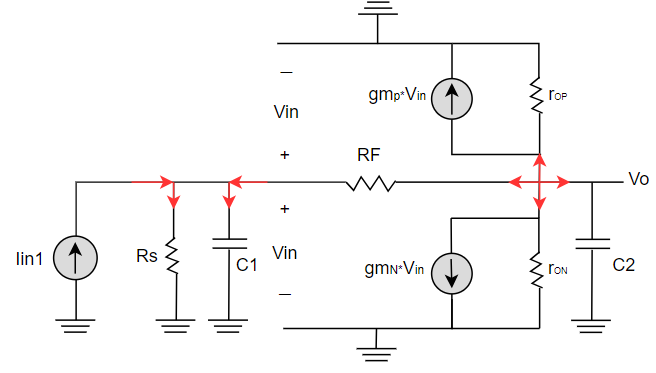
**AIC HW5**

110011222陳立珩

1. **With Feedback**
2. **Design procedure**(考慮低頻時，故 s=jω→0 )

此電路小訊號模型:

****

Iin1 + = + sC1Vin ……(1)

use KCL ⇒

sC2Vo+(+gmpVin)+ (+gmnVin)+= 0 ……(2)

1. ⇒ Vin = ( Iin + )(Rs || RF)
2. ⇒ Vin = Vo = AVo ( let A = )

By(1)and(2) ⇒ Vin = ( Iin + )(Rs || RF) = AVo

⇒ Vo(A(Rs || RF)) = Iin(Rs || RF)

⇒ Closed loop gain = = =

1. 故可知，若要讓 Closed-loop gain > 0.85kΩ， 要很大，i.e.

W / L要很大。

1. 設Iin1的DC=15uA，AC=1A (此處的 DC 電流值對於 Closed-loop gain 幾乎沒有影響)。
2. 在還沒考慮到Vout的情況下，先嘗試= (m=8)。

= (m=8)。

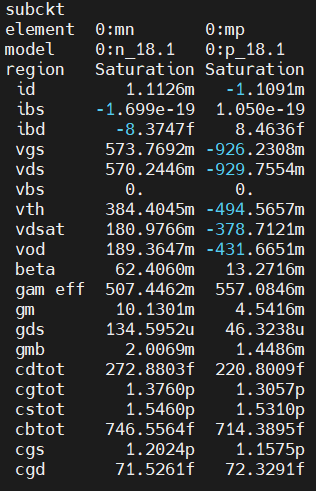
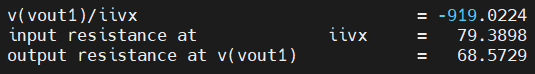
Iin1 = 15 uA。

**第 1 次測試:**

**Design parameter:**

|  |  |  |
| --- | --- | --- |
| **Wn/Ln** | **Wp /Lp** | **Iin1** |
| 25um/1um(m = 8) | 25 um/1um (m = 8) | 15 uA |

**Result:**

****

**觀察與微調:**

可以觀察到Closed-loop gain已經達到要求，然而bw和Vout沒有達到，根據下方(e)推導的pole公式可以知道，如果加大的值就可以增加pole的大小，bw因此變大，由於bw還與標準差很多所以我打算直接條小L值以達到更大的放大效果。

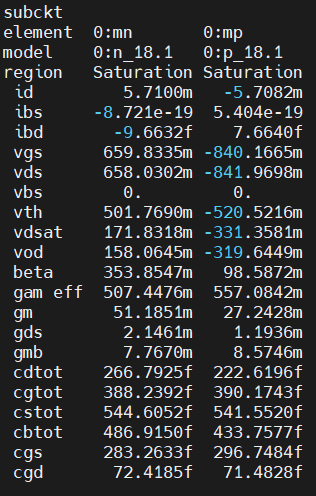
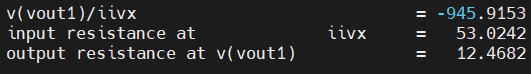
取= (m=8)，= (m=8)。

**第 2 次測試:**

**Design parameter:**

|  |  |  |
| --- | --- | --- |
| **Wn/Ln** | **Wp /Lp** | **Iin1** |
| 25um/0.2um(m = 8) | 25 um/0.2um (m = 8) | 15 uA |

**Result:**

****

****

****

**觀察與微調:**

觀察到確實因為的上升，導致bw的上升，且已經達到標準，接這就是要調整Vout值，由於Vout值是由Vx值減去一個IxRF，所以如果要使Vout值大一些，要減少IX值，根據KCL，Ix + Id,p = Id,n，因此需要盡量讓Id,p與Id,n接近。由於目前Id,n大於Id,p，因此我打算降低Id,n值，也就是降低。

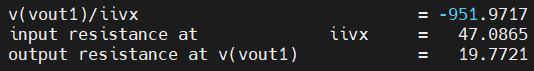
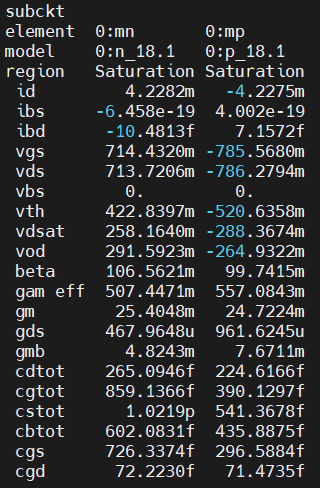
取= (m=8)，= (m=8)。

**第 3 次測試:**

**Design parameter:**

|  |  |  |
| --- | --- | --- |
| **Wn/Ln** | **Wp /Lp** | **Iin1** |
| 25um/0.6um(m = 8) | 25 um/0.2um (m = 8) | 15 uA |

**Result:**

****

****

****

**觀察與微調:**

發現Vout確實升高了，於是繼續讓Id,n變小。

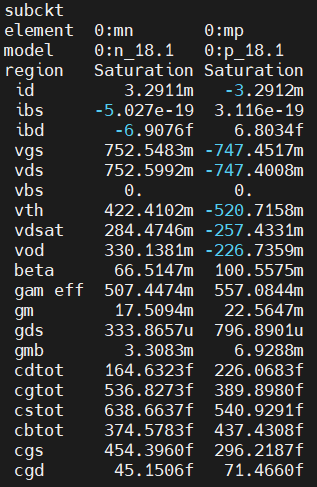
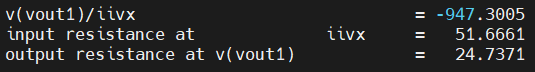
取= (m=5)，= (m=8)。

**第 4 次測試:**

**Design parameter:**

|  |  |  |
| --- | --- | --- |
| **Wn/Ln** | **Wp /Lp** | **Iin1** |
| 25um/0.6um(m = 5) | 25 um/0.2um (m = 8) | 15 uA |

**Result:**

****

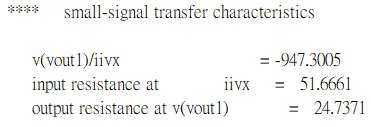
****

**觀察與微調:**

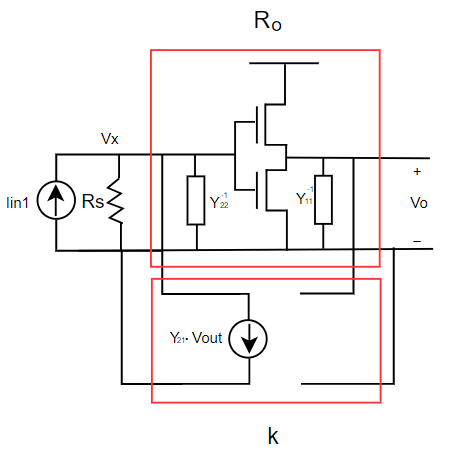
達題目要求bw>650MHz，|Closed-loop gain|>0.85kΩ，

Output common voltage>0.75V。

**b.**

****

**c. Hand calculation** (考慮低頻時，故 s=jω→0 )

****

Y11= RF-1

Y22= RF-1

Y21=-RF-1

Rin,open = RF || RS || = 50k||1k = 980.39216(Ω)

Rout,open = RF || rON || rOP || = 50k||3.127437k||1.2803964k = 476.018497(Ω)

Vo= −Vx(gmN+ gmP)(RF || rON || rOP || )

= −Iin1RF || RS ||)(gmN+ gmP)(RF || rON || rOP || )

Open-loop gain Ro = = −RF || RS ||)(gmN+ gmP)(RF || rON || rOP || )

≅ −RF || RS)(gmN+ gmP)(RF || rON || rOP)

= − (980.39216)(0.01751+0.02256)476.018497

= −18438.68(Ω)

將iF= − iRF = 代入 K = ⇒ K= Y21= = -0.001)

(1+kRo) = (1+(-0.001)( −18438.68)) = 19.43868

Rin,Closed = = = 56.21939(Ω)

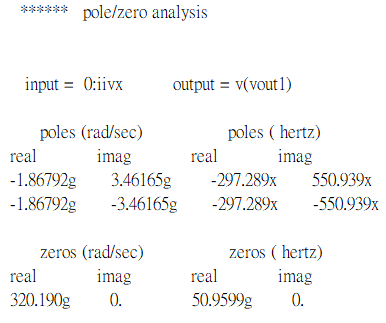
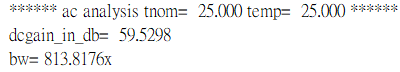
Rout,Closed = = = 26.91241(Ω)

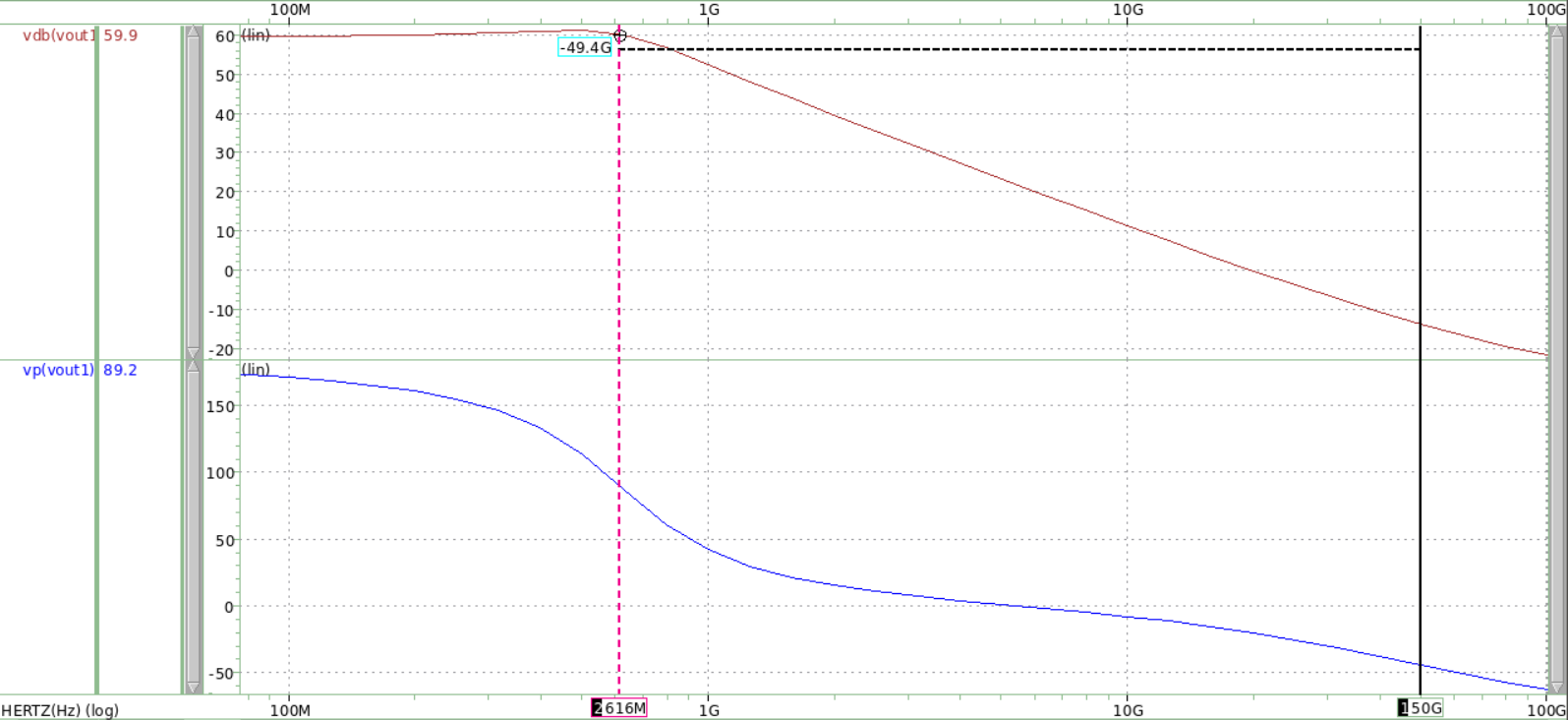
Closed loop gain = = = 1057.344(Ω)

|  |  |  |  |
| --- | --- | --- | --- |
|  | Calculate | Hspice | Error |
| Rin,Closed(Ω) | 56.21939 | 51.8785 | 7.72% |
| Rout,Closed(Ω) | 26.91241 | 25.1933 | 6.38% |
| Closed-loop gain(Ω) | -1057.344 | -947.3084 | 10.4% |

計算上有些許誤差，由於此三個數值都是由Open-loop gain推算得到，所以有可能在Open-loop gain上就有誤差存在，推測可能是沒有考慮到寄生電容和在推導的時候假設s=jω→0，省略公式其中一部分導致。

**d.**



******

***Closed loop gain (dB)***

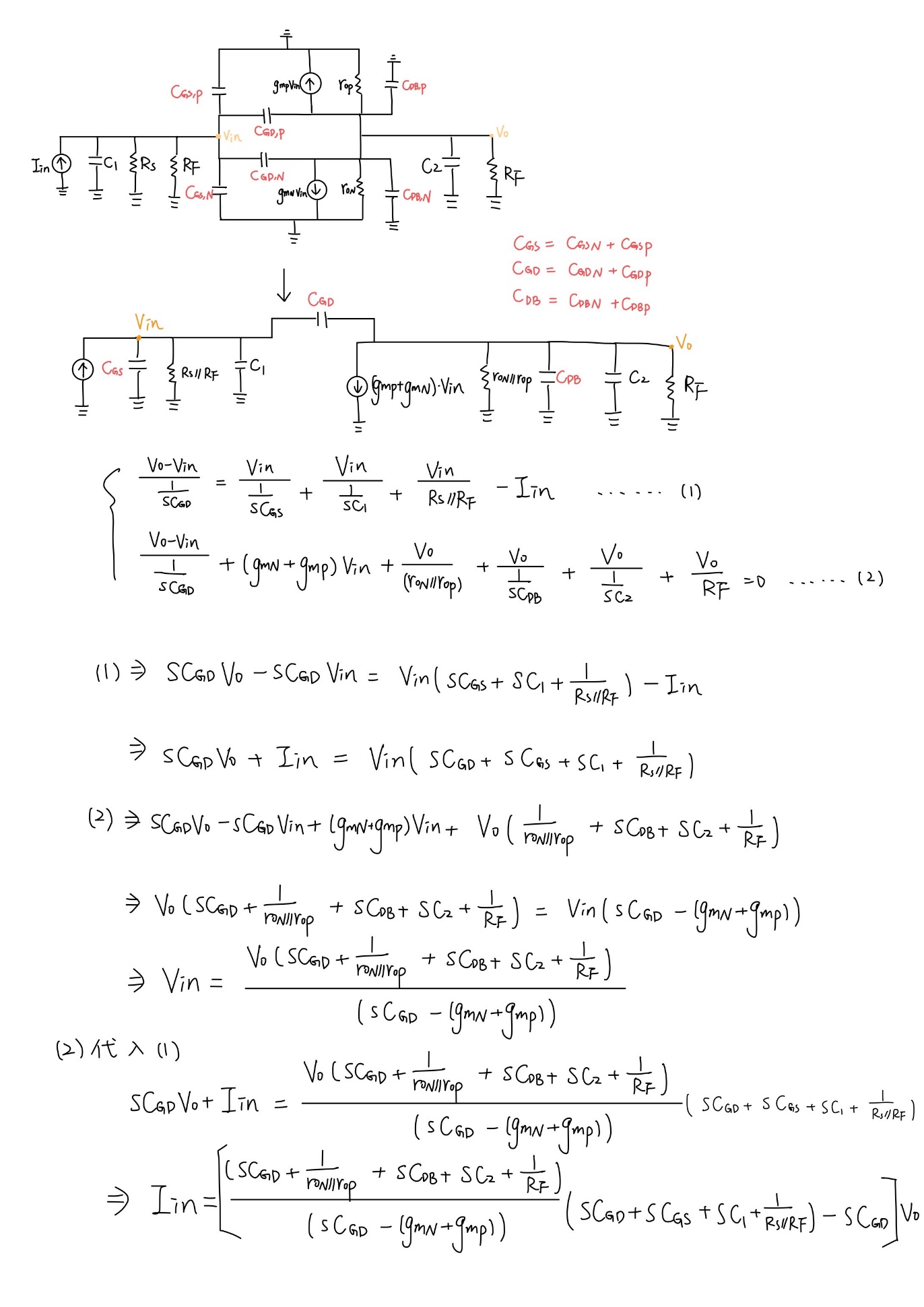
***Frequency****(****Hz****)*

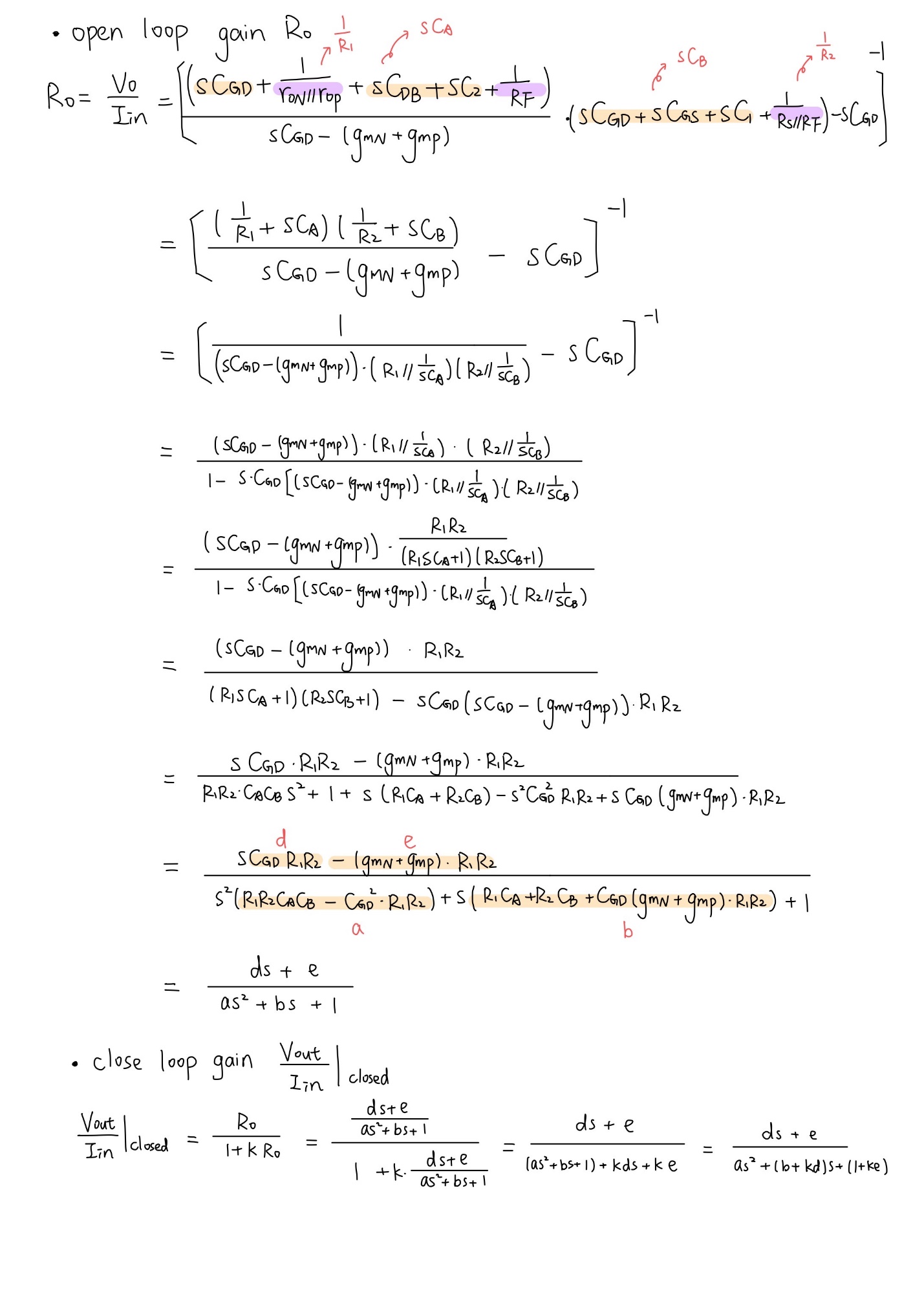
*zero*

*pole 1 & pole 2*

***Phase****(****°****)*

**e.**

****

****

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| CGS,N | CGS,P | CGD,N | CGD,P | CDB,N | CDB,P |
| 4.54E-13(F) | 2.96E-13(F) | 4.52E-14(F) | 7.14E-14(F) | 1.2E-13(F) | 1.54E-13(F) |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| CGS | CGD | CDB | rON | rOP | rON|| rOP |
| 7.5E-13(F) | 1.17E-13(F) | 2.74E-13(F) | 2995.216Ω | 1254.878Ω | 884.364Ω |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| RS | RF | RS||RF | R1 | R2 |
| 50 kΩ | 1 kΩ | 980.39216Ω | 469.3170Ω | 980.3921Ω |

|  |  |  |  |
| --- | --- | --- | --- |
| CA | CB | gmN | gmP |
| 1.39E-12(F) | 1.87E-12(F) | 0.017509(Ω-1) | 0.022564(Ω-1) |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| a | b | d | e | k |
| 1.19E-18 | 4.63E-9 | 5.37E-8 | -18438.68421 | -0.001 |

**Zero:** ds+e =0 ⇒ WZ = = 3.4364(rad/sec) = 54.691965852 (GHz)

| WZero,calculate | = 54.691965852 (GHz)

| WZero,hspice | = 50.9599 (GHz)

WZero,error = || \* 100%= 6.82%

**Poles:** as2+(b+kd)s+(1+ke) = 0 ⇒ WPole

= −1.93 ± 3.56j (rad/sec)

= −3.066397± 5.659045j (Hz)

WPole1= −306.6397 + 565.9045 j (MHz)

WPole2= −306.6397 − 565.9045 j (MHz)

| WPole,calculate | =

= 643.642650 (MHz)

| WPole,hspice | =

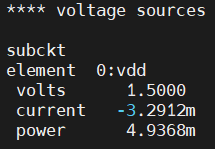
= 626.030775(MHz)

WPole,error = || \* 100%= 2.77%

|  |  |  |
| --- | --- | --- |
| Comparison | |Pole| | Zero |
| Hspice | 626.030775 (MHz) | 50.9599 (GHz) |
| Calculate | 643.642650 (MHz) | 54.691965852 (GHz) |
| Error | 2.74% | 6.82% |

誤差不大，推測造成誤差原因為電路中的寄生電容，且因為此式子較為複雜，故在計算時，各值的四捨五入也會導致最終計算上的結果有些許誤差。

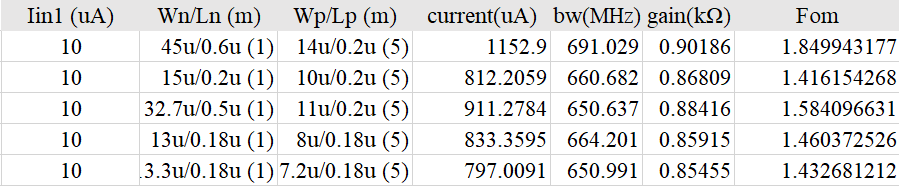
**f.**

****

FOM= = = 4.26913

可以發現我的電流值太大了造成FOM值很大，於是我打算先將電流壓下來，且從上述計算可知，current 主要來自於VDD的電流，i.e. current source 影響很小。而若要讓 current↓，需要將W/L或m值往下調。可以注意到雖然(gmN+ gmP)值會因為電流下降而降低，然而根據HW1得知rO = ，r­ON和rOP值都會上升，所以Closed-loop gain不一定會下降，至於觀察Pole公式可以發現(gmN+ gmP)和r­ON和rOP值的上升都會導致bw的下降，所以電流不能取得太小，由於r­O值不能太大所以我打算取小的L調整W和m的值控制電流。

以下經過幾次測試之後得到的FOM值:



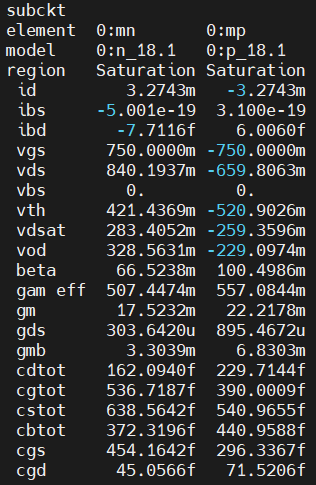
可以觀察到降低電流對於F­OM的降低有很大的幫助，但同時bw也會降低不少，而Closed-loop gain雖然也會降低，但如上述推測變化幅度不會像bw一樣那麼大，因此可以總結Current和bw、Closed-loop gain之間存在Trade-off。

**註:上傳的sp檔為還未優化過後之參數，有註解優化過的參數。**

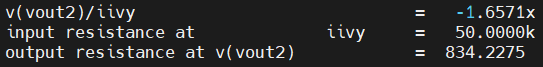
**2.Without Feedback**

**a.**

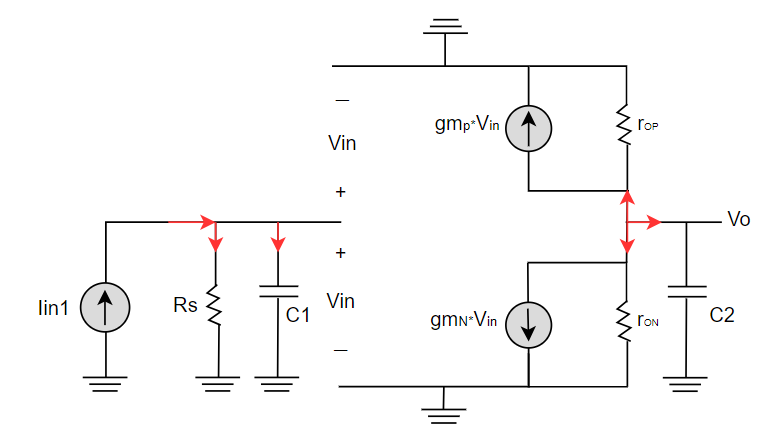
****

****

**b.**

****

**c. Hand calculation** (考慮低頻時，故 s=jω→0 )

****

Iin1 = + sC1Vin ……(1)

use KCL ⇒

sC2Vo+(+gmpVin)+ (+gmnVin)= 0 ……(2)

1. ⇒ Vin = IinRs
2. ⇒ Vin = Vo

By(1)and(2) ⇒ Ro = = −RS(gmN+ gmP)(rON || rOP)

Zout = rON || rOP || = 3.293352k||1.1167355k = 833.9524(Ω)

Ro = = −RS(gmN+ gmP)(rON || rOP)

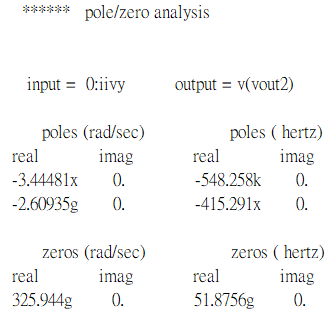
= − (50000)(0.0175232+0.0222178)833.9524

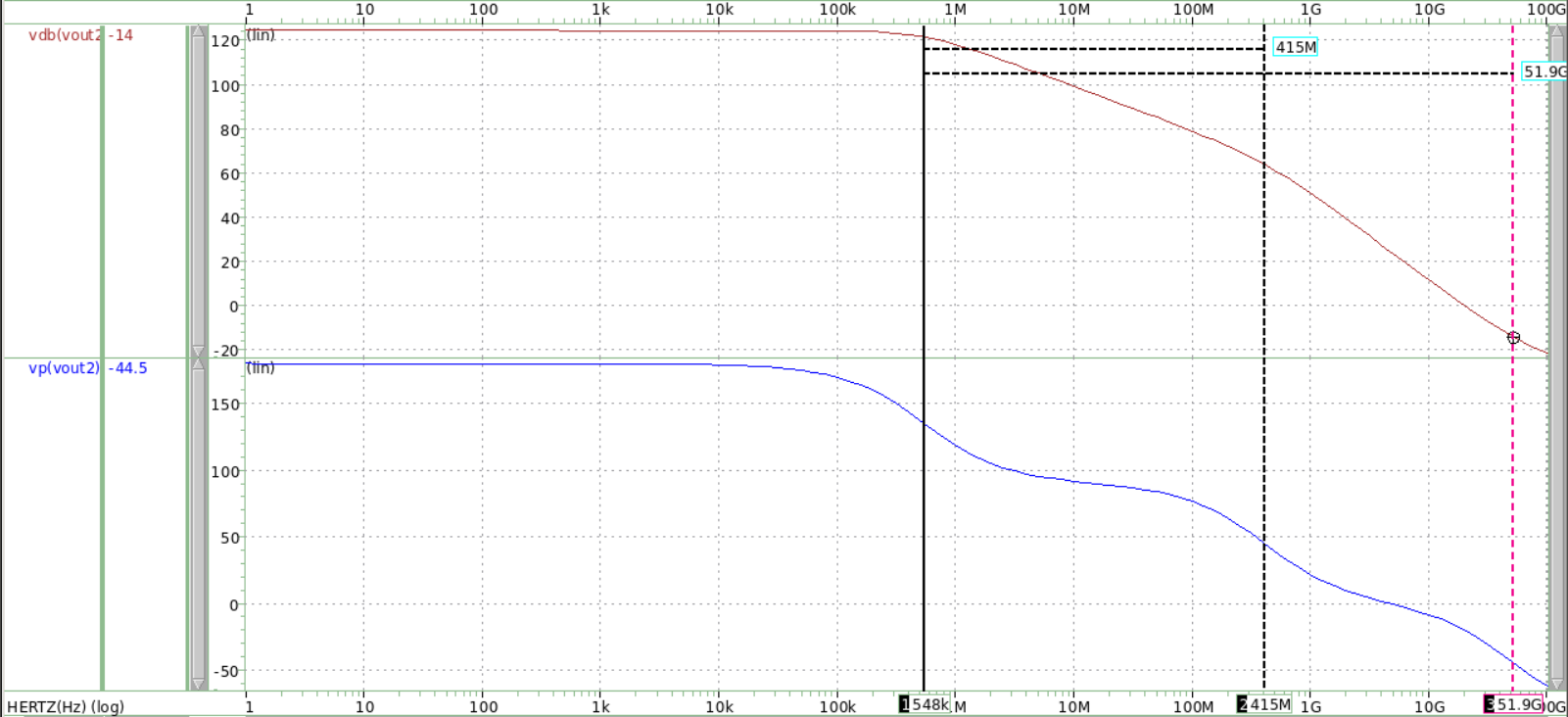
= − 1657105.12 (Ω)

|  |  |  |  |
| --- | --- | --- | --- |
|  | Calculate | Hspice | Error |
| ­Zout(Ω) | 833.9524 | 834.2275 | 0.03% |
| Trans Impe. gain(Ω) | − 1657105.12 | -1657100 | 0.0003% |

誤差很小，可能來自計算時四捨五入造成計算上誤差，公式基本上正確。

**d.**

****

****

*pole 2*

*zero*

*pole 1*

***Transimpedence gain (dB)***

***Phase****(****°****)*

***Frequency****(****Hz****)*

**e.**

Transfer Function與第一題推導的公式很像，唯將RF刪除，其餘都相同，就不再推導一次。

RO ==

其中CA = CGD + CDB + C2 , CB = CGD + CGS + C1 , R1 = rON || rOP­ , R2 = RS

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| CGS,N | CGS,P | CGD,N | CGD,P | CDB,N | CDB,P |
| 4.54E-13(F) | 2.96E-13(F) | 4.51E-14(F) | 7.15E-14(F) | 1.1E-13(F) | 1.6E-13(F) |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| CGS | CGD | CDB | rON | rOP | rON|| rOP |
| 7.51E-13(F) | 1.16E-13(F) | 2.75E-13(F) | 3293.3520Ω | 1116.735Ω | 833.9524Ω |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| CA | CB | R1 | R2 | gmN | gmP |
| 1.39E-12(F) | 1.87E-12(F) | 833.9524Ω | 50 kΩ | 0.0175232(Ω-1) | 0.0222178(Ω-1) |

|  |  |  |  |
| --- | --- | --- | --- |
| a | b | d | e |
| 1.08E-16 | 2.88E-7 | 4.86099E-6 | -1657105.124 |

**Zero:** ds−e =0 ⇒ WZ = = 3.4089856(rad/sec) = 54.2557 (GHz)

WZero,calculate = 54.2557 (GHz)

WZero,hspice = 54.8258 (GHz)

WZero,error = || \* 100%= 1.05%

**Poles:** as2+bs+1 = 0 ⇒ WPole

= −1.334525 ± 1.3310447 (rad/sec)

= −2.1239628± 2.1184235 (Hz)

WPole1,calculate= −553.928 (KHz) WPole1,hspice = −548.258(kHz)

WPole2,calculate= −424.238 (MHz) WPole2,hspice = −415.291(MHz)

WPole,error = || \* 100% = 1.10%(Pole1)

=2.06% (Pole2)

誤差不大，推測造成誤差原因為電路中的寄生電容，且因為此式子較為複雜，故在計算時，各值的四捨五入也會導致最終計算上的結果有些許誤差。

|  |  |  |  |
| --- | --- | --- | --- |
| Comparison | Pole1 | Pole2 | Zero |
| Hspice | −548.258 (kHz) | −415.291 (MHz) | 54.8258 (GHz) |
| Calculate | −553.928 (kHz) | −424.238 (MHz) | 54.2557 (GHz) |
| Error | 1.02% | 2.1% | 1.05% |

**3. Discussion**

**a.**

1. 可以發現有Feedback的電路Band-width大很多，假設不考慮Loading RF，如果有一個Feedforward 放大器的Transfer function 為 ，可以推導出Closed-loop =，也就是加了feedback的系統可以使得−3dB band-width 增加倍。
2. 然而觀察上述公式可以發現Closed-loop gain會下降許多，如果A­0很大的話，Closed-loop gain會只剩下。
3. 如果從Output Impedence 的觀點來看，因此題型形式為V-I的Feedback的系統，所以Output Impedence大幅下降了，此題可以推出

Z­out,with fb.=，其中, A = Open-loop gain。

1. 如果從input impedence 的觀點來看，因此題型形式為V-I的feedback的系統，所以input impedence大幅下降了，此題可以推出

Z­in,with fb.=，其中, A = Open-loop gain。

In summary, Negative Feedback system offers the following benefits:

1. **Desensitize the gain:**

According to the formula, if the Open-loop gain is very large, the Closed-loop gain will approach.

1. **Reduce effect of noise:**

The feedback network itself may contain resistors or transistors,degrading the overall noise performance.

1. **Control the input and output impedence:**

As the derivation of the formula, the input and output impedances are related to 1+. Depending on the type of feedback system, we can determine whether it amplifies or attenuates. If it's a voltage-current (V-I) feedback system like in this case, we can get smaller input and output impedances.

1. **Extend bandwidth of the amplifier:**

As stated in I.

However, if a Negative Feedback system is used, the advantages mentioned above are traded off with gain, as described in statement II.

**b.**

table. 1**(還未優化過後的數據)**

|  |  |  |  |
| --- | --- | --- | --- |
| Fig. 1 | | | |
| Working item | Specification | Simulation | Calculation |
| Vdd (V) | 1.5 | | |
| C1, C2 (F) | 1p | | |
| transimpedance DC gain (k) | > 0.85 | 0.947 | 1.057 |
| bandwidth (MHz) | > 650 | 813.8176 |  |
| Closed-loop poles/zeros  (rad/s) |  | WPole =  −1.86 ± 3.46j  Wzero =  3.20190 | WPole =  −1.93 ± 3.56j  Wzero =  3.4364 |
| Closed-loop  input impedance  () |  | 51.8785 | 56.2194 |
| Closed-loop  output impedance  () |  | 25.1933 | 26.9124 |
| Input common  mode current (uA) |  | 15 |  |
| Output common  mode voltage (V) | 0.75 (± 1%) | 0.752599 |  |
| M1 (W/L), m |  | 25um/0.6um  (m = 5) |  |
| M2 (W/L), m |  | 25 um/0.2um  (m = 8) |  |
| FoM (uA/) |  | 4.26913 |  |

table. 2**(還未優化過後的數據)**

|  |  |  |  |
| --- | --- | --- | --- |
| Fig. 2 | | | |
| Working item | Specification | Simulation | Calculation |
| Vdd (V) | 1.5 | | |
| C3, C4 (F) | 1p | | |
| transimpedance DC gain (k) | - | 1657.1 | 1657.105 |
| bandwidth (MHz) | - | 0.5471992 |  |
| Closed-loop poles/zeros  (rad/s) |  | WPole1 =-344.481M  WPole2 =-2.60935G  Wzero =325.944G | WPole1 =-348.043M  WPole2 =-2.66557G  Wzero =340.898G |
| Closed-loop  input impedance  () |  | 50k |  |
| Closed-loop  output impedance  () |  | 834.2275 | 833.9524 |
| Input common  mode current (uA) | same as Iin1 | 15 |  |
| Output common  mode voltage (V) | - | 0.8401937 |  |
| M3 (W/L), m | same as M1 | 25um/0.6um  (m = 5) |  |
| M4 (W/L), m | same as M2 | 25 um/0.2um  (m = 8) |  |

**註:上傳的sp檔為還未優化過後的參數。**