#HW1 Successive Approximation summary report

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- **Contribution**
  1. 林士登 - Software Program, Verilog RTL code, Testbench, Synthesis, Layout testing and Simulations, Final summary report
  2. 陳立珩 - Verilog RTL code, Testbench, Synthesis, Layout testing and Simulations

- **Outline**
  1. Software code simulation
  2. Verilog code / RTL simulation
  3. Gate-level synthesis / Gate simulation report
  4. Layout generation
  5. Post-layout simulation report
  6. Waveform comparison (RTL / pre-layout / post-layout)

- **Results and Analysis**

1. Software program - C

('hw1.c' file is included in the submit area)

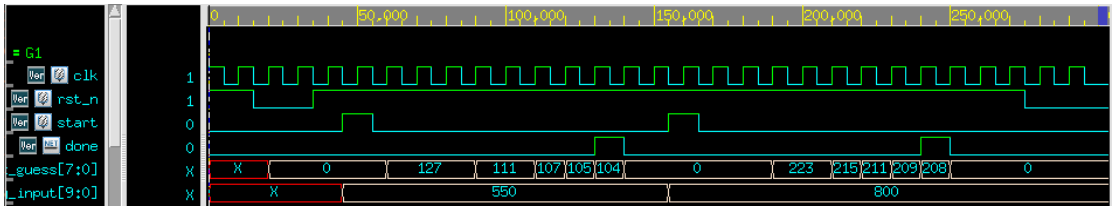
```
PS C:\Users\User\Desktop\verilog_test> cd "c:\Users\User\Desktop\veri
log_test\" ; if ($?) { gcc hw1.c -o hw1 } ; if ($?) { .\hw1 }
Corresponding y: 549.60
Closest x: 104
Closest x binary: 01101000

Corresponding y: 799.20
Closest x: 208
Closest x binary: 11010000
```

The picture above is the output result of two input y values of 550 and 800, which are 104 and 208, which makes y=104*2.4+300=549.6 and y=208*2.4+300=799.2 the closest values to the inputs.

Algorithm: To find the corresponding x, start with initializing the guessing number x, secondly, utilize the successive approximation and binary search concept with variables such as upper, lower and mid, and finally the latest result mid variable passes to the output x.

2. Verilog code and RTL simulation

('hw1.v' Verilog code file is included in the submit area)

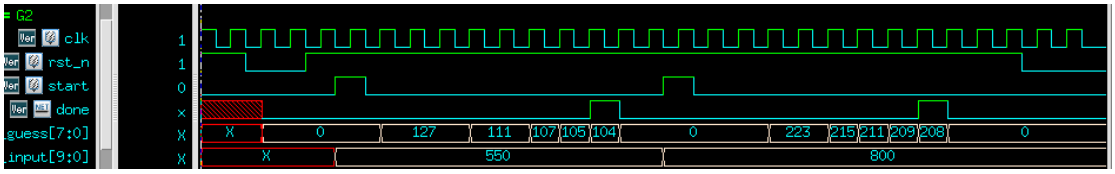


The picture above is the simulation result of RTL coding, including inputs of clk with a period of 10ns, rst_n, start, state[1:0], done, y_input[9:0] and an output x_guess[7:0].

Algorithm: The algorithm is similar to the C code and adds additional states inclusive of IDLE, CALC and FINISH to form a FSM. The initial state IDLE waits for the start signal to pull up, x_guess is reset to 0 and when start is pulled up to 1, y_input is subsequently read in. The second state CALC then do the calculations, if the calculations are not done then jump back to itself, otherwise jump to FINISH state, and done is ultimately pulled up to 1 and the final x_guess represents the answer.

3. Synthesized netlist and Gate-level-simulation

('hw1_syn.v' synthesized code file is included in the submit area)



The picture above is the simulation result of sythesized netlist hw1_syn.v

The maximum operating speed is period = 6ns

Area Report

```
Number of ports:                          362
Number of nets:                          1716
Number of cells:                         1303
Number of combinational cells:           1242
Number of sequential cells:                26
Number of macros/black boxes:               0
Number of buf/inv:                        318
Number of references:                      71

Combinational area:               5833.900868
Buf/Inv area:                      681.609622
Noncombinational area:             430.416008
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  6264.316876
```

1. The total area shown in the ‘hw1_syn.report’ file is 6264.316876 um^2.
2. The number of final gate count is 6264.316876 / 2.8224 = 2219.5 .

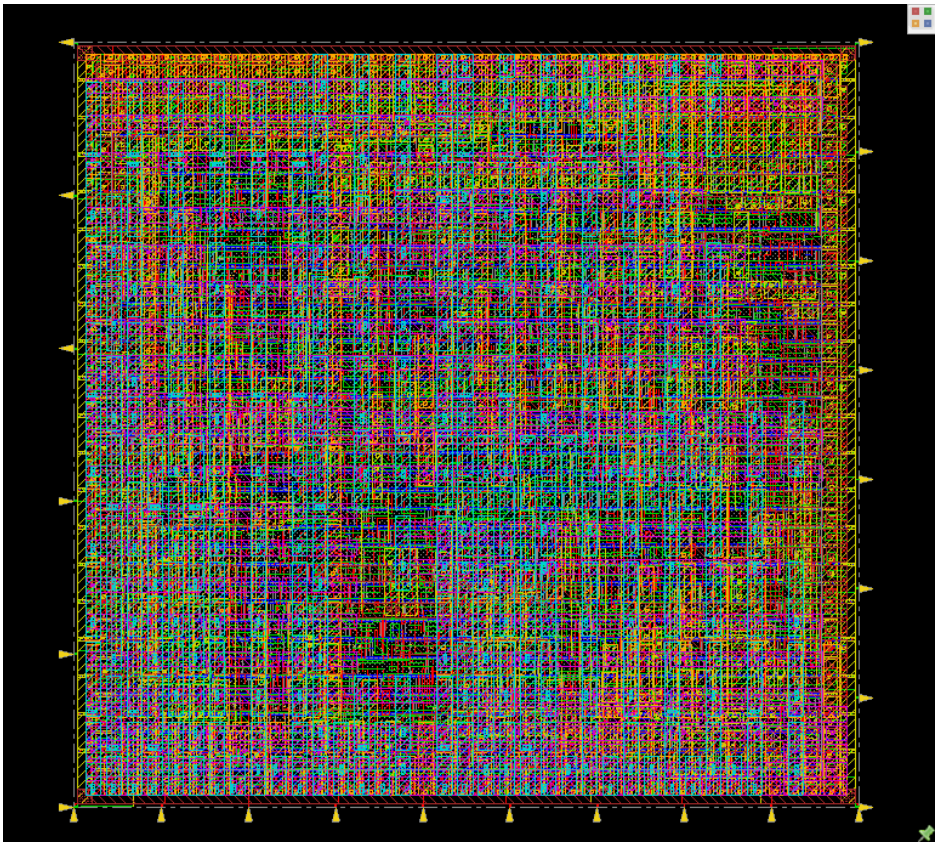
Power Report

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)
register	3.3694e-02	6.0592e-04	1.1759e+06	3.5476e-02	(33.55%)
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)
combinational	2.6790e-02	1.6128e-02	2.7361e+07	7.0279e-02	(66.45%)
Total	6.0484e-02 mW	1.6734e-02 mW	2.8537e+07 pW	0.1058 mW	

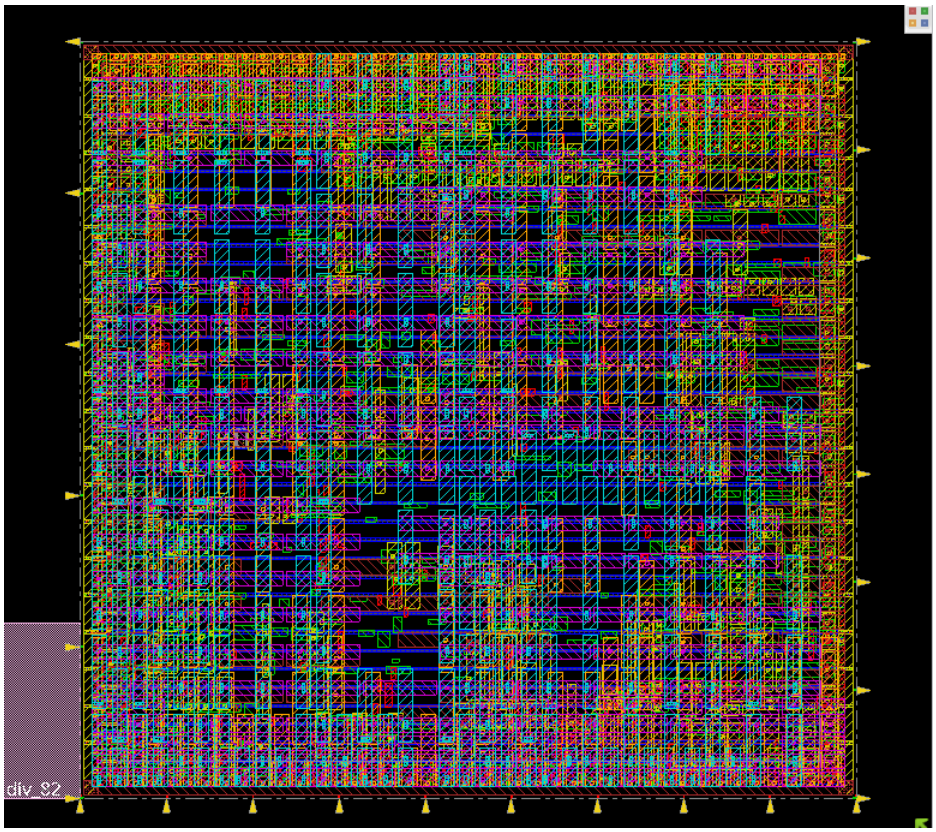
1. Cell Internal Power = 60.4845 uW (78%)
2. Net Switching Power = 16.7336 uW (22%)
3. Total Dynamic Power = 60.4845 + 16.7336 = 77.2181 uW (100%)
4. Cell Leakage Power = 28.5369 uW
5. Total Power = 0.1058 mW

4. Layout generation

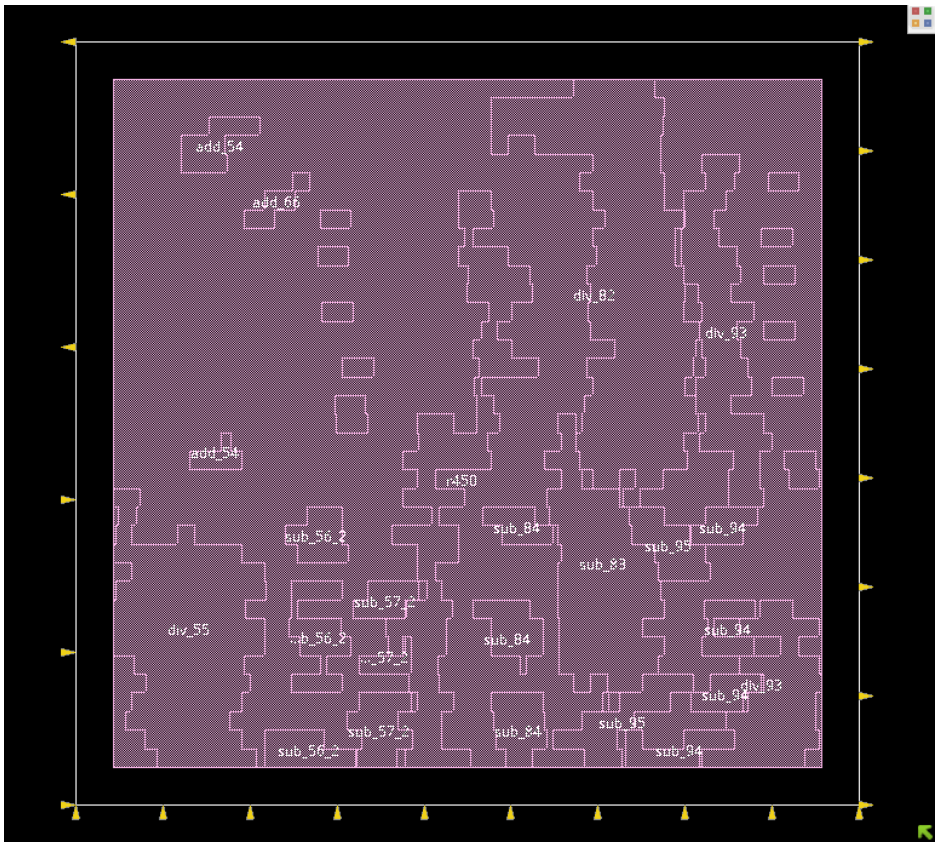
1. Physical view



2. Floorplan view



3. Amoeba view



Area Report

Layout total area = 6044.170 um^2.

```
innovus 1> report_area
    Hinst Name       Module Name                    Inst Count          Total Area
--------------------------------------------------------------------------------
functional_unit                                          1202            6044.170
 add_54              functional_unit_DW01_add_4            10             139.709
 add_66              functional_unit_DW01_inc_2             7              69.149
 add_93              functional_unit_DW01_inc_1             7              74.088
 add_97              functional_unit_DW01_inc_0             7              69.149
 div_55              functional_unit_DW_div_uns_2          85             402.192
 div_82              functional_unit_DW_div_uns_10        166             590.587
 div_93              functional_unit_DW_div_uns_0          98             450.878
 r450                functional_unit_DW_div_uns_3          88             408.542
 sub_56_2            functional_unit_DW01_sub_6            15             170.050
 sub_57_2            functional_unit_DW01_sub_5            15             170.050
 sub_83              functional_unit_DW01_sub_7            95             306.936
 sub_84              functional_unit_DW01_sub_3            15             170.050
 sub_94              functional_unit_DW01_sub_1            14             169.344
 sub_95              functional_unit_DW01_sub_0            18             176.400
```

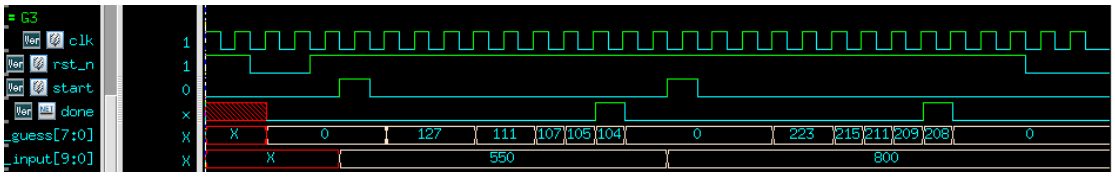
Power Report

```
Total Power
--------------------------------------------------------------------------------------------------
Total Internal Power:        0.64205708            51.7831%
Total Switching Power:       0.57938851            46.7288%
Total Leakage Power:         0.01845083             1.4881%
Total Power:                 1.23989642
--------------------------------------------------------------------------------------------------
Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1228.34MB/2775.43MB/1228.37MB)

Begin Creating Binary Database
Ended Creating Binary Database: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1744.95MB/3553.85MB/1744.96MB)

Output file is .//functional_unit.rpt
```

1. Total Internal Power = 0.64206 mW
2. Total Switching Power = 0.579389 mW
3. Total Leakage Power = 0.018451 mW
4. Total Power = 1.239896 mW

5. Post-layout simulation

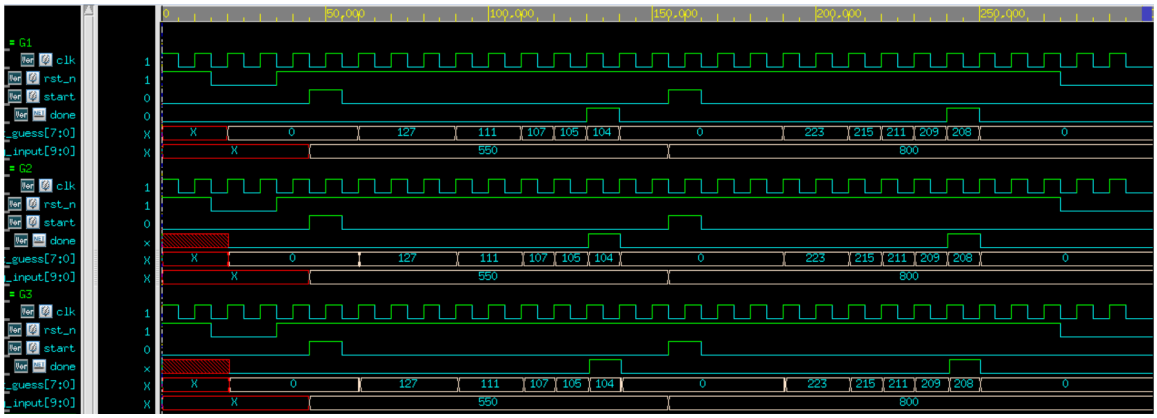
('hw1_apr.v' post-layout netlist file is included in the submit area)



The picture above is the simulation result of post-layout netlist hw1_apr.v

The maximum operating speed is period = 6ns

6. Waveform comparison



1. Done is not shown during the first two clock periods of gate-sim and post-sim.
2. Noise emerged during gate-sim and post-sim.