#HW2 Cell Based DCO Design summary report

- **Group member**
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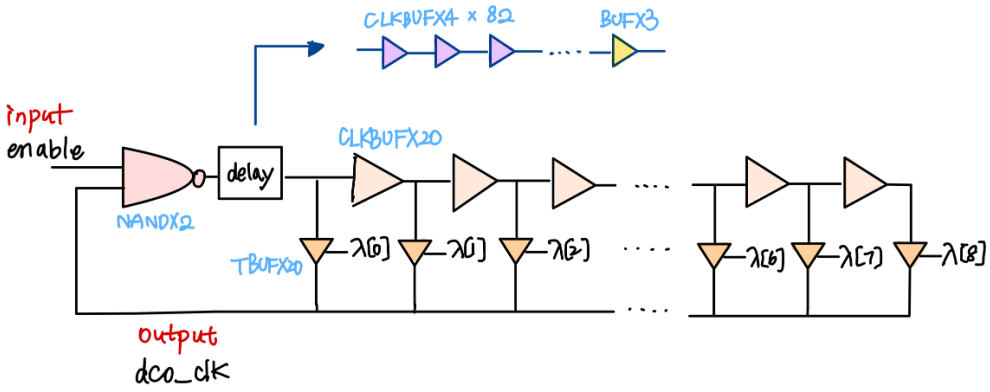
- **Contribution**
  1. 林士登 - Verilog code, Testbench, Synthesis, Layout testing and Simulations, Final summary report
  2. 陳立珩 - Verilog code, Testbench, Synthesis, Layout testing and Simulations

- **Outline**
  1. DCO Architecture
  2. DCO waveform and frequency comparison (pre-layout / post-layout)
  3. Gate-level synthesis / Gate simulation report
  4. Layout generation and analysis

- **Results and Analysis**

1. DCO Architecture



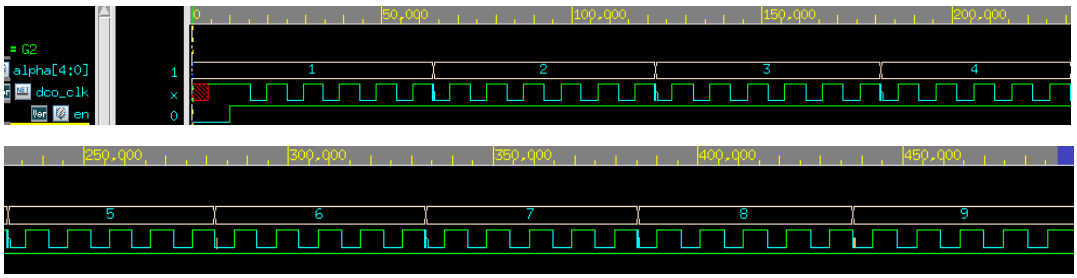
The graph indicated above represents our main DCO architecture. The gates used in the Verilog code are referred to the TSMC 180nm process standard cell library, including NAND2X2, the long delay block with 82 CLKBUFX4 and a BUFX3, and the major buffer chain CLKBUFX20 and a series of tri-state buffers TBUFX20.

Additionally, the binary to thermometer converter is designed to be a MUX. Input alpha code from decimal 1 to 9 is required to generate the corresponding 9 bit lambda code, which is responsive for the input of the tri-state buffers.

2. DCO waveform and frequency comparison

('DCO.v' and 'DCO_tb.v' code file is included in the submit area)

Pre-sim

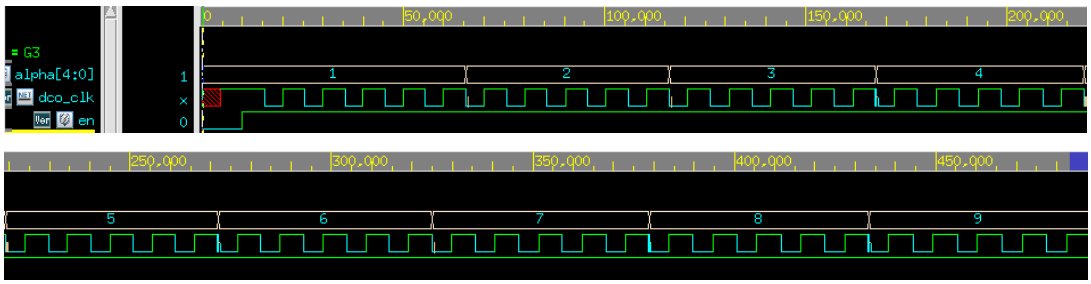


① The dco_clock period is design to be **9.626 ns** to **10.644 ns**.

② The corresponding frequency range is **93.950 MHz** to **103.885 MHz**.

③ The timing resolution is $\frac{10.644-9.626}{8} = \mathbf{0.12725\ ns}$.

Post-sim



① The dco_clock period is design to be **9.990 ns** to **11.040 ns**.

② The corresponding frequency range is **90.736 MHz** to **100.100 MHz**.

③ The timing resolution is $\frac{11.040-9.990}{8} = \mathbf{0.13125\ ns}$.

The reason why we designed the pre-layout dco_clock period to be smaller is because the gate delay might increase slightly in the post-layout stage.

Alpha Code (decimal)	dco_clk Period (ns)	dco_clk Frequency (MHz)
alpha = 1	9.99000	100.1001
alpha = 2	10.12125	98.80203
alpha = 3	10.25250	97.53719
alpha = 4	10.38375	96.30432
alpha = 5	10.51500	95.10223
alpha = 6	10.64625	93.92979
alpha = 7	10.77750	92.78590
alpha = 8	10.90875	91.66953
alpha = 9	11.04000	90.57971

3. Gate-level synthesis / Gate simulation report

Area Report

```
Combinational area:                812.145611
Buf/Inv area:                      532.728007
Noncombinational area:             184.161604
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                   996.307214
Total area:                 undefined
```

① The total area shown in the 'DCO_syn.report' file is 996.307214 um^2.

② The number of final gate count is 996.307214 / 2.8224 = 353 .

Power Report

```
                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad           0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory           0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box        0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network    0.0000           0.0000              0.0000             0.0000  (   0.00%)
register         0.0000           0.0000              0.0000             0.0000  (   0.00%)
sequential       0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational    0.4618           0.1639          7.9173e+06             0.6337  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total            0.4618 mW        0.1639 mW       7.9173e+06 pW          0.6337 mW
```

① Cell Internal Power = 461.7958 uW (74%)

② Net Switching Power = 163.9404 uW (26%)

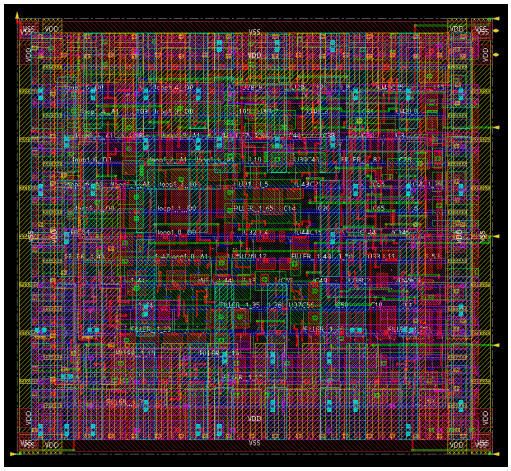
③ Total Dynamic Power = 461.7958 + 163.9404 = 625.7363 uW (100%)

④ Cell Leakage Power = 7.9173 uW

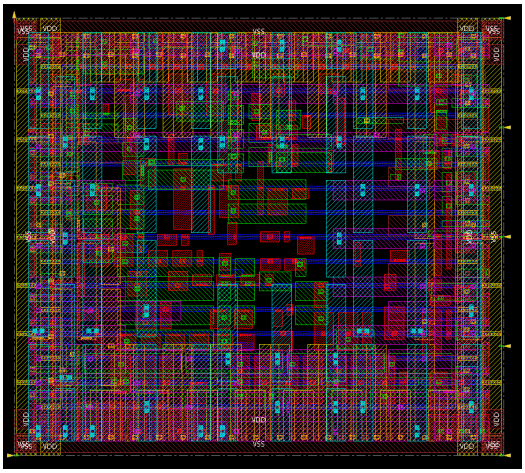
⑤ Total Power = 0.6337 mW

4. Layout generation and analysis

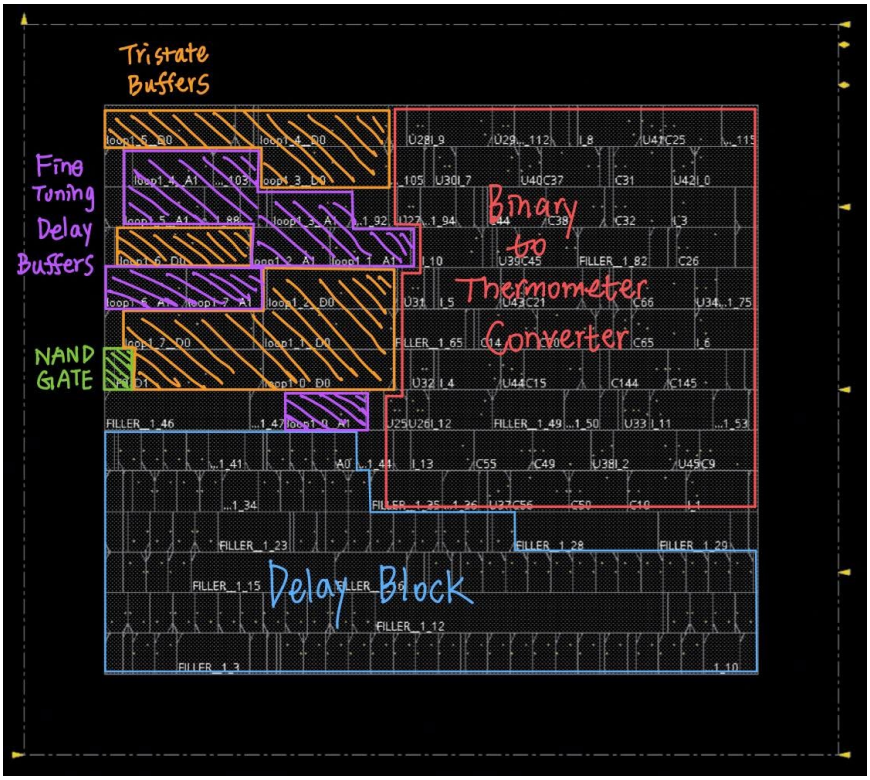
1. Physical view



2. Floorplan view



3. Layout block



Area Report

Layout total area = 996.307 um^2.

```
innovus 4> report_area
    Hinst Name       Module Name          Inst Count            Total Area
--------------------------------------------------------------------------
DCO                                            158               996.307
```

Power Report

```
Total Power
--------------------------------------------------------------------------------
Total Internal Power:        0.03312047           69.2942%
Total Switching Power:       0.01014401           21.2232%
Total Leakage Power:         0.00453239            9.4826%
Total Power:                 0.04779687
--------------------------------------------------------------------------------
Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=939.45MB/2345.54MB/939.48MB)

Begin Creating Binary Database
Ended Creating Binary Database: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1452.60MB/3115.96MB/1452.62MB)

Output file is .//DCO.rpt
```

1. Total Internal Power = 0.03312047 mW
2. Total Switching Power = 0.01014401 mW
3. Total Leakage Power = 0.00453239 mW
4. Total Power = 0.04779687 mW