

# Hardware Isolation Mechanisms for Security Improvement in FPGAs

## ABSTRACT

Field Programmable Gate Arrays (FPGAs) platform security management continues to be a strong area of concern despite recent increased adoption and integration of FPGAs into commercial scale cloud computing systems. One of the technical problems in the FPGA security management area has been the lack of hardware primitives to support multi-tenancy while enforcing proper domain isolation. In this paper, we present a tutorial on recent progress that has been made to address this issue. Specifically, we present hardware isolation mechanisms that can be used to enable domain separation on FPGA based systems. We demonstrate the viability of these mechanisms through a software-hardware codesign implementing a simple TLS/SSL encryption application.

## CCS CONCEPTS

•Security and privacy →Embedded Systems Security; Hardware Security Implementation; •Hardware →Reconfigurable Logic Applications;

## KEYWORDS

FPGA Security, Hardware Isolation, IP Containerization, CAPSL

## 1 INTRODUCTION

Many of today's critical embedded systems are increasingly relying on FPGA-based SoCs because of the useful balance between the performance, scale, flexibility, and rapid time to market they provide. This was recently exemplified with the recent Audi announcement that its 2018 A8 world's first Level 3 autonomous driving system will feature Altera's Cyclone FPGA SoCs for object and map fusion processing tasks. Though, it's not just in embedded systems space where we are seeing accelerated adoption of FPGA platforms, as they are also being continuously integrated into commercial scale cloud computing systems and data centers as evidenced by Amazon recent announcement of providing cloud compute instances with FPGAs (EC2 F1).

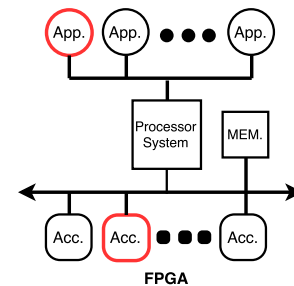
This increased adoption of FPGA into commercial scale cloud computing systems has highlighted the issue of FPGA's lack of hardware primitives, conceptually similar from a security perspective to a CPU's IO memory management unit (IOMMU), to support multi-tenancy while enforcing proper domain separation among the tenants (i.e. multiple applications utilizing the same FPGA) [3], [1], [2]. This lack of native support for isolation creates security

concerns where, since FPGA accelerators tend to run with full hardware access, a single accelerator vulnerabilities can be exploited through traditional system software stacks or if malicious, can bring down a shared compute host [3].

An effective solution to the problem of lack of proper domain separation on FPGAs should be able to enable scaling of security across a range of system parameters, such as power and performance, without significant drop in coverage. We believe and intend to demonstrate that this can only be achieved through some form of combination of measures that protect against hardware vulnerabilities directly at the hardware level and measures that enforce domain separation at the software level.

In this paper, we look at a set of research works that individually attempted to address the problem of lack of isolation support on FPGAs. We demonstrate how certain elements of these works can be put together to provide an effective and comprehensive solution to this problem. Through a tutorial, we demonstrate the viability of this solution through a real-world software-hardware codesign application which implements a simple TLS/SSL encryption application. The remainder of this paper is organized as follow: Section 2 starts by describing the specific use case scenarios and security concerns this method addresses. Section 3 gives an overview of research works that form the basis of our comprehensive solution. Section 4 and Section 5 conclude the paper with a tutorial demonstrating how a combination of the discussed approaches can be used to provide proper domain isolation on FPGA platform.

## 2 THREAT MODEL



**Figure 1: Threat Model: The adversary controls the FPGA SoC and can execute malicious code (non-trusted application + accelerator in red) remotely.**

The illustration of our threat model in Figure 1 shows the use case scenario our approach targets. We assume an adversary who can introduce hardware trojans in the IPs during development (supply chain attack). We assume this adversary has remote access to the FPGA system-on-chip (FPGA SoC) which contains some of the malicious IPs and is also aware of the trojans activation mechanisms

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. Copyrights for components of this work owned by others than ACM must be honored. Abstracting with credit is permitted. To copy otherwise, or republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee. Request permissions from [permissions@acm.org](mailto:permissions@acm.org).

(Trojans are not active and can only be activated externally by executing some malicious input for ex.). We assume the adversary may also control all the system software including the operating system. Our goal is to prevent unauthorized data access and modification by shielding non-trusted IPs execution into a hardware sandbox and providing secure isolated regions.

### 3 HARDWARE ISOLATION MECHANISMS

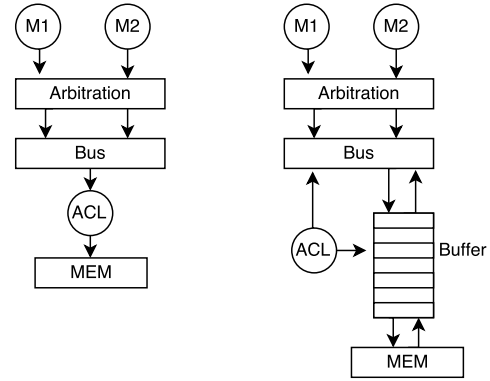
This section discusses current techniques that are employed to enforce hardware isolation on FPGAs. This list is by no means exhaustive and it is beyond the scope of this paper to discuss these techniques in greater details. The interested reader is encouraged to refer to cited works.

#### 3.1 Reference Monitors

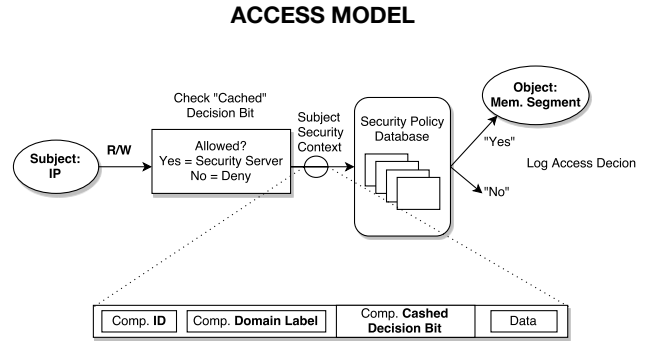
In this approach, a hardware module or a microcontroller based firmware-upgradable module is used to monitor and enforce authorized sharing of system resources among cores. Memory-access security policies are expressed in a specialized language, and a compiler translates these policies directly to a circuit (or a microcontroller) that enforces the policies. The circuit is then loaded onto the FPGA along with other components of the system.

There are many research efforts with some relation to this approach, but to the best of our current knowledge, works in [10] and in [9] are the only work with similar goals that come close to ours here. In their work, they designed and implemented a reconfigurable reference monitor (RM) which implements an access control list (ACL). They then integrated the reference monitor into the on-chip peripheral bus (OPB) and used it to regulate access to the memory and peripherals. Memory and peripherals accesses go through a reconfigurable monitor's access control list [3]. The access control list associates every object (memory ranges for ex.) in the system with a list of principals (IP cores) with the rights of each principal to access the object[3]. In their implementation, each object access has to be computed by the reference monitor's ACL at runtime. The decision is either granted access or denied access. Since this access model can create potential memory performance issues in large memory applications, they proposed a mechanism in which a buffer is used to hold the data until the ACL grants approval of the legality of the request [11]. Figure 2 illustrates the implementation. For example, in case of a write, the data to be written is stored in the buffer until the ACL grants the approval, at which time the write request is sent to the memory [11].

Authors in [8] observed that in Huffmire et al. access model implementation if you had consecutive and repeated memory access from the same "principal" to the same "object", each one of these requests would still have to go through the reference monitor's computation. This can potentially create performance issues in large designs. These issues can be avoided by adding the capability to remember access decisions. Authors in [8] built upon this observation and proposed an improved implementation of this architecture by adding capability to remember access decisions to allow them to be administered at run-time without re-computations. Figure 3 shows their proposed access model.



**Figure 2: Access Model Implementation.** On the left, there's no "caching" mechanism. On the right, a buffer is used to hold the data while access rights are being looked up.



**Figure 3: Improved Access Model Implementation.**

Both of these techniques follow a similar design flow. Systems components are defined and implemented using hardware synthesis tools such as Xilinx's Vivado or Xilinx's XPS. The hardware-enforced ACL core is generated by some policy compiler and it's then integrated with the rest of the system components similar to adding a standard custom IP to your design [CITAT],[CITAT]. In some instances, however, there can be compatibility issues. Sometimes standard integration of the ACL core can be complicated with the fact that some security-relevant attributes may not be directly available as parameters or easily derived from available parameters. For example, the current version of the AXI Interconnect IP core API available in Vivado 2016 does not present a component ID as a parameter. In situations like these, it's up to the application designer to build their own custom OPB (or AXI interconnect) IP which directly integrates this ACL security functionality.

Authors in [5], [13], [6] observed that the above described techniques assume a "trusted" reference monitor to enforce the security policies and with no mechanism through which the platform itself can authenticate the authority of the reference monitor before it administers an access policy decision. The security concern here is that an attacker could conduct a man-in-the-middle attack on the system by inserting a malicious circuit inside the only authority entrusted with administrating shared resource access decisions. To

mitigate this, they proposed an improved implementation of the reference monitor which combines the monitoring approach with a “proof-carrying hardware” concept. Their approach consisted of using a consumer-producer approach, where a consumer specifies a desired functionality of the memory access monitor and sends this specification to the producer and the producer synthesizes this information into a bitstream [5]. The producer re-extracts the logic function from this bitstream and, together with the original specification, computes some miter function (which outputs an error flag if the specification and implementation differ for at least one input vector) [13]. This proof of reference monitor correctness is then generated along side with the bitstream and is sent to the consumer. The latter verifies the proof, and in case of success partially reconfigures the monitor with security policies [13]. The consumer verifies the proof of correctness from the producer by extracting the monitor’s logic function from the bitstream and forms a miter in conjunctive normal form in the same way as the producer, but with the original specification. This new miter is compared to the producer’s miter and if they both match, the implementation is accepted and the monitor is accepted. The monitor is rejected if the the miters do not match [13], [6].

### 3.2 OS-Enforced Security: Zynq FPGA TrustZone

In this approach, systems developers rely on an embedded operating system to provide system security services. Security features provided include, but are not limited to, confidentiality and integrity protection of the external memory containing the application code and data.

A recent example of this approach is the ARM TrustZone security architecture currently available to Zynq-7000 SoCs. In this example, the Xilinx Zynq-7000 processor system supports ARM TrustZone technology in both the PS and PL domain. The ARM TrustZone architecture makes trusted computing within the embedded world possible by establishing a trusted platform, a hardware architecture that extends the security infrastructure throughout the system design. Instead of protecting all assets in a single dedicated hardware block, the TrustZone architecture runs specific subsections of the system either in a “normal world” or a “secure world.”

In the Zynq-7000 AP SoC, a normal world is defined as a hardware subset consisting of memory regions, L2 cache regions, and specific AXI devices. The Zynq-7000 AP SoC supports ARM TrustZone technology in both the PS and PL domains of the device. The PS provides a set of configuration registers related to TrustZone support for custom IPs. These configuration registers are then dynamically programmed by the software during execution. All slave IP cores instantiated in the logic can be individually assigned a Secure or Non-Secure designation. For Xilinx slave IP cores, Secure/Non-Secure configuration can be statically designated at the AXI interconnect level during system creation process.

Figure 2 shows a simplified example of how to secure your design sensitive components from illegal hardware access using Zynq-7000 AP SoC TrustZone technology

In this example, also available in [], on the hardware level the PL domain uses two custom master IP cores:

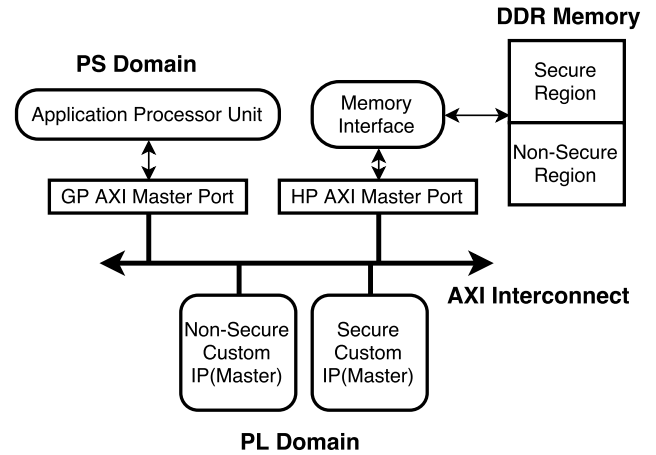


Figure 4: Improved Access Model Implementation.

- **Secure Custom IP:** This performs Secure read/write transactions to DDR using the HP slave port in the PS. It is also connected to the Application Processor Unit (APU) via a GP master port for register configuration.
- **Non-Secure Custom IP:** This is used to perform read/write transactions from/to the PS DDR upon requests from the external world. It performs Non-Secure read transactions to DDR using an HP slave port. Configuration of this IP is done by the PS processor through a GP master port.

Upon power-on, the PS processor initializes both custom IPs, configures registers to establish Secure and Non-Secure regions in DDR memory, and transfers private data/instructions to the Secure DDR region. After initialization and upon receiving a data request from the external interface, the Non-Secure custom IP first copies the data from the external interface to the Non-Secure region of DDR memory. It then interrupts the PS processor, which commands the Secure custom IP to perform the appropriate data computations using its private data/instructions in conjunction with the data just copied to the Non-Secure region of DDR memory. After computation is completed, Secure custom IP puts the computed data into the Non-Secure DDR region and interrupts the PS processor to command the Non-Secure custom IP to start transferring data from the requested location.

On the software level, application processes (and their IPs) with non-secure status designation execute in memory space separated from processes with secure status designation. When a user process running in the Non-Secure world requires Secure execution, it makes a request to the Non-Secure kernel to enable the TrustZone Secure Monitor to transfer execution of the process to the Secure world. The Secure Monitor mode links the two zones and acts as a gatekeeper to manage program flow between them.

To ensure integrity of the TrustZone software, Zynq-7000 provides a secure boot flow; where the on-chip BootROM code starts the whole security chain by ensuring that first-stage bootloader (FSBL) is signed and verified.

### 3.3 Hardware Sandboxing

The approach of utilizing hardware sandboxes for isolating and identifying potential malicious IP-internal circuits provides a flexible design process for systems designers and integrators. Similar to discussed approaches, a sandbox isolates IP by partitioning the hardware design to a trusted secure region and a non-trusted environment contained within the sandbox. It supports the following security policies: Isolation policy that limits the IP to only allowable interactions, Containment policy that minimizes the damage caused by a malicious component, and Integrity policy that enforces authorized data accessibility and modifications. These policies are implemented through two distinct but complementary mechanisms: *Complete Mediation*, and *Resources Virtualization*.

Hardware sandboxing allows the placement of interface-level behavioral monitors, collected in a “*Checker*” component that implements the *Complete Mediation* mechanism by checking every interaction made by the user IP to the system and only authorizing allowable interactions as specified by the IP interface specification.

The “*Sandbox controller*” implements the *Resources Virtualization* mechanism by providing both virtual memory buffers (local to the user IP) and virtual IO access for critical resource protection. It also generates a “*virtual resources controller*” in case there are more virtual resources competing for a single physical resource. “*Status registers*” are used to monitor and log the user IP security status. This is useful in that a subverted IP can’t launch a denial-of-service attack by repeatedly making illegal requests. Also, this can be used to log the user IP if it triggers a Trojan at run-time for example. This information can then be used to blacklist some vendors from the integrator’s list of contractors.

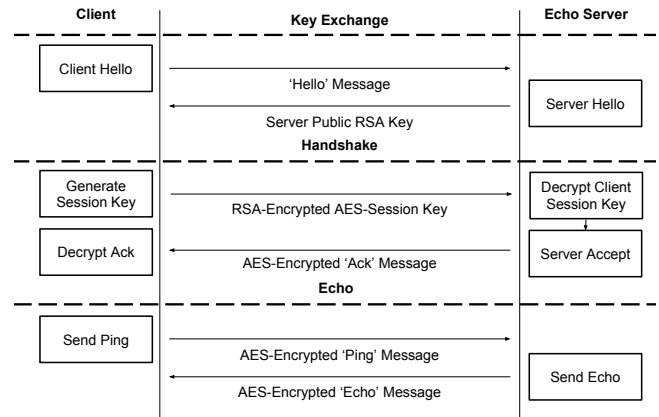
## 4 SECURITY CRITICAL EXAMPLE APPLICATION

In this section, we introduce an example application to demonstrate the various hardware isolation methods discussed above.

### 4.1 Overview

We intend to demonstrate the steps required to ensure the protection of a general security-critical system design with an SoC system providing reconfigurable fabric along with a co-processor. The discussed isolation methods enforce security at the OS/PS level down to the hardware IP interface level. Thus, our demonstration application includes process level applications running on the processing system while hardware is utilized for acceleration cores. The system requires a security critical application such an application requiring sensitive keys to be handled at the software level while relying on hardware for accelerating cryptographic functions.

**4.1.1 Secure Echo Server Process:** We utilize an echo server that encrypts client communications with a session key established through a simplified TLS/SSL handshake. This system setup assumes the server to be run on the SoC device targeted for protection while the client is run on a remote machine. The SoC hosting the echo server is designed to run on a Zynq SoC, with the zynq processor hosting a Linux OS and utilizing FPGA area for cryptographic functions. The echo server process and complementing



**Figure 5: Baseline Behavior for Client and Echo Server**

*In its initial state, the server process listens on a specified network IP address and port awaiting a client connection. Upon receiving a connection, a handshake is initiated as the server immediately shares an RSA public key. A session key computed by the client is received by the server encrypted with its public RSA credentials. Deciphering this session key allows subsequent communications to be secured, namely the server’s acknowledgement of a successful handshake, the client’s message, and finally the server’s echoed message.*

client process are implemented as Python programs. We used Xilinx’s Petalinux tool for generating the design images required to boot a Linux OS and mount the filesystem. We implemented our system on a Digilent Zybo [IT MIGHT NOT BE BIG ENOUGH for AES + RSA]...

**4.1.2 Hardware Accelerated Encryption Engine:** The handshake requires the use of both symmetric-key and public-key algorithms, as a symmetric-key (used as session key) is generated from utilizing a asymmetric-key to encrypt and publically transmit the session key. AES and RSA are commonly used to meet these requirements. As these can be computationally expensive with larger key sizes, one standard application of hardware acceleration is for performance boosts with cryptographic functions. To provide our demo system with a hardware component, an AXI-bus enabled IP core is used to accelerate the AES and RSA algorithms used by the echo server process. The PS and PL interaction is detailed in [NEED DIAGRAM].

Upon requiring the AES or RSA cores during execution, data is first written to the appropriate input data registers for each IP. After a successful write of input data, an enable signal is written to a control register to signal the IP core to perform the encryption/decryption. A set of output data registers are assigned to each core along with a status register to inform the software process of a complete computation.

The hardware cores were implemented as Vivado IP cores and exposed by supplying an AXI-bus interface for reading inputs and writing outputs to DDR memory. This is accessible by default from the OS as Petalinux images include kernel drivers for exposing DDR memory under the OS’s ‘/dev/mem’ filepath. The memory

blocks for the cryptographic core are accessible via their device-tree specified address. This will be revisited later in [POSSIBLY ANOTHER SECTION TO GO DEEP INTO DETAIL].

## 4.2 Security Vulnerabilities

Our application was designed to include vulnerabilities that could be found in designs that include software processes and hardware accelerators handling sensitive information without security measures. An operating system lacking the ability to restrict executions on sensitive data to isolated processor environments and verify process permissions for secured memory space creates potential points of attack for malicious processes. With the hardware design community's growing adoption rate of third-party IP cores, there are a multitude of infiltration points within the development and manufacturing process with which malicious parties have been able to exploit.

[General Vulnerability Descriptions?]

To exploit the vulnerabilities mentioned, we have included a non-secure process and hardware trojan for the purpose of demonstration and providing a metric of system security strength. It should be noted that it is recognized the server/client handshake is missing vital components of a true TLS/SSL scheme such as certificate based verifications performed by both client and server. However, the scope of this work omits the undertaking of securing the network layer.

*4.2.1 Software Threat Insertion:* [SECTION ABOUT A NONSECURE PROCESS INTENDED TO ACCESS SENSITIVE DATA]

We have implemented a simple C program to run alongside the echo server. It attempts to access the memory of the server process to access the sensitive keys it manages. In addition, we can attempt the access of driver memory space to read and write to the hardware accelerators.

*4.2.2 Hardware Threat Insertion:* Our encryption engine is a prime candidate for inserting a malicious circuit as it will have access to sensitive encryption key data. As our application performs a simple handshake and utilizes both AES and RSA algorithms, we can leverage the Trust-Hub.org repository of hardware trojans for AES128 and BasicRSA. Both AES128 and BasicRSA trojan classes contain variations of activation methods, from always-on trojans to internal condition triggers. We sample the set of available AES128 and BasicRSA trojans and select the variations shown in in Table [SMALL TABLE OF TROJANS]. This subset provides our demo system with a range of malicious behaviors originating from hardware circuits that are typically difficult to detect without the application of some security methods.

## 5 IMPLEMENTING ISOLATION

In this section, we discuss implementation details regarding the steps of applying the isolation methods to our security critical application. Each of the methods has unique strengths and a more comprehensive security profile can be realized upon implementing each in conjunction.

To discuss the implementation in a meaningful way, we discuss each of the isolation methods in the order they would appear in a bottom-up system development process. We begin with isolating

the cryptographic accelerators in hardware and proceed to configuring a secure execution environment. With our secure process utilizing hardware-accelerated encryption, CAPSL is utilized to secure the encryption engine and enforce the integrity of its behavior. This system suits the implementation of the discussed isolation methods with the inclusion of points of attack in both software and hardware.

### 5.1 CAPSL

To enforce a deeper security profile in our system design, we utilize hardware sandboxing to isolate the untrusted encryption cores. We leverage the secure development tool presented in [12], the Component Authentication Process for Sandboxed Layouts (CAPSL), as it supplies automation for generating hardware sandboxes, allowing for a streamlined integration of questionable components into systems.

*5.1.1 Design Flow.* A specification defining the interface and its behavior is required for each IP in order to formally model the IP and generate automata objects of each policy. The set of automata produced from all policies is used as a behavioral monitor within the sandbox. The specification enables the flexibility to define behavior at varying levels of abstraction and varying degrees of completeness. To elaborate, specification might contain partial interface definitions and/or behaviors abstracted through additional computation logic. To capture security properties, CAPSL adopts the Interface Automata (IA) formalism of De Alfaro and Hetzinger [4] along with a subset of the Properties Specification Language (PSL), Sequential Extended Regular Expression (SERE) [7]. As a baseline specification, only interface layouts are required (IP interface inputs, outputs). Beyond this, any combination of IA-based descriptions of allowed behavior, explicitly denied interactions defined as SERE statements, and computational logic is allowed.

Implementing a hardware sandbox for our demo system requires the specification of our untrusted hardware components. The specification files for AES and RSA cores are detailed in Figure 6 and Figure 7, respectively. Along with the required interface layout definition, the specifications for both AES and RSA utilize SERE statements in conjunction with additional computational logic to provide explicitly denied interactions. More specifically, the specifications are utilizing additional logic for abstracting the SERE specifications for detecting known trojan triggers. The RSA specification also utilizes the IA-based description of allowed behavior to define how the IP shares its current state. With our specification files providing policies to isolate undesired behavior, we can simply execute CAPSL to obtain a sandbox IP containing our hardware cores.

Taking a brief look at CAPSL's internal generation process, the IP models resulting from specification are first subjected to an optimization phase. The sandbox design leverages the IA composition operation to provide compatible and secure interfaces between the IP and the rest of the system through the sandbox. Applying the operation requires the environment (the IP in our case) not to perform illegal actions, i.e. actions that the sandbox and therefore the rest of the system doesn't expect. This means that interfaces are assembled only if they are compatible, resulting in a new composed interface. With all policies represented as Interface Automata with

```

// AES128.config - CAPSL Configuration File
// IP Targets: Trust-Hub AES Trojans T300, T400, T500, T600, T700, T800, T900, T1000
AES.def( // AES 128 Interface Layout and Expected Interactions
  reset      : input,
  key        : input-vector(AESKeySize),
  state      : input-vector(AESKeySize),
  out        : output-vector(AESKeySize),
  transitions() // No transitions are required
)
logic.def( // Additional Computational Logic and SERE Restrictions
  AESKeySize = 128, // AES KeySize
  logic0 : state == x"FFFFFFFFFFFFFFFFFFFFFFFF", // T400, T600 trigger input
  logic1 : state == x"00112233445566778899AABBCCDDEEFF", // T700, T1000 trigger case

  logic2 : xmit_dataH == x"3243F6A8885A308D313198A2E0370734", // T500, T800 trigger sequence
  logic3 : xmit_dataH == x"00112233445566778899AABBCCDDEEFF",
  logic4 : xmit_dataH == x"00000000000000000000000000000000",
  logic5 : xmit_dataH == x"00000000000000000000000000000001",

  counter1 : counter { // T900 Trigger counter
    on: event(out),
    start: x"00000000000000000000000000000000",
    end: x"FFFFFFFFFFFFFFFFFFFFFFFF"
  }

  prohibited( // Illegal conditions (SERE)
    {logic0 | logic1 | counter1}, // Restrict T400, T600, T700, T900, T1000 trigger cases
    {logic2 | logic3 | logic4 | logic5} // Restrict T500, T800 trigger sequence
  )
)

```

Figure 6: AES128.config - CAPSL Specification

CAPSL, the composition operation can supply an avenue for reducing the policy automata set size through merging automata with consideration for the environmental assumptions of it.

The resulting optimized set of policies is to be translated to a reference monitor. Since CAPSL translates from a formal model, it is possible to insert a variety of target IP implementations for generating the sandbox as an IP. Using a VHDL flow as a result of leveraging Trust-Hub’s RTL level trojan implementations, the "Checker" is generated by one-hot encoding of the monitoring automata as VHDL statements which capture the expected behavior of the IP. The checker module is combined together with virtual resources (BRAMs, SLRs, etc.) to generate the core logic which governs the sandbox. The generated core logic is then combined with a sandbox controller (acting as a router for all signals between interfaces and checker) to conclude the sandbox generation. The controller consists of the sandbox interface (composed with the non-trusted IP interface), physical interface, some status registers, and a multiplexer which acts as a switch to either allow IP interactions to continue or to invalidate them.

Upon finishing, the tool outputs the components of the sandbox as VHDL source files which can be immediately imported to design and synthesis tools for integration into the target system. For our demonstration system, we utilize Xilinx Vivado to design and synthesize the block design as seen in Figure [PS PL INTERACTION DIAGRAM]. Using a Digilent Zybo FPGA, with dual Zynq ARM Cortex A9 processors, we allot one processor for hosting an OS, configure the ethernet physical interface, and tie the hardware accelerator cores to the PS via an AXI Interconnect.

I think we use Petalinux still even with TRustzone?? Whatever we do, mention it here and transition to next section.

```

// BasicRSA.config - CAPSL Configuration File
// IP Targets: Trust-Hub BasicRSA Trojans T100, T200, T300, T400
BasicRSA.def( // AES 128 Interface Layout and Expected Interactions
  ds      : input,
  ready   : input,
  reset   : input,
  inExp   : input-vector(RSAKeySize),
  inMod   : input-vector(RSAKeySize),
  inData  : input-vector(RSAKeySize),
  cypher  : output-vector(RSAKeySize),
  transitions(
    s0:ds>s1, // ds asserted to signal inputs ready
    s1:!ready>s2, // ready goes low
    s2:!ds>s3, // ds goes low
    s3:ready>s0 // ready asserted when finished and prepared for next inputs
  )
)
logic.def(
  RSAKeySize = 32, // RSA KeySize
  logic0 : cypher == inExp, // Checking for plaintext key leaks (T100, T200, T300)
  logic1 : inData == x"44444444", // Checking for T100 trigger case
  logic2 : inData == x"01FA0301", // Checking for T200 trigger case

  counter1 : counter { // T300, T400 Trigger counter
    on: {logic3 : ds == '1'},
    start: x"00000000",
    end: x"FFFFFFFF"
  }

  prohibited( // Illegal conditions (SERE)
    {logic0}, // Restrict key leaks of T100, T200, T300
    {logic1 | logic2 | counter1}, // Restrict T100, T200, T300, T400 trigger cases
  )
)

```

Figure 7: BasicRSA.config - CAPSL Specification

## 5.2 ARM TrustZone

## 5.3 Reference Monitor

## 6 CONCLUSION

## REFERENCES

- [1] C. Bobda, T. J. L. Whitaker, C. Kamhoua, K. Kwiat, and L. Njilla. 2017. Synthesis of hardware sandboxes for Trojan mitigation in systems on chip. In *2017 IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*. 172–172. <https://doi.org/10.1109/HST.2017.7951836>
- [2] Stuart Byma, J. Gregory Steffan, Hadi Bannazadeh, Alberto Leon-Garcia, and Paul Chow. 2014. FPGAs in the Cloud: Booting Virtualized Hardware Accelerators with OpenStack. *2014 IEEE 22nd Annual International Symposium on Field-Programmable Custom Computing Machines* (2014), 109–116.
- [3] Fei Chen, Yi Shan, Yu Zhang, Yu Wang, Hubertus Franke, Xiaotao Chang, and Kun Wang. 2014. Enabling FPGAs in the Cloud. In *Proceedings of the 11th ACM Conference on Computing Frontiers (CF '14)*. ACM, New York, NY, USA, Article 3, 10 pages.
- [4] Luca de Alfaro and Thomas A. Henzinger. 2001. Interface Automata. *SIGSOFT Softw. Eng. Notes* 26, 5 (Sept. 2001), 109–120. <https://doi.org/10.1145/503271.503226>
- [5] S. Drzevitzky. 2010. Proof-Carrying Hardware: Runtime Formal Verification for Secure Dynamic Reconfiguration. In *2010 International Conference on Field Programmable Logic and Applications*. 255–258. <https://doi.org/10.1109/FPL.2010.59>
- [6] S. Drzevitzky, U. Kastens, and M. Platzner. 2009. Proof-Carrying Hardware: Towards Runtime Verification of Reconfigurable Modules. In *2009 International Conference on Reconfigurable Computing and FPGAs*. 189–194. <https://doi.org/10.1109/ReConFig.2009.31>
- [7] Ziv Glazberg, Mark Moulin, Avigail Orni, Sitvanit Ruah, and Emmanuel Zarpas. 2007. *PSL: Beyond Hardware Verification*. Springer Netherlands.
- [8] F. Hategekimana and C. Bobda. 2017. Applying the Flask Security Architecture to Secure SoC Design. In *2017 IEEE 25th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*. 198–198. <https://doi.org/10.1109/FCCM.2017.28>
- [9] Ted Huffmire, Brett Brotherton, Nick Callegari, Jonathan Valamehr, Jeff White, Ryan Kastner, and Tim Sherwood. 2008. Designing Secure Systems on Reconfigurable Hardware. *ACM Trans. Des. Autom. Electron. Syst.* 13, 3, Article 44 (July 2008), 24 pages. <https://doi.org/10.1145/1367045.1367053>
- [10] T. Huffmire, B. Brotherton, T. Sherwood, R. Kastner, T. Levin, T. D. Nguyen, and C. Irvine. 2008. Managing Security in FPGA-Based Embedded Systems. *IEEE Design Test of Computers* 25, 6 (Nov 2008), 590–598. <https://doi.org/10.1109/MDT.2008.166>

- [11] T. Huffmire, B. Brotherton, G. Wang, T. Sherwood, R. Kastner, T. Levin, T. Nguyen, and C. Irvine. 2007. Moats and Drawbridges: An Isolation Primitive for Reconfigurable Hardware Based Systems. In *2007 IEEE Symposium on Security and Privacy (SP '07)*. 281–295. <https://doi.org/10.1109/SP.2007.28>
- [12] T. J. L. Whitaker and C. Bobda. 2017. CAPSL: The Component Authentication Process for Sandboxed Layouts. In *2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. 409–414. <https://doi.org/10.1109/ISVLSI.2017.78>
- [13] T. Wiersema, S. Drzevitzky, and M. Platzner. 2014. Memory security in reconfigurable computers: Combining formal verification with monitoring. In *2014 International Conference on Field-Programmable Technology (FPT)*. 167–174. <https://doi.org/10.1109/FPT.2014.7082771>