

# Hardware Isolation Mechanisms for Security Improvement in FPGAs

## ABSTRACT

Field Programmable Gate Arrays (FPGAs) platform security management continues to be a strong area of concern despite recent increased adoption and integration of FPGAs into commercial scale cloud computing systems. One of the technical problems in the FPGA security management area has been the lack of hardware primitives to support multi-tenancy while enforcing proper domain isolation. In this tutorial, we present recent progress that has been made to address this issue. Specifically, we present hardware isolation mechanisms that can be used to enable domain separation on FPGA based systems. We demonstrate the viability of these mechanisms through a software-hardware codesign implementing a simple TLS/SSL encryption application.

## CCS CONCEPTS

•Security and privacy → Embedded Systems Security; Hardware Security Implementation; •Hardware → Reconfigurable Logic Applications;

## KEYWORDS

FPGA Security, Hardware Isolation, IP Containerization, CAPSL

## 1 INTRODUCTION

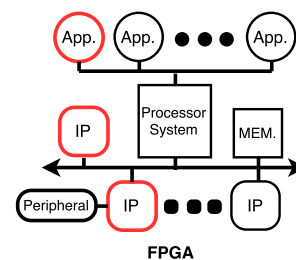
Many of today's critical embedded systems are increasingly relying on FPGA-based SoCs because of the useful balance between the performance, scale, flexibility, and rapid time to market they provide. This was recently exemplified with the recent Audi announcement that its 2018 A8 world's first Level 3 autonomous driving system will feature Altera's Cyclone FPGA SoCs for object and map fusion processing tasks. Though, it's not just in embedded systems space where we are seeing accelerated adoption of FPGA platforms, as they are also being continuously integrated into commercial scale cloud computing systems and data centers as evidenced by Amazon recent announcement of providing cloud compute instances with FPGAs (EC2 F1).

This increased adoption of FPGA into commercial scale cloud computing systems has highlighted the issue of FPGA's lack of hardware primitives, conceptually similar from a security perspective to a CPU's IO memory management unit (IOMMU), to support multi-tenancy while enforcing proper domain separation among the tenants (i.e. multiple applications utilizing the same FPGA)

[6], [4], [5]. This lack of native support for isolation creates security concerns where: 1) Since FPGA accelerators tend to run with full hardware access, a single accelerator vulnerabilities can be exploited through traditional system software stacks or if malicious, can bring down a shared compute host [6]. Or 2) tenants are not able to protect confidentiality and integrity of their application data not only from other tenants, but also from other unauthorized parties including privileged system software, such as the hypervisor [1].

An effective solution to the problem of lack of proper domain separation on FPGAs should be able to enable scaling of security across a range of system parameters, such as power and performance, without significant drop in coverage. We believe and intend to demonstrate in this tutorial that this can only be achieved through some form of combination of measures that protect against hardware vulnerabilities directly at the hardware level and measures that enforce domain separation at the software level. In this tutorial, we look at a set of research works that individually attempted to address the problem of lack of isolation support on FPGAs. We demonstrate how certain elements of these works can be put together to provide an effective and comprehensive solution to this problem. We demonstrate the viability of this solution through a real-world software-hardware codesign application which implements a simple TLS/SSL encryption.

The remainder of this work is organized as follow: Section 2 starts by describing the specific use case scenarios and security concerns this method addresses. Section 3 gives an overview of research works that form the basis of our comprehensive solution. Section 4 and Section 5 conclude the paper with a tutorial demonstrating how a combination of the discussed approaches can be used to provide proper domain isolation on FPGA platform.



**Figure 1: Embedded system threat model: The adversary controls the FPGA SoC and can execute malicious code (non-trusted application + accelerator in red) remotely and launch a denial-of-service attack to an IO component.**

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. Copyrights for components of this work owned by others than ACM must be honored. Abstracting with credit is permitted. To copy otherwise, or republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee. Request permissions from [permissions@acm.org](mailto:permissions@acm.org).

ICDSC'11, Stanford University, CA, USA

© 2017 ACM.

## 2 THREAT MODEL

This section describes the threat model for two use case scenarios our approach targets. We first look at the attack surface in FPGA-based embedded systems and then, we look at FPGA security concerns in cloud computing systems integrating FPGAs.

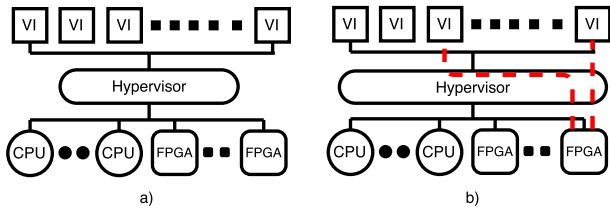
### 2.1 Embedded Systems

The illustration of our threat model in Figure 1 shows the first use case scenario our approach targets. We assume an adversary who can introduce hardware trojans in the IPs during development (supply chain attack). We assume this adversary will later have a remote access to the FPGA system-on-chip (FPGA SoC) which contains some of the malicious IPs. We assume the adversary is aware of the trojans activation mechanisms and can only activate them externally by executing some malicious input for example.

In FPGA-based SoCs, we do not currently have hardware-level support mechanism that would prevent unauthorized bus data access by a bus component. We rely on bus protocols which generally assume that bus components are going to adhere to the protocol and wait for their turn to broadcast. However, this is not always the case since a malicious component can unilaterally decide to access the bus and launch a denial-of-service (DoS) attack for example to a system peripheral.

### 2.2 FPGAs in the Cloud

The fast adoption of FPGA accelerators in cloud computing and the probable future adoption in personal computers raise additional security concerns. Cloud providers such as Amazon that provide infrastructure as a service, must address security threats posed by malicious IPs residing on FPGA without affecting the performance of the system. In general, security is enforced in cloud computing using domain separation. Users are assigned virtual instances (VIs) which are then scheduled on physical resource under by a hypervisor. The hypervisor controls the access to the hardware and insures that every virtual instance remain active within its limit. As shown on Figure 2a), such an approach requires resource virtualization, for which no viable solution currently exist in FPGA. As a result, whole FPGAs must be assigned to small accelerators thus wasting resource, or the execution on the FPGA must be emulated in the hypervisor with performance degradation.



**Figure 2: FPGA provisioning in IAAS-based cloud computers. FPGAs are virtualized in (a) and in (b), tenants are granted direct access to the FPGAs.**

An optimal use of FPGA resource would allow FPGA to be share among IPs, sometimes from different tenants for a better FPGA utilization without performance degradation. With several IPs on

the same FPGA, there is currently no mechanism to guarantee that some IPs will not perform malicious activities, even in the presence of strong protocols. The classic approach to enable IPs on the FPGA is through registers directly controlled by the hypervisor (for the purpose of domain separation), and accessible to the corresponding instance (Figure 2b). The problem here is that a trojan hidden into an IP can bypass protocol and place data on FPGA lines to cause harm. Since the connections are well known, nothing prevent an IP designer to tap long FPGA lines and read information from neighbor modules or to write on line randomly to DoS the design on the FPGA in cloud. As we will show in this tutorial, hardware isolation can address domain separation in hardware to provide an increase protection in the cloud.

## 3 HARDWARE ISOLATION MECHANISMS

Protection of sensitive data in networked and embedded systems has become a critical problem with far-reaching financial and societal implications. Among the 10 paradigms (Deception, Separation, Diversity, Consistency, Depth, Discretion, Collection, Correlation, Awareness, Response) used to address cybersecurity, separation is one of the most effective and relatively easy to implement and, thus increasingly used to address security, in particular in web application where security concerns have been the highest ([7, 10, 15, 16]. The Google Chrome and Adobe have been successfully relying on isolation in the form of sandboxes ([2, 3]) to isolate non-trusted code remotely provided to users for execution on their computers. Isolation has proved to be a very effective mechanism and could play a vital role in protection of malicious activities in hardware. The goal of this tutorial is therefore to provide users a tool for a seamless design and deployment of efficient hardware isolation techniques to address security concerns in FPGA-based systems.

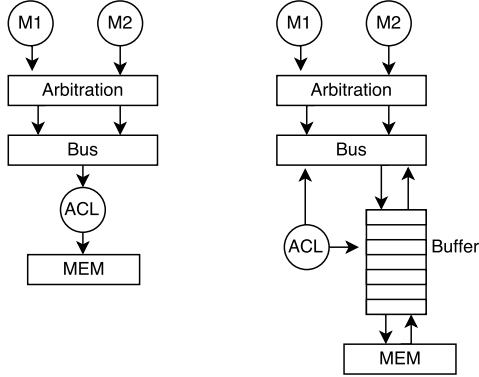
The remainder of this section discusses current techniques that are employed to enforce hardware isolation on FPGAs. This list is by no means exhaustive and it is beyond the scope of this paper to discuss these techniques in greater details. The interested reader is encouraged to refer to cited works.

### 3.1 Reference Monitors

In this approach, a hardware module or a microcontroller based firmware-upgradable module is used to monitor and enforce authorized sharing of system resources among cores. Memory-access security policies are expressed in a specialized language, and a compiler translates these policies directly to a circuit (or a microcontroller) that enforces the policies. The circuit is then loaded onto the FPGA along with other components of the system.

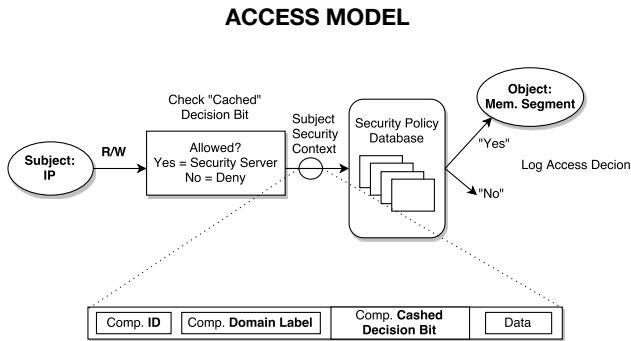
There are many research efforts with some relation to this approach, but to the best of our current knowledge, works in [13] and in [12] are the only work with similar goals that come close to ours here. In their work, they designed and implemented a reconfigurable reference monitor (RM) which implements an access control list (ACL). They then integrated the reference monitor into the on-chip peripheral bus (OPB) and used it to regulate access to the memory and peripherals. Memory and peripherals accesses go through a reconfigurable monitor's access control list [3]. The access control list associates every object (memory ranges for ex.) in the system with a list of principals (IP cores) with the rights of

each principal to access the object[3]. In their implementation, each object access has to be computed by the reference monitor's ACL at runtime. The decision is either granted access or denied access. Since this access model can create potential memory performance issues in large memory applications, they proposed a mechanism in which a buffer is used to hold the data until the ACL grants approval of the legality of the request [14]. Figure 3 illustrates the implementation. For example, in case of a write, the data to be written is stored in the buffer until the ACL grants the approval, at which time the write request is sent to the memory [14].



**Figure 3: Access Model Implementation. On the left, there's no "caching" mechanism. On the right, a buffer is used to hold the data while access rights are being looked up.**

Authors in [11] observed that in Huffmire et al. access model implementation if you had consecutive and repeated memory access from the same "principal" to the same "object", each one of these requests would still have to go through the reference monitor's computation. This can potentially create performance issues in large designs. These issues can be avoided by adding the capability to remember access decisions. Authors in [11] built upon this observation and proposed an improved implementation of this architecture by adding capability to remember access decisions to allow them to be administered at run-time without re-computations. Figure 4 shows their proposed access model.



**Figure 4: Improved Access Model Implementation.**

Both of these techniques follow a similar design flow. Systems components are defined and implemented using hardware synthesis tools such as Xilinx's Vivado or Xilinx's XPS. The hardware-enforced ACL core is generated by some policy compiler and it's then integrated with the rest of the system components similar to adding a standard custom IP to your design [CITAT],[CITAT]. In some instances, however, there can be compatibility issues. Sometimes standard integration of the ACL core can be complicated with the fact that some security-relevant attributes may not be directly available as parameters or easily derived from available parameters. For example, the current version of the AXI Interconnect IP core API available in Vivado 2016 does not present a component ID as a parameter. In situations like these, it's up to the application designer to build their own custom OPB (or AXI interconnect) IP which directly integrates this ACL security functionality.

Authors in [8], [17], [9] observed that the above described techniques assume a "trusted" reference monitor to enforce the security policies and with no mechanism through which the platform itself can authenticate the authority of the reference monitor before it administers an access policy decision. The security concern here is that an attacker could conduct a man-in-the-middle attack on the system by inserting a malicious circuit inside the only authority entrusted with administering shared resource access decisions. To mitigate this, they proposed an improved implementation of the reference monitor which combines the monitoring approach with a "proof-carrying hardware" concept. Their approach consisted of using a consumer-producer approach, where a consumer specifies a desired functionality of the memory access monitor and sends this specification to the producer and the producer synthesizes this information into a bitstream [8]. The producer re-extracts the logic function from this bitstream and, together with the original specification, computes some miter function (which outputs an error flag if the specification and implementation differ for at least one input vector) [17]. This proof of reference monitor correctness is then generated along side with the bitstream and is sent to the consumer. The latter verifies the proof, and in case of success partially reconfigures the monitor with security policies [17]. The consumer verifies the proof of correctness from the producer by extracting the monitor's logic function from the bitstream and forms a miter in conjunctive normal form in the same way as the producer, but with the original specification. This new miter is compared to the producer's miter and if they both match, the implementation is accepted and the monitor is rejected if the mitters do not match [17], [9].

### 3.2 Secure Enclave: Zynq FPGA TrustZone

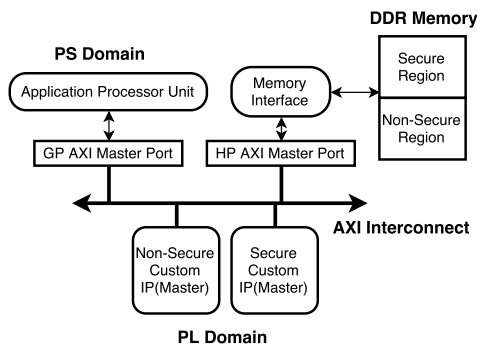
In this approach, systems developers rely on an operating system and some hardware-level enforcement mechanisms to provide system security services. Security features provided include, but are not limited to, confidentiality and integrity protection of the external memory containing the sensitive application code and data.

A recent example of this approach is the ARM TrustZone security architecture currently available to Zynq-7000 SoC. The latter supports ARM TrustZone technology in both the PS and PL domain. The ARM TrustZone architecture makes trusted computing within the embedded world possible by establishing a trusted platform,

a hardware architecture that extends the security infrastructure throughout the system design. Instead of protecting all assets in a single dedicated hardware block, the TrustZone architecture runs specific subsections of the system either in a “normal world” or a “secure world.”

In the Zynq-7000 AP SoC, a normal world is defined as a hardware subset consisting of memory regions, L2 cache regions, and specific AXI devices. The Zynq-7000 AP SoC supports ARM TrustZone technology in both the PS and PL domains of the device. The PS provides a set of configuration registers related to TrustZone support for custom IPs. These configuration registers are then dynamically programmed by the software during execution. All slave IP cores instantiated in the logic can be individually assigned a Secure or Non-Secure designation. For Xilinx slave IP cores, Secure/Non-Secure configuration can be statically designated at the AXI interconnect level during system creation process.

Figure 3 shows a simplified example of how to secure your design sensitive components from illegal hardware access using Zynq-7000 AP SoC TrustZone technology



**Figure 5: Improved Access Model Implementation.**

In this example, also available in [], on the hardware level the PL domain uses two custom master IP cores:

- **Secure Custom IP:** This performs Secure read/write transactions to DDR using the HP slave port in the PS. It is also connected to the Application Processor Unit (APU) via a GP master port for register configuration.
- **Non-Secure Custom IP:** This is used to perform read/write transactions from/to the PS DDR upon requests from the external world. It performs Non-Secure read transactions to DDR using an HP slave port. Configuration of this IP is done by the PS processor through a GP master port.

Upon power-on, the PS processor initializes both custom IPs, configures registers to establish Secure and Non-Secure regions in DDR memory, and transfers private data/instructions to the Secure DDR region. After initialization and upon receiving a data request from the external interface, the Non-Secure custom IP first copies the data from the external interface to the Non-Secure region of DDR memory. It then interrupts the PS processor, which commands the Secure custom IP to perform the appropriate data computations using its private data/instructions in conjunction with the data just copied to the Non-Secure region of DDR memory. After computation is completed, Secure custom IP puts the computed data into

the Non-Secure DDR region and interrupts the PS processor to command the Non-Secure custom IP to start transferring data from the requested location.

On the software level, application processes (and their IPs) with non-secure status designation execute in memory space separated from processes with secure status designation. When a user process running in the Non-Secure world requires Secure execution, it makes a request to the Non-Secure kernel to enable the TrustZone Secure Monitor to transfer execution of the process to the Secure world. The Secure Monitor mode links the two zones and acts as a gatekeeper to manage program flow between them.

To ensure integrity of the TrustZone software, Zynq-7000 provides a secure boot flow; where the on-chip BootROM code starts the whole security chain by ensuring that first-stage bootloader (FSBL) is signed and verified.

### 3.3 CAPSL: Automatic Generation of Hardware Sandboxes

The approach of utilizing hardware sandboxes for isolating and identifying potential malicious IP-internal circuits provides a flexible design process for systems designers and integrators. Similar to discussed approaches, a sandbox isolates IP by partitioning the hardware design to a trusted secure region and a non-trusted environment contained within the sandbox. Hardware sandboxing allows the placement of an interface-level reference monitor to ensure the integrity of non-trusted IP interactions. In addition, virtual resources can be provided to protect critical system resources. The sandbox approach allows unrestricted access to resources used by the trusted IP, while containing potential negative effects of untrusted components behind a behavioral monitor and resource virtualization.

CAPSL, the Component Authentication Process for Sandboxed Layouts supplies automation for generating hardware sandboxes, allowing for a streamlined integration of questionable components into secure systems. The design flow is summarized in the following tasks:

**3.3.1 Construct Internal IP Interface Models:** A specification defining the interface and its behavior is required for each IP in order to formally model the IP and generate automata objects of each policy. The set of automata produced from all policies is used as a behavioral monitor within the sandbox. The specification enables the flexibility to define behavior at varying levels of abstraction and varying degrees of completeness. To elaborate, specification might contain partial interface definitions and/or behaviors abstracted through additional computation logic. To capture security properties, CAPSL adopts the Interface Automata (IA) formalism of De Alfaro and Hetzinger [CITATION NEEDED] along with a subset of the Properties Specification Language (PSL), Sequential Extended Regular Expression (SERE) [CITATION NEEDED]. As a baseline requirement, interface layouts are required (IP interface inputs, outputs). Beyond this, any combination of IA-based descriptions of allowed behavior, explicitly denied interactions defined as SERE statements, and computational logic is allowed.

**3.3.2 Optimize Models:** We chose IA as our internal model due to its capability to handle *composition* and *refinement*. While composition insures that two communicating components do not perform illegal actions, i.e. one automaton produces an input that the other cannot consume, refinement allows breakdown within component boundary while still maintaining the compatibility. The sandbox design leverages these two properties to provide compatible and secure interfaces between the IP and the rest of the system through the sandbox. Applying the composition operation of IA requires the environment (the IP in our case) not to perform illegal actions, i.e. actions that the sandbox and therefore the rest of the system doesn't expect. This means that interfaces are assembled only if they are compatible, resulting in a new composed interface. With all policies respresented as Interface Automata, the composition operation can supply an avenue for reducing the policy automata set size through merging automata with consideration for the environmental assumptions of it.

**3.3.3 Generate/Package Sandbox IP:** The resulting optimized set of policies can now be translated to a reference monitor. When translating from a formal model, it is possible to insert a variety of target IP implemetnations for generating the sandbox as an IP. Initial development of CAPSL produced the sandbox as Vivado IP implemented as VHDL. CAPSL, using a VHDL flow, generates a "checker" module. The module is generated by one-hot encoding our monitoring automata as VHDL statements which capture the expected behavior of the IP. The checker module is combined together with virtual resources (BRAMs, SLRs, etc.) to generate the core logic which governs the sandbox. The generated core logic is then combined with a sandbox controller (routing all signals between interfaces and checker) to conclude the sandbox generation. The controller consists of the sandbox interface (composed with the non-trusted IP interface), physical interface, some status registers, and a multiplexer which acts as a switch to either allow IP interactions to continue or to invalidate them.

## 4 SECURITY CRITICAL EXAMPLE APPLICATION

In this section, we introduce an example application to demonstrate the various hardware isolation methods discussed above. Each of the methods has unique strengths and a more comprehensive security profile can be realized upon implementing each in conjunction. We propose a system that performs secure encryption processes (via Hardware-enforced Access Lists and TrustZone) alongside potentially malicious non-secured processes. With our secure process utilizing hardware-accelerated encryption, CAPSL is utilized to secure the encryption engine and enforce the integrity of its behavior. This system suits the implementation of the discussed hardware isolation methods with the inclusion of points of attack in both software and hardware. Below, we detail the example application and address the security vulnerabilites with regard to the introduced isolation methods.

### 4.1 Overview

We intend to demonstrate the steps required to ensure the protection of a general security-critical system design with an SoC system

providing reconfigurable fabric along with a co-processor. The discussed isolation methods enforce security at the OS/PS level down to the hardware IP interface level. Thus, our demonstration application includes process level applications running on the processing system while hardware is utilized for acceleration cores. The system requires a security critical application such an application requiring sensitive keys to be handled at the software level while relying on hardware for accelerating cryptographic functions.

**4.1.1 Secure Echo Server Process:** We utilize an echo server that encrypts client communcations with a session key established through a simplified TLS/SSL handshake. This system setup assumes the server to be run on the SoC device targeted for protection while the client is run on a remote machine. The SoC hosting the echo server is designed to run on a Zynq SoC, with the zynq processor hosting a Linux OS and utilizing FPGA area for cryptographic functions. The echo server process and complementing client process are implemented as Python programs. We used Xilinx's Petalinux tool for generating the design images required to boot a Linux OS and mount the filesystem. We implemented our system on a Digilent Zybo [IT MIGHT NOT BE BIG ENOUGH for AES + RSA]...

To further elaborate on our application, we begin with the echo server process. The its initial state, the server process listens on a specified network IP address and port awaiting a client connection. Upon receiving a connection, a handshake is initiated as the server immediately shares an RSA public key. A session key computed by the client is received by the server encrypted with its public RSA credentials. Deciphering this session key allows subsequent communications to be secured, namely the server's acknowledgement of a successful handshake, the client's message, and finally the server's echoed message. This system behavior as seen at the process level can be seen in [NEED DIAGRAM].

**4.1.2 Hardware Accelerated Encryption Engine:** The handshake requires the use of both symmetric-key and public-key algorithms, as a symmetric-key (used as session key) is generated from utilizing a asymmetric-key to encrypt and publically transmit the session key. AES and RSA are commonly used to meet these requirements. As these can be computationally expensive with larger key sizes, one standard application of hardware acceleration is for performance boosts with cryptographic functions. To provide our demo system with a hardware component, an AXI-bus enabled IP core is used to accelerate the AES and RSA algorithms used by the echo server process. The PS and PL interaction is detailed in [NEED DIAGRAM].

Upon requiring the AES or RSA cores during execution, data is first written to the appropriate input data registers for each IP. After a successful write of input data, an enable signal is written to a control register to signal the IP core to perform the encryption/decryption. A set of output data registers are assigned to each core along with a status register to inform the software process of a complete computation.

The hardware cores were implemented as Vivado IP cores and exposed by supplying an AXI-bus interface for reading inputs and writing outputs to DDR memory. This is accessible by default from the OS as Petalinux images include kernel drivers for exposing DDR memory under the OS's '/dev/mem' filepath. The memory

blocks for the cryptographic core are accessible via their device-tree specified address. This will be revisited later in [POSSIBLY ANOTHER SECTION TO GO DEEP INTO DETAIL].

## 4.2 Security Vulnerabilities

Our application was designed to include vulnerabilities that could be found in designs that include software processes and hardware accelerators handling sensitive information without security measures. An operating system lacking the ability to restrict executions on sensitive data to isolated processor environments and verify process permissions for secured memory space creates potential points of attack for malicious processes. With the hardware design community's growing adoption rate of third-party IP cores, there are a multitude of infiltration points within the development and manufacturing process with which malicious parties have been able to exploit. It should be noted that it is recognized the server/client handshake is missing vital components of a true TLS/SSL scheme such as certificate based verifications performed by both client and server. However, the scope of this work omits the undertaking of securing the network layer.

To exploit the vulnerabilities mentioned, we have included a non-secure process, a secure process, and hardware trojans for the purpose of demonstration and providing a metric of system security strength.

**4.2.1 Software Threat Insertion:** For the purpose of this tutorial, we wrote a (non-secure) process thread as part of our application software to randomly read memory regions associated with cryptographic functions keys management code variables and data structures (secure code). The non-secure process conducts unauthorized code injection on these privileged locations and tries to gain privileged secure execution status (privilege escalation attack).

**4.2.2 Hardware Threat Insertion:** Our encryption engine is a prime candidate for inserting a malicious circuit as it will have access to sensitive encryption key data. As our application performs a simple handshake and utilizes both AES and RSA algorithms, we can leverage the Trust-hub.org repository of hardware trojans for AES128 and BasicRSA. Both AES128 and Basic RSA trojan classes contain variations of activation methods, from always-on trojans to internal condition triggers. We chose the following trojans...

## 4.3 Addressing Vulnerabilities with Isolation

An accepted paradigm of security for our proposed system would require secure execution for sensitive computations with dedicated hardware resources that are deemed secure. We address the system vulnerabilities as follows:

**4.3.1 Reference Monitor and TrustZone:** We assume no a priori knowledge of specific vulnerabilities within the application code running on the FPGA SoC. All we know is that we are tasked to provide a secure implementation of the application. TrustZone provides us with the ability to create memory regions that are isolated from all other code in the system (including privileged code such as OS kernel). Depending on the size of the code that's going to execute in this secure regions, we may have to segment these memory regions into smaller segments whose utilization and access permissions can be tracked through a hardware-implemented reference

monitor. Segmenting these isolated secure regions is important since it allows us to create a tiered trust model in our system. This way we can guarantee confidentiality of our application software most sensitive data (cryptographic keys) by isolating it from all privileged code.

**4.3.2 Hardware Sandboxing:** The protections put in place with reference monitors and Trustzone are limited as they do not consider malicious hardware components interacting with secure processes. Though the process execution environment may be secured with relevant memory blocks protected, an assumed-secure IP core could house a malicious hardware trojan.

To complement the methods discussed for secure process execution, we propose the use of CAPSL to extend policy-driven and isolation-based security to the programmable logic of an SoC. We have addressed all components of our demo systems with the exception of our cryptographic hardware cores. With the security-critical server/client processes utilizing hardware cores, it is essential that the IP are behaving as expected. Hardware sandboxing provides a way to safely integrate nontrusted IP into a secure system. By securing the cores within a sandbox, we are able to monitor all non-trusted IP interface interactions and isolate unexpected interactions with secured resources.

## 5 IMPLEMENTING ISOLATION

In this section, we discuss implementation details regarding the steps of applying the isolation methods.

### 5.1 Software Level

**5.1.1 TrustZone.**

**5.1.2 Reference Monitor.**

### 5.2 Hardware Level

**5.2.1 CAPSL.** As discussed in Section 3.3, the CAPSL design flow requires specifications for nontrusted IP (Cryptographic cores) purposed for defining interface connections and behavior. The IP models resulting from specification are then subjected to an optimization phase. The collection of models are translated to a reference monitor implementation following optimization. The final output is an implementation of the hardware sandbox packaged as an IP.

**IP Specification:** To utilize CAPSL's sandbox generation process, we must define the IP we wish to include. Due to the underlying modeling of the untrusted IP, specification at the interface level, or any abstraction of this, is required. That is, specification might contain partial interface definitions and/or behaviors abstracted through additional computation logic. The specification files for AES and RSA cores are explained in Figure [RSA AND AES SPEC FILES EXPLANATION DIAGRAM].

Along with the required interface layout definition, the specifications for both AES and RSA utilize SERE statements in conjunction with additional computational logic to provide explicitly denied interactions. More specifically, the specifications are utilizing additional logic for abstracting the SERE specifications for detecting known trojan triggers. The RSA specification also utilizes the IA-based

description of allowed behavior to define how the IP shares its current state.

*Optimization:*

*Sandbox Generation:*

## 6 CONCLUSION

## REFERENCES

- [1] Sergei Arnautov, Bohdan Trach, Franz Gregor, Thomas Knauth, Andre Martin, Christian Priebe, Joshua Lind, Divya Muthukumaran, Dan O’Keeffe, Mark L. Stillwell, David Goltzsche, Dave Evers, Rüdiger Kapitza, Peter Pietzuch, and Christof Fetzer. 2016. SCONE: Secure Linux Containers with Intel SGX. In *12th USENIX Symposium on Operating Systems Design and Implementation (OSDI 16)*. USENIX Association, GA, 689–703.
- [2] Adobe Blog. Security@Adobe. [http://blogs.adobe.com/security/.\(????\)](http://blogs.adobe.com/security/.(????)).
- [3] Chromium Blog. 2008. A new approach to browser security: the Google Chrome Sandbox. <https://blog.chromium.org/2008/10/new-approach-to-browser-security-google.html>. (Oct 2008).
- [4] C. Bobda, T. J. L. Whitaker, C. Kamhoua, K. Kwiat, and L. Njilla. 2017. Synthesis of hardware sandboxes for Trojan mitigation in systems on chip. In *2017 IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*. 172–172. <https://doi.org/10.1109/HST.2017.7951836>
- [5] Stuart Byma, J. Gregory Steffan, Hadi Bannazadeh, Alberto Leon-Garcia, and Paul Chow. 2014. FPGAs in the Cloud: Booting Virtualized Hardware Accelerators with OpenStack. *2014 IEEE 22nd Annual International Symposium on Field-Programmable Custom Computing Machines* (2014), 109–116.
- [6] Fei Chen, Yi Shan, Yu Zhang, Yu Wang, Hubertus Franke, Xiaotao Chang, and Kun Wang. 2014. Enabling FPGAs in the Cloud. In *Proceedings of the 11th ACM Conference on Computing Frontiers (CF ’14)*. ACM, New York, NY, USA, Article 3, 10 pages.
- [7] Lance Cottrell. 2017. Isolation Technology Protects Against Risky Cyberenvironments. <https://ntrepidcorp.com/cyber-security/isolation-technology-protects-against-risky-cyberenvironments/>. (Feb 2017).
- [8] S. Drzevitzky. 2010. Proof-Carrying Hardware: Runtime Formal Verification for Secure Dynamic Reconfiguration. In *2010 International Conference on Field Programmable Logic and Applications*. 255–258. <https://doi.org/10.1109/FPL.2010.59>
- [9] S. Drzevitzky, U. Kastens, and M. Platzner. 2009. Proof-Carrying Hardware: Towards Runtime Verification of Reconfigurable Modules. In *2009 International Conference on Reconfigurable Computing and FPGAs*. 189–194. <https://doi.org/10.1109/ReConFig.2009.31>
- [10] Fireglass. 2016. Fireglass Emerges From Stealth with a Military-Grade, Enterprise-Ready Threat Isolation Platform to Put an End to Security Challenges. (Feb 2016).
- [11] F. Hategekimana and C. Bobda. 2017. Applying the Flask Security Architecture to Secure SoC Design. In *2017 IEEE 25th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*. 198–198. <https://doi.org/10.1109/FCCM.2017.28>
- [12] Ted Huffmire, Brett Brotherton, Nick Callegari, Jonathan Valamehr, Jeff White, Ryan Kastner, and Tim Sherwood. 2008. Designing Secure Systems on Reconfigurable Hardware. *ACM Trans. Des. Autom. Electron. Syst.* 13, 3, Article 44 (July 2008), 24 pages. <https://doi.org/10.1145/1367045.1367053>
- [13] T. Huffmire, B. Brotherton, T. Sherwood, R. Kastner, T. Levin, T. D. Nguyen, and C. Irvine. 2008. Managing Security in FPGA-Based Embedded Systems. *IEEE Design Test of Computers* 25, 6 (Nov 2008), 590–598. <https://doi.org/10.1109/MDT.2008.166>
- [14] T. Huffmire, B. Brotherton, G. Wang, T. Sherwood, R. Kastner, T. Levin, T. Nguyen, and C. Irvine. 2007. Moats and Drawbridges: An Isolation Primitive for Reconfigurable Hardware Based Systems. In *2007 IEEE Symposium on Security and Privacy (SP ’07)*. 281–295. <https://doi.org/10.1109/SP.2007.28>
- [15] Franklyn Jones. Cyber Security for Credit Unions: Managing the Unique Challenges. [https://www.bankinfosecurity.com/webinars/how-isolation-technology-protects-cus-from-cyber-attacks-w-575.\(????\)](https://www.bankinfosecurity.com/webinars/how-isolation-technology-protects-cus-from-cyber-attacks-w-575.(????)).
- [16] John P. Mello Jr. 2015. Is Isolating the Internet Key to Bulletproof Security? <http://www.technewsworld.com/story/82245.html>. (July 2015).
- [17] T. Wiersema, S. Drzevitzky, and M. Platzner. 2014. Memory security in reconfigurable computers: Combining formal verification with monitoring. In *2014 International Conference on Field-Programmable Technology (FPT)*. 167–174. <https://doi.org/10.1109/FPT.2014.7082771>