Lab7 Report

Submitted By:

Mayank Singla

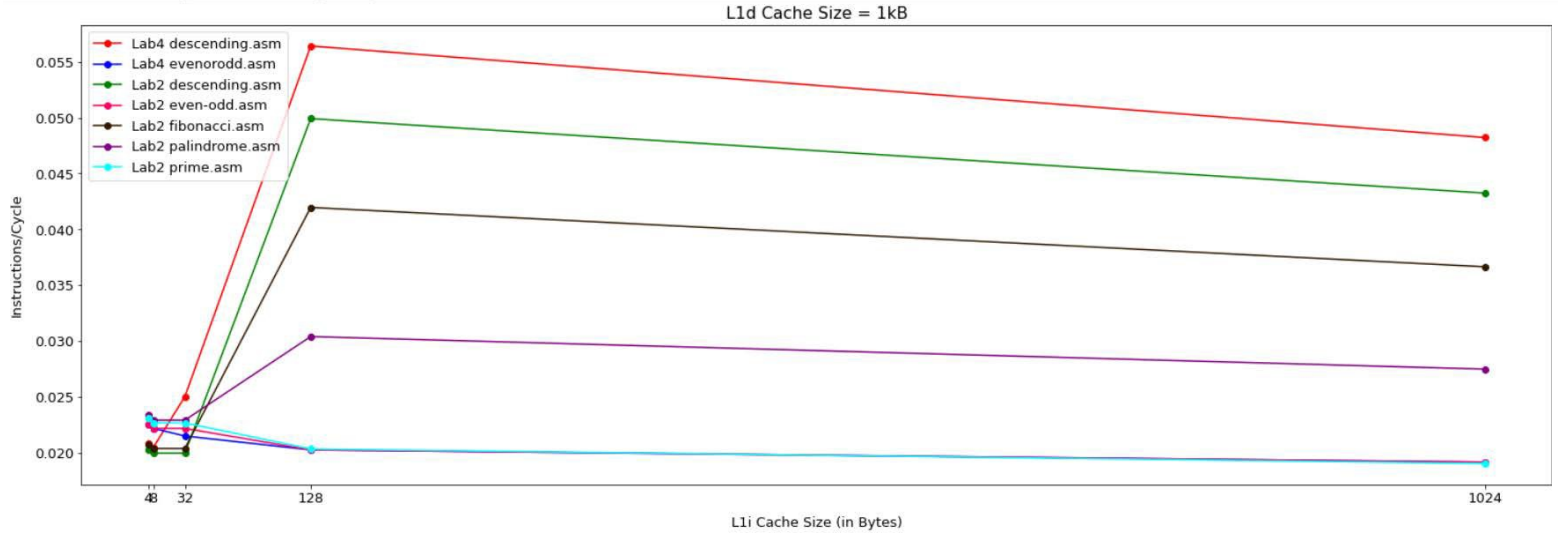
L1d Cache: Size = 1kB, Latency = 12 Cycles

Throughput table (in terms of Number of instructions per cycle)

(Detailed Results about each program are written at the end)

L1i Cache Size	Lab4 descending .asm	Lab4 evenorodd .asm	Lab2 descending .asm	Lab2 even-odd.asm	Lab2 fibonacci .asm	Lab2 palindrome .asm	Lab2 prime .asm
4B	0.020846386056843424	0.022508038585209004	0.020281746428214606	0.022508038585209004	0.020721769499417928	0.023379383634431455	0.023090586145648313
8B	0.02046865387841843	0.022151898734177215	0.019935186094471178	0.022151898734177215	0.020356816102470265	0.022892819979188347	0.02264808362369338
32B	0.025	0.02147239263803681	0.019935186094471178	0.022151898734177215	0.020356816102470265	0.022892819979188347	0.02264808362369338
128B	0.05643793369313801	0.02023121387283237	0.049926217412690606	0.02023121387283237	0.041961338991041965	0.03038674033149171	0.0203125
1kB	0.0482276979839241	0.01912568306010929	0.04324669791222838	0.01912568306010929	0.03664059283655825	0.02746566791510612	0.019005847953216373

Plot obtained: (Plotted using Matplotlib)



Observations:

- Most of the benchmarks achieve their highest IPC when the size of L1i cache is 128B. In the initial sizes of L1i cache (at 4B, 8B and 32B), IPC does not appreciably increase indicating that an increase in size of the cache is equally weighed out by a two-fold increase in the latency. But, as the cache size is increased to 128B, there are many cache hits and this outweighs the effect of latency.
- But, as we further increase cache size, since the earlier cache size was already sufficient to hold the instructions with a good hit rate, this increase has no appreciable effect rather the increase in latency now has an upper hand leading to a decrease in IPC.
- The effect of varying cache size is more profound on descending.asm as it has very much greater number of instructions when compared to other benchmarks. Also, evenorodd.asm shows a different linear decreasing trend as the number of dynamic instructions are very less for cache size to have any effect at all on its IPC. However, even then, latency dominates at higher cache sizes.

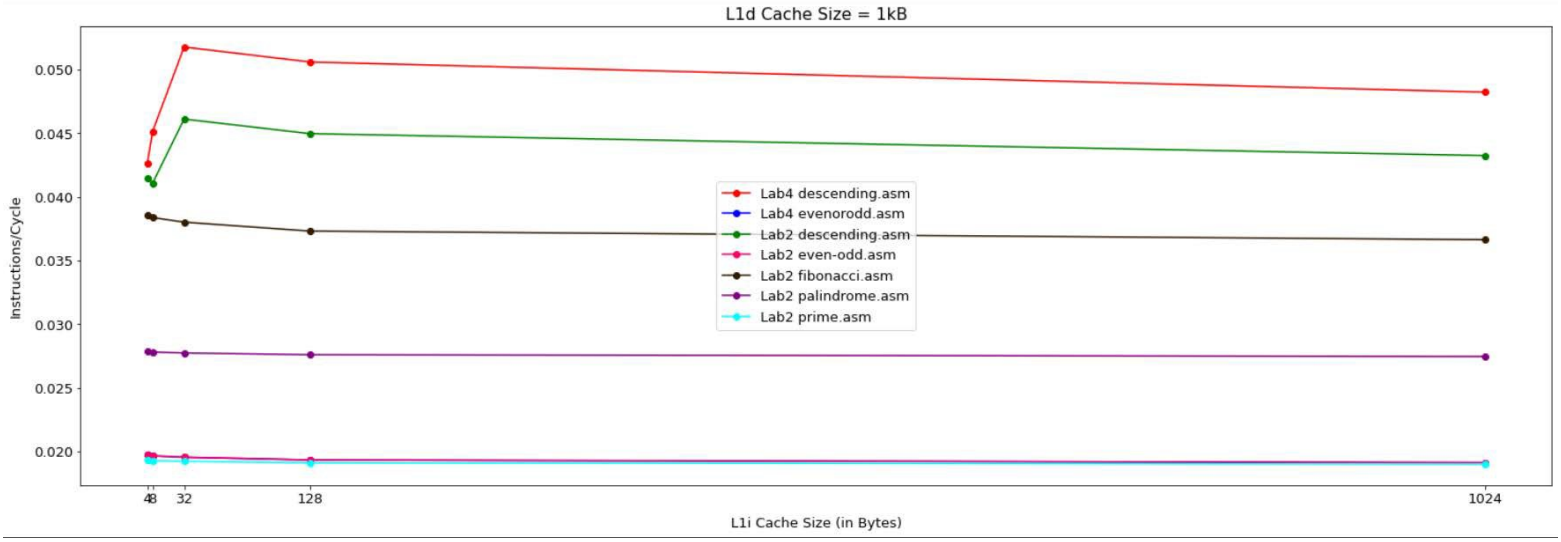
L1i Cache: Size = 1kB, Latency = 12 Cycles

Throughput table (in terms of Number of instructions per cycle)

(Detailed Results about each program are written at the end)

L1d Cache Size	Lab4 descending .asm	Lab4 evenorodd .asm	Lab2 descending .asm	Lab2 even-odd.asm	Lab2 fibonacci .asm	Lab2 palindrome .asm	Lab2 prime .asm
4B	0.0426672884122173	0.01971830985915493	0.04146241830065359	0.01971830985915493	0.03856152512998267	0.027848101265822784	0.019316493313521546
8B	0.04514616997656346	0.019662921348314606	0.04108480064764218	0.019662921348314606	0.038378611470461406	0.02781289506953224	0.019287833827893175
32B	0.05177535719337954	0.019553072625698324	0.04611540208995911	0.019553072625698324	0.038017941050832976	0.027742749054224466	0.019230769230769232
128B	0.05060141020323517	0.019337016574585635	0.044971200708905625	0.019337016574585635	0.03731656184486373	0.027603513174404015	0.01911764705882353
1kB	0.0482276979839241	0.01912568306010929	0.04324669791222838	0.01912568306010929	0.03664059283655825	0.02746566791510612	0.019005847953216373

Plot obtained: (Plotted using Matplotlib)



Observations:

- As the number of data memory accesses is quite low, varying the cache size does not have a significant effect on all other benchmarks except for descending.asm, which again shows a similar trend as in the previous case and can explained exactly in the same terms.
- Hence the curves obtained are linear for most of the programs.

Details of Each Program

L1d Cache Size = 1kB
Latency = 12 Cycles

L1i Cache Size = 4B
Latency = 1 Cycle

Lab4-descending.asm
Number of instructions executed = 366
Number of cycles taken = 17557
Number of times an instruction on a wrong branch path entered the pipeline = 88
Number of times the OF stage needed to stall because of a data hazard = 0
Throughput in terms of Number of instructions per cycle = 0.020846386056843424

Lab4-evenorodd.asm
Number of instructions executed = 7
Number of cycles taken = 311
Number of times an instruction on a wrong branch path entered the pipeline = 0
Number of times the OF stage needed to stall because of a data hazard = 0
Throughput in terms of Number of instructions per cycle = 0.022508038585209004

Lab2-descending.asm
Number of instructions executed = 203
Number of cycles taken = 10009
Number of times an instruction on a wrong branch path entered the pipeline = 27
Number of times the OF stage needed to stall because of a data hazard = 0
Throughput in terms of Number of instructions per cycle = 0.020281746428214606

Lab2-even-odd.asm
Number of instructions executed = 7
Number of cycles taken = 311
Number of times an instruction on a wrong branch path entered the pipeline = 0
Number of times the OF stage needed to stall because of a data hazard = 0
Throughput in terms of Number of instructions per cycle = 0.022508038585209004

Lab2-fibonacci.asm
Number of instructions executed = 89
Number of cycles taken = 4295
Number of times an instruction on a wrong branch path entered the pipeline = 9
Number of times the OF stage needed to stall because of a data hazard = 0
Throughput in terms of Number of instructions per cycle = 0.020721769499417928

Lab2-palindrome.asm
Number of instructions executed = 22
Number of cycles taken = 941
Number of times an instruction on a wrong branch path entered the pipeline = 4
Number of times the OF stage needed to stall because of a data hazard = 0
Throughput in terms of Number of instructions per cycle = 0.023379383634431455

Lab2-prime.asm
Number of instructions executed = 13
Number of cycles taken = 563
Number of times an instruction on a wrong branch path entered the pipeline = 1
Number of times the OF stage needed to stall because of a data hazard = 0
Throughput in terms of Number of instructions per cycle = 0.023090586145648313

L1i Cache Size = 8B

Latency = 2 Cycles

Lab4-descending.asm

Number of instructions executed = 366

Number of cycles taken = 17881

Number of times an instruction on a wrong branch path entered the pipeline = 88

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.02046865387841843

Lab4-evenorodd.asm

Number of instructions executed = 7

Number of cycles taken = 316

Number of times an instruction on a wrong branch path entered the pipeline = 0

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.022151898734177215

Lab2-descending.asm

Number of instructions executed = 203

Number of cycles taken = 10183

Number of times an instruction on a wrong branch path entered the pipeline = 27

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.019935186094471178

Lab2-even-odd.asm

Number of instructions executed = 7

Number of cycles taken = 316

Number of times an instruction on a wrong branch path entered the pipeline = 0

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.022151898734177215

Lab2-fibonacci.asm

Number of instructions executed = 89

Number of cycles taken = 4372

Number of times an instruction on a wrong branch path entered the pipeline = 9

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.020356816102470265

Lab2-palindrome.asm

Number of instructions executed = 22

Number of cycles taken = 961

Number of times an instruction on a wrong branch path entered the pipeline = 4

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.022892819979188347

Lab2-prime.asm

Number of instructions executed = 13

Number of cycles taken = 574

Number of times an instruction on a wrong branch path entered the pipeline = 1

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.02264808362369338

L1i Cache Size = 32B

Latency = 4 Cycles

Lab4-descending.asm

Number of instructions executed = 366

Number of cycles taken = 14640

Number of times an instruction on a wrong branch path entered the pipeline = 88

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.025

Lab4-evenorodd.asm

Number of instructions executed = 7

Number of cycles taken = 326

Number of times an instruction on a wrong branch path entered the pipeline = 0

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.02147239263803681

Lab2-descending.asm

Number of instructions executed = 203

Number of cycles taken = 10183

Number of times an instruction on a wrong branch path entered the pipeline = 27

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.019935186094471178

Lab2-even-odd.asm

Number of instructions executed = 7

Number of cycles taken = 316

Number of times an instruction on a wrong branch path entered the pipeline = 0

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.022151898734177215

Lab2-fibonacci.asm

Number of instructions executed = 89

Number of cycles taken = 4372

Number of times an instruction on a wrong branch path entered the pipeline = 9

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.020356816102470265

Lab2-palindrome.asm

Number of instructions executed = 22

Number of cycles taken = 961

Number of times an instruction on a wrong branch path entered the pipeline = 4

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.022892819979188347

Lab2-prime.asm

Number of instructions executed = 13

Number of cycles taken = 574

Number of times an instruction on a wrong branch path entered the pipeline = 1

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.02264808362369338

L1i Cache Size = 128B

Latency = 8 Cycles

Lab4-descending.asm

Number of instructions executed = 366

Number of cycles taken = 6485

Number of times an instruction on a wrong branch path entered the pipeline = 88

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.05643793369313801

Lab4-evenorodd.asm

Number of instructions executed = 7

Number of cycles taken = 346

Number of times an instruction on a wrong branch path entered the pipeline = 0

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.02023121387283237

Lab2-descending.asm

Number of instructions executed = 203

Number of cycles taken = 4066

Number of times an instruction on a wrong branch path entered the pipeline = 27

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.049926217412690606

Lab2-even-odd.asm

Number of instructions executed = 7

Number of cycles taken = 346

Number of times an instruction on a wrong branch path entered the pipeline = 0

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.02023121387283237

Lab2-fibonacci.asm

Number of instructions executed = 89

Number of cycles taken = 2121

Number of times an instruction on a wrong branch path entered the pipeline = 9

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.041961338991041965

Lab2-palindrome.asm

Number of instructions executed = 22

Number of cycles taken = 724

Number of times an instruction on a wrong branch path entered the pipeline = 4

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.03038674033149171

Lab2-prime.asm

Number of instructions executed = 13

Number of cycles taken = 640

Number of times an instruction on a wrong branch path entered the pipeline = 1

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.0203125

L1i Cache Size = 1kB

Latency = 12 Cycles

Lab4-descending.asm

Number of instructions executed = 366

Number of cycles taken = 7589

Number of times an instruction on a wrong branch path entered the pipeline = 88

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.0482276979839241

Lab4-evenorodd.asm

Number of instructions executed = 7

Number of cycles taken = 366

Number of times an instruction on a wrong branch path entered the pipeline = 0

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.01912568306010929

Lab2-descending.asm

Number of instructions executed = 203

Number of cycles taken = 4694

Number of times an instruction on a wrong branch path entered the pipeline = 27

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.04324669791222838

Lab2-even-odd.asm

Number of instructions executed = 7

Number of cycles taken = 366

Number of times an instruction on a wrong branch path entered the pipeline = 0

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.01912568306010929

Lab2-fibonacci.asm

Number of instructions executed = 89

Number of cycles taken = 2429

Number of times an instruction on a wrong branch path entered the pipeline = 9

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.03664059283655825

Lab2-palindrome.asm

Number of instructions executed = 22

Number of cycles taken = 801

Number of times an instruction on a wrong branch path entered the pipeline = 4

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.02746566791510612

Lab2-prime.asm

Number of instructions executed = 13

Number of cycles taken = 684

Number of times an instruction on a wrong branch path entered the pipeline = 1

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.019005847953216373

L1i Cache Size = 1kB
Latency = 12 Cycles

L1d Cache Size = 4B
Latency = 1 Cycle

Lab4-descending.asm
Number of instructions executed = 366
Number of cycles taken = 8578
Number of times an instruction on a wrong branch path entered the pipeline = 88
Number of times the OF stage needed to stall because of a data hazard = 0
Throughput in terms of Number of instructions per cycle = 0.0426672884122173

Lab4-evenorodd.asm
Number of instructions executed = 7
Number of cycles taken = 355
Number of times an instruction on a wrong branch path entered the pipeline = 0
Number of times the OF stage needed to stall because of a data hazard = 0
Throughput in terms of Number of instructions per cycle = 0.01971830985915493

Lab2-descending.asm
Number of instructions executed = 203
Number of cycles taken = 4896
Number of times an instruction on a wrong branch path entered the pipeline = 27
Number of times the OF stage needed to stall because of a data hazard = 0
Throughput in terms of Number of instructions per cycle = 0.04146241830065359

Lab2-even-odd.asm
Number of instructions executed = 7
Number of cycles taken = 355
Number of times an instruction on a wrong branch path entered the pipeline = 0
Number of times the OF stage needed to stall because of a data hazard = 0
Throughput in terms of Number of instructions per cycle = 0.01971830985915493

Lab2-fibonacci.asm
Number of instructions executed = 89
Number of cycles taken = 2308
Number of times an instruction on a wrong branch path entered the pipeline = 9
Number of times the OF stage needed to stall because of a data hazard = 0
Throughput in terms of Number of instructions per cycle = 0.03856152512998267

Lab2-palindrome.asm
Number of instructions executed = 22
Number of cycles taken = 790
Number of times an instruction on a wrong branch path entered the pipeline = 4
Number of times the OF stage needed to stall because of a data hazard = 0
Throughput in terms of Number of instructions per cycle = 0.027848101265822784

Lab2-prime.asm
Number of instructions executed = 13
Number of cycles taken = 673
Number of times an instruction on a wrong branch path entered the pipeline = 1
Number of times the OF stage needed to stall because of a data hazard = 0
Throughput in terms of Number of instructions per cycle = 0.019316493313521546

L1d Cache Size = 8B

Latency = 2 Cycles

Lab4-descending.asm

Number of instructions executed = 366

Number of cycles taken = 8107

Number of times an instruction on a wrong branch path entered the pipeline = 88

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.04514616997656346

Lab4-evenorodd.asm

Number of instructions executed = 7

Number of cycles taken = 356

Number of times an instruction on a wrong branch path entered the pipeline = 0

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.019662921348314606

Lab2-descending.asm

Number of instructions executed = 203

Number of cycles taken = 4941

Number of times an instruction on a wrong branch path entered the pipeline = 27

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.04108480064764218

Lab2-even-odd.asm

Number of instructions executed = 7

Number of cycles taken = 356

Number of times an instruction on a wrong branch path entered the pipeline = 0

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.019662921348314606

Lab2-fibonacci.asm

Number of instructions executed = 89

Number of cycles taken = 2319

Number of times an instruction on a wrong branch path entered the pipeline = 9

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.038378611470461406

Lab2-palindrome.asm

Number of instructions executed = 22

Number of cycles taken = 791

Number of times an instruction on a wrong branch path entered the pipeline = 4

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.02781289506953224

Lab2-prime.asm

Number of instructions executed = 13

Number of cycles taken = 674

Number of times an instruction on a wrong branch path entered the pipeline = 1

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.019287833827893175

L1d Cache Size = 32B

Latency = 4 Cycles

Lab4-descending.asm

Number of instructions executed = 366

Number of cycles taken = 7069

Number of times an instruction on a wrong branch path entered the pipeline = 88

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.05177535719337954

Lab4-evenorodd.asm

Number of instructions executed = 7

Number of cycles taken = 358

Number of times an instruction on a wrong branch path entered the pipeline = 0

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.019553072625698324

Lab2-descending.asm

Number of instructions executed = 203

Number of cycles taken = 4402

Number of times an instruction on a wrong branch path entered the pipeline = 27

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.04611540208995911

Lab2-even-odd.asm

Number of instructions executed = 7

Number of cycles taken = 358

Number of times an instruction on a wrong branch path entered the pipeline = 0

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.019553072625698324

Lab2-fibonacci.asm

Number of instructions executed = 89

Number of cycles taken = 2341

Number of times an instruction on a wrong branch path entered the pipeline = 9

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.038017941050832976

Lab2-palindrome.asm

Number of instructions executed = 22

Number of cycles taken = 793

Number of times an instruction on a wrong branch path entered the pipeline = 4

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.027742749054224466

Lab2-prime.asm

Number of instructions executed = 13

Number of cycles taken = 676

Number of times an instruction on a wrong branch path entered the pipeline = 1

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.019230769230769232

L1d Cache Size = 128B

Latency = 8 Cycles

Lab4-descending.asm

Number of instructions executed = 366

Number of cycles taken = 7233

Number of times an instruction on a wrong branch path entered the pipeline = 88

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.05060141020323517

Lab4-evenorodd.asm

Number of instructions executed = 7

Number of cycles taken = 362

Number of times an instruction on a wrong branch path entered the pipeline = 0

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.019337016574585635

Lab2-descending.asm

Number of instructions executed = 203

Number of cycles taken = 4514

Number of times an instruction on a wrong branch path entered the pipeline = 27

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.044971200708905625

Lab2-even-odd.asm

Number of instructions executed = 7

Number of cycles taken = 362

Number of times an instruction on a wrong branch path entered the pipeline = 0

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.019337016574585635

Lab2-fibonacci.asm

Number of instructions executed = 89

Number of cycles taken = 2385

Number of times an instruction on a wrong branch path entered the pipeline = 9

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.03731656184486373

Lab2-palindrome.asm

Number of instructions executed = 22

Number of cycles taken = 797

Number of times an instruction on a wrong branch path entered the pipeline = 4

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.027603513174404015

Lab2-prime.asm

Number of instructions executed = 13

Number of cycles taken = 680

Number of times an instruction on a wrong branch path entered the pipeline = 1

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.01911764705882353

L1d Cache Size = 1kB

Latency = 12 Cycles

Lab4-descending.asm

Number of instructions executed = 366

Number of cycles taken = 7589

Number of times an instruction on a wrong branch path entered the pipeline = 88

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.0482276979839241

Lab4-evenorodd.asm

Number of instructions executed = 7

Number of cycles taken = 366

Number of times an instruction on a wrong branch path entered the pipeline = 0

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.01912568306010929

Lab2-descending.asm

Number of instructions executed = 203

Number of cycles taken = 4694

Number of times an instruction on a wrong branch path entered the pipeline = 27

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.04324669791222838

Lab2-even-odd.asm

Number of instructions executed = 7

Number of cycles taken = 366

Number of times an instruction on a wrong branch path entered the pipeline = 0

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.01912568306010929

Lab2-fibonacci.asm

Number of instructions executed = 89

Number of cycles taken = 2429

Number of times an instruction on a wrong branch path entered the pipeline = 9

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.03664059283655825

Lab2-palindrome.asm

Number of instructions executed = 22

Number of cycles taken = 801

Number of times an instruction on a wrong branch path entered the pipeline = 4

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.02746566791510612

Lab2-prime.asm

Number of instructions executed = 13

Number of cycles taken = 684

Number of times an instruction on a wrong branch path entered the pipeline = 1

Number of times the OF stage needed to stall because of a data hazard = 0

Throughput in terms of Number of instructions per cycle = 0.019005847953216373