CS2610: Computer Organization and Architecture

Lab 1

Objective:
In this lab you will analyse the efficiency of different adder topologies in terms of processing delay.

Problem:
You are given two 4-bit unsigned numbers A and B in two 4-bit registers. You are required to implement the addition of A and B in Verilog for the below mentioned scenarios:

1. You are provided with 4 full adders and two 4-bit registers R0 and R1.
2. You are provided with only 1 full adder and two 4-bit registers R0 and R1.

Compare the performance of the two scenarios in terms of processing delay.

Resources: For the implementation you may choose any one of the tools shown below. Since Vivado is a large tool and bit complicated, if you wish you may complete this assignment with EDA playground.

1) EDA Playground: https://eda-playground.readthedocs.io/en/latest/intro.html#libraries-methodologies
    a. You may choose to you eda playground for simulation and synthesis. From the simulator option select VTR7. It will generate all the timing information for your design.
    b. There are several examples available in EDA playground which you may use to understand the simulation and synthesis process.

2) Xilinx Vivado Design Suite : https://www.xilinx.com/support/university/students.html#software
    a. Download Vivado Design Suite: WebEdition
    b. You may use this tutorial to understand flow better https://www.xilinx.com/support/documentation/university/Vivado-Teaching/HDL-Design/2015x/Verilog/docs-pdf/Vivado_tutorial.pdf