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## PART - A

1. What is Structure of Control Unit?

Ans:

Purpose of control unit is to control the system operations by routing the selected data items to the selected processing HW at right time. Control unit's responsibility is to drive the associated processing HW by generating a set of signals that are synchronized with the master clock. In order to carry out a task such as ADD. The control unit must generate a set of control signals in a predefined sequence governed by the HW structure of the processing section.

2. Define Micro operation.

Ans:

Micro operation is an elementary operation performed (during one clock pulse), on the information stored in one or more registers

3. Define Synchronous Communication.

Ans:

If the registers in the interface share a common clock with the CPU registers, the transfer between the two units is said to be synchronous

4. What is I/O interface?

Ans:

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In computing, an interface is a shared boundary across which two or more separate components of a computer system exchange information. The exchange can be between software, computer hardware, peripheral devices, humans, and combinations of these.

5. What is Sector?

Ans:

In a hard disk, bits are stored in the magnetized surface in spots along concentric circles called tracks. The tracks are commonly divided into sections called sectors.

6. Define Paging.

Ans:

Memory paging is a memory management scheme by which a computer stores and retrieves data from secondary storage for use in main memory.

7. What is Flag Register?

Ans:

Flag Register determines the current state of the processor. They are modified automatically by CPU after mathematical operations, this allows to determine the type of the result, and to determine conditions to transfer control to other parts of the program.

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8. Define Pipelining.

Ans:

Pipelining is a technique of decomposing a sequential process into sub operations with each sub process being executed in a special dedicated segment that operates concurrently with all other segments.

9. What is Cluster?

Ans:

A cluster is a group of interconnected, whole computers working together as a unified computing resource.

10. Define Uniform Memory Access.

Ans:

Uniform memory access is where all processors have access to all parts of memory. Access time to all regions of memory is the same and access time to memory for different processors is the same(SMP).

PART – B

11. Explain Register Transfer using RTL.

Ans:

It is a:

- A symbolic language

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- A convenient tool for describing the internal organization of digital computers
- Can also be used to facilitate the design process of digital systems.

Register Transfer is:

- Copying the contents of one register to another.

A register transfer is indicated as:

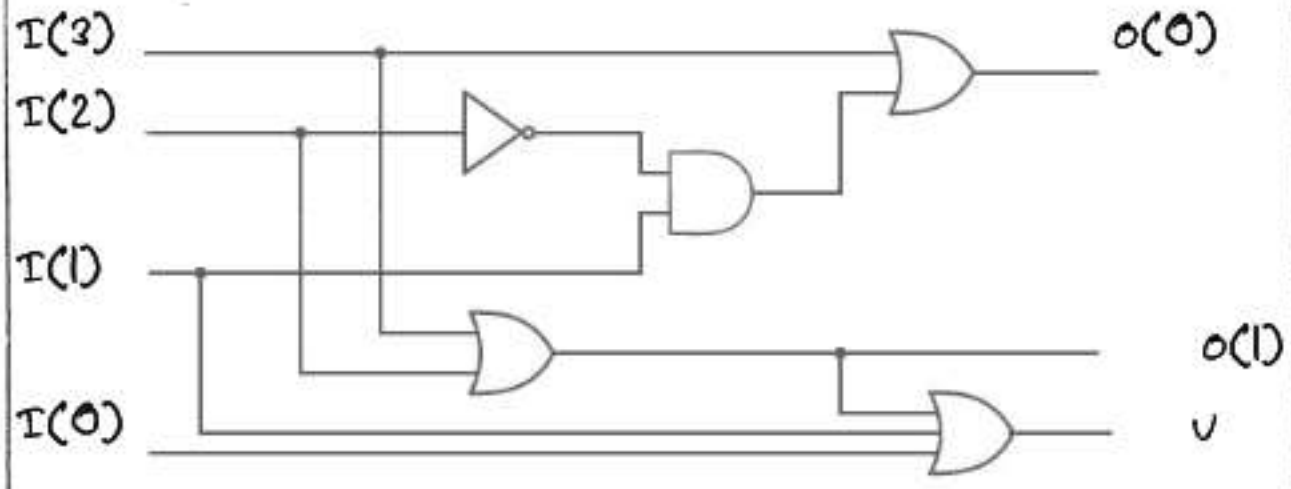
$$R2 \leftarrow R1$$

In this case the contents of register R1 are copied (loaded) into register R2. A simultaneous transfer of all bits from the source R1 to the destination register R2, during one clock pulse takes place. It should be noted that this is non-destructive; i.e. the contents of R1 are not altered by copying (loading) them to R2.

12. Draw a Priority encoder circuit with its truth table.

Ans:

Diagram:

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Truth Table:

| Inputs | | | | outputs | | |
|---|---|---|---|---|---|---|
| I0 | I1 | I2 | I3 | x | y | IST |
| 1 | x | x | x | 0 | 0 | 1 |
| 0 | 1 | x | x | 0 | 0 | 1 |
| 0 | 0 | 1 | x | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | x | x | 0 |

13. Explain hit ratio.

Ans:

When the CPU refers to memory and finds the word in cache it is said to produce hit. If the word is not found in cache it is in main memory and it count as miss. The ratio of the number of bits divided by the total CPU references to memory (hit+miss) is the hit ratio. For best performance the hit ratio should be high.

14. Explain the various general purposes registers of 8086

Ans:

General Purpose Registers of 8086 These registers can be used as 8-bit registers individually or can be used as 16-bit in pair to have Ax, Bx, Cx, and Dx. 1. Ax Register: Ax register is also known as accumulator register that stores operands for arithmetic operation like divided, rotate. 2. Bx Register: This register is mainly used as a base register. It holds the starting base location of a memory region within a data segment. 3. Cx Register: It is defined as a counter. It is primarily used in loop instruction to store loop counter. 4. Dx Register: Dx

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register is used to contain I/O port address for I/O instruction.

15. Explain the features of an SMP.

Ans:

The characteristics of a symmetric multiprocessor are:

* There are two or more similar processors of equal capability.
* These processors share the same main memory and I/O facilities.
* The memory access time of the processors is almost the same for each processor.
* All processors can perform the same function.
* The system is controlled by a single operating system.

PART - C

16 A) Explain Bus and Bus transfer with neat block diagram.

Ans:

* Bus is a path (of a group of wires) over which information is transferred, from any of several sources to any of several destinations.
* A common bus system can be constructed using multiplexers. The multiplexers select the source register whose binary information is then placed on the bus.
* The transfer of information from a bus into one of many destination registers can be accomplished by connecting the bus lines to the inputs of all destination register and

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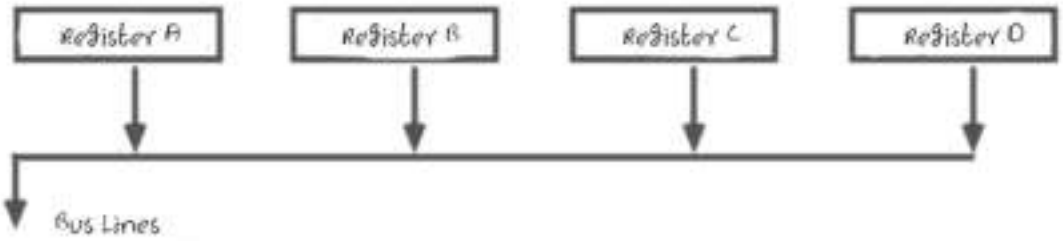
activating the load control of the particular destination register selected.

* Transfer from a register to bus (figure): BUS ← R

Diagram:




Bus Transfer In RTL:

* Depending on whether the bus is to be mentioned explicitly or not, register transfer can be indicated as either

* R2 ← R1

Or

BUS ← R1, R2 ← BUS

In the former case the bus is implicit, but in the latter, it is explicitly indicated.

17. A) Explain strobe controller data transfer.

Ans:

DMA Transfer:

* The position of the DMA controller among the other components in a computer system explained.

*The CPU communicates with the DMA through the address and data buses as with any interface unit.

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*The DMA has its own address which activates the DS and RS lines.

*The CPU initialize the DMA through data bus.

* Once the DMA receives the start control command it can start the transfer between peripheral and memory.

- Peripheral device sends DMA Request line to DMA controller
- DMA controller activates BR line
- The CPU responds with BG line
- The DMA puts the current value of its address register into the address bus, initiates RD and WR signal and send DMA acknowledge line to the peripheral
- The RD and WR lines in the DMA controller are bidirectional. The direction of transfer depends on the status of the BG line.
- When BG=0 the RD and WR are input lines allowing the CPU to communicate with the internal DMA registers.
- When BG =1 the RD and WR are output lines from the DMA controller to the RAM to specify the read or write operation for the data.
- If the word count register reaches zero, the DMA stops any further transfer and removes its bus request.
- It also informs the CPU of the termination by means of an interrupt.

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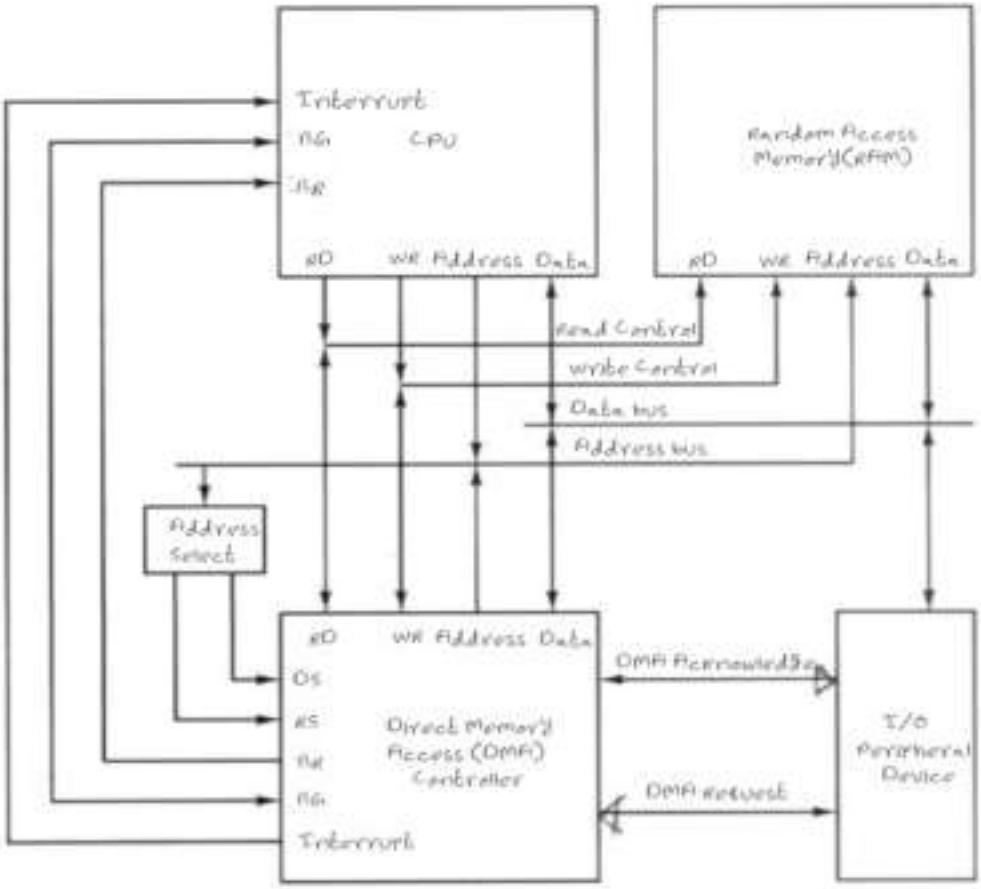
Diagram:




18 B) Explain the page replacement technique in detail.

Ans:

Page Replacement Technique:

* When a page fault occurs in a virtual memory system it signifies that the page referenced by the CPU is not in main memory. A new page is then transferred from auxiliary memory to main memory.

* If main memory is full it would be necessary to remove a page from memory block to make room for the new page. The policy for choosing pages to remove is determined from the replacement algorithm used.

* Two of the most common replacement algorithms used are the first in first out and the least recently used.

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* The FIFO algorithm selects for replacement the page that has been in memory the longest time.

* Each time a page is loaded into memory its identification number is pushed into a FIFO stack.

* FIFO will be full whenever memory has no more empty blocks. When a new page must be loaded the page least recently brought in is removed.

* The page to be removed is easily determined because its identification number is at the top of the FIFO stack.

* The FIFO replacement policy having advantage of being easy to implement.

* It has the disadvantage that under certain circumstances pages are removed and loaded from memory too frequently.

*The LRU policy is more difficult to implement but has been more attractive.

* The algorithm can be implemented by associating a counter with every page that is in main memory. When a page is referenced its associated counter is set to zero.

* At fixed intervals of time the counters associated with all the pages presently in memory are incremented by 1.

* The least recently used page is the page with the highest count. The counters are often called aging registers as their count indicates their age, that is how long ago their associated pages have been referenced.

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19 B) Explain the various stages of an instruction pipeline with block diagram.

Ans:

* An instruction pipeline reads consecutive instructions from memory while previous instructions are being executed in other segments.

* This causes the instruction fetch and execute phases to overlap and perform simultaneous operations.

* In case of a branch instruction the pipeline is emptied and all the instructions that have been read from memory after the branch instruction must be discarded.

* Computers with complex instructions require other phases in addition to the fetch and execute to process an instruction completely.

* Computer processes each instruction with the following sequence of steps:

- Fetch the instruction from memory.
- Decode the instruction.
- Calculate the effective address.
- Fetch the operands from memory.
- Execute the instruction.
- Store the result in the proper place.

* Four Segment Instruction pipeline diagram shows how the instruction cycle in the CPU can be processed with a four segment pipeline.

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* While an instruction is being executed in segment 4, the next instruction in sequence is busy fetching an operand from memory in segment 3.

* The effective address may be calculated in a separate arithmetic circuit for the third instruction and whenever memory is available the fourth and subsequent instructions can be fetched and placed in an instruction FIFO.

* Thus up to four suboperations in the instruction cycle can overlap and up to four different instructions can be in progress of processed at the same time Once in a while an instruction in the sequence may be a program control type that causes a branch out of normal sequence.

* In that case the pending operations in the last two segments are completed and all information stored in the instruction buffer is deleted. The pipeline then restarts from the new address stored in the program counter.

* Similarly, an interrupt request will cause the pipeline to empty and start again from a new address value.

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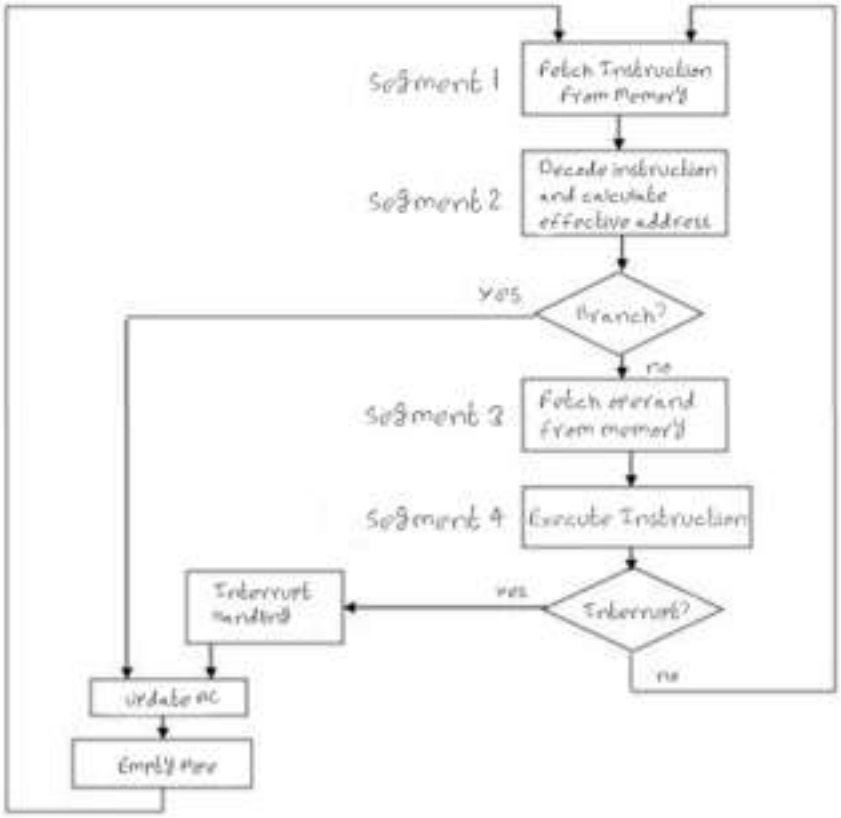
Diagram:




20. A) Explain the organization and features of core i7 processors

Ans:

Core i7:

* The Intel Core i7, introduced in November of 2008, implements four x86 SMT processors, each with a dedicated L2 cache, and with a shared L3 cache.

* The general structure of the Intel Core i7 is shown in the diagram. Each core has its own dedicated L2 cache and the four cores share an 8-MB L3 cache. The main features are:

- Four x86 SMT processors
- Dedicated L2, shared L3 cache
- Speculative pre-fetch for caches

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- On chip DDR3 memory controller
- Three 8 byte channels (192 bits)

giving 32GB/s

- No front side bus
- QuickPath Interconnection
- Cache coherent point-to-point link
- High speed communications between

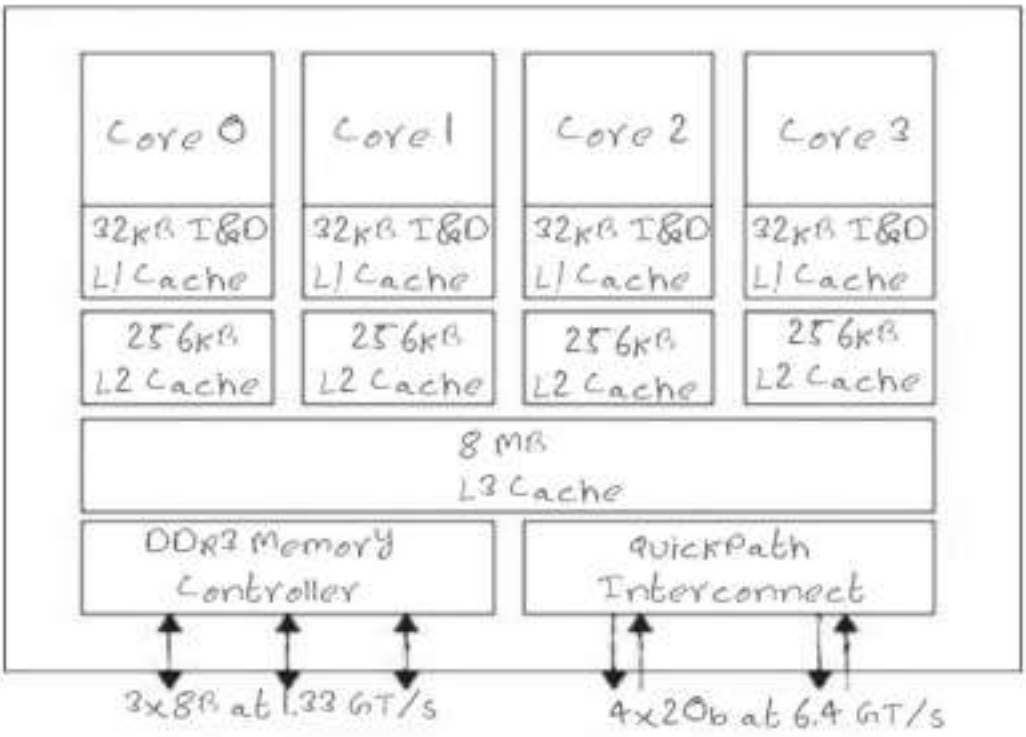
processor chips

- 6.4G transfers per second, 16 bits

per transfer

- Dedicated bi-directional pairs
- Total bandwidth 25.6GB/s

Diagram:

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