Ho Chi Minh City University of Technology
Faculty of Computer Science and Engineering

Computer Architecture

Practical session - Week 8, Semester 1 2020

Notes:

- The main purpose of this week is to review the course.
- Students are NOT requested to submit anything.

Chapter 1

Question 1. Assume a program requires the execution of:

- 50×10^6 FP instructions,
- 110×10^6 INT instructions,
- 80×10^6 L/S instructions,
- and 16×10^6 branch instructions.

The CPI for each type of instruction is 1, 1, 4, and 2, respectively. Assume that the processor has a 2 GHz clock rate.

a. By how much must we improve the CPI of FP instructions if we want the program to run two times faster?

b. By how much must we improve the CPI of L/S instructions if we want the program to run two times faster?

c. By how much is the execution time of the program improved if the CPI of INT and FP instructions is reduced by 40% and the CPI of L/S and Branch is reduced by 30%?

Chapter 2

Question 2. Assume that the sequence of instructions is executed by a standard MIPS processor. The pseudo instruction **`la`** will assign the base address of an array to a register (as MARS MIPS simulator program).

```
.data
array: .word 2018, -20, 18
.text
main: la $t0,  array
lbu $s0, 2($t0)
lbu $s1, 7($t0)
addu $s3, $s1, $s0
sw $s3, 8($t0)
lb $s4, 11($t0)
```

a. What is value of the `$s0` register?

b. What is value of the `$s1` register?

c. What is value of the `$s4` register?

d. How many instructions are there in R-format, I-format, and J-format?

Question 3. Given the following MIPS instructions

```
label: bne  $t0, $t1, exit
addi $t0, $t0, -1
addi $t1, $t1, 1
j label
exit:
```

a. What is offset (16 bit) of the **bne** `$t0,$t1,exit` instruction?

b. Given that the **bne** `$t0, $t1, exit` instruction is stored at memory location 8_{10}. Which is the offset field (26 bit) of MIPS instruction `j label` (value in decimal)?

Chapter 3

Question 4. Given the following MIPS instructions:

```
lui $t0, 0
ori $t0, $t0, 7
lui $t1, 0
ori $t1, $t1, 2
div $t0, $t1
mfhi $s0
mflo $s1
```

What are values in the `$s0` and `$t0` registers after the above instructions are executed?

Chapter 4

Question 5. Given the following MIPS instructions executed in a 5-stage pipeline MIPS processors (IF, ID, EXE, MEM, WB):

```
lw $t1, 0($a0)
lw $t2, 4($a0)
add $t3, $t1, $t2
sw $t3, 8($a0)
lw $t4, 4($a0)
lw $t5, 8($a0)
add $t6, $t4, $t5
sw $t6, 12($a0)
```

a. If only the stall insertion method is used for data hazards, what is execution time of the sequence of instructions in term of cycles?

b. What is the average CPI of the above sequence when only the stall insertion method is used for data hazard?

c. When both the forwarding method and the stall insertion method are used, what is the speed-up compared to stall insertion?

Question 6. Given the following MIPS program.

```
 addi $t1, $zero, 100
 addi $t2, $zero, 0
loop:
 beq $t1, $t2, exit
 addi $t1, $t1, -1
 addi $t2, $t2, 1
 j loop
exit:
 ...
```

Assume that the MIPS processor is designed as 5 stages pipeline architecture. The delay of pipeline states is described as follow:

Stage	**Delay**
IF	150
ID	100
Register access	120
ALU	100
MEM	150

a. Determine the number of clock cycles of the above programs with pipeline and non-pipeline architecture.

b. Assume that the processor works at 200 MHz frequency, calculate the execution time of the above program with pipeline and non-pipeline architecture.

c. Calculate the speed up of pipeline in comparison with non-pipeline architecture of the above program.

d. What is maximum speed up of pipeline in comparison with non-pipeline architecture.

e. Determine the data-dependency of the above program.

f. If we solve the data-dependency of the above program by adding stall, how many stall we should add to solve the data hazard.

g. If we use forwarding, stall to solve hazard (data, control), how many stall should we add.

h. If we use forwarding, stall, prediction, to solve hazard (data, control), how many stall should we add.

——————the end——————