Ho Chi Minh City University of Technology
Faculty of Computer Science and Engineering

Computer Architecture

Practical session - Week 7 - Semester 1 - 2020

Notes:

- The main purpose of this week is to understand how cache work.
- Students do all exercises on the report (.pdf) and submit on e-learning before the deadline.

Question 1. A memory uses 32 bits for address, the size of cache is 4MB, the size of block is 256B. The system supports byte access. Determine the size of tag, index, offset in each following scenarios:

1. Direct mapped
2. 4-way set associative
3. Fully associative

Question 2. A memory has a size of 256MB, the size of cache is 256KB, each block contains 64 words. The system supports half-word access. Determine the tag, index, offset with the following cache's configuration:

1. Direct mapped
2. 8-way set associative.
3. Fully associative

Question 3. A system integrates a 256B cache that is configured as direct mapped. The size of each cache block is 4 words. The system supports byte access. Assume that we access consecutively the following addresses:
$0 \rightarrow 4 \rightarrow 1 \rightarrow 5 \rightarrow 65 \rightarrow 1 \rightarrow 67 \rightarrow 46 \rightarrow 1 \rightarrow 70 \rightarrow 2 \rightarrow 0$
Determine the number of HIT/MISS with the following configuration:

1. Direct mapped
2. 2-ways set associative
3. 4-ways set associative
4. Full associative

Question 4. Define the following concept:

- Page
- Page fault
- Cache miss
- Write bach/ Write through
- PTE
- TLB

Question 5. Calculate the average CPI of a pipeline system where the miss rate of instruction memory is 5%, the miss rate of data memory is 10%. Miss penalty is 100 cycles. Base CPI is 1.5. The proportion of load/store instructions is 36%.

——————the end——————