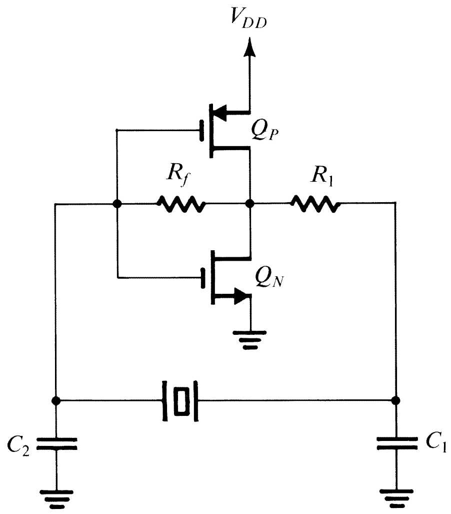

Figure 18.18 A Pierce crystal oscillator utilizing a CMOS inverter as an amplifier.

The extremely stable resonance characteristics and the very high Q factors of quartz crystals result in oscillators with very accurate and stable frequencies. Crystals are available with resonance frequencies in the range of a few kilohertz to hundreds of megahertz. Temperature coefficients of ω_0 of 1 or 2 parts per million (ppm) per degree Celsius are achievable. Unfortunately, however, crystal oscillators, being mechanical resonators, are fixed-frequency circuits.

EXERCISE

18.13 A 2-MHz quartz crystal is specified to have $L = 0.52$ H, $C_s = 0.012$ pF, $C_p = 4$ pF, and $r = 120\ \Omega$. Find f_s, f_p, and Q.
Ans. 2.015 MHz; 2.018 MHz; 55,000

18.4 Bistable Multivibrators

In this section we begin the study of waveform-generating circuits of the other type—nonlinear oscillators or function generators. These devices make use of a special class of circuits known as **multivibrators**. As mentioned earlier, there are three types of multivibrator: bistable, monostable, and astable. This section is concerned with the first, the bistable multivibrator.[4]

As its name indicates, the **bistable multivibrator** has *two stable states*. The circuit can remain in either stable state indefinitely and moves to the other stable state only when appropriately *triggered*.

[4] Digital implementations of multivibrators were presented in Chapter 16. Here, we are interested in implementations utilizing op amps.

18.4.1 The Feedback Loop

Bistability can be obtained by connecting a dc amplifier in a positive-feedback loop having a loop gain greater than unity. Such a feedback loop is shown in Fig. 18.19; it consists of an op amp and a resistive voltage divider in the positive-feedback path. To see how bistability is obtained, consider operation with the positive input terminal of the op amp near ground potential. This is a reasonable starting point, since the circuit has no external excitation. Assume that the electrical noise that is inevitably present in every electronic circuit causes a small positive increment in the voltage v_+. This incremental signal will be amplified by the large open-loop gain A of the op amp, with the result that a much greater signal will appear in the op amp's output voltage v_O. The voltage divider (R_1, R_2) will feed a fraction $\beta \equiv R_1/(R_1 + R_2)$ of the output signal back to the positive input terminal of the op amp. If $A\beta$ is greater than unity, as is usually the case, the fed-back signal will be greater than the original increment in v_+. This *regenerative* process continues until eventually the op amp saturates with its output voltage at the positive saturation level, L_+. When this happens, the voltage at the positive input terminal, v_+, becomes $L_+R_1/(R_1 + R_2)$, which is positive and thus keeps the op amp in positive saturation. This is one of the two stable states of the circuit.

In the description above we assumed that when v_+ was near zero volts, a positive increment occurred in v_+. Had we assumed the equally probable situation of a negative increment, the op amp would have ended up saturated in the negative direction with $v_O = L_-$ and $v_+ = L_-R_1/(R_1 + R_2)$. This is the other stable state.

We thus conclude that the circuit of Fig. 18.19 has two stable states, one with the op amp in positive saturation and the other with the op amp in negative saturation. The circuit can exist in either of these two states indefinitely. We also note that the circuit cannot exist in the state for which $v_+ = 0$ and $v_O = 0$ for any length of time. This is a state of *unstable equilibrium* (also known as a **metastable state**); any disturbance, such as that caused by electrical noise, causes the bistable circuit to switch to one of its two stable states. This is in sharp contrast to the case when the feedback is negative, causing a virtual short circuit to appear between the op amp's input terminals and maintaining this virtual short circuit in the face of disturbances. A physical analogy for the operation of the bistable circuit is depicted in Fig. 18.20.

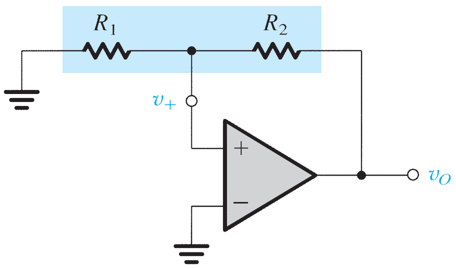

Figure 18.19 A positive-feedback loop capable of bistable operation.

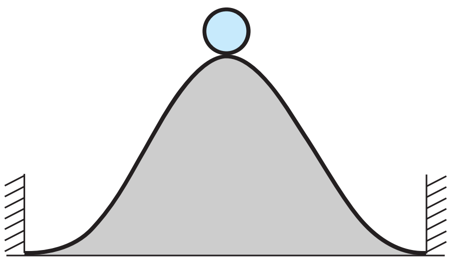

Figure 18.20 A physical analogy for the operation of the bistable circuit. The ball cannot remain at the top of the hill for any length of time (a state of unstable equilibrium or metastability); the inevitably present disturbance will cause the ball to fall to one side or the other, where it can remain indefinitely (the two stable states).

18.4.2 Transfer Characteristic of the Bistable Circuit

The question naturally arises as to how we can make the bistable circuit of Fig. 18.19 change state. To help answer this crucial question, we derive the transfer characteristic of the bistable circuit. Reference to Fig. 18.19 indicates that either of the two nodes that are connected to ground can serve as an input terminal. We investigate both possibilities.

Figure 18.21(a) shows the bistable circuit with a voltage v_I applied to the inverting input terminal of the op amp. To derive the transfer characteristic v_O–v_I, assume that v_O is at one of its two possible levels, say L_+, and thus $v_+ = \beta L_+$. Now as v_I is increased from 0 V, we can see from the circuit that nothing happens until v_I reaches a value equal to v_+ (i.e., βL_+). As

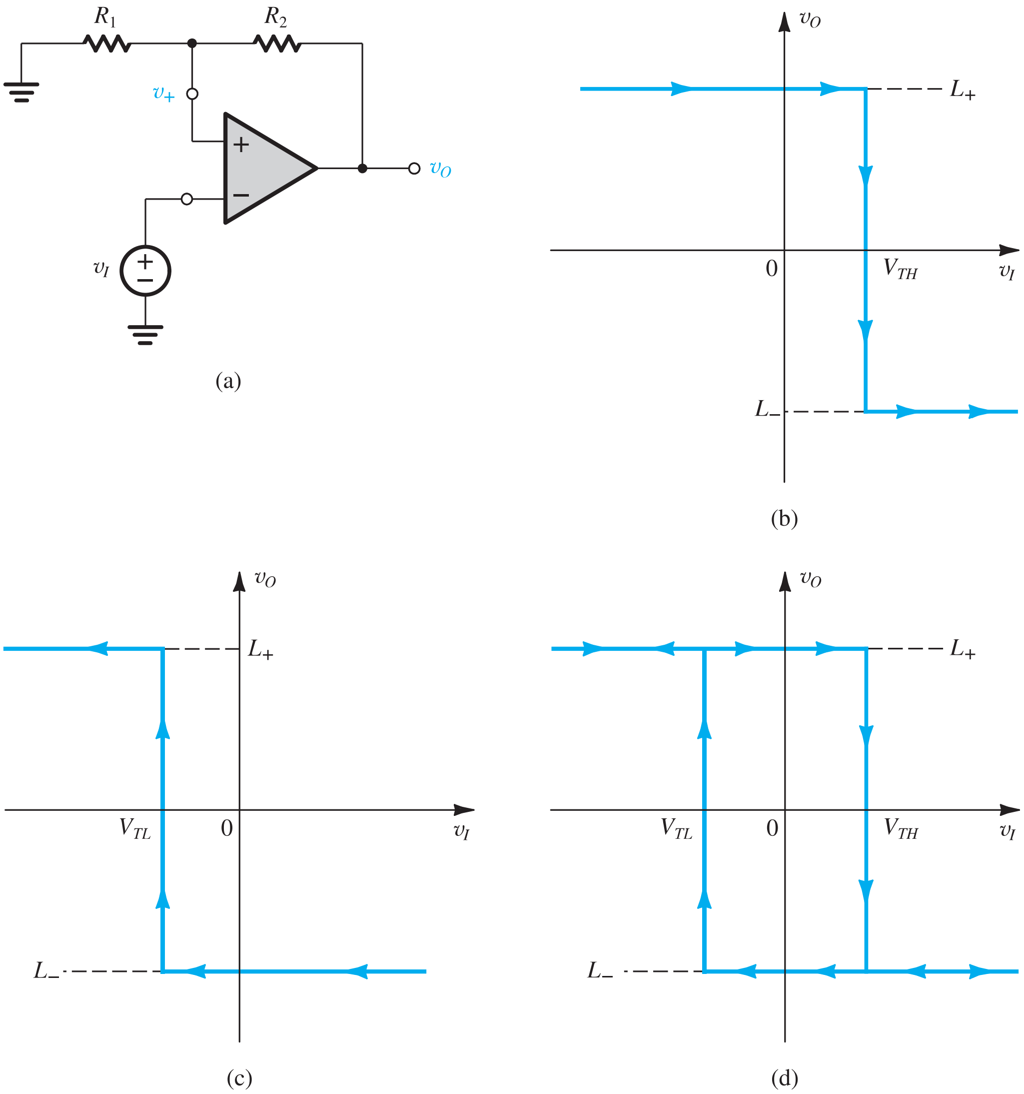

Figure 18.21 **(a)** The bistable circuit of Fig. 18.19 with the negative input terminal of the op amp disconnected from ground and connected to an input signal v_I. **(b)** The transfer characteristic of the circuit in **(a)** for increasing v_I. **(c)** The transfer characteristic for decreasing v_I. **(d)** The complete transfer characteristics.

v_I begins to exceed this value, a net negative voltage develops between the input terminals of the op amp. This voltage is amplified by the open-loop gain of the op amp, and thus v_O goes negative. The voltage divider in turn causes v_+ to go negative, thus increasing the net negative input to the op amp and keeping the regenerative process going. This process culminates in the op amp saturating in the negative direction: that is, with $v_O = L_-$ and, correspondingly, $v_+ = \beta L_-$. It is easy to see that increasing v_I further has no effect on the acquired state of the bistable circuit. Figure 18.21(b) shows the transfer characteristic for increasing v_I. Observe that the characteristic is that of a comparator with a threshold voltage denoted V_{TH}, where $V_{TH} = \beta L_+$.

Next consider what happens as v_I is decreased. Since now $v_+ = \beta L_-$, we see that the circuit remains in the negative-saturation state until v_I goes negative to the point that it equals βL_-. As v_I goes below this value, a net positive voltage appears between the op amp's input terminals. This voltage is amplified by the op-amp gain and thus gives rise to a positive voltage at the op amp's output. The regenerative action of the positive-feedback loop then sets in and causes the circuit eventually to go to its positive saturation state, in which $v_O = L_+$ and $v_+ = \beta L_+$. The transfer characteristic for decreasing v_I is shown in Fig. 18.21(c). Here again we observe that the characteristic is that of a comparator, but with a threshold voltage $V_{TL} = \beta L_-$.

The complete transfer characteristics, v_O–v_I, of the circuit in Fig. 18.21(a) can be obtained by combining the characteristic in Fig. 18.21(b) and (c), as shown in Fig. 18.21(d). As indicated, the circuit changes state at different values of v_I, depending on whether v_I is increasing or decreasing. Thus the circuit is said to exhibit *hysteresis;* the width of the hysteresis is the difference between the high threshold V_{TH} and the low threshold V_{TL}. Also note that the bistable circuit is in effect a comparator with hysteresis. As will be shown shortly, adding hysteresis to a comparator's characteristics can be very beneficial in certain applications. Finally, observe that because the bistable circuit of Fig. 18.21 switches from the positive state ($v_O = L_+$) to the negative state ($v_O = L_-$) as v_I is increased past the positive threshold V_{TH}, the circuit is said to be *inverting*. A bistable circuit with a *noninverting* transfer characteristic will be presented shortly.

18.4.3 Triggering the Bistable Circuit

Returning now to the question of how to make the bistable circuit change state, we observe from the transfer characteristics of Fig. 18.21(d) that if the circuit is in the L_+ state it can be switched to the L_- state by applying an input v_I of value greater than $V_{TH} \equiv \beta L_+$. Such an input causes a net negative voltage to appear between the input terminals of the op amp, which initiates the regenerative cycle that culminates in the circuit switching to the L_- stable state. Here it is important to note that the input v_I merely initiates or *triggers* regeneration. Thus we can remove v_I with no effect on the regeneration process. In other words, v_I can be simply a pulse of short duration. The input signal v_I is thus referred to as a **trigger signal**, or simply a **trigger**.

The characteristics of Fig. 18.21(d) indicate also that the bistable circuit can be switched to the positive state ($v_O = L_+$) by applying a negative trigger signal v_I of magnitude greater than that of the negative threshold V_{TL}.

18.4.4 The Bistable Circuit as a Memory Element

We observe from Fig. 18.21(d) that for input voltages in the range $V_{TL} < v_I < V_{TH}$, the output can be either L_+ or L_-, *depending on the state that the circuit is already in*. Thus, for this input range, the output is determined by the *previous* value of the trigger signal (the trigger signal that caused the circuit to be in its current state). Thus the circuit exhibits *memory*. Indeed, the bistable multivibrator is the basic memory element of digital systems, as we have seen in Chapter 16. Finally, note that in analog-circuit applications, such as the ones of concern to us in this chapter, the bistable circuit is also known as a **Schmitt trigger**.

18.4.5 A Bistable Circuit with Noninverting Transfer Characteristic

The basic bistable feedback loop of Fig. 18.19 can be used to derive a circuit with noninverting transfer characteristic by applying the input signal v_I (the trigger signal) to the terminal of R_1 that is connected to ground. The resulting circuit is shown in Fig. 18.22(a). To obtain the transfer characteristic we first employ superposition to the linear circuit formed by R_1 and R_2, thus expressing v_+ in terms of v_I and v_O as

$$v_+ = v_I \frac{R_2}{R_1 + R_2} + v_O \frac{R_1}{R_1 + R_2} \tag{18.30}$$

From this equation we see that if the circuit is in the positive stable state with $v_O = L_+$, positive values for v_I will have no effect. To trigger the circuit into the L_- state, v_I must be made negative and of such a value as to make v_+ decrease below zero. Thus the low-threshold V_{TL} can be found by substituting in Eq. (18.30) $v_O = L_+$, $v_+ = 0$, and $v_I = V_{TL}$. The result is

$$V_{TL} = -L_+(R_1/R_2) \tag{18.31}$$

Similarly, Eq. (18.30) indicates that when the circuit is in the negative-output state ($v_O = L_-$), negative values of v_I will make v_+ more negative with no effect on operation. To initiate the regeneration process that causes the circuit to switch to the positive state, v_+ must be made to

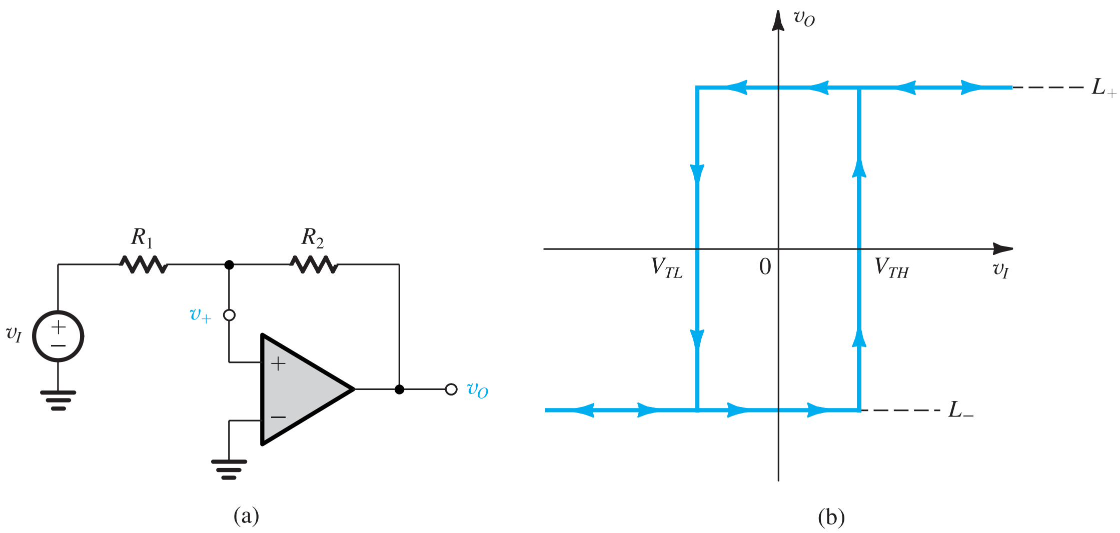

Figure 18.22 **(a)** A bistable circuit derived from the positive-feedback loop of Fig. 18.19 by applying v_I through R_1. **(b)** The transfer characteristic of the circuit in **(a)** is noninverting. [Compare it to the inverting characteristic in Fig. 18.21(d).]

go slightly positive. The value of v_I that causes this to happen is the high-threshold voltage V_{TH}, which can be found by substituting in Eq. (18.30) $v_O = L_-$ and $v_+ = 0$. The result is

$$V_{TH} = -L_-(R_1/R_2) \tag{18.32}$$

The complete transfer characteristic of the circuit of Fig. 18.22(a) is displayed in Fig. 18.22(b). Observe that a positive triggering signal v_I (of value greater than V_{TH}) causes the circuit to switch to the positive state (v_O goes from L_- to L_+). Thus the transfer characteristic of this circuit is noninverting.

18.4.6 Application of the Bistable Circuit as a Comparator

The comparator is an analog-circuit building block that is used in a variety of applications ranging from detecting the level of an input signal relative to a preset threshold value to the design of analog-to-digital (A/D) converters. Although one normally thinks of the comparator as having a single threshold value [see Fig. 18.23(a)], it is useful in many applications to add hysteresis to the comparator characteristic. If this is done, the comparator

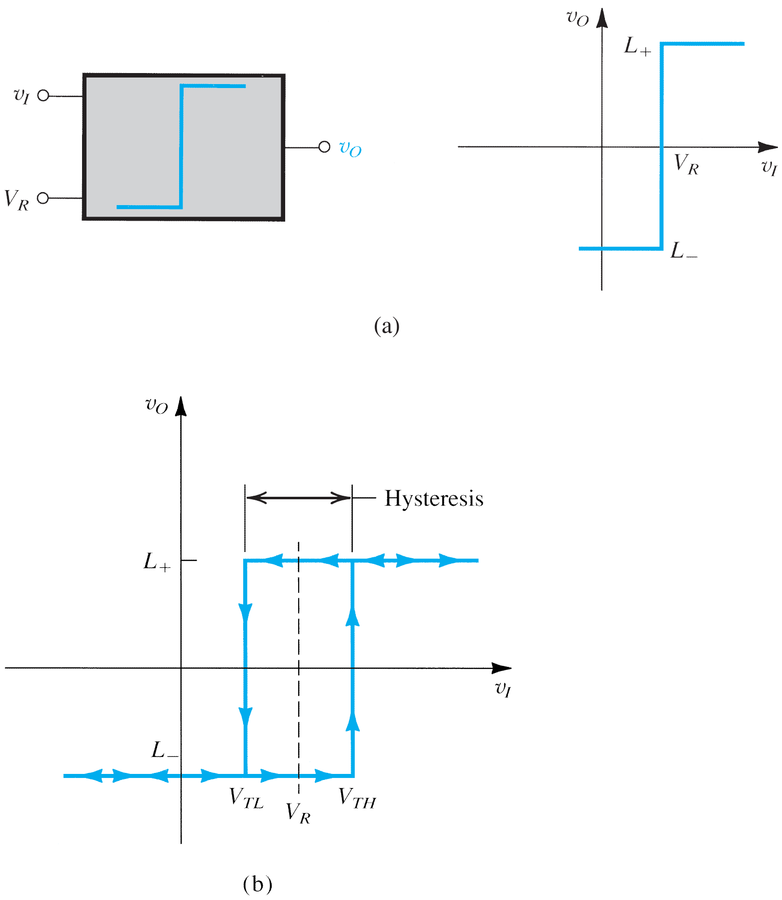

Figure 18.23 **(a)** Block diagram representation and transfer characteristic for a comparator having a reference, or threshold, voltage V_R. **(b)** Comparator characteristic with hysteresis.

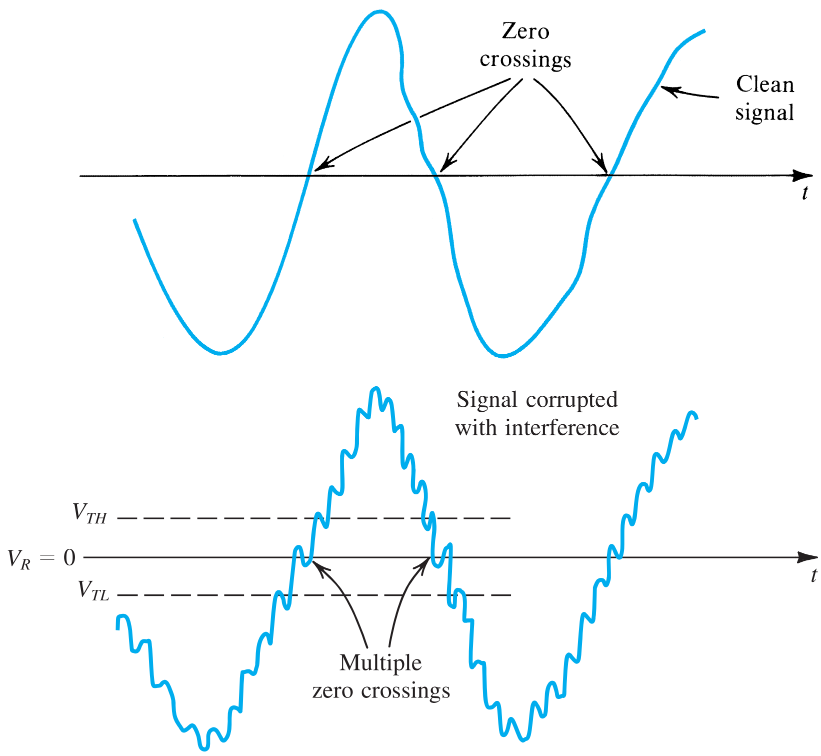

Figure 18.24 Illustrating the use of hysteresis in the comparator characteristic as a means of rejecting interference.

exhibits two threshold values, V_{TL} and V_{TH}, symmetrically placed about the desired reference level, as indicated in Fig. 18.23(b). Usually V_{TH} and V_{TL} are separated by a small amount, say 100 mV.

To demonstrate the need for hysteresis, we consider a common application of comparators. It is required to design a circuit that detects and counts the zero crossings of an arbitrary waveform. Such a function can be implemented using a comparator whose threshold is set to 0 V. The comparator provides a step change at its output every time a zero crossing occurs. Each step change can be used to generate a pulse, and the pulses are fed to a counter circuit.

Imagine now what happens if the signal being processed has—as it usually does have—interference superimposed on it, say of a frequency much higher than that of the signal. It follows that the signal might cross the zero axis a number of times around each of the zero-crossing points we are trying to detect, as shown in Fig. 18.24. The comparator would thus change state a number of times at each of the zero crossings, and our count would obviously be in error. However, if we have an idea of the expected peak-to-peak amplitude of the interference, the problem can be solved by introducing hysteresis of appropriate width in the comparator characteristics. Then, if the input signal is increasing in magnitude, the comparator with hysteresis will remain in the low state until the input level exceeds the high threshold V_{TH}. Subsequently the comparator will remain in the high state even if, owing to interference, the signal decreases below V_{TH}. The comparator will switch to the low state only if the input signal is decreased below the low threshold V_{TL}. The situation is illustrated