DIC Experiment Lab1

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Contents

1 Introduction **2**

2 Lab Procedures and Results **3**
2.1 Simulation Settings 3
2.2 Task1. Plot $I_{DS} - V_{DS}$ Curves 3
2.2.1 Part1. bulk Silicon MOSFETs 3
2.2.2 Part2. FinFETs 4
2.3 Task2. Measure important parameters 5
2.3.1 Measure I_{on} and I_{off} 5
2.3.2 Measure thershold voltage V_T 6
2.3.3 Measure Subthrehold Slope(SS) 7

3 Technical Analysis of the Simulation Results **8**
3.1 Measurement methods 8
3.2 Effect of Channel Width Variation on Device Characteristics 8
3.3 Effects of Temperature Variation on Device Characteristics 9
3.4 Comparison of different devices: bulk Si-MOSFETs and FinFET 9

4 Observations and conclusions **11**

1 Introduction

This lab focuses on the simulation and comparison of two key transistor technologies: the planar bulk Silicon MOSFET and the 3D FinFET. As device scaling reaches nanoscale dimensions, the planar MOSFET suffers from poor gate electrostatic control, leading to significant short-channel effects like high leakage current. The FinFET architecture addresses this by employing a vertical "fin" structure, allowing the gate to control the channel from three sides, which dramatically improves performance and reduces leakage.

A critical difference in designing with FinFETs is the concept of width quantization. Unlike planar bulk Silicon MOSFETs, whose width can be arbitrarily sized, the effective width of a FinFET is determined by its physical geometry. The minimum width for a single fin is given by equation (1):

$$W_{\text{min}} = 2 \times H_{\text{fin}} + t_{\text{si}} \tag{1}$$

To achieve a larger drive strength of gate, multiple fins are used, making the total effective width given by equation (2):

$$W_{\text{total}} = n \times (2 \times H_{\text{fin}} + t_{\text{si}}) \tag{2}$$

The objective of this lab is to use HSPICE simulations with Predictive Technology Models (PTM) to analyze the DC characteristics of 16nm bulk MOSFETs and 20nm FinFETs. Key tasks include:

1. Plot $I_{\text{DS}} - V_{\text{DS}}$ Curves
2. Measure important parameters: I_{on}, I_{off} and V_{T}
3. Optional: Subthrehold Slope(SS)

2 Lab Procedures and Results

2.1 Simulation Settings

- $L_g = 20$nm for ptm16hp FinFETs while $L_g = 16$nm for ptm16hp bulk Si-MOSFETs.
- Supply voltage is 0.75V for both FinFETs and bulk SiMOSFETs.
- Simulation temperature: $T = 25°C$.
- Under 16nm process, $\lambda = 8$nm.

2.2 Task1. Plot $I_{DS} - V_{DS}$ Curves

2.2.1 Part1. bulk Silicon MOSFETs

Requirements

For both N-Channel and P-Channel bulk silicon MOSFETs, plot the $I_{DS} - V_{DS}$ Curves when the gate-source voltage is fixed at 0.75V.

At the same time, scanning parameter **width** increases from 16λ to 48λ with a step size of 8λ.

Procedures

step1. Parameter Settings and Lib importing

```
* parameter config
.param lambda=8nm
.param Width='16*lambda'
.param Vgs_n=0.75
.param Vgs_p=-0.75
.temp 25
* lib config
.include '../Lab_LIB/Bulk/16nm_HP.pm'
```

Step2. Stimulus and Device Definition

Set the NMOS gate voltage to 0.75V, the source and bulk to ground (0V), the channel length to 16nm, and the channel width as the parameter to be scanned, with the value parameter: "Width". Repeat the similar process for the PMOS.

```
* motivation source for nmos
VGS_N gate_n 0 'Vgs_n'
VDS_N drain_n 0 0
* motivation source for nmos
VGS_P gate_p 0 'Vgs_p'
VDS_P drain_p 0 0
* Bulk device definition for NMOS
MNFET drain_n gate_n 0 0 nmos L='2*lambda' W='Width'
* Bulk device definition for PMOS
MPFET drain_p gate_p 0 0 pmos L='2*lambda' W='Width'
```

Step3. DC Simulatiojn

For NMOS, sweep V_{DS} from 0V to 0.85V, take a point every 0.01V, obtain the drain-source current at each DC operating point, then draw a curve.

Repeat the similar process for the PMOS. It is worth noting that the drain-source V_{DS} voltage of PMOS needs to be swept from 0V to -0.85V.

```
* DC analysis - Sweep VDS from 0 to 0.85V for different fin numbers
.dc VDS_N 0 0.85 0.01 sweep Width '16*lambda' '48*lambda' '8*lambda'
.probe DC I(VDS_N)
.dc VDS_P 0 -0.85 -0.01 sweep Width '16*lambda' '48*lambda' '8*lambda'
.probe DC I(VDS_P)
```

Step4. Plot the $I_{DS} - V_{DS}$ curve

From above procedures we obtain two waveform data files: Task1_Bulk.sw0 and Task_Bulk.sw1.

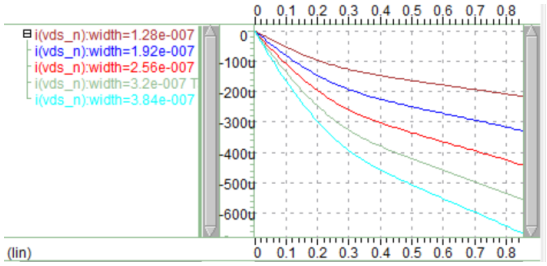
In CustomExplorer, we plot the $I_{DS}-V_{DS}$ curve for both NMOS(Fig.1a) and PMOS(Fig.1b).

It is worth noting that in hspice, the direction of current is defined as positive when flowing into the voltage source and negative when flowing out of the voltage source.

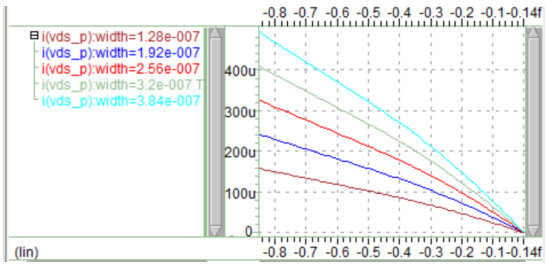
Results

1. Widths/lengths of transistors: Length: 16nm, Width: 128nm, 192nm, 256nm, 320nm, 384nm.

2. $U_{DS} - V_{DS}$ curves:



(a) NMOS: $I_{DS} - V_{DS}$



(b) PMOS: $I_{DS} - V_{DS}$

Figure 1: $I_{DS} - V_{DS}$ curve

2.2.2 Part2. FinFETs

Requirements

For both N-Channel and P-Channel FinFETs, plot the $I_{DS} - V_{DS}$ Curves when the gate-source voltage is fixed at 0.75V.

At the same time, scanning parameter **fin number** increases from 4 to 8 with a step size of 2.

Procedures

Aside from the parameter sweep during DC simulation, the FinFET simulation steps are identical to those for bulk silicon MOSFETs. In a FinFET, the effective channel length L_g is 20nm, and the channel width is defined by equation (2). A key parameter is the counts of fins. During the FinFET simulation, the counts of fins is swept from 4 to 8 with a step size of 2:

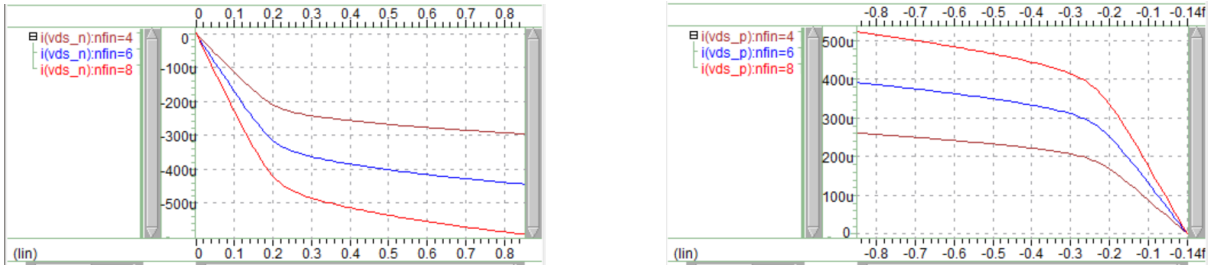
```
* DC analysis - Sweep VDS from 0 to 0.85V for different fin numbers
.dc VDS_N 0 0.85 0.01 sweep Nfin 4 8 2
.probe DC I(VDS_N)
```

```
.dc VDS_P 0 -0.85 -0.01 sweep Nfin 4 8 2
.probe DC I(VDS_P)
```

In CustomExplorer, we plot the $I_{DS}-V_{DS}$ curve for both NFET(Fig.2a) and PFET(Fig.2b).

Results

1. **Widths/lengths of transistors:** Length: 20nm, Width: 256, 384nm, 512nm
2. $U_{DS} - V_{DS}$ **curves:**



(a) NMOS: $I_{DS} - V_{DS}$ (b) PMOS: $I_{DS} - V_{DS}$

Figure 2: $I_{DS} - V_{DS}$ curve

2.3 Task2. Measure important parameters

Requirements

For both bulk silicon MOSFETs and FinFETs, for both N-Channel and P-Channel:

- All metrics need to be measured at 25°C and 9°C respectively
- The supply voltage is 0.75V for both FinFETs and bulk Si-MOSFETs
- Width = 128nm for ptm16hp bulk Si-MOSFETs while fin number = 2 for ptm16hp FinFETs.

Procedures

2.3.1 Measure I_{on} and I_{off}

For N-Channel, the on-state current I_{on} is measured when $V_{GS} = V_{DD}$ and $V_{DS} = V_{DD}$ while the off-state current I_{off} is measured when $V_{GS} = 0$ and $V_{DS} = V_{DD}$.

For P-Channel, the on-state current I_{on} is measured when $V_{GS} = 0$ and $V_{DS} = -V_{DD}$ while the off-state current I_{off} is measured when $V_{GS} = -V_{DD}$ and $V_{DS} = -V_{DD}$.

For bulk Silicon MOSFETs, the HSPICE codes to measure the two currents are as follows, which has considered situations both in 25°C and 90°C.

```
********** temperature = 25 *****************
.dc VG_N 0 0.8 0.01
.probe DC I(VG_N)
.measure DC Ion_n FIND I(VD_N) WHEN V(gate_n) = 'supply'
.measure DC Ioff_n FIND I(VD_N) WHEN V(gate_n) = 0
.dc VG_P 0 -0.8 -0.01
.probe   DC I(VG_P)
.measure DC Ion_p FIND I(VD_P) WHEN V(gate_p) = '-supply'
.measure DC Ioff_p FIND I(VD_P) WHEN V(gate_p) = 0
```

```
********** temperature = 90 *****************
.alter
.temp 90
.dc VG_N 0 0.8 0.01
.probe DC I(VG_N)
.measure DC Ion_n FIND I(VD_N) WHEN V(gate_n) = 'supply'
.measure DC Ioff_n FIND I(VD_N) WHEN V(gate_n) = 0
.dc VG_P 0 -0.8 -0.01
.probe   DC I(VG_P)
.measure DC Ion_p FIND I(VD_P) WHEN V(gate_p) = '-supply'
.measure DC Ioff_p FIND I(VD_P) WHEN V(gate_p) = 0
```

When we consider FinFETs, the code is almost completely consistent, thus omitted here.

2.3.2 Measure thershold voltage V_T

Constant current method defines threshold as the gate voltage at a given drain current I_{crit}. A typical choice of I_{crit} is $\frac{W}{L} \times 0.3\mu A$. In this experiment, we choose $\frac{W}{L} \times 0.3\mu A$ as I_{crit}. But it is worth noting that for different process, the width and length of the channel of the transistor are different. In bulk silicon MOSFETs, the length is 16nm and width is 128nm. However, in FinFETs, the length is 20nm and width is also 128nm, which is calculated by equation (2) when the fin counts is 2.

Take the HSPICE code of measuring the V_T of FinFETs as an example. In this time, we sweep the voltage of gate-source, from 0V to 0.8V for NFET and from 0V to -0.8V for PFET. What we should pay more attention to is that the level of source and bulk should be the same.

```
********** temperature = 25 *****************
.dc VG_N 0 0.8 0.01
.probe DC I(VG_N)
.measure DC VTH_n FIND V(gate_n) WHEN I(VD_N) =
   '-0.3u*Width/Lg_fin'
.dc VG_P 0 -0.8 -0.01
.probe DC I(VG_P)
.measure DC VTH_p FIND V(gate_p) WHEN I(VD_P) =
   '0.3u*Width/Lg_fin'
********** temperature = 90 *****************
.alter
.temp 90
.dc VG_N 0 0.8 0.01
.probe DC I(VG_N)
.measure DC VTH_n FIND V(gate_n) WHEN I(VD_N) =
   '-0.3u*Width/Lg_fin'
.dc VG_P 0 -0.8 -0.01
.probe DC I(VG_P)
.measure DC VTH_p FIND V(gate_p) WHEN I(VD_P) =
   '0.3u*Width/Lg_fin'
```

Results

1. Widths/lengths of transistors

bulk Silicon MOSFETs: Length: 16nm, Width: 128nm

bulk Silicon MOSFETs: Length: 20nm, Width: 128nm

2. Date Table

The turn-on current I_{on}, turn-off current I_{off}, and threshold voltage V_T of MOSFETs of different processes and channel types at different temperatures measured using the HSPICE measure statement are shown in Tab.1 and Tab.2.

Process	Channel	Width/Width$_{eff}$(nm)	I_{on}	I_{off}	I_{on}/I_{off}	V_T
Bulk	NMOS	128	200.1μA	85.42nA	2343	0.1465V
	PMOS	128	142.1μA	116.5nA	1220	-0.1364V
FinFET	NMOS	128 (Fin num=2)	144.5μA	9.412nA	15353	0.1758V
	PMOS	128 (Fin num=2)	126.9μA	8.594nA	14766	-0.1800V

Table 1: I_{on}, I_{off} and V_T for four transistors at temp = 25°C

Process	Channel	Width/Width$_{eff}$(nm)	I_{on}	I_{off}	I_{on}/I_{off}	V_T
Bulk	NMOS	128	168.3μA	185nA	910	0.1377V
	PMOS	128	92.59μA	204.7nA	452	-0.1333V
FinFET	NMOS	128 (Fin num=2)	157.3μA	89.76nA	1752	0.1246V
	PMOS	128 (Fin num=2)	141.4μA	127.5nA	1109	-0.1120V

Table 2: I_{on}, I_{off} and V_T for four transistors at temp = 90°C

2.3.3 Measure Subthrehold Slope(SS)

Procedures

The subthreshold slope is defined as the change in voltage for every tenfold change in current in the subthreshold region. Therefore, using the constant current method, given a current, simulation can determine the gate-source voltage of the transistor at that current and one-tenth of that current. The difference provides an approximate value for the subthreshold slope.

It is worth noting that as the aspect ratio increases, transistor drain-source current increases, and the selected constant current should also increase accordingly. Therefore, at the same temperature, since the aspect ratio of FinFETs is 6.4 and that of bulk Silicon MOSFETs is 8, the constant current selected for FinFETs should be smaller than that for bulk Silicon MOSFETs. Furthermore, as temperature increases, the transistor threshold voltage decreases, and the selected constant current should also increase accordingly.

Take the HSPICE code of measuring the V_T of bulk Silicon as an example. In this time, we sweep the voltage of gate-source, from 0V to 0.8V for NMOS and from 0V to -0.8V for PMOS. When we find the current I_{DS} reaching the specified value, we record the current gate voltage. The voltage difference between the two recordings is the subthreshold slope.

results

bulk Silicon MOSFETs: Length: 16nm, Width: 128nm

bulk Silicon MOSFETs: Length: 20nm, Width: 128nm

2. Date Table

The SS of MOSFETs of different processes and channel types at different temperatures measured using the HSPICE measure statement are shown in Tab.3 and Tab4.

Process	Channel	Width/Width$_{\text{eff}}$(nm)	V_1	V_2	SS
Bulk	NMOS	128	0.1727V	0.06428V	0.1084V/dec
	PMOS	128	-0.1640V	-0.05218V	0.1118V/dec
FinFET	NMOS	128 (Fin num=2)	0.1875V	0.1055V	0.082V/dec
	PMOS	128 (Fin num=2)	-0.2017V	-0.1160V	0.0917V/dec

Table 3: SS for four transistors at temp = 25°C

Process	Channel	Width/Width$_{\text{eff}}$(nm)	V_1	V_2	SS
Bulk	NMOS	128	0.1802V	0.04894V	0.1331V/dec
	PMOS	128	-0.1787V	-0.04347V	0.1352V/dec
FinFET	NMOS	128 (Fin num=2)	0.1381V	0.04102V	0.097V/dec
	PMOS	128 (Fin num=2)	-0.1257V	-0.02725V	0.0985V/dec

Table 4: SS for four transistors at temp = 90°C

3 Technical Analysis of the Simulation Results

3.1 Measurement methods

In this lab, key device parameters are extracted using HSPICE measurement statements.

I_{on} and I_{off} are measured by fixing VGS and VDS at supply voltage levels corresponding to ON and OFF states, respectively. For NMOS, Ion is obtained at (VGS = VDD, VDS = VDD), while Ioff is taken at (VGS = 0, VDS = VDD). For PMOS, symmetric conditions with negative supply are applied.

Threshold voltage V_{T} is extracted using the constant current method, with $I_{\text{crit}} = \frac{W}{L} \times 0.3\mu\text{A}$.

Subthreshold slope SS is measured by identifying the gate voltages corresponding to drain currents differing by one decade (e.g., 0.5 μA and 0.05 μA for NMOS in 25°C), and calculating the voltage difference.

3.2 Effect of Channel Width Variation on Device Characteristics

Fig.1 shows that for both NMOS and PMOS transistors, when the gate length remains constant and the gate width increases from 128nm to 384nm in a planar silicon process, drain-source current increases nearly threefold across all voltage ranges. For example, at a drain voltage of 0.75V, the drain-source current is approximately 200μA with a 128nm gate width, but increases to 600μA with a 384nm gate width.

A similar phenomenon occurs in FinFET processes. When the number of fins increases from 4 to 8, the transistor's drain-source current also increases by a factor of two, as shown in Fig.2. This is because the gate width is proportional to the number of fins.

The nearly linear increase in on-state drain-source current with increasing aspect ratio can be reflected by the following drain-source current equation:

$$I_{\text{DS}} = k' \frac{W}{L} [(V_{\text{GS}} - V_{\text{min}}) V_{\text{min}} - \frac{1}{2} V_{\text{min}}^2], V_{\text{min}} = \min\{V_{\text{GT}}, V_{\text{DSAT}}, V_{\text{DS}}\} \tag{3}$$

3.3 Effects of Temperature Variation on Device Characteristics

Temperature effects exhibited significant technology dependence. At 90°C compared to 25°C:

For bulk silicon MOSFETs: I_{on}/I_{off} ratio decreased by 61% for NMOS (2343 → 910) and 63% for PMOS (1220 → 452), primarily due to I_{off} increasing by 117% for NMOS and 76% for PMOS.

FinFETs I_{on}/I_{off} ratio decreased by 89% for NMOS (15353 → 1752) and 92% for PMOS (14766 → 1109), with more rapid I_{off} increases.

The threshold voltage temperature coefficient was more pronounced in FinFETs, with V_T decreasing by 29% for NFET and 38% for PFET, compared to 6% and 2% respectively in bulk devices. This proves why the off-state current of FinFET increases so dramatically when the temperature increases from 25°C Celsius to 90°C Celsius. Because we have eq.4:

$$I_{\mathrm{DS_{sub}}} \propto e^{\frac{V_{\mathrm{GS}}-V_{\mathrm{T}}}{nV_{\mathrm{T}}}} \tag{4}$$

This suggests different carrier transport mechanisms and mobility temperature dependence between the two technologies.

3.4 Comparison of different devices: bulk Si-MOSFETs and FinFET

The data from Tab.1 and Tab.2 reveals FinFET's obvious advantages in nanoscale regimes:

Leakage Performance: FinFETs show dramatically lower off-state currents: 9.4nA vs 85.4nA for NMOS and 8.6nA vs 116.5nA for PMOS at 25°C, representing 89% and 93% reduction respectively. This severe deterioration can be seen in the Fig.3. The blue curve represents the $I_{\mathrm{DS}} - V_{\mathrm{GS}}$ curve at 25°C, and the red curve represents the case at 90°C. It can be obviously seen that the leakage current at 90°C has increased significantly compared to the case at 25°C.

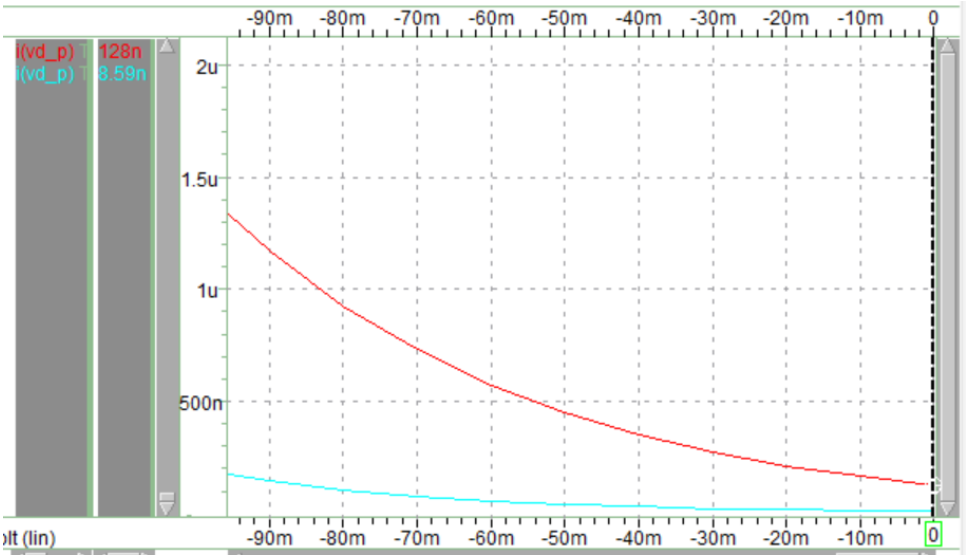


Figure 3: I_{off} comparison for PFET at 25°C and 90°C

Current Ratio: The I_{on}/I_{off} ratio favors FinFETs by 6.5 times for NMOS and 12 times for PMOS at 25°C, highlighting better switching characteristics.

Electrostatic Control: FinFETs exhibit superior subthreshold characteristics with SS values of 82-98 mV/dec compared to 108-135 mV/dec for bulk MOSFETs. The 25% better SS at 25°C demonstrates enhanced gate control.

4 Observations and conclusions

From the simulation experiments, several key observations can be made:

About Temperature dependence:

Both bulk silicon MOSFETs and FinFETs experience an increase in off-state leakage current I_{off} with rising temperature. However, the increase is much more pronounced in FinFETs. This is consistent with the stronger temperature sensitivity of FinFET threshold voltage, which drops significantly as temperature rises. The sharp reduction in V_{T} shifts the device into stronger inversion even at low gate voltages, resulting in a dramatic Ioff increase.

About Device comparison:

At room temperature, FinFETs clearly outperform bulk MOSFETs with lower leakage current, higher $I_{\text{on}}/I_{\text{off}}$ ratio, and steeper subthreshold slope. But at elevated temperature, while FinFETs still maintain advantages, their Ioff increases faster than in bulk devices, narrowing the performance gap.

About my understanding to DIC course:

Through this experiment, I learned the fundamentals of transistor-level circuit simulation using HSpice. By comparing bulk silicon MOSFETs and FinFETs, I also intuitively experienced the detrimental effects of rising temperature on transistor leakage, as well as the FinFET's highly effective gate-controlled structure in suppressing leakage at room temperature.

This experiment deepened my understanding of transistor-level design metrics in basic digital integrated circuits, including aspect ratio, leakage current, and subthreshold characteristics. This will be beneficial for my future studies.