# Digital Integrated Circuits

## Lab 2

## Inverter Simulation

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2025/10/21

# Outline

- Hspice
- Lab Contents
- Report Requirements

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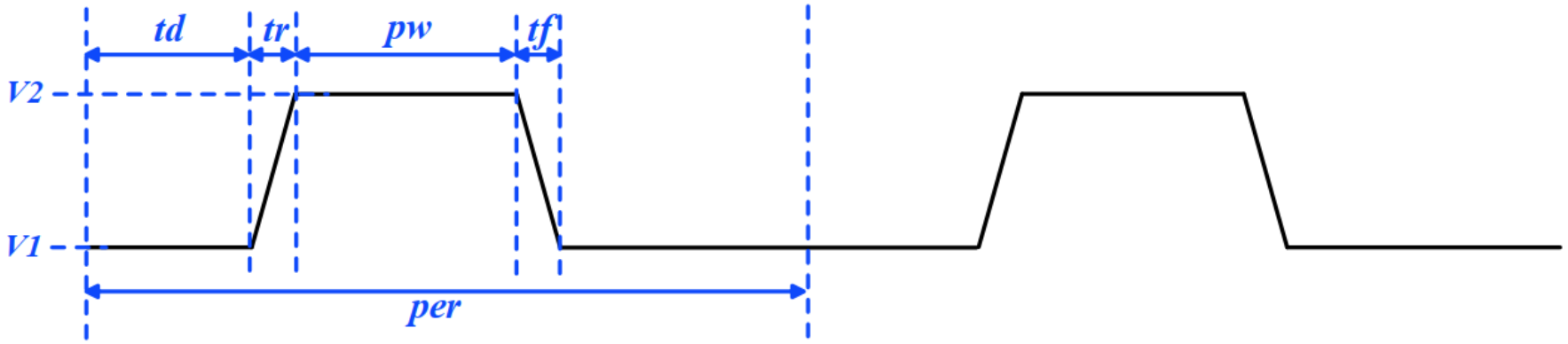
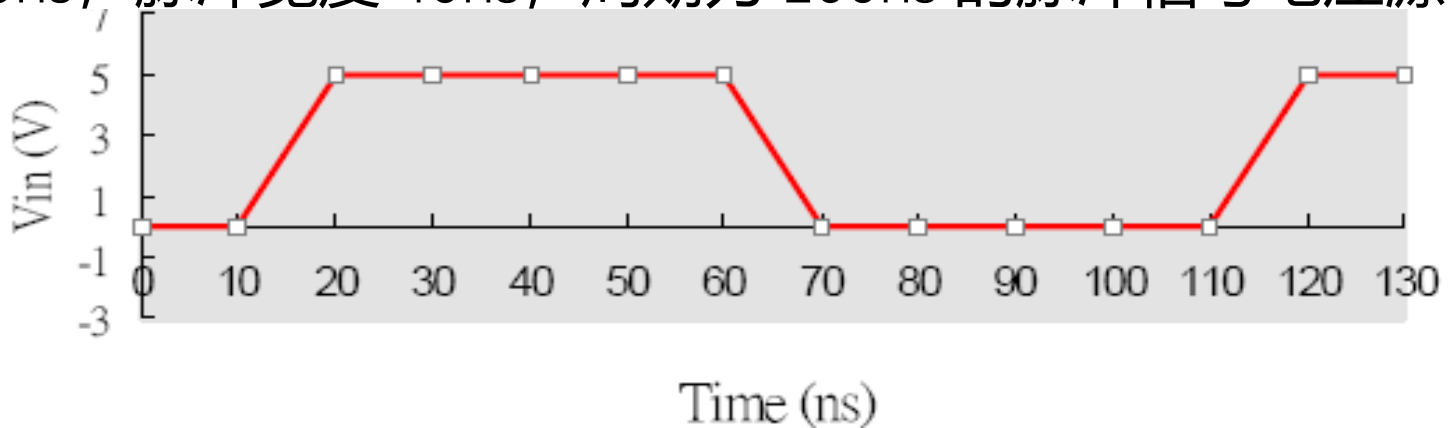
# 常用激励源 — 脉冲电压源

**Vxxx n+ n- pulse/pu <(> V1 V2 <td<tr<tf<pw<per>>>> <)>**




➢ **示例：Vin 1 0 PULSE ( 0V 5V 10ns 10ns 10ns 40ns 100ns )**

定义了一个低电平为 0V，高电平为 5V，延迟为 10ns，脉冲上升延迟10ns，下降延迟 10ns，脉冲宽度 40ns，周期为 100ns 的脉冲信号电压源



# 上升/下降时间、延时测量

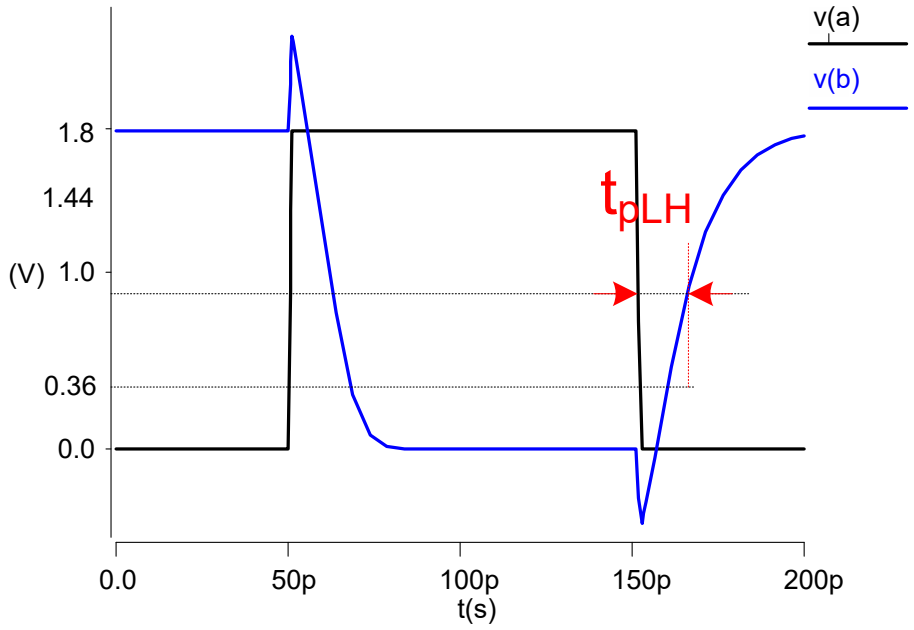
- TRIG 和 TRAG 可以配合.MEASURE 语句测量特定事件发生之间的延迟

.MEASURE <DC|AC|TRAN> result TRIG … TARG … <MINVAL=val> <WEIGHT=val>

**示例：**

.MEASURE TRAN tpLH
+ TRIG  V(a) VAL='SUPPLY/2’  FALL=1
+ TARG V(b) VAL='SUPPLY/2’  RISE=1

**本示例测量了从 a 节点第一次在下降沿中达到 SUPPLY/2 开始，到 b 节点第一次在上升沿中达到 SUPPLY/2 结束间的延迟时间。**



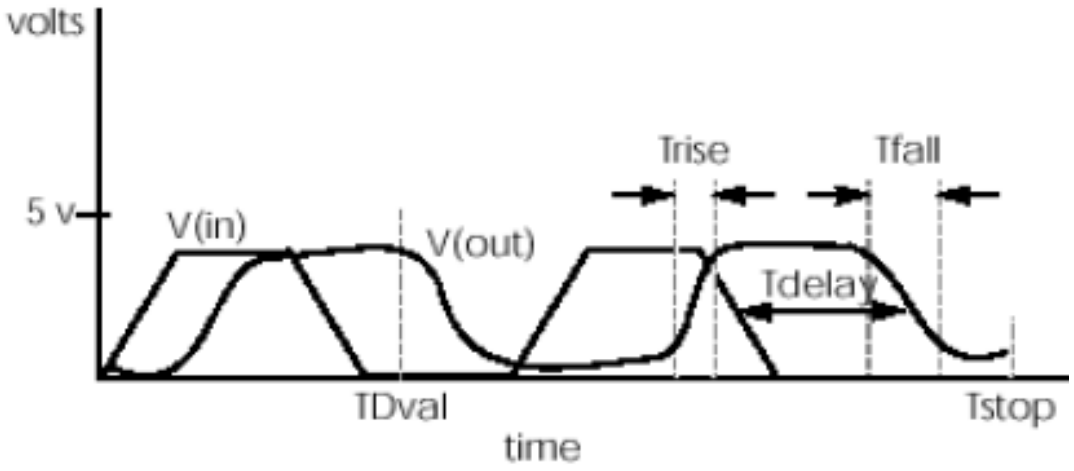
# 上升/下降时间、延时测量（cont.）

- **TRIG 和 TRAG 可以配合.MEASURE 语句测量特定事件发生之间的延迟**

**.MEASURE <DC|AC|TRAN> result TRIG … TARG … <MINVAL=val> <WEIGHT=val>**

**示例：**

.meas TRAN Trise
+ TRIG v(out) VAL='Vmin+0.1*Vmax' RISE=1
+ TARG v(out) VAl='0.9*Vmax' RISE=1
.meas TRAN Tfall
+ TRIG v(out) VAL='0.9*Vmax' FALL=2
+ TARG v(out) VAl='Vmin+0.1*Vmax' FALL=2
.meas TRAN Tdelay
+ TRIG v(in) VAL=2.5 FALL=1
+ TARG v(out) VAL=2.5 FALL=2



# 功耗测量

- HSPICE can measure power
  - Instantaneous P(t)
  - Or average P over some interval

```
.print P(vdd)
.measure pwr AVG P(vdd) FROM=0ns TO=10ns
```

⇨**测量电压源 Vdd在 0ns-100ns 间的平均功耗**

- Power in single gate
  - Connect to separate $V_{DD}$ supply
  - Be careful about input power

# 输入控制语句 .DATA

## .data

- 基于数据驱动的分析允许用户修改任意数量的参数。
- 可以系统罗列需要分析扫描的参数列表。

```
* Inline .DATA example
.Tran 1n 100n SWEEP DATA=devinf
.AC DEC 10Hz 100kHz SWEEP DATA=devinf
.DC TEMP -55 125 10 SWEEP DATA=devinf
*
.DATA devinf Width Length Vth Cap
+                10u   100u   2v   5p
+                50u   600u  10v 10p
+               100u   200u   5v  20p
.ENDDATA
```

```
* Multiline .DATA example
.PARAM Vds=0 Vbs=0 L=1.0u
.DC DATA=vdot
.DATA vdot
 Vbs        Vds        L
+0          0.1        1.0u
+0          0.1        1.5u
+-1         0.1        1.0u
+0          0.5        1.0u
.ENDDATA
```

DATA Statement: Inline or Multiline

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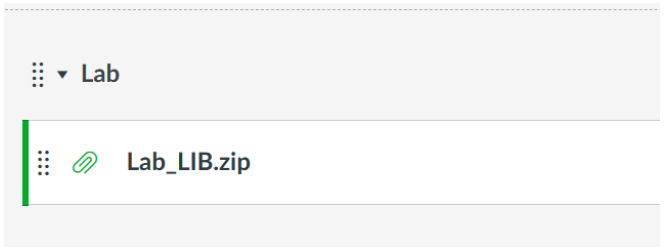
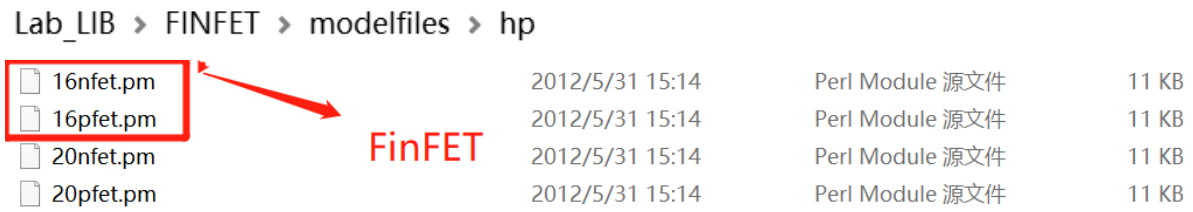
# Device Models for Inverter Simulation

- Use the Predictive Technology Model (PTM) to evaluate the DC characteristics of ptm16hp FinFETs
  - PTM model is released in Lab section
  - Use the high-power (HP) models
  - For both n-channel and p-channel devices



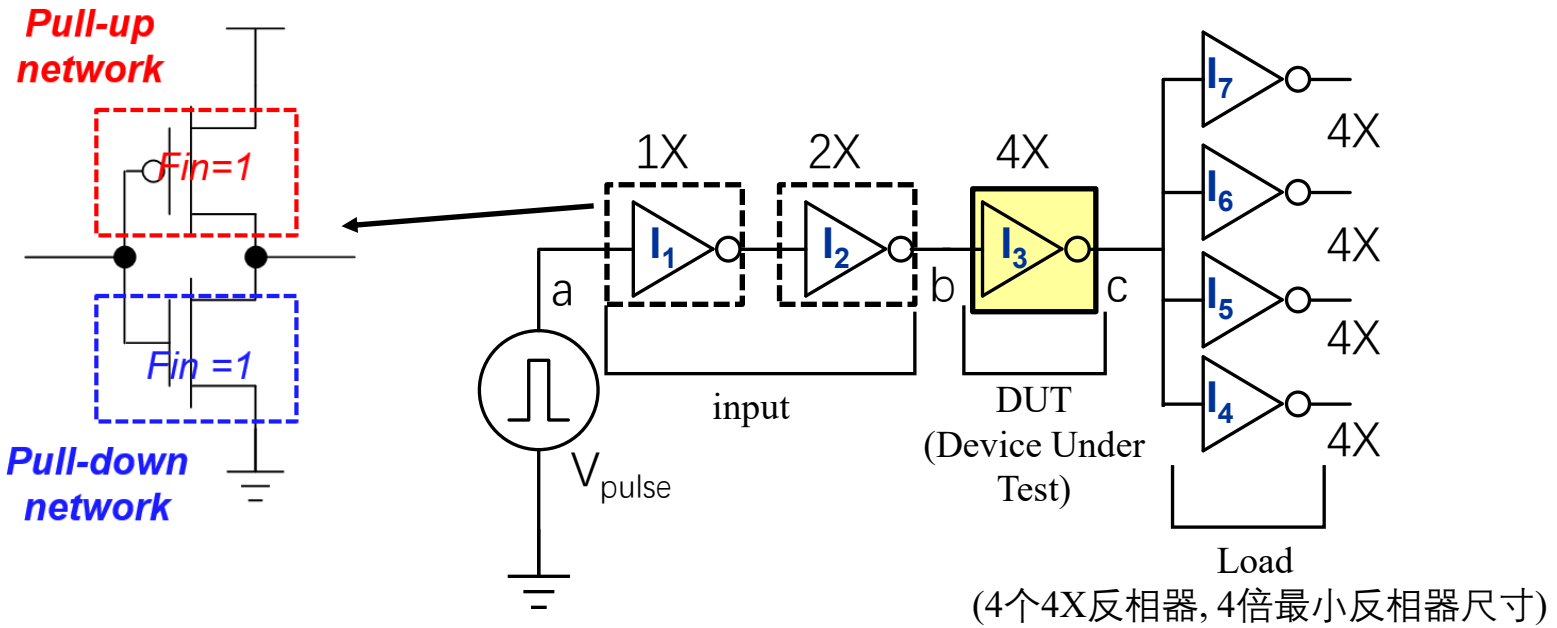



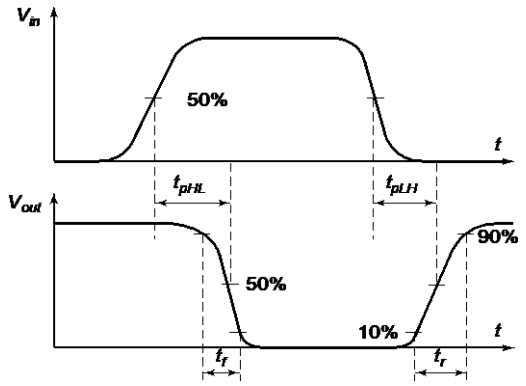
# Simulation Settings

- Lg = 20nm for ptm16hp FinFETs
- Supply voltage is 0.75V for FinFETs
- Simulation temperature
  - T = 25˚C

# Task 1: CMOS Inverter FO4 Delay Measurement

- Measure FO4 delay ($t_{pLH}$, $t_{pHL}$, $t_p$) of inverter



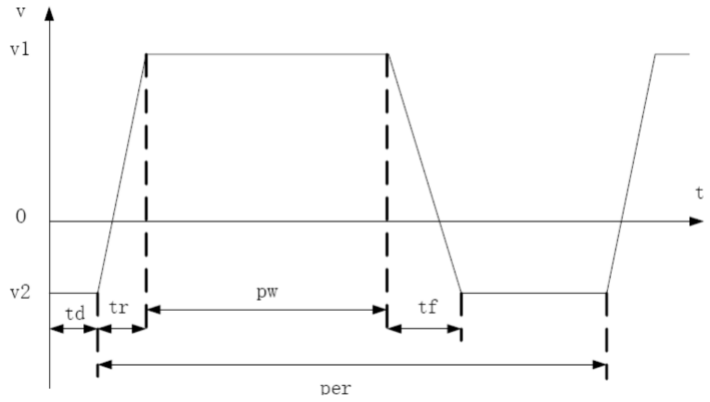




$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$

| Vpulse | Value |
|---|---|
| V1 | 0V |
| V2 | 0.75V |
| Delay Time | 400ps |
| Raise Time | 25ps |
| Fall Time | 25ps |
| Pulse Width | 400ps |
| Period | 800ps |

# Task 1: 语法提示

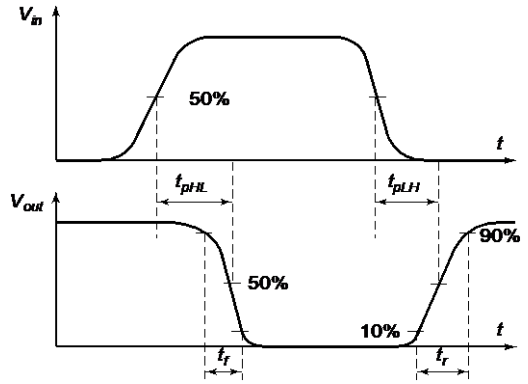
- Trapezoidal pulse : pulse




PULSE (v2 v1 td tr tf pw per)
*e.g.* VIN in 0 PULSE 0 5 2ns 2ns 2ns 30ns 80ns

- Measure delay

You can use the .MEASURE command to measure the propagation delay
For example (measure the propagation delay from b to c for L->H transition):
.MEASURE TRAN $t_{pLH}$
+ TRIG V(b)='0.5*SUPPLY' FALL=2
+ TARG V(c)='0.5*SUPPLY' RISE=2



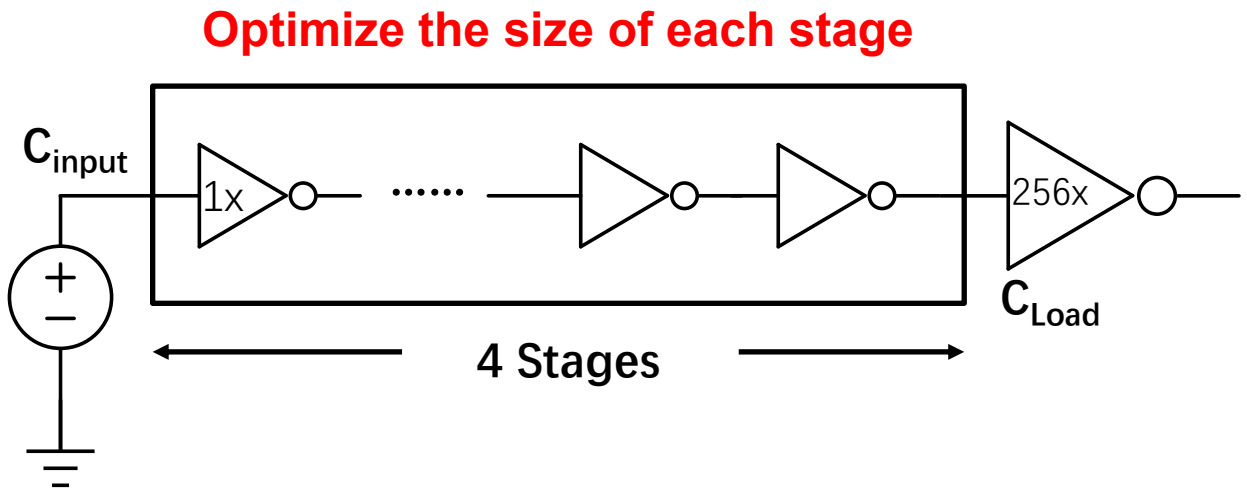

- Use function to measure tp

.measure tran tp param='(TpLH+TpHL)/2'

$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$

# Task 2: Delay Optimization for Inverter Chain

- For a inverter chain with 4 stages and 256X $C_{load}$, find the minimum delay chain design




- Design the optimum delay chain by FinFET technology

Hint:

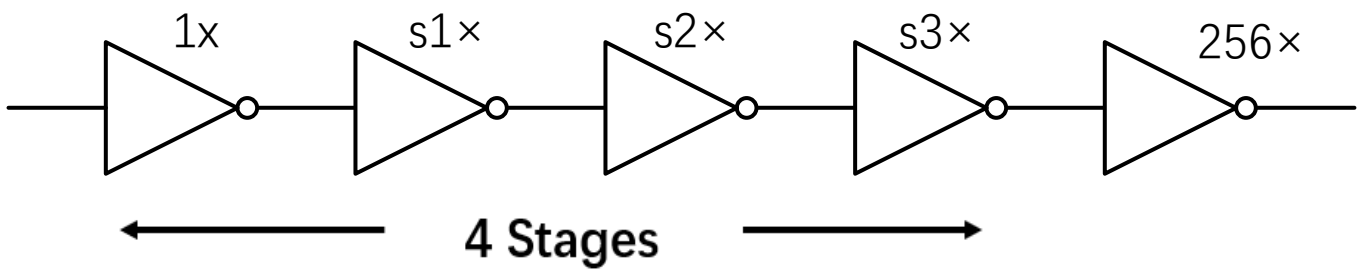
- For a given stage N, the optimum f is determined by $f = \sqrt[N]{F}$
- Note that the sizes of FinFETs should be integer number
- Different rounding method may induce different results

# Task 2: 语法提示

- Multi-points sweep

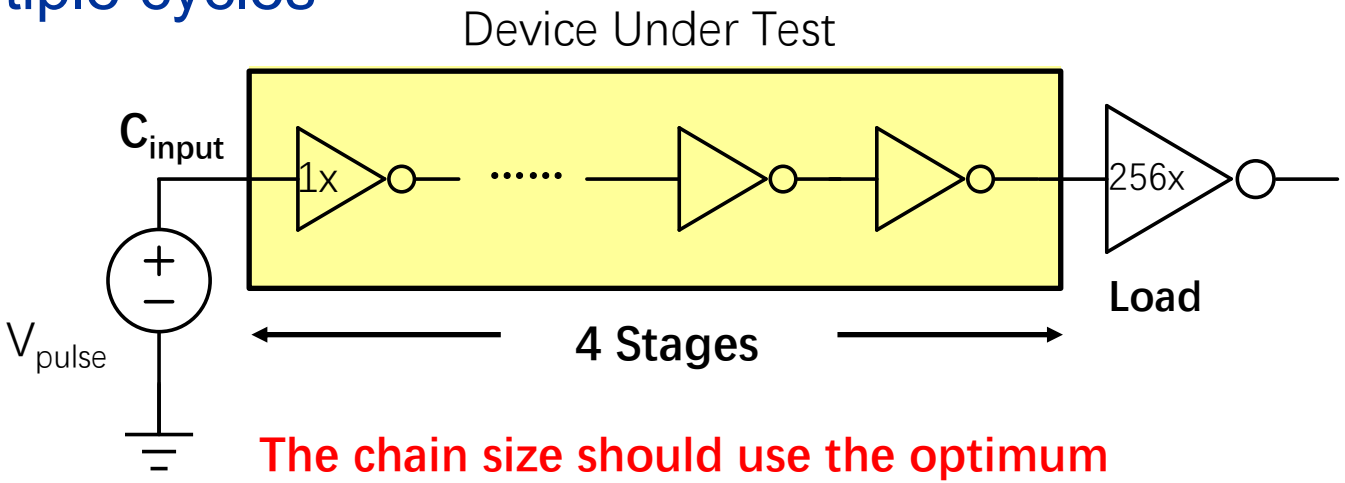
  Hint: The first inverter's fin number is one. And you can use parameters to represent the fin numbers of the following three inverters and sweep their different combinations.

```
*For example, suppose the following three inverter has fin number of s1,s2,s3

.tran 1ps 10ns sweep data=datam

.data datam s1 s2 s3
4   16   64
4   15   60
4   20   80
.enddata
```



# Task 3: CMOS Inverter Power

- Measure the power of inverter chain
  - Only include the power consumption of inverter chain
  - Apply a pulse voltage on the input node and measure the power averaging for multiple cycles




**The chain size should use the optimum values you have found**

- You can use two different power supply sources for the DUT inverter and other parts (for example, use $V_{DD1}$ for the DUT inverter while using $V_{DD2}$ for the other parts, if you have)
- The power consumption of the load part does not need to be included in the power consumption of the inverter chain under test.

# Task 3: 语法提示

- Measure power

  Hint: You can use the .MEASURE command to measure the power consumption

```
.MEASURE <DC|AC|TRAN> result func out_var FROM=val TO=val

*For example (measure the energy of the circuit from VDD)

.MEASURE TRAN avgpower AVG P(VDD) FROM=1ns TO=80ns
```

- The power consumption measurement may be negative because the current direction is flowing out of VDD.

# Task 4: EDP measurement

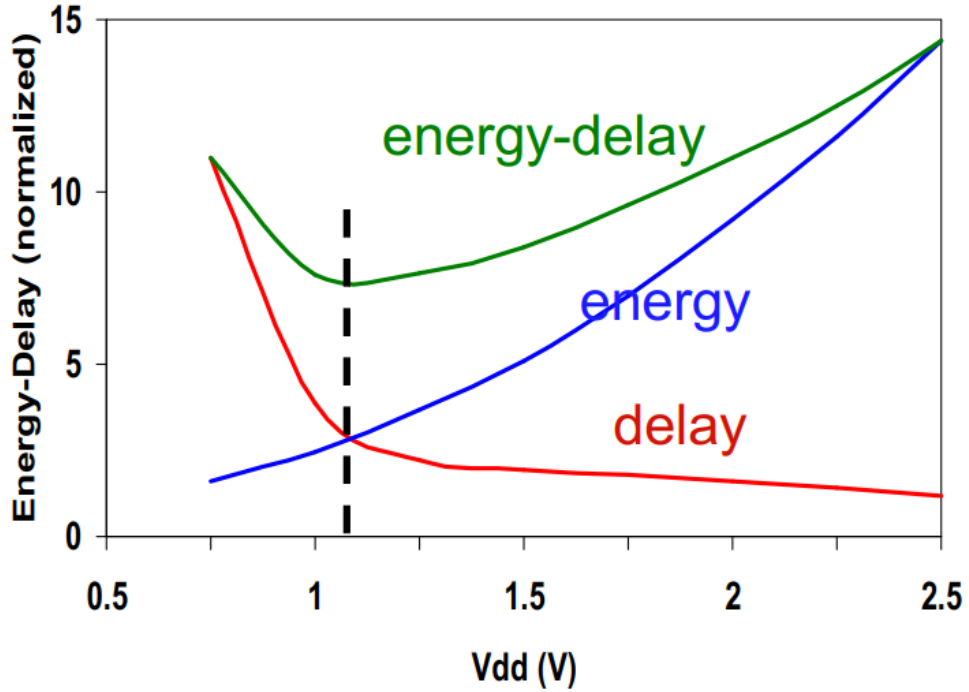
- Using optimized chain to find optimal point of Energy and delay

**Power-Delay Product (PDP):**

$$PDP = P_{av} t_p$$

**Energy-Delay Product (EDP):**

$$EDP = PDP * t_p = P_{av} t_p^2 = \frac{C_L V_{DD}^2}{2} t_p$$




Hint:

- To find ensure your results, you can sweep the VDD beyond the standard supply
- Ultral-low VDD may result in unfunctional circuit

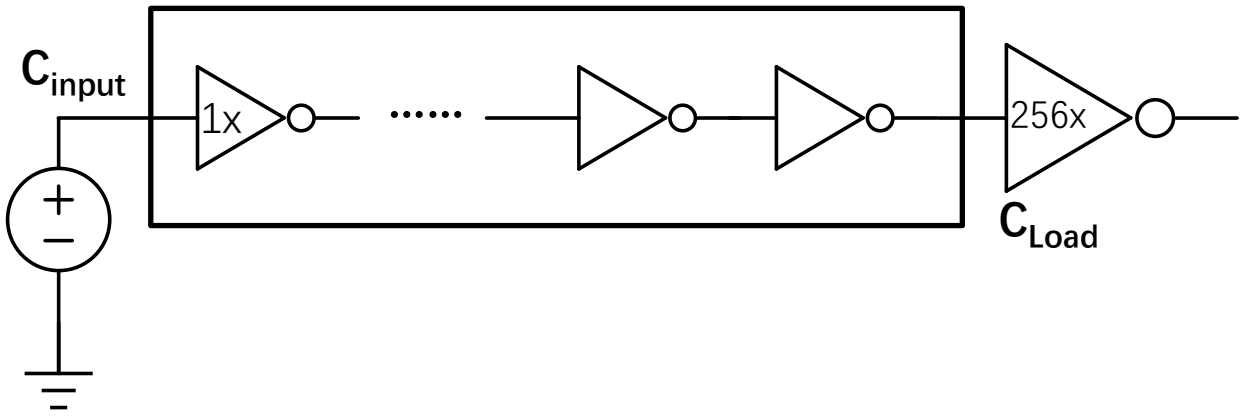
- Use function to measure EDP

```
.measure tran edp param='abs(avgpower*tp*tp)'
```

# Task 5 (Optional): Inverter chain optimization with unfixed stages

- For a given Initial stage and Cload, find the minimum delay chain design

**Optimize Stage Number and Size of each stage**




- Design the optimum delay chain by FinFET technology

Hint:

- For a given stage N, the optimum f is determined by $f = \sqrt[N]{F}$
- Sweep the N to find corresponding f
- In theory, the optimum f should satisfy

$C_L = F \cdot C_{in} = f^N C_{in}$ with $N = \frac{\ln F}{\ln f}$ $C_{int} = \gamma C_g$

$$f = \exp(1 + \gamma / f)$$

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# Report Requirement

- Write your lab report like writing a technical document (readable, comprehensive analysis, no typo…)
- You may include
  - Introduction/background
  - Lab procedures
  - Lab results
  - Technical analysis of the simulation results
  - Observations and conclusions

# Submission

- You need to submit your report and code
  - Name of report (in PDF format): lab2_report_[Name]_[Student No.].pdf
  - Name of code (compressing the files): lab2_code__[Name]_[Student No.].zip
- Please upload your report to Canvas course website
- Submission of lab2 report and code will be due on

**4th November 2025**