DIC Lab2 Report

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1 Introduction and Background

This report presents the results of Digital Integrated Circuit Lab 2, focusing on the analysis and optimization of CMOS inverter chains using FinFET technology. The primary objectives of this laboratory are:

- Measurement and characterization of inverter delay parameters (FO4 delay)
- Optimization of multi-stage inverter chains for minimum delay
- Power consumption analysis of optimized inverter chains
- Energy-Delay Product (EDP) optimization through supply voltage scaling
- Investigation of optimal stage number selection for inverter chain design

The experiments utilize HSPICE simulation with 16nm FinFET technology models. FinFET technology offers superior electrostatic control and reduced short-channel effects compared to traditional planar MOSFETs, making it suitable for advanced technology nodes. Throughout this lab, we explore fundamental trade-offs in digital circuit design, including the relationship between delay, power consumption, and energy efficiency.

The inverter chain optimization problem is particularly important in practical circuit design, where signals must drive large capacitive loads through multiple stages. By carefully selecting the number of stages and the sizing factor of each stage, we can minimize propagation delay while maintaining acceptable power consumption.

2 Task 1: FO4 Delay Measurement

2.1 Lab Procedures

The objective of Task 1 is to measure the Fan-Out-4 (FO4) delay of an inverter, which is a fundamental metric for characterizing the speed of a technology. The FO4 delay represents the propagation delay of an inverter driving four identical copies of itself.

The measurement setup consists of a chain of inverters where each inverter drives the next stage. HSPICE simulation is performed with the following key steps:

1. Define an inverter subcircuit using FinFET models
2. Create a chain of inverters with proper fan-out configuration
3. Apply a pulse input signal to the first stage
4. Measure the propagation delay **at the third inverter output**
5. Calculate both high-to-low (t_{pHL}) and low-to-high (t_{pLH}) delays using ".measure" statements

The measurement statements in HSPICE trigger on the 50% point of the supply voltage (0.5*SUPPLY) to accurately capture the propagation delay:

```
.measure tran tpLH TRIG V(in) = 0.5*SUPPLY FALL = 2 TARG V(out) =
   0.5*SUPPLY RISE = 2
.measure tran tpHL TRIG V(in) = 0.5*SUPPLY RISE = 2 TARG V(out) =
   0.5*SUPPLY FALL = 2
.measure tran tp param='(tpLH+tpHL)/2'
```

2.2 Lab Results

The simulation results for the third inverter in the chain show the following delay characteristics 1:

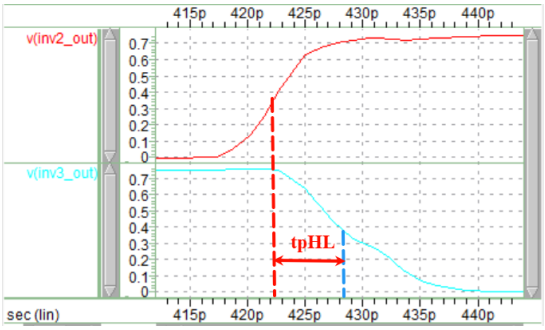
The waveform plots demonstrating the delay measurements are shown in Figures 1a and 1b.

2.3 Technical Analysis

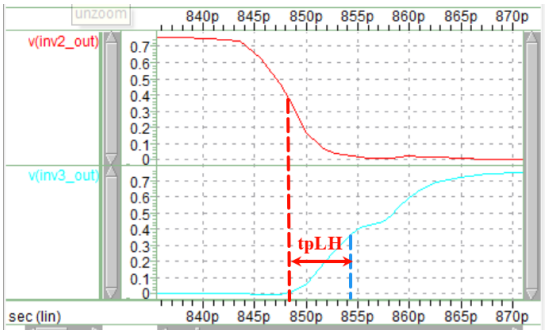
The measured FO4 delay of approximately 5.9 ps demonstrates the high-speed capability of 16nm FinFET technology. Several observations from the results:

Parameter	Value (ps)	Temperature (°C)	Alter #
t_{pLH}	6.190	25.0	1
t_{pHL}	5.633	25.0	1
t_p	5.911	25.0	1

表 1: Measured FO4 delay parameters



(a) t_{pHL} measurement waveform(for illustration only)



(b) t_{pLH} measurement waveform(for illustration only)

图 1: $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ curve

1. The t_{pHL} (5.633 ps) is slightly faster than t_{pLH} (6.190 ps), indicating that the NMOS pull-down network has higher drive strength than the PMOS pull-up network in this technology and sizing.

2. The difference between the rising delay and falling delay is only 9%, which shows that the current process and transistor size parameters are well characterized.

3 Task 2: Delay Optimization for Inverter Chain

3.1 Lab Procedures

Task 2 focuses on finding the optimal sizing of a 4-stage inverter chain driving a 256× load. The design challenge is to minimize the total propagation delay through proper selection of sizing factors for each stage.

HSPICE simulation is performed with the following key steps:

1. Fix the first stage inverter size at 1× (nfin = 1) and the load inverter size at 256× (nfin = 256)
2. Sweep sizing factors for stages 2, 3, and 4
3. Measure individual stage delays and sum to total chain delay
4. Compare results with theoretical predictions, select the optimal configuration for afterward experiment

The HSPICE circuit topology is configured as:

```
Xinv1 in inv1_out vdd 0 inv nfin = 1
Xinv2 inv1_out inv2_out vdd 0 inv nfin = 'f2'
Xinv3 inv2_out inv3_out vdd 0 inv nfin = 'f3'
Xinv4 inv3_out inv4_out vdd 0 inv nfin = 'f4'
XinvL inv4_out invL_out vdd 0 inv nfin = 256
```

Six different sizing combinations were simulated using parametric sweep:

```
.data sweepdata f2 f3 f4
+ 4  16 64
+ 4  15 60
+ 4  20 80
+ 5  16 64
+ 5  15 60
+ 5  20 80
```

3.2 Lab Results

The simulation results for all six configurations are summarized in Table 2. Key measurements include individual stage delays (t_{p1} through t_{p4}) and total chain delay (t_{p_total}).

The optimal configuration is found to be $f_2 = 5, f_3 = 15, f_4 = 60$ with a minimum total delay of **37.32 ps**.

Index	**f2**	**f3**	**f4**	t_{p1} **(ps)**	t_{p2} **(ps)**	t_{p3} **(ps)**	t_{p4} **(ps)**	t_{p_total} **(ps)**
1	4	16	64	8.360	18.86	5.991	7.738	40.95
2	4	15	60	8.295	17.76	6.012	7.785	39.86
3	4	20	80	8.428	22.65	6.429	7.929	45.43
4	5	16	64	9.439	15.88	5.600	7.255	38.18
5	5	15	60	9.492	15.09	5.506	7.238	37.32
6	5	20	80	9.414	19.16	5.762	7.446	41.78

表 2: Inverter chain delay measurements for different sizing configurations

3.3 Technical Analysis

The experimental results reveal some important deviations from classical design theory:

For a 4-stage chain with load factor F = 256, the optimal sizing factor should be $f = F^{1/N} = 256^{1/4} = 4$, suggesting uniform scaling with $f_2 = 4, f_3 = 16, f_4 = 64$. However, the practical result is that $f_2 = 5, f_3 = 15, f_4 = 60$, which deviates from the theoretical 4-16-64 progression.

The classical theory assumes identical stage designs with pure capacitive loading. However, in practical FinFET technology, input capacitance includes both gate and parasitic components, while our theory model neglects parasitics capacitance. Moreover, wire parasitic capacitance becomes significant at small feature sizes. That cause drive strength varies non-linearly with transistor sizing. The optimal factor may be slightly larger than 4 (closer to e 2.718).

Stage-by-stage analysis:

1. Stage 1 and stage 3 shows slightly higher delay with f2=5 vs f2=4 (9.5 ps vs 8.4 ps for stage 1) due to increased load

2. Stage 2 and stage 4 benefits significantly from f2=5, showing much lower delay (15.1 ps vs 18.9 ps for stage 2), while the overall delay mainly relies on stage 2 and stage 4 because their larger magnitude.

The results demonstrate that practical optimization requires consideration of technology-specific effects beyond simple analytical models.

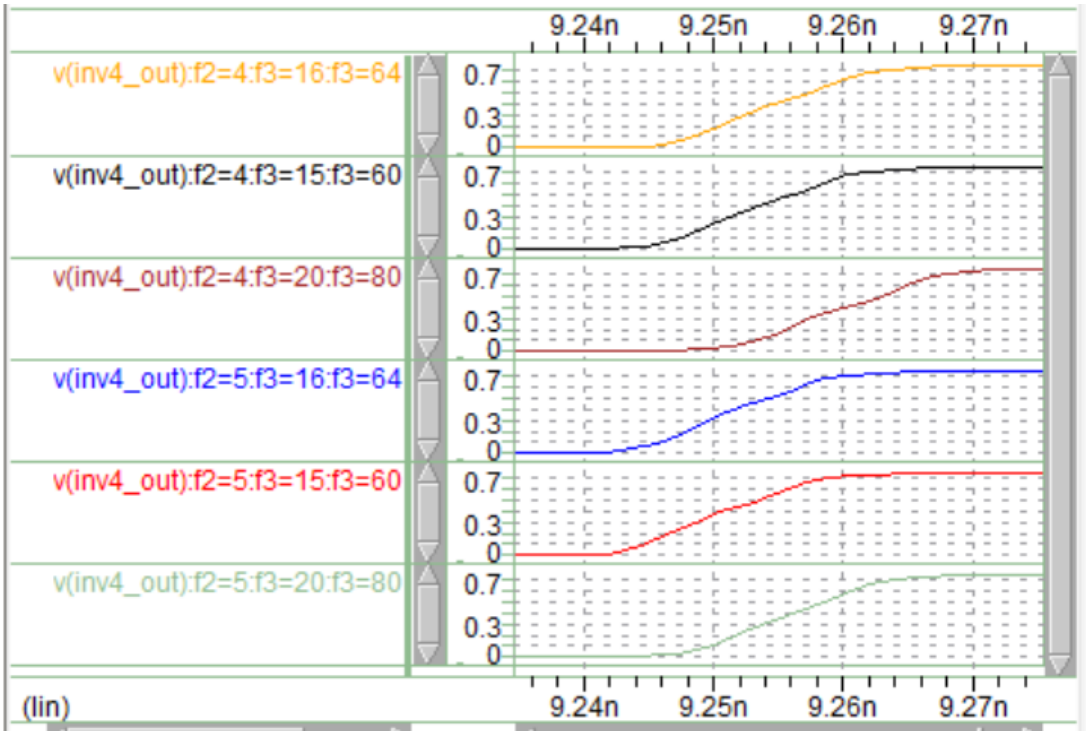


图 2: Rising delay waveforms of inverter chains with different sizing configurations(for illustration only)

4 Task 3: CMOS Inverter Power Consumption

4.1 Lab Procedures

Task 3 measures the power consumption of the optimized inverter chain from Task 2. HSPICE simulation is performed with the following key steps:

1. The optimal sizing configuration: f2 = 5, f3 = 15, f4 = 60
2. A pulse voltage source applied to the input
3. Power measurement averaged over multiple switching cycles

The key HSPICE measurement statement:

```
.measure tran avgpower AVG P(vdd_inv) from=1n to=10n
```

This measures the average power consumption from 1 ns to 10 ns, capturing multiple complete switching cycles to obtain accurate steady-state power consumption.

4.2 Lab Results

The measured power consumption results are:

Parameter	Value	Temperature (°C)
Average Power	-33.20 W	25.0

表 3: Power consumption of optimized inverter chain

Note: The negative sign indicates power consumption (current flowing from the supply source into the circuit).

4.3 Technical Analysis

The power consumption analysis reveals several important characteristics:

1. **Total power**: The measured average power of 33.20 μW represents the combined dynamic and static power consumption of the 4-stage inverter chain.

2. **Dynamic power dominance**: At nominal supply voltage (0.75V) and room temperature, dynamic switching power typically dominates over static leakage power. The dynamic power is given by:

$$P_{dynamic} = C_{load} \cdot V_{DD}^2 \cdot P_{0\to1} \cdot f_{clk}$$

   where $P_{0\to1}$ is the activity factor, C_{load} is the total load capacitance, and f_{clk} is the switching frequency.

3. **Power-delay trade-off**: While the optimized sizing minimizes delay (37.32 ps), it requires larger transistors in intermediate stages, which increases both switching capacitance and short-circuit current, leading to higher power consumption.

These power measurements establish the baseline for energy-delay optimization in Task 4.

5 Task 4: Energy-Delay Product Optimization

5.1 Lab Procedures

Task 4 investigates the optimal operating point (V_{dd}) by sweeping supply voltage to minimize the Energy-Delay Product (EDP). The EDP metric captures the trade-off between performance and energy efficiency:

$$EDP = Power \times Delay^2$$

HSPICE simulation is performed with the following key steps:

1. Use the optimized chain configuration (f2 = 5, f3 = 15, f4 = 60)
2. Sweep supply voltage from 0.5V to 1.0V in 20mV steps
3. Measure total propagation delay (t_{p_total}) for each voltage
4. Measure average power consumption at each voltage
5. Calculate EDP for each operating point

Key HSPICE measurement statements:

```
.measure tran tp_total param='tp1+tp2+tp3+tp4'
.measure TRAN avgpower AVG P(vdd_inv) from=1n to=8n
.measure tran EDP param='abs(avgpower*tp_total*tp_total)'
```

A Python script named ”parser_mt.py” was used to extract data from the .mt0 output file and generate visualization plots for analysis.

5.2 Lab Results

The simulation swept 26 voltage points from 0.5V to 1.0V. For example, several operating points are summarized in the table below:

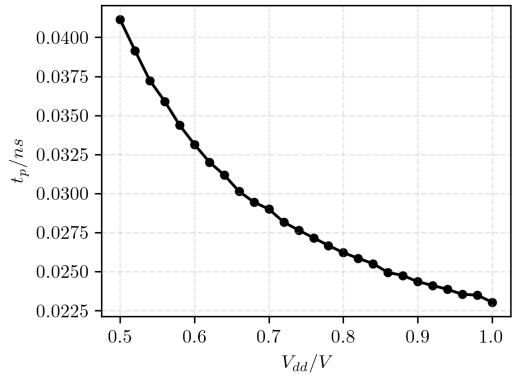
The **optimal supply voltage is 0.58V**, achieving the minimum EDP of $\mathbf{2.141 \times 10^{-26}}$ $\mathbf{W \cdot s^{-2}}$.

5.3 Technical Analysis

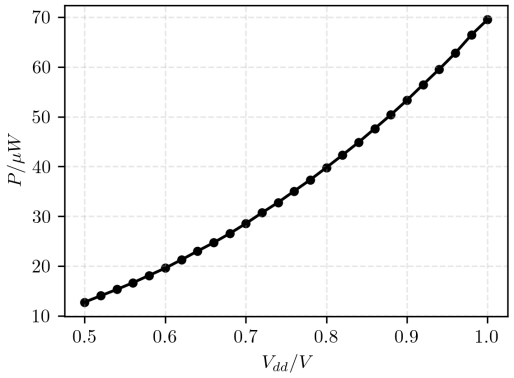
The voltage scaling results demonstrate fundamental trade-offs in digital circuit design:

Supply (V)	t_{p_total} **(ps)**	**Power (W)**	**EDP (W · s²)**
0.50	41.14	-12.74	2.155×10^{-26}
0.58	34.37	-18.12	2.141×10^{-26}
0.70	29.00	-28.53	2.399×10^{-26}
0.80	26.21	-39.79	2.735×10^{-26}
1.00	23.04	-69.53	3.692×10^{-26}

表 4: Selected EDP measurements at different supply voltages



(a) Total propagation delay vs. supply voltage



(b) Average power consumption vs. supply voltage

图 3: Delay and Power vs. Supply Voltage

1. **Delay characteristics**: As shown in Figure 3a, delay increases exponentially as supply voltage decreases to threshold. At 0.5V, the circuit operates near the threshold voltage region where transistor drive current is severely degraded.

2. **Power characteristics**: Figure 3b shows that power consumption decreases quadratically with supply voltage, following the relationship $P \propto V_{DD}^2$. At 1.0V, power is 69.53 μW, while at 0.58V it drops to 18.12 μW (a 74% reduction).

3. **EDP optimization**: Figure 4 reveals a minimum at 0.58V. This represents the optimal balance between:

   – Speed: Still reasonable at 34.37 ps (49% slower than at 1.0V)

   – Energy efficiency: Power reduced by 74% compared to nominal voltage

The EDP metric effectively captures the energy-performance trade-off, making it a valuable tool for system-level power management decisions.

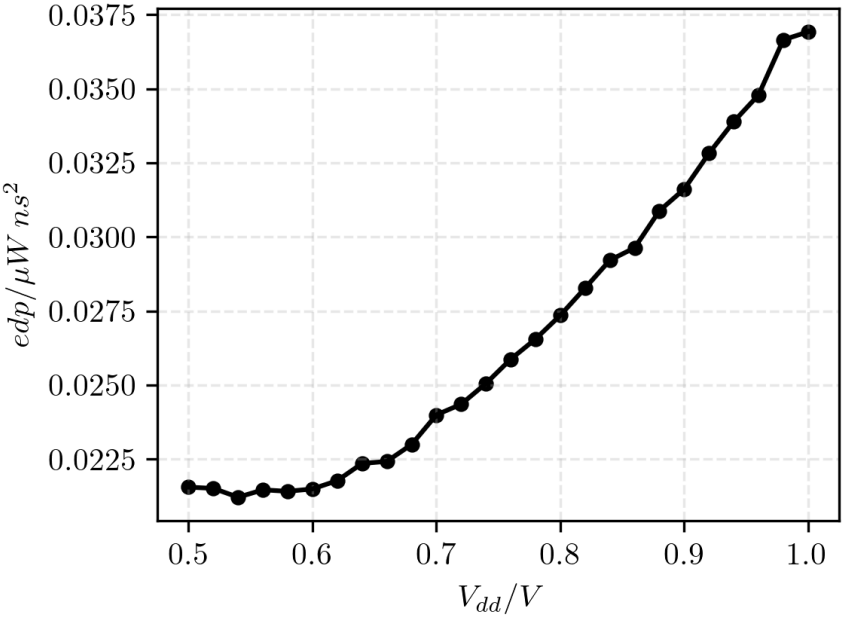


图 4: Energy-Delay Product vs. supply voltage

6 Task 5: Inverter Chain Optimization with Unfixed Stages

6.1 Lab Procedures

Task 5 extends the optimization problem by allowing the number of stages (N) to vary. The goal is to find both the optimal number of stages and the sizing factor for each stage to minimize total delay.

Theoretical background:

- For a given stage number N, the optimal sizing factor is $f = F^{1/N}$ where F = 256 (load factor)
- If N is not given, the optimal number of stages should satisfy: $f = \exp(1 + \gamma/f) \approx 3.6$ (from calculus of variations)
- This suggests N = $\ln(256)/\ln(3.6) \approx 4.32$ stages

HSPICE simulation is performed with the following key steps:

1. Generate separate HSPICE netlists for N = 1 to 10 stages
2. For each N, calculate optimal sizing as $f = 256^{1/N}$
3. Use Python scripts to automatically generate netlists and batch simulate

4. Extract total delay for each configuration
5. Compare results to identify optimal stage number

Python scripts used for automation work are:

1. `generate_task5.py`: Generates HSPICE netlists for different N values
2. `run_task5.py`: Batch executes all simulations
3. `parser_mt.py`: Parses .mt0 output files
4. `run_stat.py`: Consolidates results into summary spreadsheet
5. `summary_plot.py`: Generates visualization plots

6.2 Lab Results

The simulation results for stage numbers from 1 to 10 are summarized:

N (Stages)	t_{p_total} **(ps)**	**Optimal f**
1	208.8	256.00
2	46.43	16.00
3	31.96	6.35
4	29.63	4.00
5	29.12	3.03
6	30.34	2.52
7	31.82	2.20
8	33.02	1.97
9	34.87	1.81
10	36.95	1.68

表 5: Total delay vs. number of stages

The **optimal configuration is N = 5 stages** with a minimum total delay of **29.12 ps**.

6.3 Technical Analysis

The results validate theoretical predictions and reveal practical design insights:

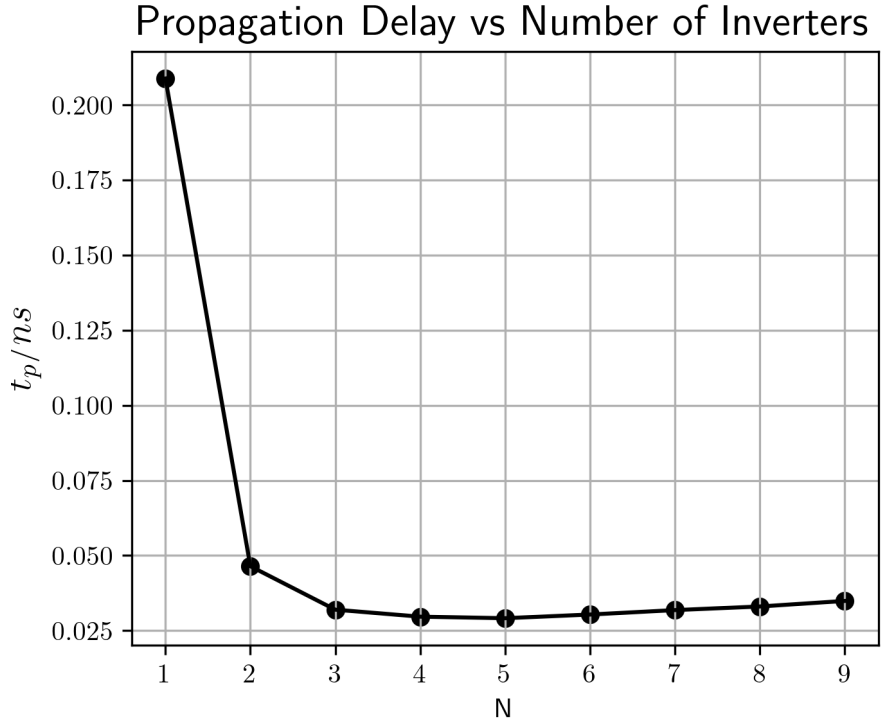


图 5: Total propagation delay vs. number of stages

1. **Optimal stage number**: The experimental optimum of N = 5 closely matches the theoretical prediction of $N \approx 4.32$ stages. This confirms that the optimal sizing factor should be near $f \approx 3.6$. At N = 5, $f = 256^{1/5} = 3.03$, which is reasonably close to 3.6.

2. **Delay vs. stages curve**: Figure 5 shows a minimum at N = 5:

   – N < 5: Too few stages means each stage must provide large gain, resulting in excessive delay per stage

   – N > 5: Too many stages accumulate delay despite each being individually fast

   – N = 5: Optimal balance between stage count and individual stage delay

3. **Single stage penalty**: Using just 1 stage (N=1) results in 208.8 ps delay - over 7× slower than the optimum. This dramatic penalty demonstrates why direct drive of large loads is impractical.

4. **Diminishing returns**: The delay reduction from N=4 to N=5 is 0.51 ps (1.7% improvement), while further increasing stages degrades performance. This suggests the optimization landscape is relatively flat near the optimum, which provides design flexibility.

5. **Comparison with Task 2**:
   - Task 2 (fixed 4 stages): Best delay = 37.32 ps
   - Task 5 (optimized 5 stages): Delay = 29.12 ps
   - Improvement: 22% faster by adding one stage and optimizing sizing

- **Technology scaling**: The optimal N depends on the ratio of intrinsic delay to loading delay. As technology scales to smaller nodes with lower supply voltages, this ratio changes, potentially shifting the optimal N.

This task demonstrates the importance of holistic optimization - considering both stage count and transistor sizing to achieve optimal circuit performance.

7 Observations and Conclusions

This laboratory investigation of CMOS inverter chains using 16nm FinFET technology has provided valuable insights into fundamental digital circuit design principles and optimization techniques.

7.1 Key Observations

1. **FO4 Delay Characterization**: The measured FO4 delay of 5.9 ps demonstrates the high-speed capability of advanced FinFET technology. The slight asymmetry between t_{pLH} and t_{pHL} (9% difference) reflects inherent mobility differences between NMOS and PMOS devices.

2. **Theoretical vs. Practical Optimization**: While classical theory predicts uniform 4× scaling for optimal delay, experimental results show that $f_2 = 5, f_3 = 15, f_4 = 60$ provides superior performance. This deviation highlights the importance of parasitic effects, non-ideal scaling, and technology-specific characteristics that simple analytical models may overlook.

3. **Voltage Scaling for Energy Efficiency**: The EDP analysis revealed that operating at 0.58V (27% below nominal) achieves optimal energy efficiency. This represents a 74% power reduction with only 49% delay penalty, making it highly attractive for energy-constrained applications.

4. **Architectural Optimization**: Allowing variable stage count (Task 5) achieved 22% better performance compared to fixed 4-stage design (Task 2). The optimal $N = 5$ stages with $f \approx 3.03$ validates theoretical predictions based on $f = 3.6$.

7.2 Conclusions

1. **Multi-dimensional optimization**: Optimal circuit design requires simultaneous consideration of multiple parameters - transistor sizing, stage count, and supply voltage. No single parameter can be optimized in isolation without considering its impact on other design objectives.

2. **Technology awareness**: Practical design must account for real-world effects including parasitic capacitance, wire resistance, velocity saturation, and short-channel effects, which becomes increasingly important at advanced technology nodes.

3. **Design metrics matter**: Different optimization metrics (minimum delay, minimum power, minimum EDP) lead to different optimal designs:

- Minimum delay: Large transistors, nominal voltage, optimal staging
- Minimum power: Small transistors, reduced voltage
- Minimum EDP: Balanced sizing, near-threshold voltage

In conclusion, this lab has successfully demonstrated the application of systematic optimization techniques to inverter chain design, validating theoretical models while revealing the importance of practical considerations in advanced technology nodes. The methodologies and insights gained are directly applicable to real-world digital circuit design problems.