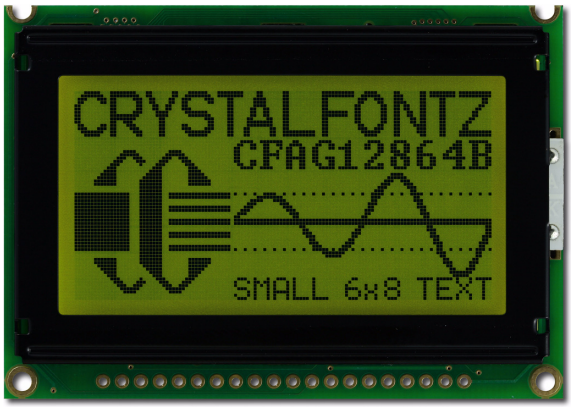
Crystalfontz America, Incorporated

GRAPHIC LCD MODULE SPECIFICATIONS



Crystalfontz Model Number	CFAG12864B-YYH-V
Hardware Version	Revision C, September 2008
Data Sheet Version	Revision 2.0, February 2009
Product Pages	www.crystalfontz.com/product/CFAG-12864B-YYH-V.html

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REVISION HISTORY

HARDWARE	
2008/09/01	Current Hardware Version: vC ● Appendixes for controller Samsung S6B0107 64 CH Common Driver and S6B0108 64 CH Segment Driver were replaced with APPENDIX C: NEOTEC NT7107C 64 CH COMMON DRIVER SPECIFICATIONS and APPENDIX D: NEOTEC N7108C 64 CHANNEL SEGMENT DRIVE SPECIFICATIONS.
2005/09/01	Hardware Version: vA

DATA SHEET	
2009/02/05	Data Sheet: v2.0 Changes since last revision (v1.0): ● Improved drawings, tables, and text. ● Added Quick Reference for Pin Functions (Front & Back Photos) (Pg. 14). ● Added instructions on How to Calculate the Power Rating of the Resistor (Pg. 20).
2006/12/15	Data Sheet: v1.0

The Fine Print

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CONTENTS

LIST OF FIGURES

MAIN FEATURES

- 128 x 64 dots graphic LCD module has a large display area in a compact 75.0 (W) x 52.7 (H) x 8.9 (D) millimeter package (2.95" (W) x 2.07" (H) x .35" (D)).
- 8-bit parallel interface.
- The CFA-10006 Demonstration Board Kits have everything you need to easily demonstrate and experiment with this module. The CFA-10006 User Guide is included at the end of this PDF.
- Built-in Neotec controllers. See APPENDIX C: NEOTEC NT7107C 64 CH COMMON DRIVER SPECIFICATIONS and APPENDIX D: NEOTEC N7108C 64 CHANNEL SEGMENT DRIVE SPECIFICATIONS.
- Yellow-green edge LED backlight with STN positive transflective mode LCD. Displays dark dots on an illuminated yellow-green background.
- On-board negative voltage generator. Connect a 20K potentiometer from Pin 18 (V_{EE} which is -5v output generated by the module) to Pin 1 (V_{DD} which is +5V supplied by you), with the wiper connected to Pin 3 (V_O, contrast adjustment.) This will take advantage of the negative voltage generator to enable operation at wider temperatures. See System Block Diagram (Pg. 9).
- Wide temperature operation: -20°C to +70°C.
- RoHS compliant.

MODULE CLASSIFICATION INFORMATION

CFA G 128 64 B - Y Y H - V *
❶ ❷ ❸ ❹ ❺ ❻ ❼ ❽ ❾ ❿

❶	Brand	Crystalfontz America, Inc.
❷	Display Type	G – Graphic
❸	Number of Dots (Width)	128 Dots
❹	Number of Dots (Height)	64 Dots
❺	Model Identifier	B
❻	Backlight Type & Color	Y – LED, yellow-green
❼	Fluid Type, Image (Positive or Negative), & LCD Glass Color	Y – STN Positive, yellow-green
❽	Polarizer Film Type, Wide Temperature (WT) Range, & View Angle (O 'Clock)	H – Transflective, WT, 6:00[1]
❾	Special Code	V – Built-in negative voltage generator (on the board)
❿	Special Codes	* – May have additional manufacturer's codes at this location.

[1] *Note: For more information on Viewing Angle, see Definition of 6 O'Clock and 12:00 O'Clock Viewing Angles (Pg. 18).*

ORDERING INFORMATION

PART NUMBER	BUILT-IN NEGATIVE VOLTAGE GENERATOR	FLUID	LCD GLASS COLOR	IMAGE	POLARIZER FILM	BACKLIGHT COLOR/TYPE
CFAG12864B-YYH-V	No	STN	yellow-green	positive	transflective	yellow-green edge LEDs 
Additional variant (same form factor, different LCD mode or backlight):						
CFAG12864B-TFH-V	Yes	FSTN	light-gray	positive	transflective	white edge LEDs 
CFAG12864B-TMI-V	Yes	STN	blue	negative	transmissive	white edge LEDs 
CFAG12864B-WGH-V	Yes	STN	gray	positive	transflective	white EL lamp 
CFAG12864B-WGH-N	No	STN	gray	positive	transflective	white EL Lamp 
CFAG12864B-YYH-N	Yes	STN	yellow-green	positive	transflective	yellow-green edge LEDs 

MECHANICAL SPECIFICATIONS

PHYSICAL CHARACTERISTICS

ITEM	SIZE
Number of Dots	128 x 64 dots
Module Dimensions	75.0 (W) x 52.7 (H) x 8.9 (D) mm
Viewing Area	60.0 (W) x 32.6 (H) mm
Active Area	55.0 (W) x 27.48 (H) mm
Dot Size	.39 (W) x .39 (H) mm
Dot Pitch	.43 (W) x .43 (H) mm
Weight	33.5 grams (typical)

MODULE OUTLINE DRAWING

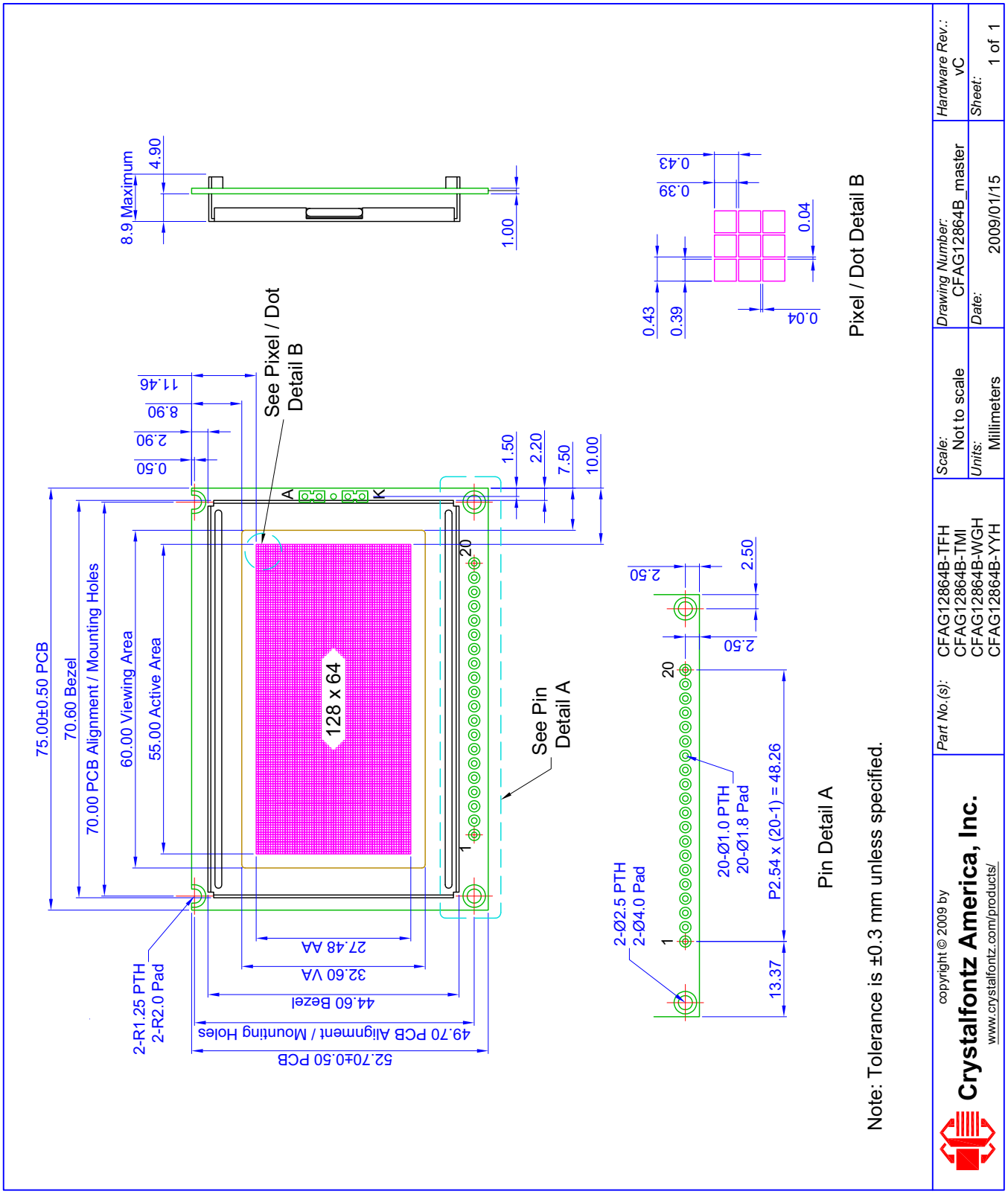
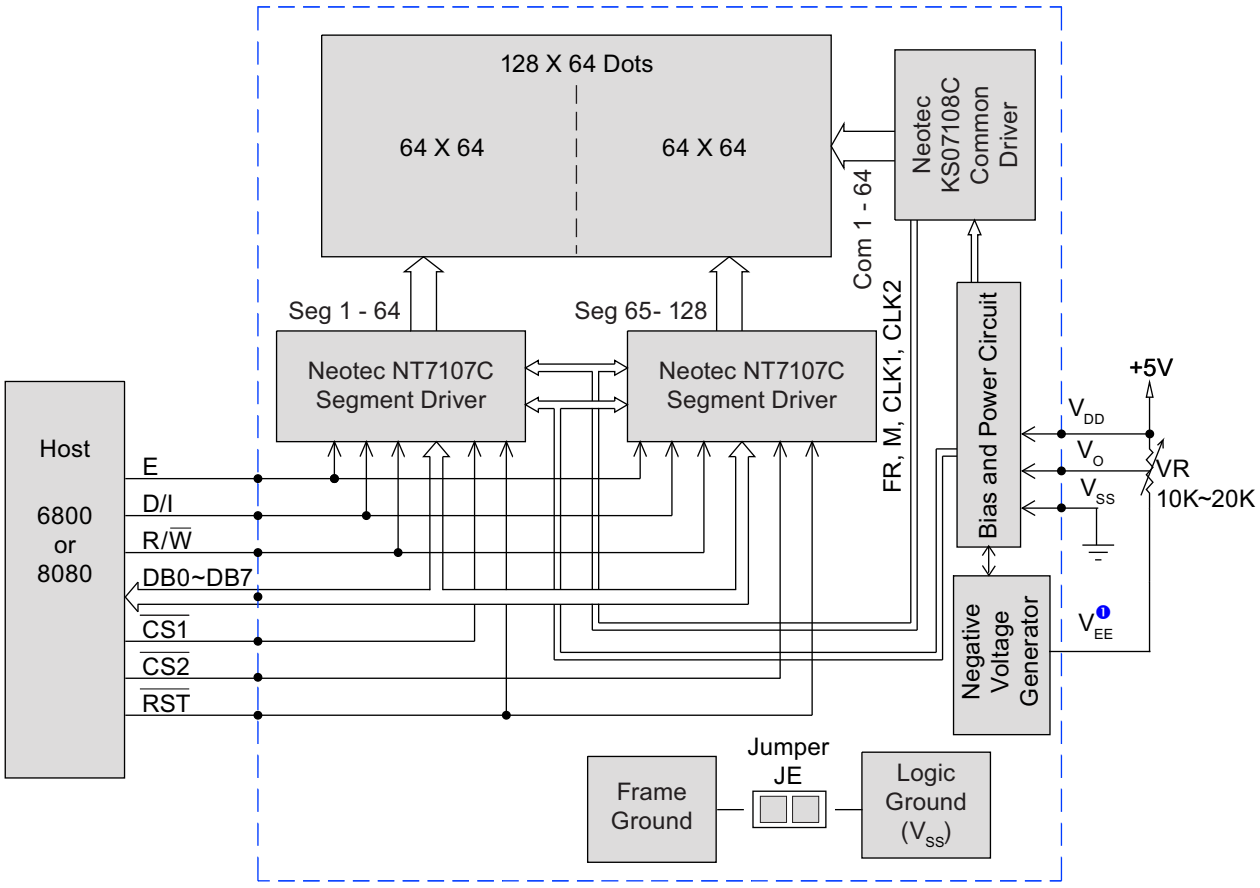


Figure 1. Module Outline Drawing

ELECTRICAL SPECIFICATIONS

SYSTEM BLOCK DIAGRAM



[1] V_{EE} = output pin of on-board negative voltage generator

Figure 2. System Block Diagram

FRAME GROUND

Frame Ground (shown in the System Block Diagram above) is a trace that connects some of the bezel tabs. To connect Frame Ground to the Logic Ground (V_{SS}, Pin 2), use an “0805” package 0 ohm resistor to close jumper **JE**.

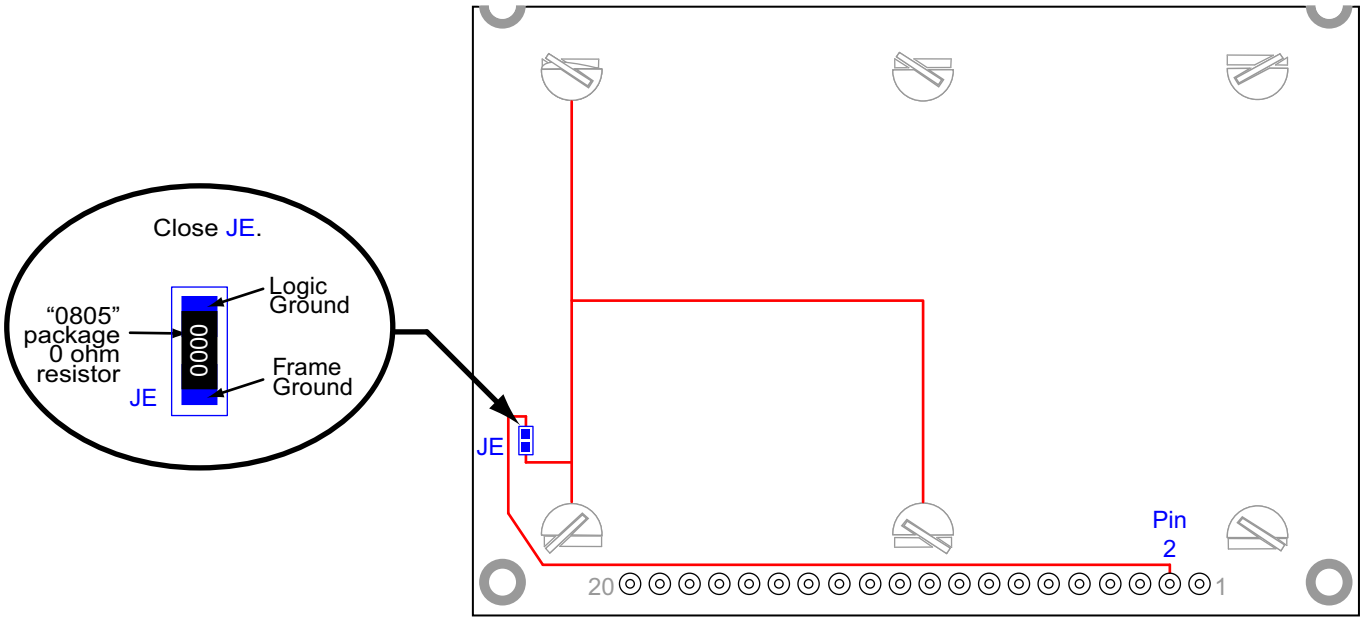


Figure 3. Frame Ground (Back View of Module)

DRIVING METHOD

DRIVING METHOD	SPECIFICATION
Duty	1/64
Bias	1/9

ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS	SYMBOL	MINIMUM	MAXIMUM
Operating Temperature	T_{OP}	-20°C	+70°C
Storage Temperature*	T_{ST}	-30°C	+80°C
Input Voltage	V_I	0	V_{DD}
Supply Voltage for Logic	V_{DD}	0	6.7v
Supply Voltage for LCD	V_{DD}–V_O		16.7v
**Note: Prolonged exposure at temperatures outside of this range may cause permanent damage to the module.*			

DC CHARACTERISTICS

PART	DC CHARACTERISTICS*	Test Condition	SYMBOL	MINIMUM	TYPICAL	MAXIMUM
Controller and Board	Supply Voltage for Logic		V_{DD} - V_{SS}	+4.5v	+5.0v	+5.5v
	Input High Voltage	V_{DD} = 5v	V_{IH}	3.5v		V_{DD}
	Input Low Voltage		V_{IL}	0 (V_{SS})		+0.8v
	Supply Current (Logic only, not including backlight)	without backlight	I_{DD}	1.5 mA		4.0 mA
LCD Glass	Supply voltage for driving LCD	T_A = -20ºC	V_{DD} - V_O			+9.8v
		T_A = +25ºC			+8.0v	
		T_A = +70ºC		+7.6v		

**For detailed information, DC Characteristics in* APPENDIX C: NEOTEC NT7107C 64 CH COMMON DRIVER SPECIFICATIONS (Pg. 35).

INTERFACE PIN FUNCTIONS

PIN	SIGNAL	LEVEL	DIRECTION	DESCRIPTION
1	V_{DD}	+5.0v	–	Supply voltage for logic
2	V_{SS}	0v	–	Ground
3	V_O	variable	–	Supply voltage for driving LCD V_O = -3.0v typical at V_{DD} = +5v which gives $V_{LCD} = (V_{DD} - V_O)$ = 8v
4	DB0	H/L	I/O	Data bit 0
5	DB1	H/L	I/O	Data bit 1
6	DB2	H/L	I/O	Data bit 2
7	DB3	H/L	I/O	Data bit 3
8	DB4	H/L	I/O	Data bit 4
9	DB5	H/L	I/O	Data bit 5
10	DB6	H/L	I/O	Data bit 6
11	DB7	H/L	I/O	Data bit 7
12	$\overline{CS1}$	L	I	Chip select for controller #1 Columns 1 to 64 Chip select for controller #2 Columns 65 to 128
13	$\overline{CS2}$	L	I	Select Column 65 to Column 128
14	$\overline{RST}$	L	I	Controller reset signal
15	R/$\overline{W}$	H/L		Read/write selection input H: read (MPU←module) L: write (MPU→module)
16	D/$\overline{I}$	H/L	I	H: Data L: Instruction
17	E	H, H→L	I	Read/write enable signal H: read data is enabled by a high level H→L: write data is latched on the falling edge
18	**VEE**	**-5v**	**O**	**Negative voltage output**

PIN	SIGNAL	LEVEL	DIRECTION	DESCRIPTION
19	A (LED+)			Supply voltage for LED. “A” (anode) or “+” of LED backlight
20	K (LED-)			Supply voltage for LED. “K” (cathode or kathode for German and original Greek spelling) or “-” of LED backlight
For Backlight connections, please refer to LED BACKLIGHT (Pg. 19).				

QUICK REFERENCE FOR PIN FUNCTIONS (FRONT & BACK PHOTOS)

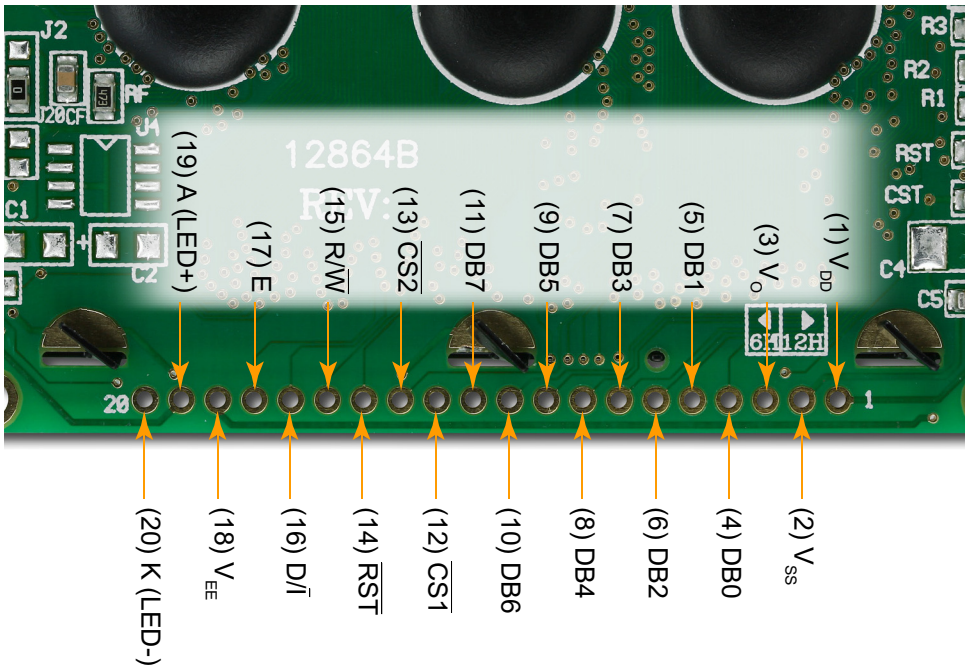


Figure 4. Back View of Pins (Labeled)

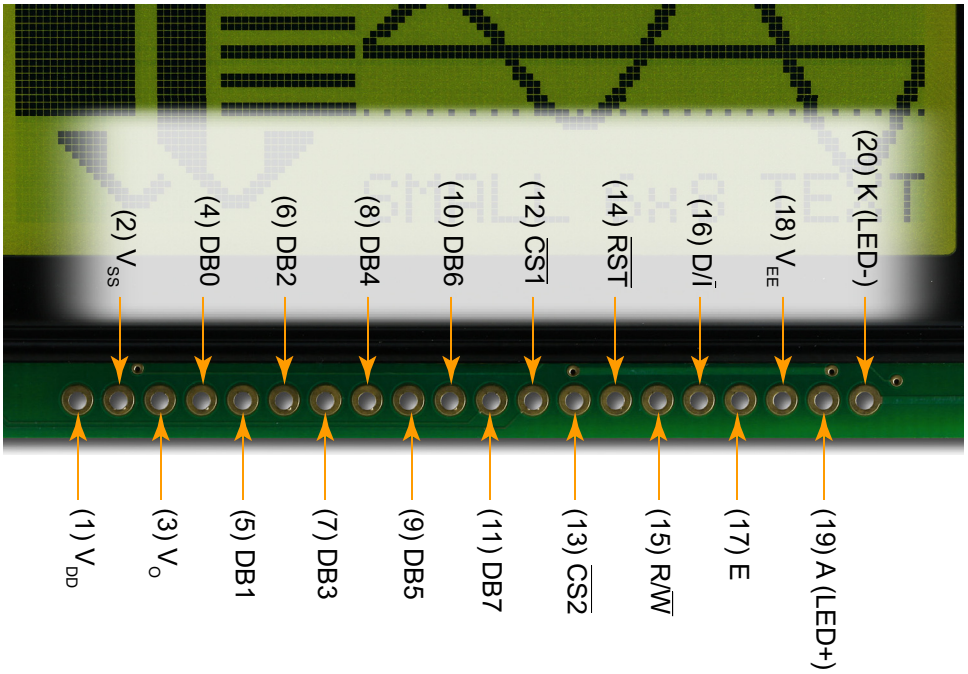
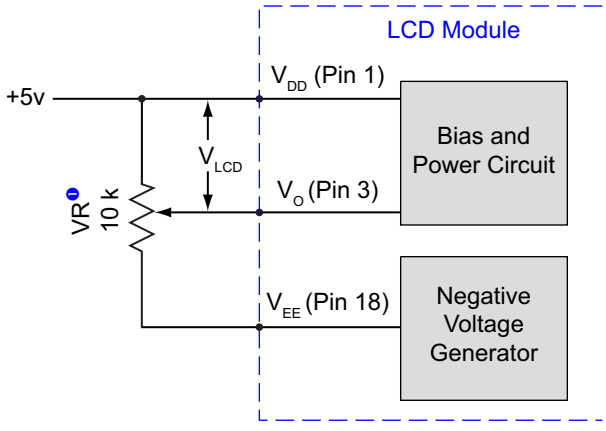


Figure 5. Front View of Pins (Labeled)

TYPICAL V_O CONNECTIONS FOR DISPLAY CONTRAST

Adjust V_O to -3.0v (V_{LCD} = 8.0v) as an initial setting. When the module is operational, readjust V_O for optimal display appearance.



Use external control to adjust for optimal display appearance.

Figure 6. Typical V_O Connections for Display Contrast

NEOTEC NT7107C/NT7108C CONTROLLERS

The CFAG12864B-YYH-V uses two Neotec controllers: NT7107 64 channel common driver and a NT7108 64 channel segment driver.

For your reference, the most recent versions (2002) of the Neotec driver specifications are included as appendixes in this Data Sheet.

Here are links to some of the commonly used sections:

- For DC characteristics, see page 8 of Appendix C, “DC Characteristics”.
- For functional description, see page 11 of Appendix C, “Functional Description”.
- For host interface timing characteristics (read and write), see page 19 of Appendix D, “MPU Interface”.
- For display control instruction, see page 12 of Appendix D, “Display Control Instruction”.

OPTICAL SPECIFICATIONS

ITEM	SYMBOL	CONDITION	MINIMUM	TYPICAL	MAXIMUM
View Angle (Vertical, Horizontal)	(V)θ	CR≥2	20°		40°
	(H)φ	CR≥2	-30°		+30°
Contrast Ratio	CR			3	
LCD Response Time*	T rise	Ta = 25°C		200 ms	300 ms
	T fall	Ta = 25°C		200 ms	300 ms
**Response Time: The amount of time it takes a liquid crystal cell to go from active to inactive or back again.*					

TEST CONDITIONS AND DEFINITIONS FOR OPTICAL CHARACTERISTICS

Test Conditions

- Operating Voltage (V_{LCD}): V_{OP}
- Viewing Angle
  - Vertical (V)θ: 0°
  - Horizontal (H)φ): 0°
- Frame Frequency: 64 Hz (nominal)
- Driving Waveform: 1/64 Duty, 1/9 Bias
- Ambient Temperature (Ta): 25°C

Definition Operation Voltage (V_{op})

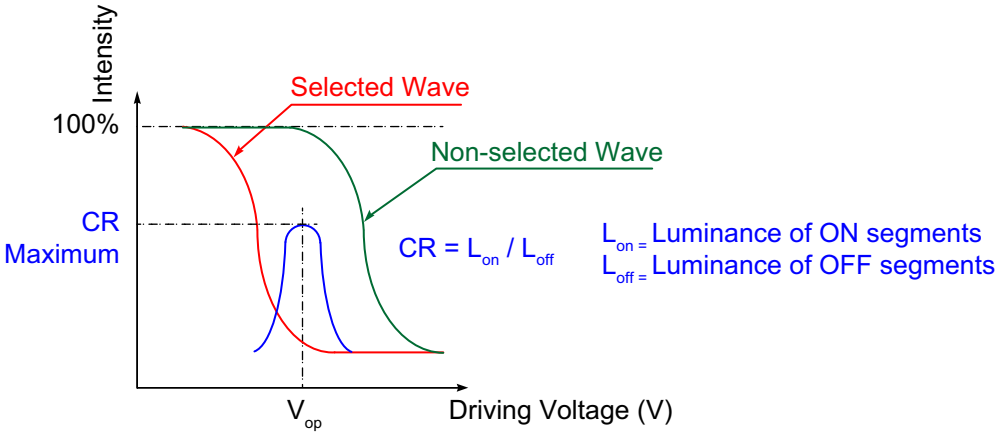


Figure 7. Definition of Operation Voltage (V_{OP}) (Positive)

Definition of Response Time (Tr, Tf)

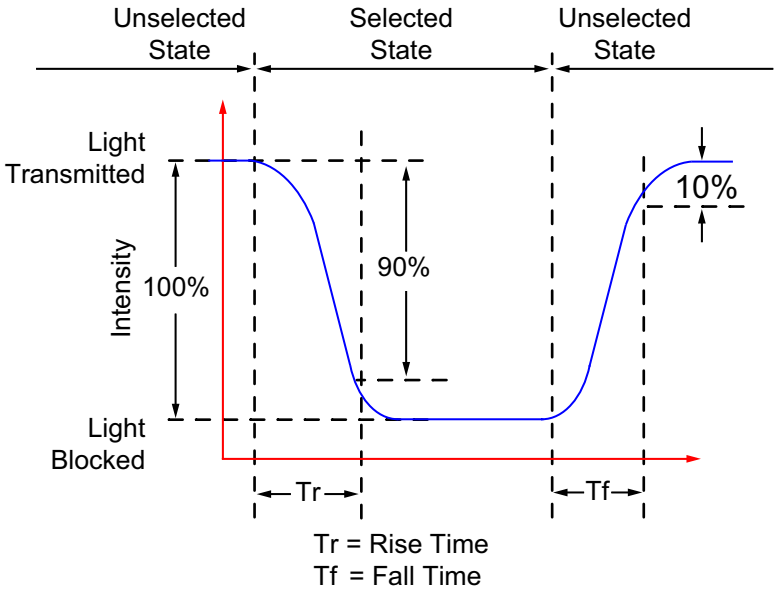


Figure 8. Definition of Response Time (Tr, Tf) (Positive)

Definition of Vertical and Horizontal Viewing Angles (CR>2)

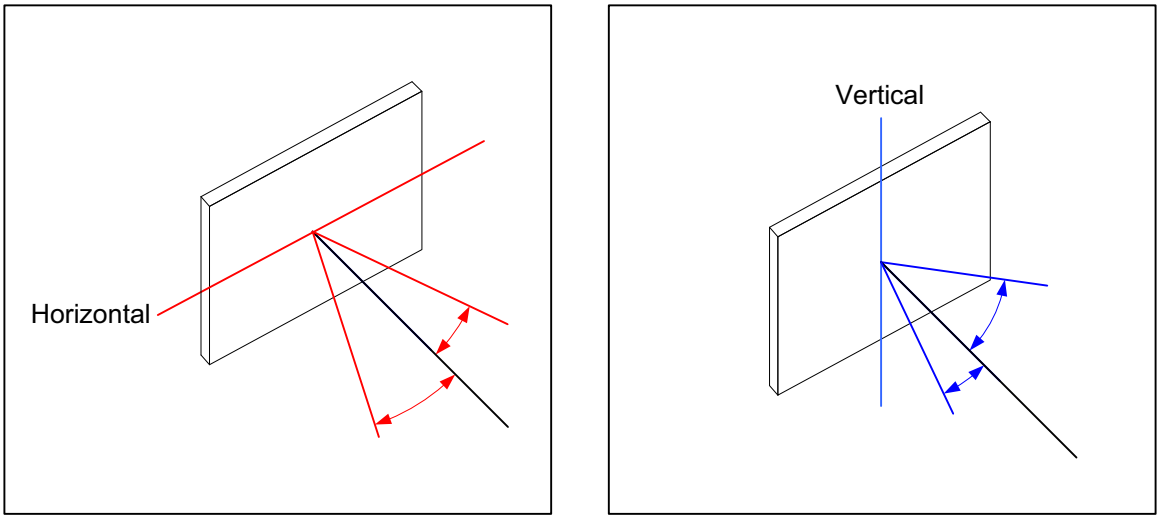


Figure 9. Definition of Horizontal and Vertical Viewing Angles (CR>2)

Definition of 6 O'Clock and 12:00 O'Clock Viewing Angles

A 6:00 o'clock viewing angle is a bottom viewing angle like what you would see when looking at a cell phone or calculator. A 12:00 o'clock viewing angle is a top viewing angle like what you would see when looking at the gauges in a golf cart or airplane.

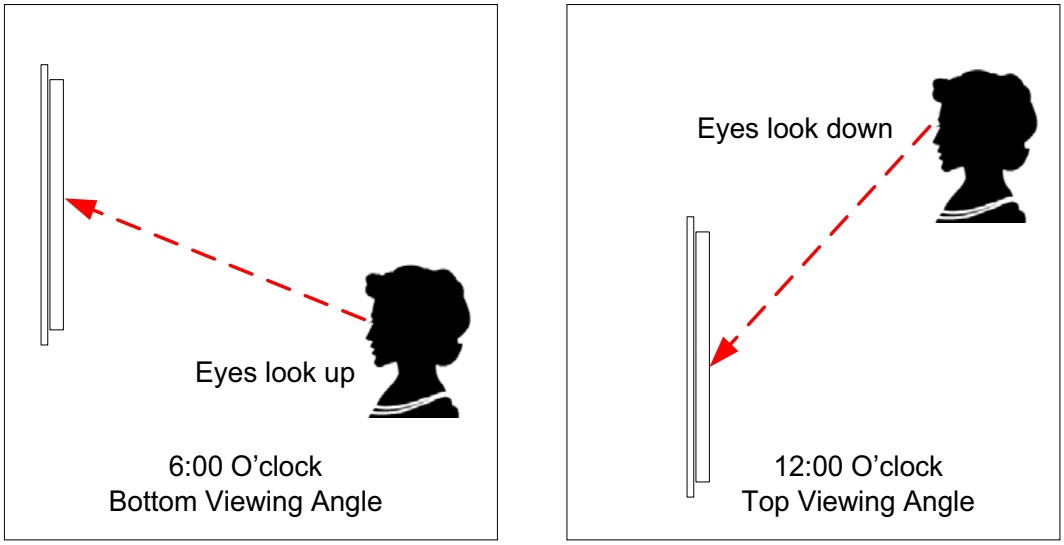


Figure 10. 6:00 O'Clock and 12:00 O'Clock Viewing Angles

LED BACKLIGHT

You can connect the CFAG12864B-YYH-V backlight by one of these two methods:

- Solder leads from your PCB's circuit to the "A" and "K" connectors on the right edge of the display (glass facing up).
- Make connections to your PCB using Pins 19 (A (LED+)) and 20 (K (LED+)) on the display module's connector.

Backlight Characteristics
dark dots on yellow-green background

PARAMETER	MINIMUM	TYPICAL	MAXIMUM
Forward Current (I_{LED}) V = +4.2v	80 mA	100 mA	150 mA*
Forward Voltage (V_{LED})	+4.0v	+4.2v	+4.4v
Reverse Voltage ($V_{R)}$		+8v	
Luminous Intensity** (IV) I_{LED} = 100 mA	14 cd/m^2	18 cd/m^2	
Wavelength (λ p) I_{LED} = 100 mA	565 nm	570 nm	575 nm

The CFAG12864B-YYH-V backlight uses LEDs. The backlight is easy to use properly but it is also easily damaged by abuse.

NOTE

Do not connect +5v directly to the backlight terminals. This will ruin the backlight.

NOTE

We recommend that the white LED backlight be dimmed or turned off during periods of inactivity to conserve the LEDs' lifetime.

LEDs are "current" devices. The brightness is controlled by the current flowing through it, not the voltage across it. Ideally, a current source would be used to drive the LEDs. In practice, a simple current limiting resistor will work well in most applications and is much less complex than a current source.

How to Calculate the R_{LIMIT}

You need to know what the supply (forward) voltage of the LEDs will be so you can calculate a current limiting resistor (R_{LIMIT}). The forward voltage will vary slightly from display to display.

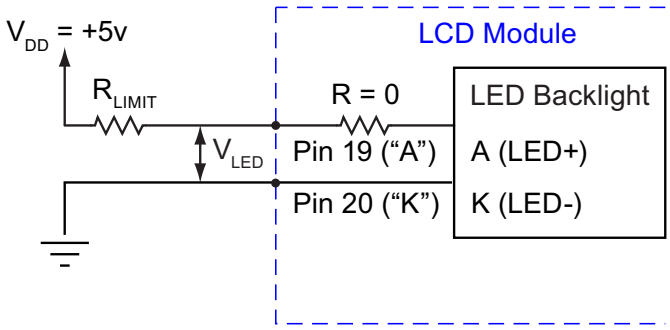


Figure 11. LED Backlight Connection Using Pin 19 and Pin 20

The general equation to calculate R_{LIMIT} is:

$$R_{LIMIT}\text{ (minimum)} = \frac{V_{DD}\text{ (supply voltage)} - V_{LED}\text{ (LED forward voltage)}}{I_{LED}\text{ (maximum LED current)}}$$

The specific R_{LIMIT} calculation for the CFAG12864B-YYH-Vat V_{DD} = +5v is:

$$R_{LIMIT} = \frac{5v - 4.2v}{0.10\text{ A (maximum)}} = 8\Omega\text{ (minimum)}$$

How to Calculate the Power Rating of the Resistor

The general equation to calculate the power rating of the resistor is:

W (power) = I (current) x E (voltage)

The specific power rating calculation for CFAG12864B-YYH-V is:

Power = 0.01 x (5v - 4.2v) = 0.08W = 80mW

Nominally, an 1/8 watt (125 mW) resistor should work, however to keep the temperature of the resistor cooler, a 1/4 or 1/2 watt resistor would typically be used.

PWM Dimming

The backlight may be dimmed by PWM (Pulse Width Modulation). The typical range for the PWM frequency is from 100 to 300 Hz.

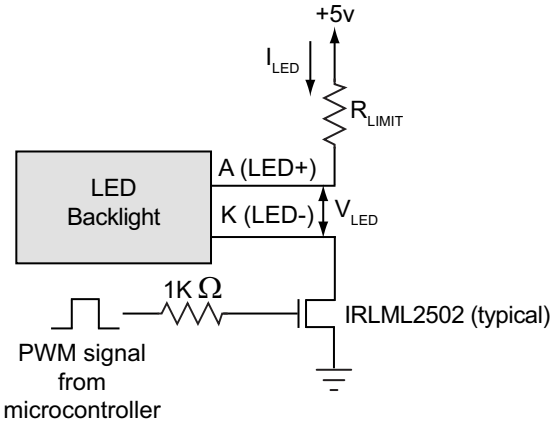


Figure 12. Typical LED Backlight Connections for PWM Dimming

PRODUCT RELIABILITY

MODULE RELIABILITY

ITEM	SPECIFICATION
Module, excluding backlight.	50,000 to 100,000 hours (typical)
Yellow-green LED Backlight	50,000 to 100,000 hours (typical)

MODULE LONGEVITY (EOL / REPLACEMENT POLICY)

Crystalfontz is committed to making all of our LCD modules available for as long as possible. For each module we introduce, we intend to offer it indefinitely. We do not preplan a module's obsolescence. The majority of modules we have introduced are still available.

We recognize that discontinuing a module may cause problems for some customers. However, rapidly changing technologies, component availability, or low customer order levels may force us to discontinue ("End of Life", EOL) a module. For example, we must occasionally discontinue a module when a supplier discontinues a component or a manufacturing process becomes obsolete. When we discontinue a module, we will do our best to find an acceptable replacement module with the same fit, form, and function.

In most situations, you will not notice a difference when comparing a "fit, form, and function" replacement module to the discontinued module it replaces. However, sometimes a change in component or process for the replacement module results in a slight variation, perhaps an improvement, over the previous design.

Although the replacement module is still within the stated Data Sheet specifications and tolerances of the discontinued module, changes may require modification to your circuit and/or firmware. Possible changes include:

- *LCD fluid, polarizers, or the LCD manufacturing process.* These items may change the appearance of the display, requiring an adjustment to V_O. See Typical V_O Connections For Display Contrast (Pg. 15).
- *Backlight LEDs.* Brightness may be affected (perhaps the new LEDs have better efficiency) or the current they draw may change (new LEDs may have a different VF).
- *Controller.* A new controller may require minor changes in your code.
- *Component tolerances.* Module components have manufacturing tolerances. In extreme cases, the tolerance stack can change the visual or operating characteristics.

Please understand that we avoid changing a module whenever possible; we only discontinue a module if we have no other option. We will post Part Change Notices on the product's webpage as soon as possible. If interested, you can subscribe to future part change notifications.

CARE AND HANDLING PRECAUTIONS

For optimum operation of the module and to prolong its life, please follow the precautions described below.

ESD (ELECTRO-STATIC DISCHARGE)

The circuitry is industry standard CMOS logic and susceptible to ESD damage. Please use industry standard anti-static precautions as you would for any other PCB such as expansion cards or motherboards.

DESIGN AND MOUNTING

- The exposed surface of the LCD “glass” is actually a polarizer laminated on top of the glass. To protect the polarizer from damage, the CFAG12864B-YYH-V ships with a protective film over the polarizer. Please peel off the protective film slowly. Peeling off the protective film abruptly may generate static electricity.
- The polarizer is made out of a soft plastic and is easily scratched or damaged. To protect the polarizer from damage, place a transparent plate (for example, acrylic, polycarbonate, or glass) in front of the CFAG12864B-YYH-V, leaving a small gap between the plate and the display surface. We recommend GE HP-92 Lexan, which is readily available and works well.
- Do not disassemble or modify the module.
- Do not modify the mounting tab of the metal bezel or make connections to it.
- Solder only to the I/O terminals. Use care when removing solder—it is possible to damage the PCB.
- Do not reverse polarity to the power supply connections. Reversing polarity will immediately ruin the module.

AVOID SHOCK, IMPACT, TORQUE, AND TENSION

- Do not expose the module to strong mechanical shock, impact, torque, and tension.
- Do not drop, toss, bend, or twist the module.
- Do not place weight or pressure on the module.

IF LCD PANEL BREAKS

- If the LCD panel breaks, be careful to not get the liquid crystal fluid in your mouth or eyes.
- If the liquid crystal fluid touches your skin, clothes, or work surface, wash it off immediately using soap and plenty of water.
- Do not eat the LCD panel.

CLEANING

- The polarizer (laminated to the glass) is made out of a soft plastic and is easily scratched or damaged. Be very careful when you clean the polarizer. Use the removable protective film to remove smudges (for example, fingerprints) and any foreign matter.
- Do not clean the polarizer with liquids. Do not wipe the polarizer with any type of cloth or swab (for example, Q-tips). Damage will be especially obvious on "negative" modules (module that appear dark when "off").

OPERATION

- We do not recommend connecting this module to a PC's parallel port as an "end product". This module is not "user friendly" and connecting them to a PC's parallel port is often difficult, frustrating, and can result in a "dead" display due to mishandling. For more information, see our forum thread at http://www.crystalfontz.com/forum/showthread.php?s=&threadid=3257.
- Your circuit should be designed to protect the module from ESD and power supply transients.
- Observe the operating temperature limitations: a minimum of -20°C to +70°C maximum with minimal fluctuations. Operation outside of these limits may shorten the life and/or harm the display.
  - At lower temperatures of this range, response time is delayed.
  - At higher temperatures of this range, display becomes dark. (You may need to adjust the contrast.)
- Operate away from dust, moisture, and direct sunlight.

STORAGE

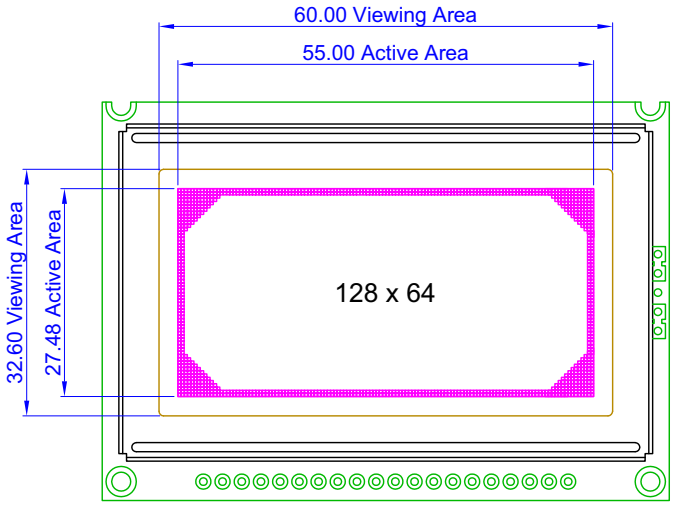
- Store in an ESD-approved container away from dust, moisture, and direct sunlight.
- Observe the storage temperature limitations: a minimum of -30°C minimum to +80°C maximum with minimal fluctuations. Rapid temperature changes can cause moisture to form, resulting in permanent damage.
- Do not allow weight to be placed on the modules while they are in storage.

APPENDIX A: QUALITY ASSURANCE STANDARDS

INSPECTION CONDITIONS

- Environment
  - Temperature: 25±5°C
  - Humidity: 30~85% RH
- For visual inspection of active display area
  - Source lighting: two 20 Watt or one 40 Watt fluorescent light
  - Display adjusted for best contrast
  - Viewing distance: 30±5 cm (about 12 inches)
  - Viewable angle: inspect at 45° angle of vertical line right and left, top and bottom

DEFINITION OF ACTIVE AREA AND VIEWING AREA



ACCEPTANCE SAMPLING

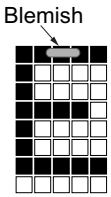
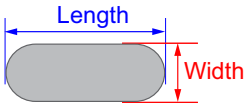
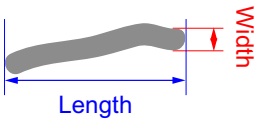
DEFECT TYPE	AQL*
Major	≤.65%
Minor	<1.0%
* Acceptable Quality Level: maximum allowable error rate or variation from standard	

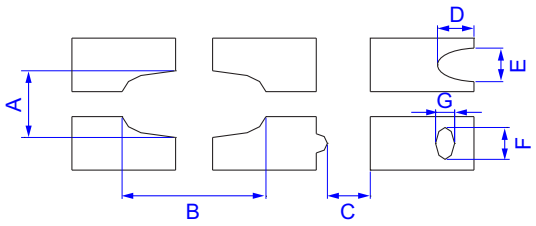
DEFECTS CLASSIFICATION

Defects are defined as:

- Major Defect: results in failure or substantially reduces usability of unit for its intended purpose
- Minor Defect: deviates from standards but is not likely to reduce usability for its intended purpose

ACCEPTANCE STANDARDS

#	DEFECT TYPE	CRITERIA			MAJOR / MINOR
1	Electrical defects	1. No display, display malfunctions, or shorted segments. 2. Current consumption exceeds specifications.			Major
2	Viewing area defect	Viewing area does not meet specifications. (See Inspection Conditions (Pg. 24)).			Major
3	Contrast adjustment defect	Contrast adjustment fails or malfunctions.			Major
4	Blemishes or foreign matter on display segments		*Defect Size*	*Acceptable Qty*	Minor
			≤0.3 mm	3	
			≤2 defects within 10 mm of each other		
5	Blemishes or foreign matter outside of display segments	Defect Size = (Width + Length)/2 	*Defect Size*	*Acceptable Qty*	Minor
			≤0.15 mm	Ignore	
			0.15 to 0.20 mm	3	
			0.20 to 0.25 mm	2	
			0.25 to 0.30 mm	1	
6	Dark lines or scratches in display area 	*Defect Width*	*Defect Length*	*Acceptable Qty*	Minor
		≤0.03 mm	≤3.0 mm	3	
		0.03 to 0.05	≤2.0 mm	2	
		0.05 to 0.08	≤2.0 mm	1	
		0.08 to 0.10	≤3.0 mm	0	
		≥0.10	>3.0 mm	0	

<table>
<tr><th>#</th><th>DEFECT TYPE</th><th colspan="3">CRITERIA</th><th>MAJOR / MINOR</th></tr>
<tr><td rowspan="5">7</td><td rowspan="5">Bubbles between polarizer film and glass</td><td colspan="2">Defect Size</td><td>Acceptable Qty</td><td rowspan="5">Minor</td></tr>
<tr><td colspan="2">≤2.0 mm</td><td>Ignore</td></tr>
<tr><td colspan="2">0.20 to 0.40 mm</td><td>3</td></tr>
<tr><td colspan="2">0.40 to 0.60 mm</td><td>2</td></tr>
<tr><td colspan="2">≥0.60 mm</td><td>0</td></tr>
<tr><td rowspan="6">8</td><td rowspan="6">Display pattern defect</td><td colspan="3"> 
</td><td></td></tr>
<tr><td>Dot Size</td><td colspan="2">Acceptable Qty</td><td>Minor</td></tr>
<tr><td>((A+B)/2)≤0.2 mm</td><td colspan="2" rowspan="4">≤3 total defects
≤2 pinholes per digit</td><td rowspan="4"></td></tr>
<tr><td>C>0 mm</td></tr>
<tr><td>((D+E)/2)≤0.25 mm</td></tr>
<tr><td>((F+G)/2)≤0.25 mm</td></tr>
<tr><td>9</td><td>Backlight defects</td><td colspan="3">1. Light fails or flickers. (Major)
2. Color and luminance do not correspond to specifications. (Major)
3. Exceeds standards for display's blemishes or foreign matter (see test 5, Pg. 25), and dark lines or scratches (see test 6, Pg. 25). (Minor)</td><td>See list ←</td></tr>
<tr><td>10</td><td>PCB defects</td><td colspan="3">1. Oxidation or contamination on connectors.*
2. Wrong parts, missing parts, or parts not in specification.*
3. Jumpers set incorrectly. (Minor)
4. Solder (if any) on bezel, LED pad, zebra pad, or screw hole pad is not smooth. (Minor)
*Minor if display functions correctly. Major if the display fails.</td><td>See list ←</td></tr>
<tr><td>11</td><td>Soldering defects</td><td colspan="3">1. Unmelted solder paste.
2. Cold solder joints, missing solder connections, or oxidation.*
3. Solder bridges causing short circuits.*
4. Residue or solder balls.
5. Solder flux is black or brown.
*Minor if display functions correctly. Major if the display fails.</td><td>Minor</td></tr>
</table>

APPENDIX B: SAMPLE CODE

SOURCES FOR DRIVER LIBRARIES

Graphic LCD driver libraries may save you a lot of time and help you develop a more professional product. Two library sources are RAMTEX and easyGUI.

C INITIALIZATION EXAMPLE

Below is an example of an initialization sequence based on Atmel's ATmega32.

```
//=============================================================================
// LOW_LCD.C: Low-level lcd display routines.
// Samsung KS0107+KS0108 (S6B0107+S6B0108) LCD Controller
// Atmel ATMega32 processor @ 16MHz
// WinAVR / AVR GCC + Atmel AVR Studio
// Copyright 2005, Crystalfontz America, Inc. http://www.crystalfontz.com
//=============================================================================
#include <avr/io.h>
#include <avr/iom32.h>
#include <string.h>
#include <avr/delay_x.h>
#include "typedefs.h"
#include "utils.h"
#include "low_lcd.h"
//=============================================================================
//This is the display memory.
ubyte
  display[8][128];  //1024 bytes
//=============================================================================
void write_both_lcd_control_registers(ubyte data)
  {
  //We need to wait until both controller's busy bits are clear.
  //Talk to the status (instruction) register.
  //(Must happen 140nS before the RISING edge of E.)
  PORTC&=~PORTC1_LCD_DI;
  //Tell the LCD we are going to be reading it
  //(Must happen 140nS before the RISING edge of E.)
  PORTC|=PORTC6_LCD_RW;
  //Talk to the left controller only
  //(Must happen 140nS before the RISING edge of E.)
  PORTC&=~PORTC0_LCD_CS1;
  PORTD|=PORTD6_LCD_CS2;
  //Make port A high-impedance
  DDRA=0x00;
  //Enable the selected controller's read data onto the port
  PORTC|=PORTC7_LCD_E;
  //The data is not valid for 320nS
  _delay_cycles(4); //375nS
  //Wait for the busy bit to drop
```

```
  while(PINA&0x80);
  //Terminate the read
  PORTC&=~PORTC7_LCD_E;

  //Talk to the right controller only
  PORTC|=PORTC0_LCD_CS1;   //125nS
  PORTD&=~PORTD6_LCD_CS2;  //125nS
  //(Must happen 140nS before the RISING edge of E.)
  //(E LOW pulse must be 450mS min)
  _delay_cycles(2);      //250nS

  //Enable the selected controller's read data onto the port
  PORTC|=PORTC7_LCD_E;
  //The data is not valid for 320nS
  _delay_cycles(4);
  //Wait for the busy bit to drop
  while(PINA&0x80);
  //Terminate the read
  PORTC&=~PORTC7_LCD_E;

  //Tell the LCD that we are writing to it.
  //(Must happen 140nS before the RISING edge of E.)
  PORTC&=~PORTC6_LCD_RW;    //125nS
   //Talk to both controllers
  //(Must happen 140nS before the RISING edge of E.)
  PORTC&=~PORTC0_LCD_CS1;   //125nS
  //stretch LOW E pulse width above the minimum of 450nS
  _delay_cycles(2);        //250nS
  //Strobe the E pin. We are still aimed at the status/instruction register.
  PORTC|=PORTC7_LCD_E;
  //Write the data to the output latches of port A
  //(Must happen 200nS before the FALLING edge of E.)
  PORTA=data;           //62.5nS
  //Go back to port A as an output
  DDRA=0xFF;            //125nS
  //stretch HIGH E pulse width above the minimum of 450nS
  _delay_cycles(3);    //312.5nS
  PORTC&=~PORTC7_LCD_E;
  }
//===============================================================================
// PORTC0_LCD_CS1 and PORTD6_LCD_CS2 must be set to select the desired
// controller
//-------------------------------------------------------------------------------
void write_lcd_data(ubyte data)
  {
  //We need to wait until the busy bit is clear.
  //Talk to the status (instruction) register.
  //(Must happen 140nS before the RISING edge of E.)
  PORTC&=~PORTC1_LCD_DI;
  //Tell the LCD we are going to be reading it
  //(Must happen 140nS before the RISING edge of E.)
  PORTC|=PORTC6_LCD_RW;
  //Make port A high-impedance
  DDRA=0x00;
```

```
  //Enable the selected controller's read data onto the port
  PORTC|=PORTC7_LCD_E;
  //The data from the LCD is not valid for 320nS
  _delay_cycles(4); //375nS
  //Wait for the busy bit to drop
  while(PINA&0x80);
  //Terminate the read
  PORTC&=~PORTC7_LCD_E;
  //Tell the LCD that we are writing to it.
  //(Must happen 140nS before the RISING edge of E.)
  PORTC&=~PORTC6_LCD_RW;   //125nS
  //Aim at the data register.
  //(Must happen 140nS before the RISING edge of E.)
  PORTC|=PORTC1_LCD_DI;   //125nS
  //stretch LOW E pulse width above the minimum of 450nS
  _delay_cycles(2);      //250nS
  //Strobe the E pin.
  PORTC|=PORTC7_LCD_E;
  //Write the data to the output latches of port A
  //(Must happen 200nS before the FALLING edge of E.)
  PORTA=data;            //62.5nS
  //Go back to port A as an output
  DDRA=0xFF;             //125nS
  //stretch HIGH E pulse width above the minimum of 450nS
  _delay_cycles(3);     //312.5nS
  //Terminate the write
  PORTC&=~PORTC7_LCD_E;
  }
//===============================================================================
// Takes about 5.08ms (201.7KB/S) reading busy flag
void UpdateLCD(void)
  {
  register ubyte
    *left_data;
  register ubyte
    *right_data;
  register ubyte
    page_address;
  register ubyte
    column_address;

  //Initialize our source data pointers.
  left_data=&display[0][0];
  right_data=&display[0][64];

  //Make sure we are not in a write cycle
  PORTC&=~PORTC7_LCD_E;

  //Make sure the LCD thinks we are writing
  PORTC&=~PORTC6_LCD_RW;

  for(page_address=0;page_address<=7;page_address++)
    {
```

```
    //Set Y address (page, or horizontal stripe of 8 pixels) (controller docs call this
"X")
    write_both_lcd_control_registers(0xB8|page_address);
    //Set X address 0 (right to left) (controller docs call this "Y")
    write_both_lcd_control_registers(0x40);

    for(column_address=0;column_address<=63;column_address++)
      {
      //Talk to the left controller only
      PORTC&=~PORTC0_LCD_CS1;
      PORTD|=PORTD6_LCD_CS2;
      write_lcd_data(*left_data++);
      //Talk to the right controller only
      PORTC|=PORTC0_LCD_CS1;
      PORTD&=~PORTD6_LCD_CS2;
      write_lcd_data(*right_data++);
      }
    //Skip down to the next line
    left_data+=64;
    right_data+=64;
    }
  }
//=============================================================================
void InitializeLCD(void)
  {
  //Display on
  write_both_lcd_control_registers(0x3F);

  //Set Start Line 0
  write_both_lcd_control_registers(0xC0);

  //Clear the display memeory
  memset(display,0x00,sizeof(display));
  }
//=============================================================================
```

EXAMPLE TO USE WITH THE CFA-10006 DEMONSTRATION BOARD KIT

```
//=============================================================================
// CFA-10006-12864B Demonstration code
// LOW_LCD.C: Low-level lcd display routines.
// Samsung KS0107+KS0108 (S6B0107+S6B0108) LCD Controller
// Atmel ATMega32 processor @ 16MHz
// WinAVR / AVR GCC + Atmel AVR Studio
// Written by Brent A. Crosby
// Copyright 2005, Crystalfontz America, Inc. http://www.crystalfontz.com
//=============================================================================
#include <avr/io.h>
#include <util/delay.h>
#include <avr/iom2561.h>
```

```
#include <avr/pgmspace.h>
#include <string.h>
#include "utils.h"
#include "low_lcd.h"
#include "logo_screen.h"
//===========================================================================
//This is the display memory.
volatile unsigned char display[8][128];  //1024 bytes

//===========================================================================
volatile unsigned char display_status;

//===========================================================================
void write_both_lcd_control_registers(unsigned char data)
{
      //We need to wait until both controller's busy bits are clear.
      //Talk to the status (instruction) register.
      CLR_RS;
      //Tell the LCD we are going to be reading it
      SET_RW;
      //Talk to the left controller only
      SET_CS2;
      CLR_CS1;
      //Make port A high-impedance so we can read from the LCD
      LCD_DATA_DDR = LCD_DATA_ALL_INPUTS;
      //Enable the selected controller's read data onto the port
      SET_E;
      _delay_us(6500);
      //Wait for the busy bit to drop
      while(PINA&0x80);
      //Terminate the read
      CLR_E;
      _delay_us(6500);       //stretch LOW E pulse width

      //Talk to the right controller only
      CLR_CS2;
      SET_CS1;
      _delay_us(6500);

      //Enable the selected controller's read data onto the port
      SET_E;
      _delay_us(6500);
      //Wait for the busy bit to drop
      while(PINA&0x80);
      //Terminate the read
      CLR_E;
      _delay_us(6500);    //stretch LOW E pulse width

      //Write the data to the output latches of port A
      LCD_DATA_PORT = data;
      //Tell the LCD that we are writing to it.
      CLR_RW;
      //Talk to both controllers (right controller already active)
      CLR_CS1;
```

```
	//Strobe the E pin. We are still aimed at the status/instruction register.
	SET_E;
	//Go back to port A as an output
	LCD_DATA_DDR = LCD_DATA_ALL_OUTPUTS;
	_delay_us(6500);    //stretch LOW E pulse width
	CLR_E;
	_delay_us(6500);    //stretch LOW E pulse width
}

//===========================================================================
// PORTC0_LCD_CS1 and PORTD6_LCD_CS2 must be set to select the desired
// controller
//---------------------------------------------------------------------------
void write_lcd_data(unsigned char data)
{
	//We need to wait until both controller's busy bits are clear.
	//Talk to the status (instruction) register.
	CLR_RS;
	//Tell the LCD we are going to be reading it
	SET_RW;
	//Make port A high-impedance
	LCD_DATA_DDR = LCD_DATA_ALL_INPUTS;
	//Enable the selected controller's read data onto the port
	SET_E;
	_delay_us(6500);
	//Wait for the busy bit to drop
	while(PINA&0x80);
	//Terminate the read
	CLR_E;
	_delay_us(6500);      //stretch LOW E pulse width

	//Write the data to the output latches of port A
	LCD_DATA_PORT = data;
	//Tell the LCD that we are writing to it.
	CLR_RW;
	//Aim at the data register.
	SET_RS;
	//Strobe the E pin.
	SET_E;
	//Go back to port A as an output
	LCD_DATA_DDR = LCD_DATA_ALL_OUTPUTS;            //125nS
	_delay_us(6500);     //stretch LOW E pulse width
	//Terminate the write
	CLR_E;
	_delay_us(6500);     //stretch LOW E pulse width
}


//===========================================================================
// Takes about 5.08ms (201.7KB/S) reading busy flag
void UpdateLCD(void)
{
	register volatile unsigned char *left_data;
	register volatile unsigned char *right_data;
```

```
      register unsigned char page_address;
      register unsigned char column_address;

      //Initialize our source data pointers.
      left_data =& display[0][0];
      right_data =& display[0][64];

      for (page_address = 0; page_address <= 7; page_address++)
      {
            //Set Y address (page, or horizontal stripe of 8 pixels) (controller docs
call this "X")
            write_both_lcd_control_registers(0xB8 | page_address);
            //Set X address 0 (right to left) (controller docs call this "Y")
            write_both_lcd_control_registers(0x40);

            for (column_address = 0; column_address <= 63; column_address++)
            {
                  //Talk to the left controller only
                  SET_CS2;
                  CLR_CS1;
                  write_lcd_data(*left_data++);
                  //Talk to the right controller only
                  CLR_CS2;
                  SET_CS1;
                  write_lcd_data(*right_data++);
            }
            //Skip down to the next line
            left_data += 64;
            right_data += 64;
      }

      // Clear both chip selects
      SET_CS2;
      SET_CS1;

}

void ResetLCD(void)
{
      LCD_CTRL_PORT &= ~(1 << LCD_RST);
      _delay_us(6500);
      LCD_CTRL_PORT |= (1 << LCD_RST);
}

//===========================================================================
void InitializeLCD(void)
{
      /* Take the LCD out of reset (if reset was low)
*/
      LCD_CTRL_PORT |= (1 << LCD_RST);

      /* Never reading status, clear LCD_RW low for writes only
* Clear LCD_E to low
*/
```

```
	CLR_RW;
	_delay_us(6500);
	LCD_CTRL_PORT &= ~(1 << LCD_E);

	//Display on
	write_both_lcd_control_registers(0x3F);

	//Set Start Line 0
	write_both_lcd_control_registers(0xC0);

	//Clear the display memeory
	memset(display, 0x00, sizeof(display));
}
//=============================================================================
```

APPENDIX C: NEOTEC NT7107C 64 CH COMMON DRIVER SPECIFICATIONS

The complete Neotec NT7107C 64 channel common driver specifications follows.

NT7107

Appendix

INTRODUCTION

The NT7107 is a LCD driver LSI with 64 channel outputs for dot matrix liquid crystal graphic display systems. This device provides 64 shift registers and 64 output drivers. It generates the timing signal to control the NT7108.

The NT7107 is fabricated by low power CMOS high voltage process technology, and is composed of the liquid crystal display system in combination with the NT7108 (64 channel segment driver).

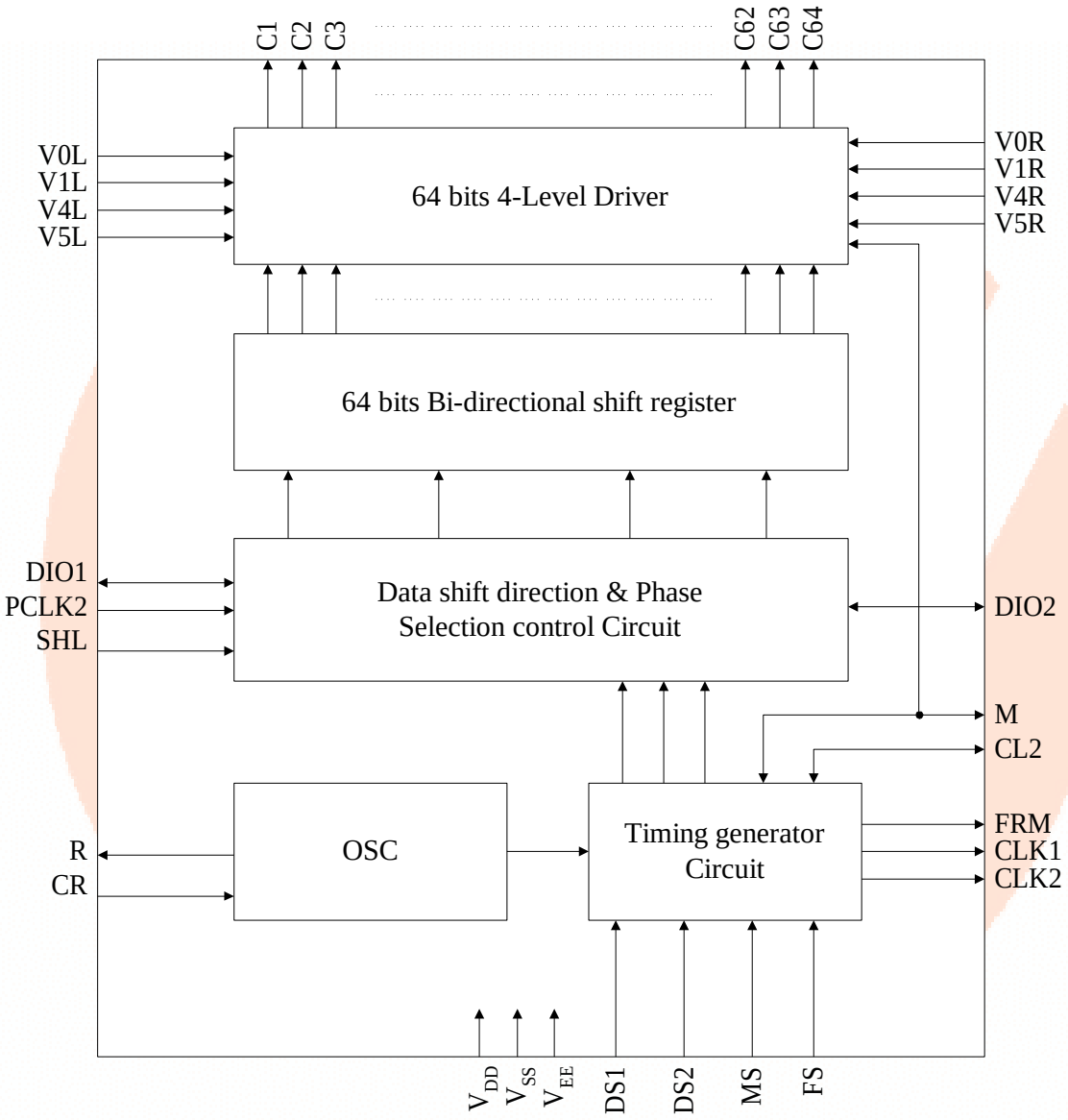
FEATURES

- Dot matrix LCD common driver with 64 channel output
- 64-bit shift register at internal LCD driver circuit
- Internal timing generator circuit for dynamic display
- Selection of master/slave mode
- Applicable LCD duty: 1/48, 1/64, 1/96, 1/128
- Power supply voltage:+2.7~+5.5V
- LCD driving voltage: 8V~17V (VDD-VEE)
- Interface

Driver		**Controller**
COMMON	SEGMENT	
Other NT7107	Other NT7108	MPU

- High voltage CMOS process
- 100QFP or bare chip available

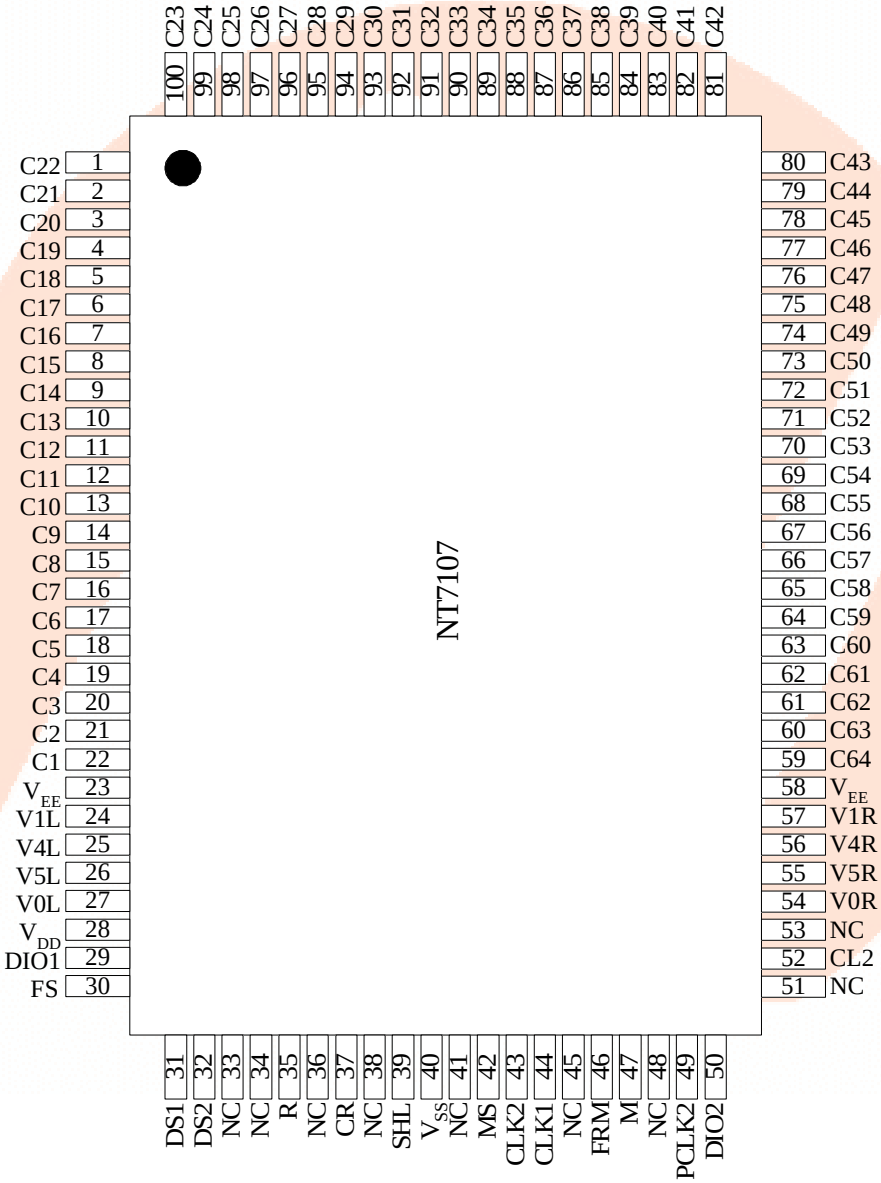
BLOCK DIAGRAM



Appendix

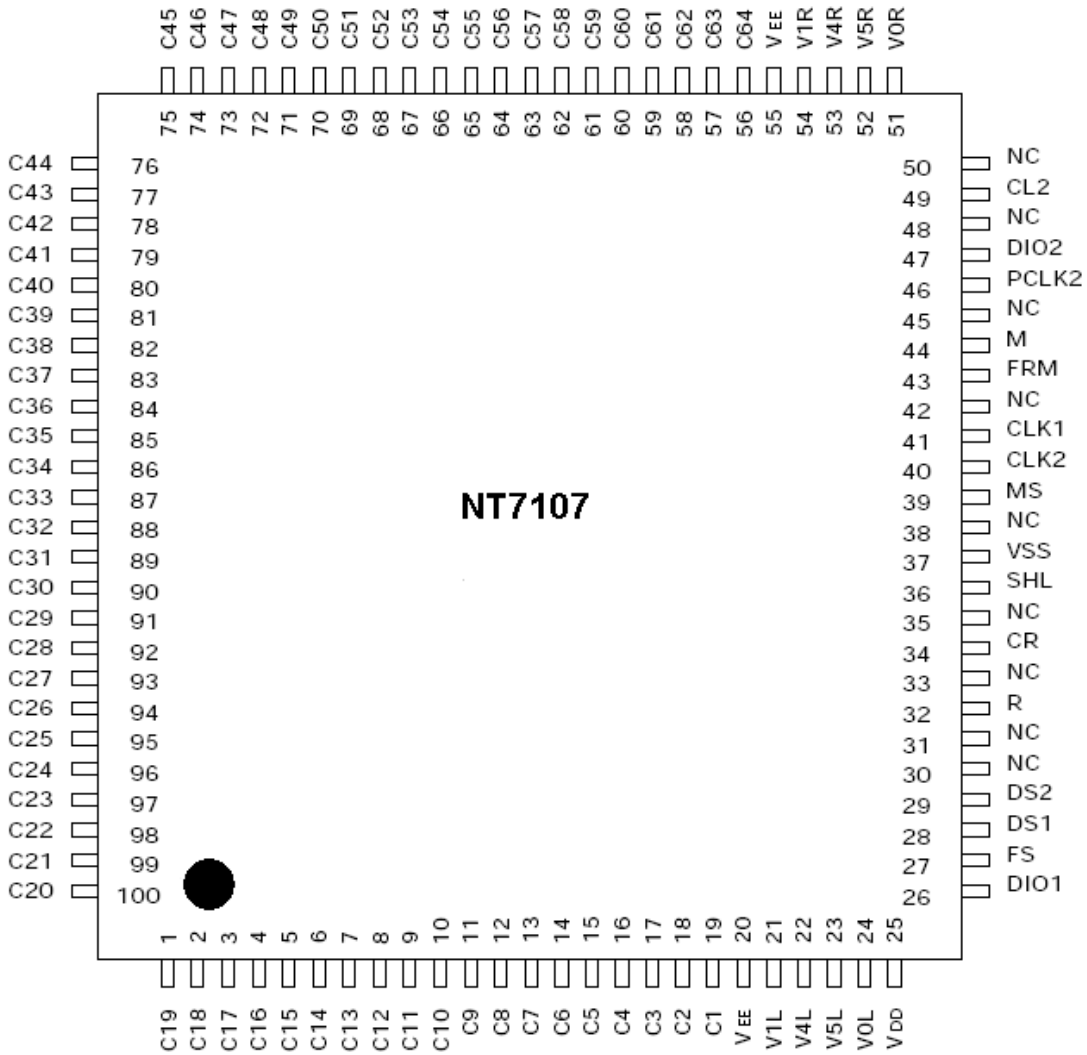
PIN CONFIGULATION

100 PQFP PACKAGE



Appendix

100 PQ PACKAGE



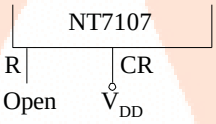
PIN DESCIPTION

Table 1. Pin Description

Pin Number QFP	Symbol	I/O	Description
28	V_{DD}	Power	For internal logic circuit (+2.7~+5.5V)
40	V_{SS}		GND (=0V)
23,58	V_{EE}		For LCD driver circuit
27,54	V0L,V0R	Power	Bias supply voltage terminals to drive LCD.
24,57	V1L,V1R		**Select Level** / **Non-Select Level**: V0L (R), V5L (R) / V1L (R), V4L (R)
25,56	V4L,V4R		
26,55	V5L,V5R		The same voltage should connect V0L and V0R (V1L & V1R, V4L & V4R, V5L & V5R).
42	MS	Input	Section of master/slave mode · Master mode (MS=1) DIO1, DIO2, CL2 and M is output state. · Salve mode (MS=0) SHL=1 DIO1 is input state (DIO2 is output state) SHL=0 DIO2 is input state (DIO1 is output state) CL2 and M are input state.
39	SHL	Input	Selection of data shift direction. **SHL** / **Data Shift Direction**: H / DIO1 C1....C64 DIO2; L / DIO2 C64....C1 DIO1
49	PCLK2	Input	Selection of shift clock (CL2) phase. **PCLK2** / **Data Clock (CL2) Phase**: H / Data shift at the rising edge of CL2; L / Data shift at the falling edge of CL2
30	FS	Input	Selection of oscillation frequency. · Master mode when the frame frequency is 70 Hz, the oscillation frequency should be fosc=430kHz at FS=1(V_{DD}) fosc=215kHz at FS=0(Vss) · Slave mode Connect to V_{DD}
31 32	DS1 DS2	Input	Selection of display duty. · Master mode **DS1** / **DS2** / **Duty**: L / L / 1/48; L / H / 1/64; H / L / 1/96; H / H / 1/128 · Slave mode Connect to V_{DD}

Appendix

<table>
<tr><th>Pin Number
QFP</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>35
37</td><td>R
CR</td><td></td><td>RC Oscillator (Built-in capacitor)
· Master mode: Use these terminals as shown below.
 

· Slave mode: Stop the oscillator as shown below.
 
</td></tr>
<tr><td>44
43</td><td>CLK1
CLK2</td><td>Output</td><td>Operating clock output for the NT7108
· Master mode: connection to CLK1 and CLK2 of the NT7108
· Slave mode: open</td></tr>
<tr><td>46</td><td>FRM</td><td>Output</td><td>Synchronous frame signal.
· Master mode: connection to FRM of the NT7108
· Slave mode: open</td></tr>
<tr><td>47</td><td>M</td><td>Input/
Output</td><td>Alternating signal input for LCD driving.
· Master mode: output state Connection to M of the NT7108
· Slave mode: input state Connection to the controller</td></tr>
<tr><td>52</td><td>CL2</td><td>Input/
Output</td><td>Data shift clock
· Master mode: output state Connection to CL of the NT7108
· Slave mode: input state connection to shift clock terminal of the controller.</td></tr>
<tr><td>29
50</td><td>DIO1
DIO2</td><td>Input/
Output</td><td>Data input/output pins of internal shift register.
<table>
<tr><th>MS</th><th>SHL</th><th>DIO1</th><th>DIO2</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Output</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>22-1
100-59</td><td>C1-C64</td><td>Output</td><td>Common signal output for LCD driving.
<table>
<tr><th>Data</th><th>M</th><th>Out</th></tr>
<tr><td rowspan="2">L</td><td>L</td><td>V1</td></tr>
<tr><td>H</td><td>V4</td></tr>
<tr><td rowspan="2">H</td><td>L</td><td>V5</td></tr>
<tr><td>H</td><td>V0</td></tr>
</table></td></tr>
<tr><td>33
34,36
38,41
45,48
51,53</td><td>NC</td><td></td><td>No connection</td></tr>
</table>

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit	Note
Operating voltage	V_{DD}	-0.3 to +7.0	V	(1)
Supply voltage	V_{EE}	VDD-19.0 to VDD+0.3		(4)
Driver supply voltage	V_B	-0.3 to VDD+0.3		(1),(2)
	V_{LCD}	VEE-0.3 to VDD+0.3		(3),(4)
Operating temperature	T_{OPR}	-30 to +85	℃	-
Storage temperature	T_{STG}	-55 to +125		-

NOTES:

1. Based on Vss=0V
2. Applies to input terminals and I/O terminals at high impedance. (Except V0L(R), V1L(R), V4L(R) and V5L(R))
3. Applies to V0L(R), V1L(R), V4L(R) and V5L(R).
4. Voltage level: VDD≧V0L=V0R≧V1L=V1R≧V4L=V4R≧V5L=V5R≧VEE.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{DD}=+5.0V, Vss=0V, $|V_{DD}-V_{EE}|$=8~17V, TA=-30 ~+85℃)

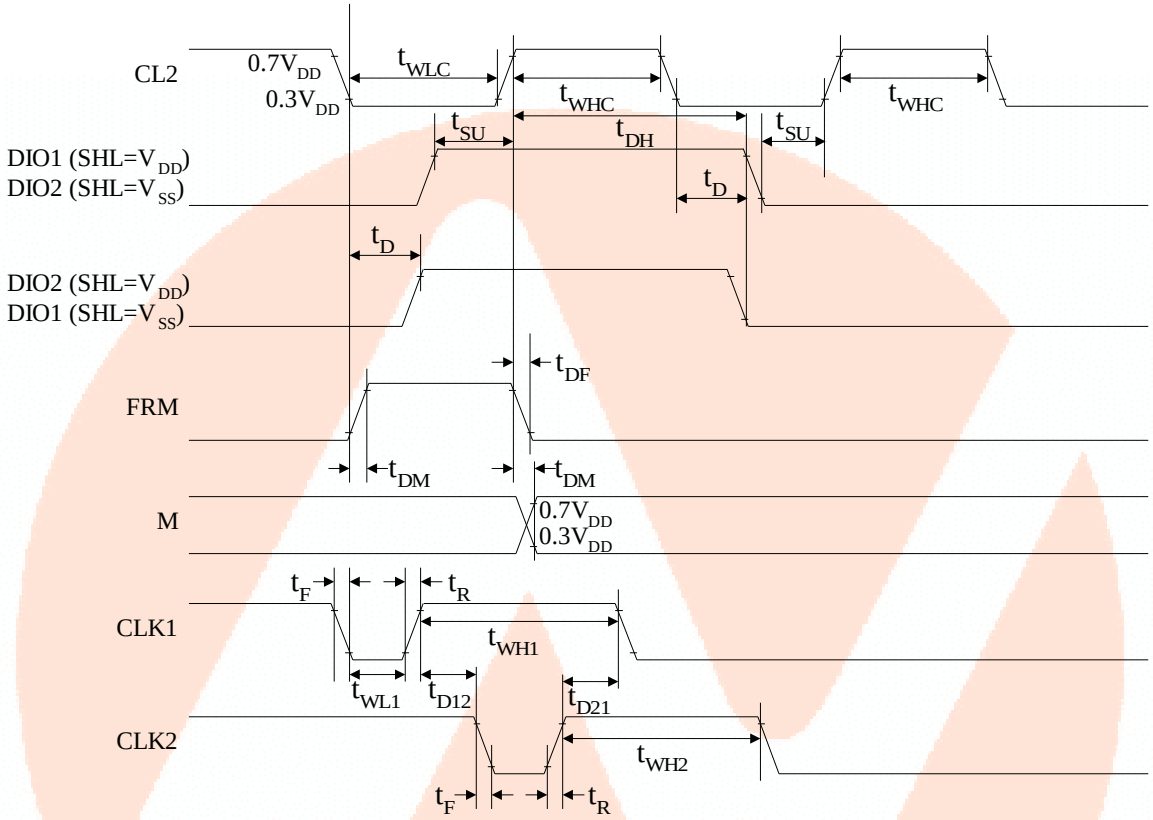
Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating voltage		V_{DD}	-	2.7	-	5.5	V	
Input Voltage	High	V_{IH}	-	$0.7V_{DD}$	-	V_{DD}		(1)
	Low	V_{IL}	-	V_{SS}	-	$0.3V_{DD}$		
Output Voltage	High	V_{OH}	I_{OH}=-0.4mA	V_{DD}-0.4	-	-		(2)
	Low	V_{OL}	I_{OL}=0.4mA	-	-	0.4		
Input leakage current		I_{LKG}	$V_{IN}=V_{DD}-V_{SS}$	-1.0	-	1.0	μA	(1)
OSC frequency		f_{OSC}	Rf=47KΩ±2%	315	450	585	kHz	
On resistance (V_{DIV} - C_i)		R_{ON}	$V_{DD}-V_{EE}$=17V Load current = ±150 μA	-	-	1.5	KΩ	
Operating current		I_{DD1}	Master mode; 1/128duty	-	-	1.0	mA	(3)
		I_{DD2}	Slave mode; 1/128 duty	-	-	200	μA	(4)
Supply current		I_{EE}	Master mode; 1/128 duty	-	-	100		(5)
Operating Frequency		f_{OP1}	Master mode; External clock	50	-	600	kHz	
		f_{OP2}	Slave mode	0.5	-	1500		

NOTES:

1. Applies to input terminals FS, DS1, DS2, CR, SHL, MS and PCLK2 and I/O terminals DIO1, DIO2, M and CL2 in the input state.
2. Applies to output terminals CLK1, CLK2 and FRM and I/O terminals DIO1, DIO2, M and CL2 in the Output State.
3. This value is specified at about the current flowing through Vss. Internal oscillation circuit: Rf = 47kΩ, Each terminal of DS1, DS2, FS, SHL and MS is connected to V_{DD} and out is no load.
4. This value is specified at about the current flowing through Vss. Each terminal of DS1, DS2, FS, SHL, PCLK2 and CR is connected to V_{DD}, and MS is connected to Vss. CL2, M, DIO1 is external clock.
5. This value is specified at the current flowing through V_{EE}. Don connect to V_{LCD} (V1-V5).

AC CHARACTERISTICS (V_{DD}=5V±10%, TA=-30 ~+85℃)

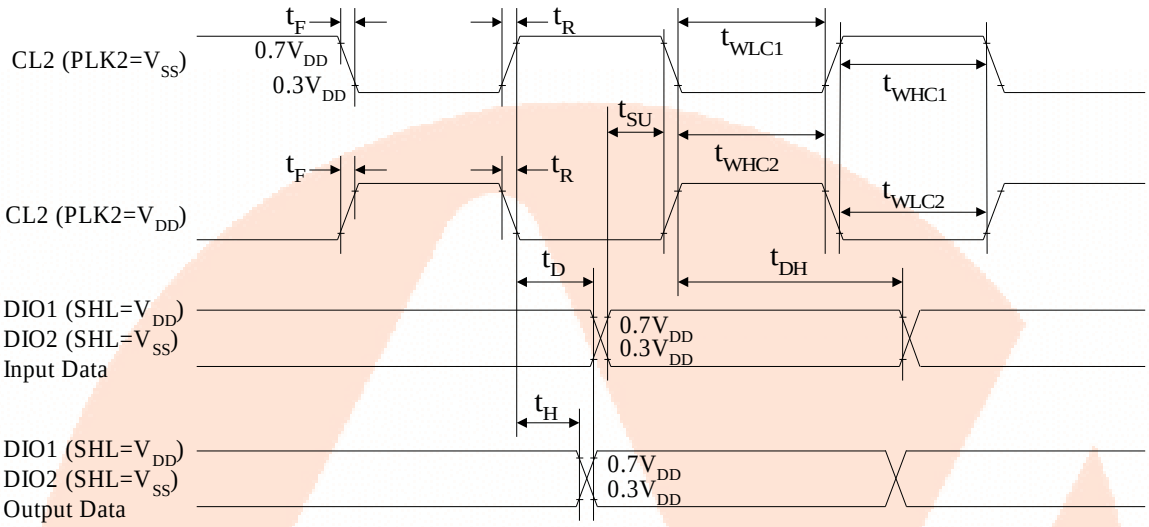
Master Mode (MS=V_{DD}, PCLK2=V_{DD})



Master Mode

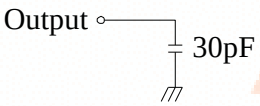
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Data setup time	t_{SU}	20	-	-	μs
Data hold time	t_{DH}	40	-	-	
Data delay time	t_D	5	-	-	
FRM delay time	t_{DF}	-2	-	2	
M delay time	t_{DM}	-2	-	2	
CL2 low level width	t_{WLC}	35	-	-	
CL2 high level width	t_{WHC}	35	-	-	
CLK1 low level width	t_{WL1}	700	-	-	ns
CLK2 low level width	t_{WL2}	700	-	-	
CLK1 high level width	t_{WH1}	2100	-	-	
CLK2 high level width	t_{WH2}	2100	-	-	
CLK1-CLK2 phase difference	t_{D12}	700	-	-	
CLK2-CLK1 phase difference	t_{D21}	700	-	-	
CLK1,CLK2 rise/fall time	t_R/ t_F	-	-	150	

Slave Mode (MS=V_{SS})



Characteristic	Symbol	Min.	Typ.	Max.	Unit	Note
CL2 low level width	t_{WLC1}	450	-	-	ns	PCLK2=V_{SS}
CL2 high level width	t_{WHC1}	150	-	-		PCLK2=V_{SS}
CL2 low level width	t_{WLC2}	150	-	-		PCLK2=V_{DD}
CL2 high level width	t_{WHC2}	450	-	-		PCLK2=V_{DD}
Data setup time	t_{SU}	100	-	-		
Date hold time	t_{DH}	100	-	-		
Data delay time	t_D	-	-	200		(NOTE)
Output data hold time	t_H	10	-	-		
CL2 rise/fall time	t_R/ t_F	-	-	30		

NOTE: Connect load CL = 30pF

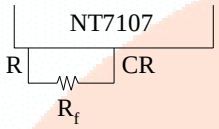


FUNCTIONAL DESCRIPTION

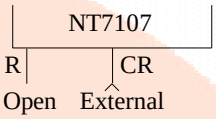
RC Oscillator

The RC Oscillator generates CL2, M, FRM of the NT7107, and CLK1 and CLK1 of the NT7108 by the oscillation resister R and internal capacitor C. When selecting the master/slave mode, the oscillation circuit is as following:

Master Mode: In the master mode, use these terminals as shown below.

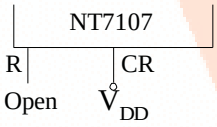


Internal Oscillation(Rf=47kΩ)



External Clock

Slave Mode: In the slave mode, stop the oscillator as shown below.



Timing Generation Circuit

It generates CL2, M, FRM, CLK1 and CLK2 by the frequency from the oscillation circuit.

Selection of Master/Slave (M/S) Mode

When MS is H, it generates CL2, M, FRM, CLK1 and CLK2 internally.

When MS is L, it operates by receiving M and CL2 from the master device.

Frequency Selection (FS)

To adjust FRM frequency by 70Hz, the oscillation frequency should be as follows:

FS	Oscillation Frequency
H	f_{OSC}=430kHz
L	f_{OSC}=215kHz

In the slave mode, it is connected to V_{DD}.

Duty Selection (DS1, DS2)

It provides various duty selections according to DS1 and DS2.

DS1	DS2	Duty
L	L	1/48
	H	1/64
H	L	1/96
	H	1/128

Data Shift & Phase Select Control

Phase Selection

It is a circuit to shift data on synchronization of rising edge, or falling edge of the CL2 according to PCLK2.

PCLK2	Phase Selection
H	Data shift on rising edge of CL2
L	Data shift on falling edge of CL2

Data shift Direction Selection

When MS is connected to VDD, DIO1 and DIO2 terminal is only output.

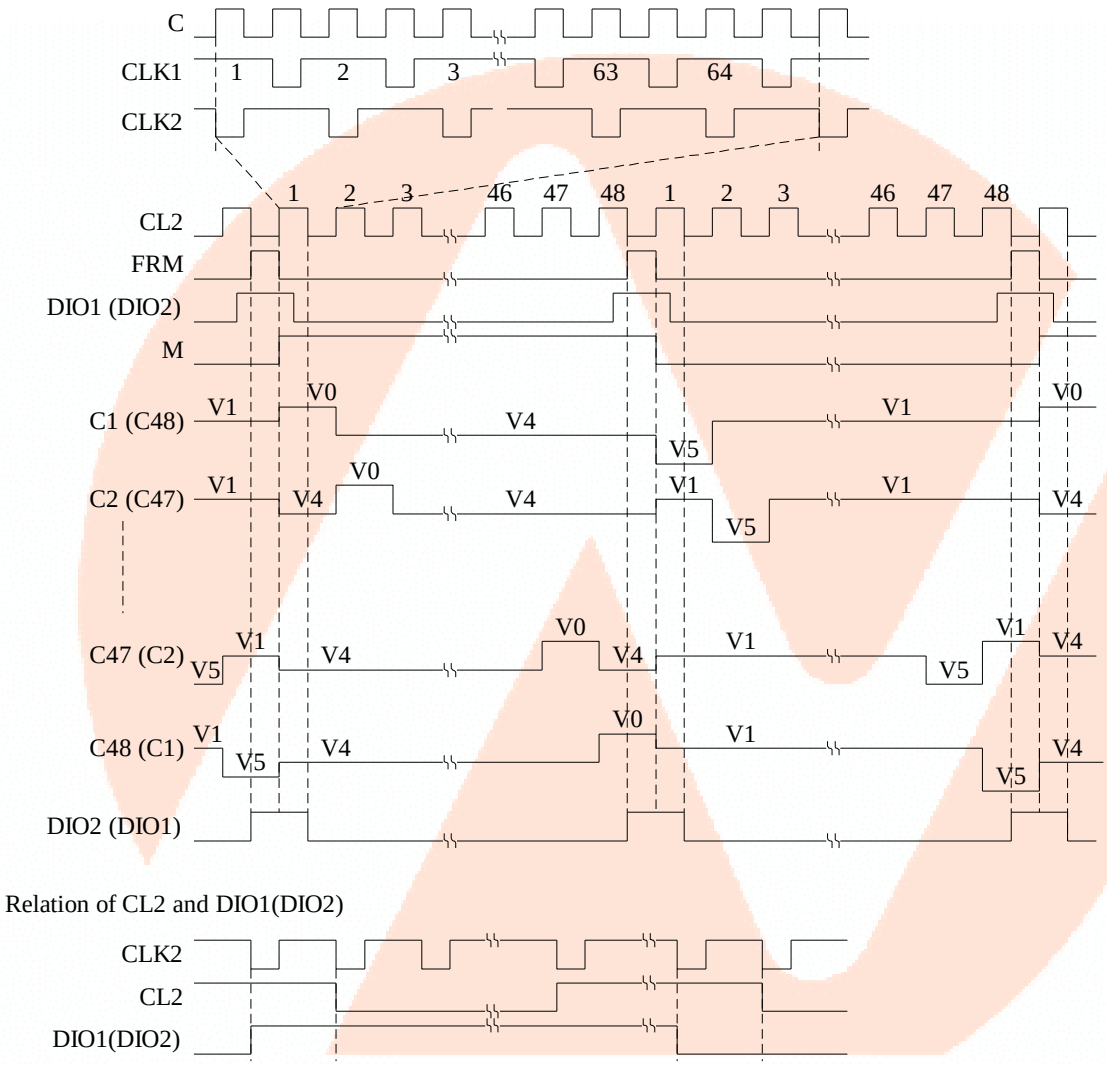
When MS is connected to Vss, it depends on the SHL.

MS	SHL	DIO1	DIO2	Direction of Data
H	H	Output	Output	C1 **à** C64
	L	Output	Output	C64 **à** C1
L	H	Input	Output	DIO1 **à** C1 **à** C64 **à** DIO2
	L	Output	Input	DIO2 **à** C64 **à** C1 **à** DIO1

TIMING DIAGRAM

1/48 DUTY TIMING (MASTER MODE)

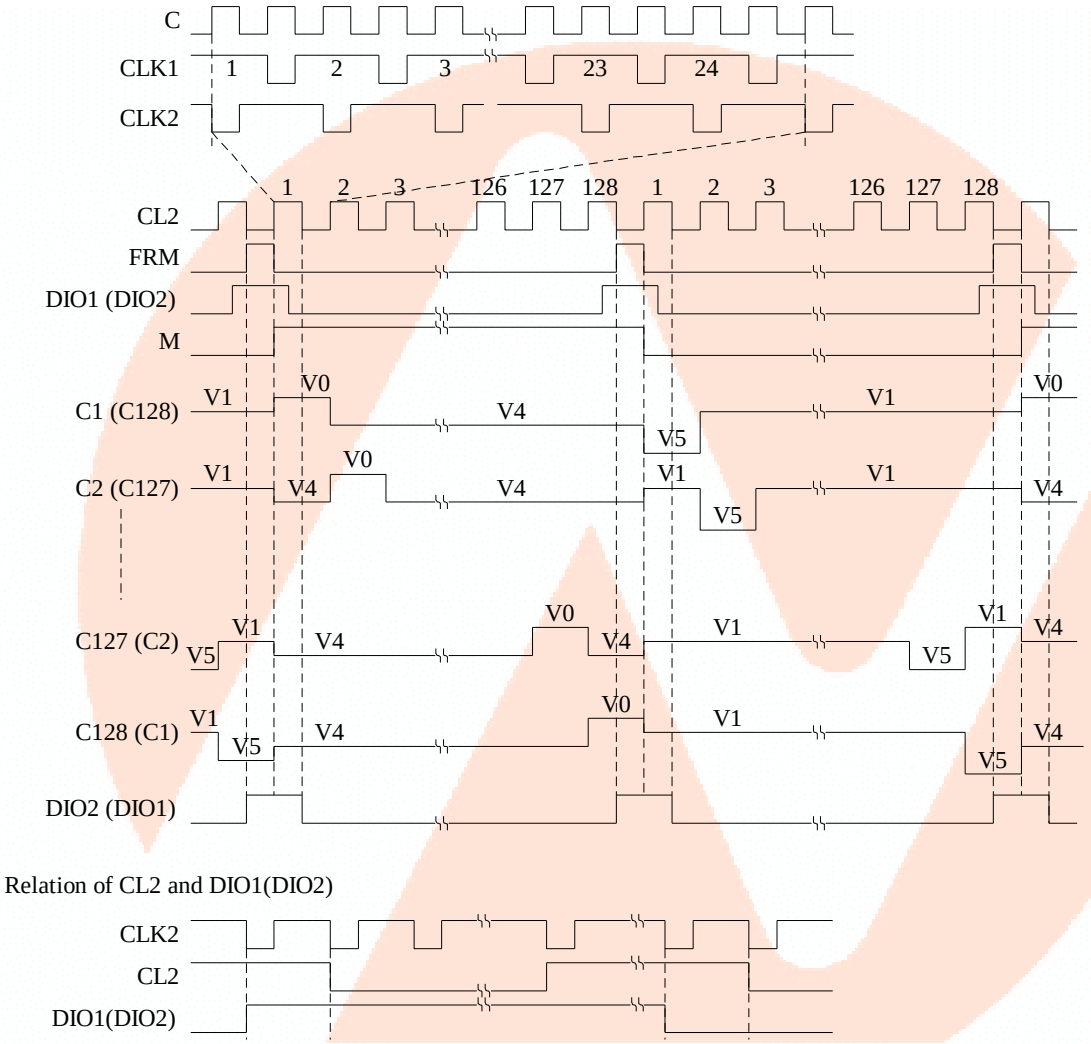
Condition: DS1=L, DS2=L, SHL=H (L), PCLK2=H



Relation of CL2 and DIO1(DIO2)

1/128 DUTY TIMING (MASTER MODE)

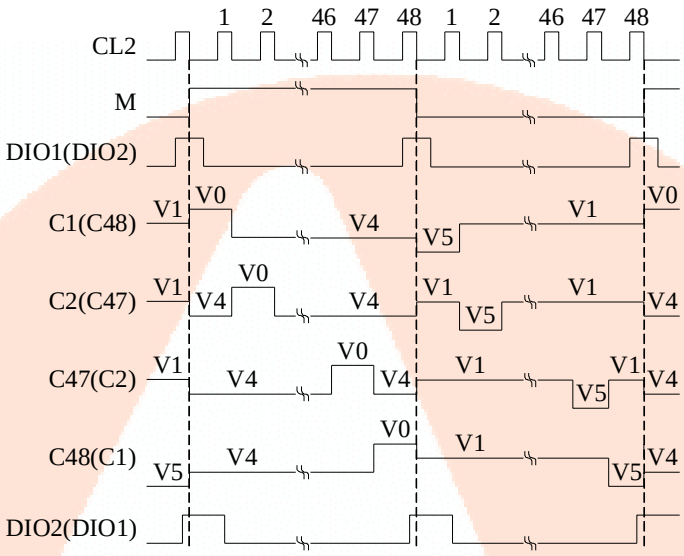
Condition: DS1=H, DS2=H, SHL=H(L), PCLK2=H



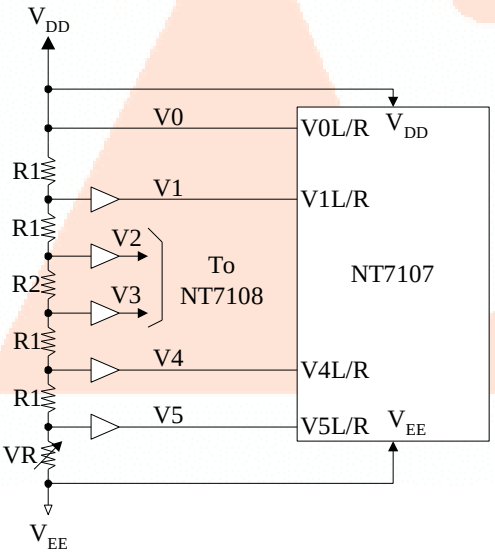
Relation of CL2 and DIO1(DIO2)

1/48 DUTY TIMING (SLAVE MODE)

Condition: SHL=H (L), PCLK2=L



POWER DRIVER CIRCUIT



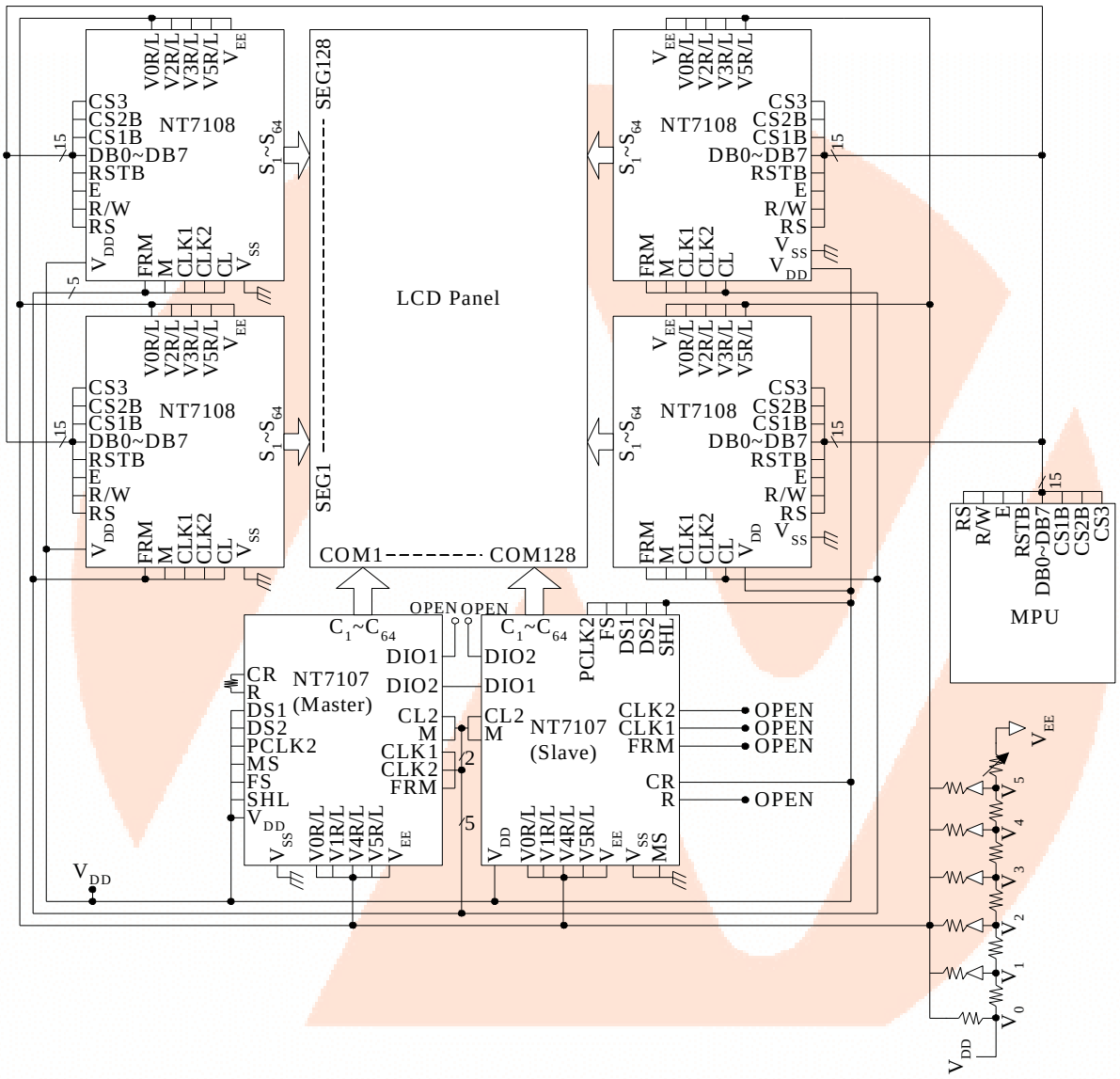
Relation of Duty & Bias

Duty	Bias	RDIV
1/48	1/8	R2=4R1
1/64	1/9	R2=5R1
1/96	1/11	R2=7R1
1/128	1/12	R2=8R1

When duty factor is 1/48, the value of R1 & R2 should satisfy.
R1/(4R1 + R2)=1/8 ;
R1=3kΩ , R2=12kΩ

APPLICATION CIRCUIT

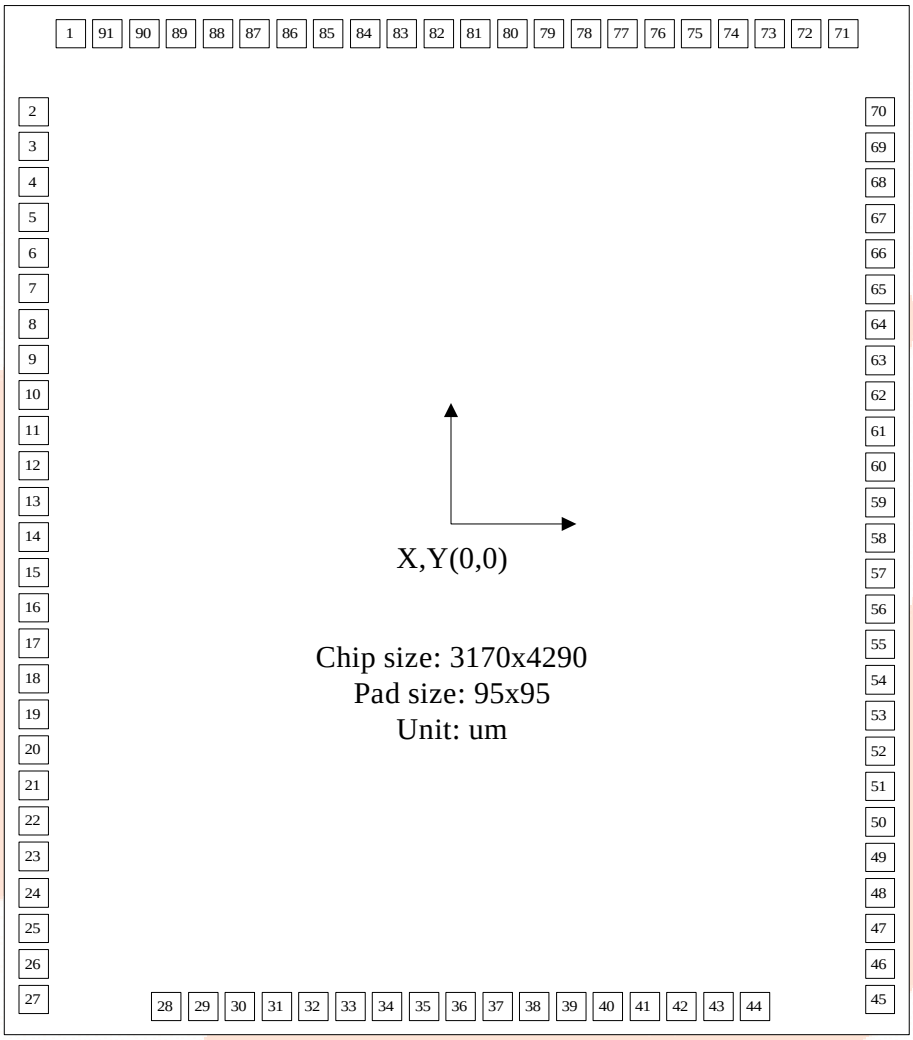
1/128 duty Segment driver (NT7108) interface circuit



Appendix

PAD DIAGRAM

Note: Please connects the substrate to V_{DD} or floating.



PAD DIAGRAM

Pad No.	Pad name	X(μm)	Y(μm)	Pad No.	Pad name	X(μm)	Y(μm)
1	C22	-1312.5	2019	47	V4R	1461.3	-1743.5
2	C21	-1461.4	1131.5	48	V1R		-1618.5
3	C20		1006.5	49	VEE		-1493.5
4	C19		881.5	50	C64		-1368.5
5	C18		756.5	51	C63		-1243.5
6	C17		631.5	52	C62		-1118.5
7	C16		506.5	53	C61		-993.5
8	C15		381.5	54	C60		-868.5
9	C14		256.5	55	C59		-743.5
10	C13		131.5	56	C58		-618.5
11	C12		6.5	57	C57		-493.5
12	C11		-118.5	58	C56		-368.5
13	C10		-243.5	59	C55		-243.5
14	C9		-368.5	60	C54		-118.5
15	C8		-493.5	61	C53		6.5
16	C7		-618.5	62	C52		131.5
17	C6		-743.5	63	C51		256.5
18	C5		-868.5	64	C50		381.5
19	C4		-993.5	65	C49		506.5
20	C3		-1118.5	66	C48		631.5
21	C2		-1243.5	67	C47		756.5
22	C1		-1368.5	68	C46		881.5
23	VEE		-1493.5	69	C45		1006.5
24	V1L		-1618.5	70	C44		1131.5
25	V4L		-1743.5	71	C43	1312.5	2019.9
26	V5L		-1868.5	72	C42	1187.5	
27	V0L		-1993.5	73	C41	1062.5	
28	VDD	-1029.598	-2019.8	74	C40	937.5	
29	DIO1	-904.598		75	C39	812.5	
30	FS	-773.200		76	C38	687.5	
31	DS1	-648.198		77	C37	562.5	
32	DS2	-523.198		78	C36	437.5	
33	R	-398.198		79	C35	312.5	
34	CR	-273.198		80	C34	187.5	
35	SHL	-148.198		81	C33	62.5	
36	GND	-8.198		82	C32	-62.5	
37	MS	131.800		83	C31	-187.5	
38	CLK2	262.600		84	C30	-312.5	
39	CLK1	392.600		85	C29	-437.5	
40	FRM	522.800		86	C28	-562.5	
41	M	655.600		87	C27	-687.5	
42	PCLK2	785.800		88	C26	-812.5	
43	DIO2	916.000		89	C25	-937.5	
44	CL2	1046.000		90	C24	-1062.5	
45	V0R	1461.300	-1993.5	91	C23	-1187.5	
46	V5R	1461.300	-1868.5	-	-	-	-

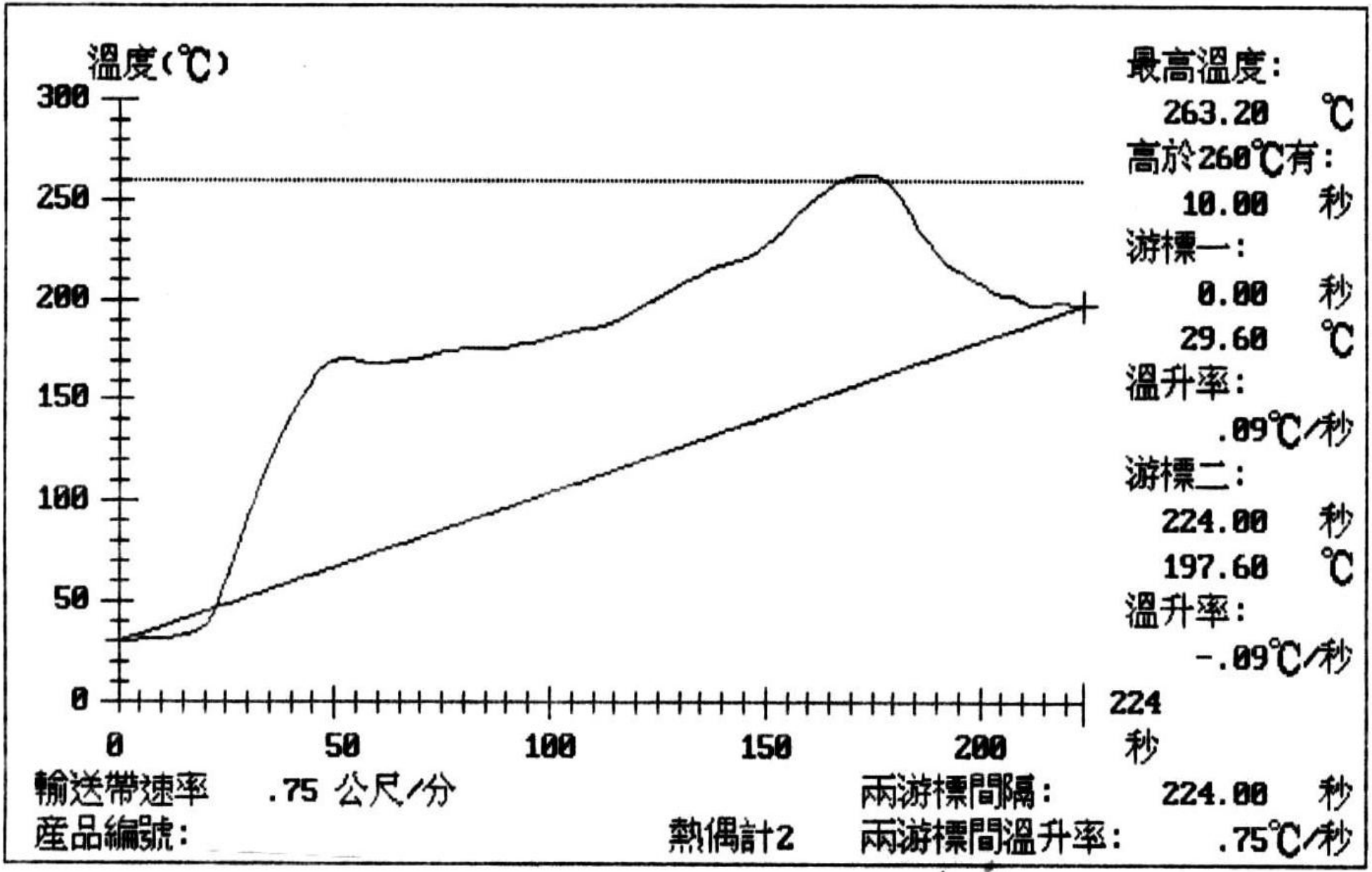
Appendix

VERSION HISTORY

Date	Description
6/5/2002	Add the notice of substrate connection.
12/11/2002	To correct some mistakes at page 6,8,10,11,15
12/18/2002	To correct some mistakes at page 4,5,6,8,9,14,15
03/15/2006	Add 100LQFP pin configuration

溫度監控系統V2.52a

新德科技　　無鉛製程　IR Reflow Profile



APPENDIX D: NEOTEC N7108C 64 CHANNEL SEGMENT DRIVE SPECIFICATIONS

The complete Neotec ICNT7108C64 channel segment driver specifications follows.

NT7108

Appendix

INTRODUCTION

The NT7108 is a LCD driver LSI with 64 channel outputs for dot matrix liquid crystal graphic display systems. This device consists of the display RAM, 64 bits data latch, 64 bit drivers and decoder logic. It has the internal display RAM for storing the display data transferred from a 8 bit micro controller and generates the dot matrix liquid crystal driving signals corresponding to stored data. The NT7108 composed of the liquid crystal display system in combination with the NT7107.

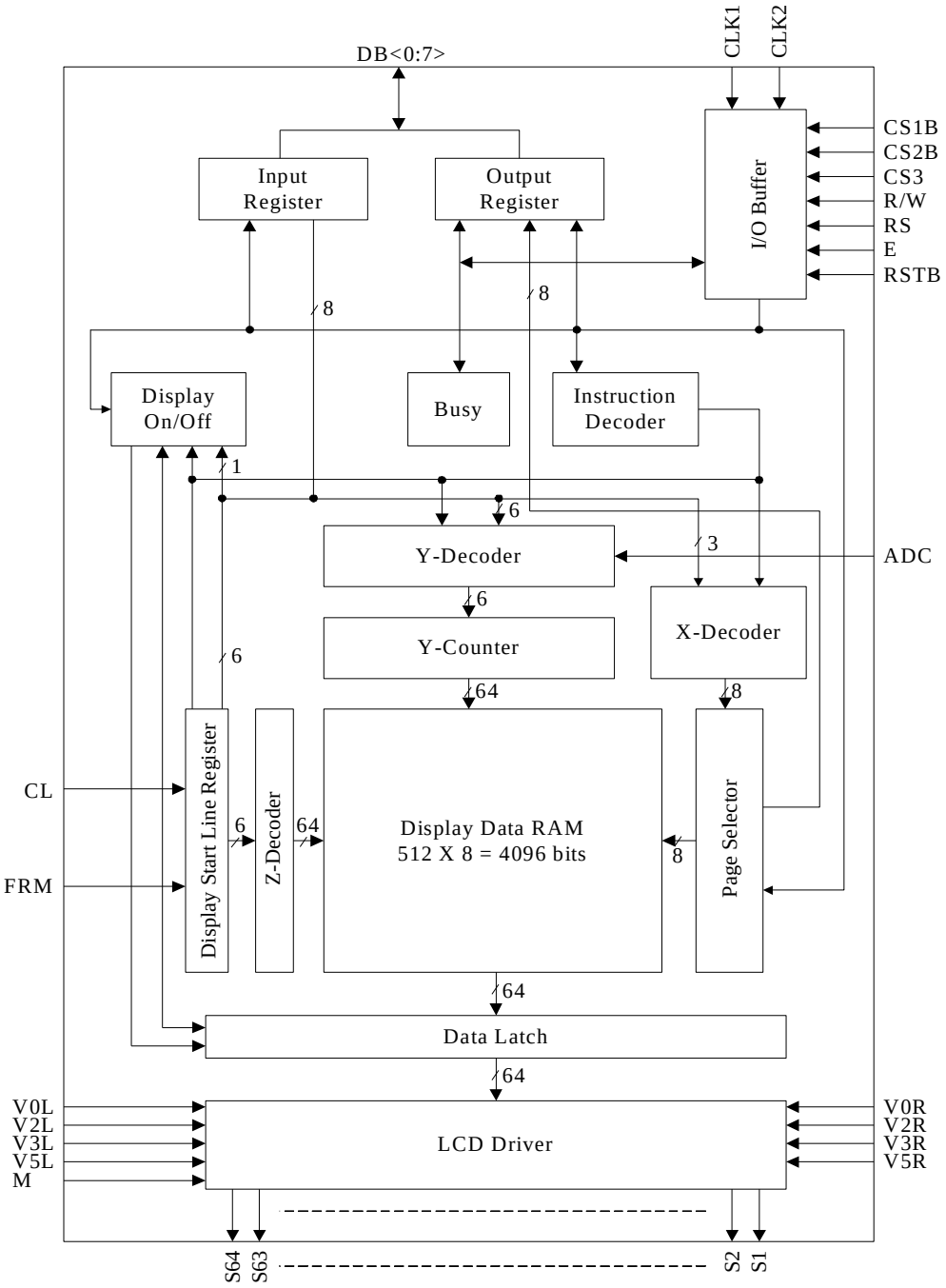
FEATURES

- Dot matrix LCD segment driver with 64 channel output
- Input and output signal
  - -Input: 8bit parallel display data control signal from MPU divided bias voltage (V0R, V0L, V2R, V2L, V3R, V3L, V5R, V5L)
  - -Output: 64 channels for LCD driving.
- Display data is stored in display data RAM from MPU.
- Interface RAM
  - -Capacity: 512 bytes (4096 bits)
  - -RAM bit data: RAM bit data = 1: On
    RAM bit data = 0: Off
- Applicable LCD duty:1/32-1/64
- LCD driving voltage: 8V-17V(VDD-VEE)
- Power supply voltage:+2.7~+5.5V
- Interface

Driver		Controller
COMMON	SEGMENT	
Other NT7107	Other NT7108	MPU

- High voltage CMOS process.
- 100QFP or bare chip available.

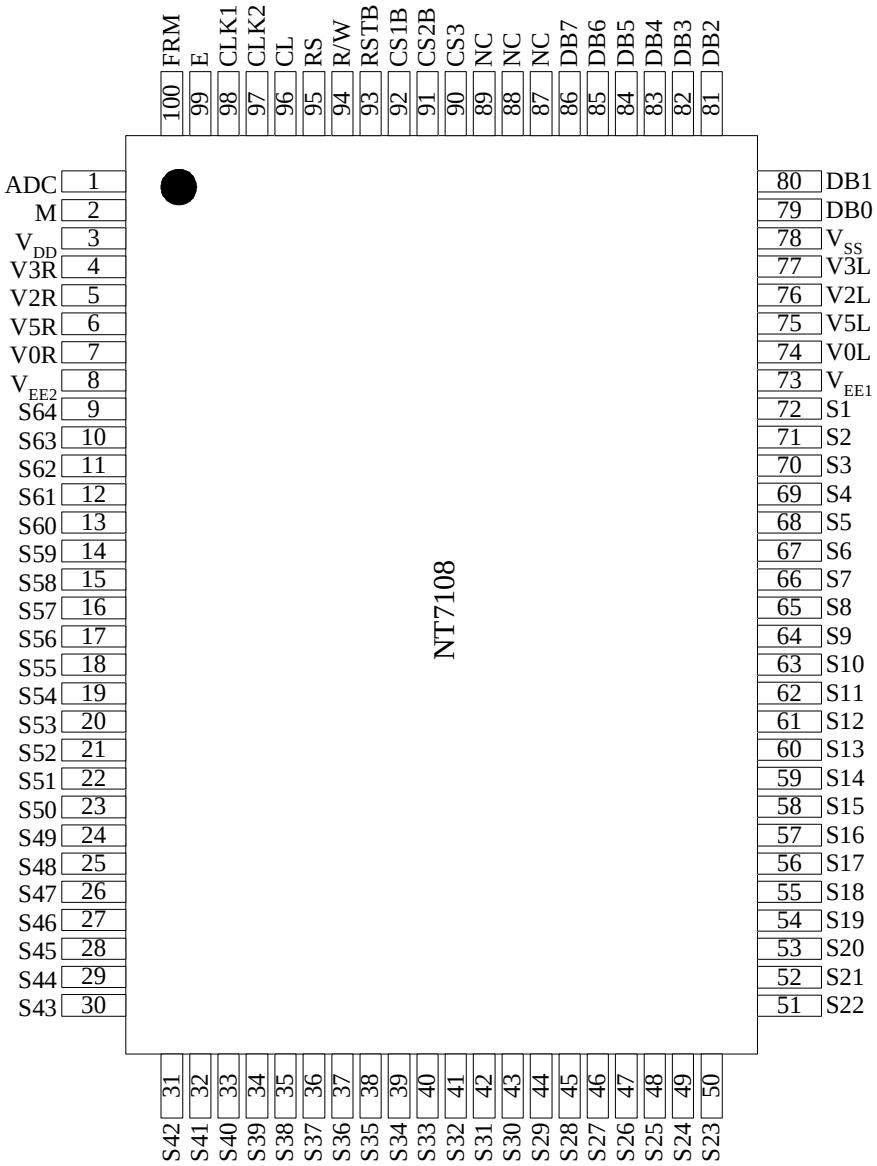
BLOCK DIAGRAM



Appendix

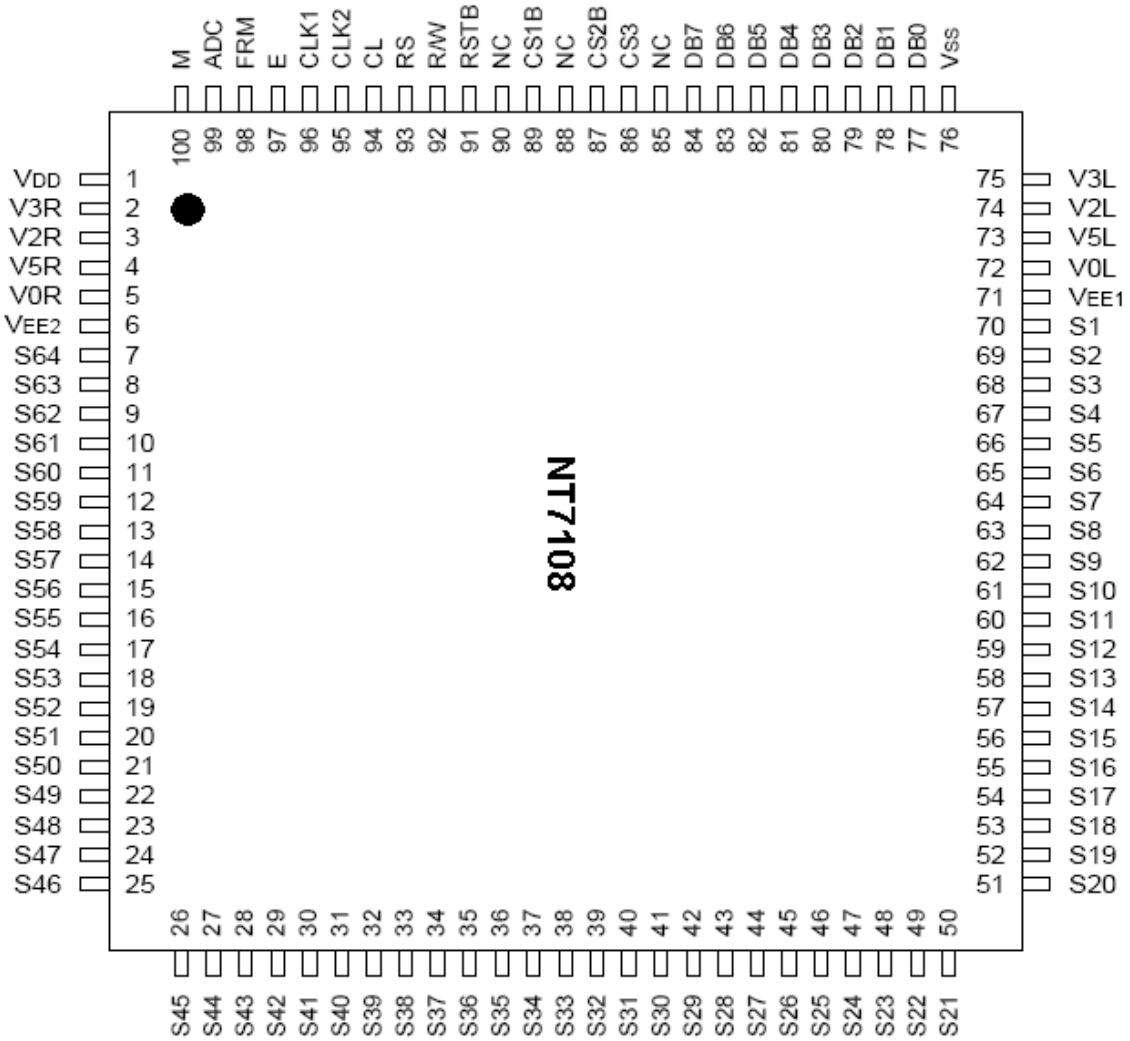
PIN CONFIGURATION

100 PQFP PACKAGE



Appendix

100 PQ PACKAGE



Appendix

PIN DESCRIPTION

Table 1. Pin Description

Pin Number QFP	Symbol	I/O	Description
3 78 73,8	VDD VSS VEE1,2	Power	For internal logic circuit (+2.7~+5.5V) GND (0V) For LCD driver circuit VSS = 0V, VDD = +5V±10%, VDD - VEE = 8V - 17V The same voltage should be connected to VEE1 and VEE2.
74,7 76,5 77,4 75,6	V0L,V0R, V2L,V2R, V3L,V3R, V5L,V5R	Power	Bias supply voltage terminals to drive LCD. Select Level: V0L (R), V5L (R) / Non-Select Level: V2L (R), V3L (R) The same voltage should connect V0L and V0R (V2L & V2R, V3L & V3R, V5L & V5R).
92 91 90	CS1B CS2B CS3	Input	Chip selection In order to interface data for input or output, the terminals have to be CS1B=L, CS2B=L, and CS3=H.
2	M	Input	Alternating signal input for LCD driving.
1	ADC	Input	Address control signal to determine the relation between Y address of display RAM and terminals from which the data is output. ADC=H Y0:S1-Y63:S64 ADC=L Y0:S64-Y63:S1
100	FRM	Input	Synchronous control signal. Presets the 6-bit Z counter and synchronizes the common signal with the frame signal when the frame signal becomes high.
99	E	Input	Enable signal. Write mode (R/W=L) à data of DB<0:7> is latched at the falling edge of E Read mode (R/W=H) à DB<0:7> appears the reading data while E is at high level.
98 97	CLK1 CLK2	Input	2 phase clock signal for internal operation Used to execute operations for input/output of display RAM data and others.
96	CL	Input	Display synchronous signal. Display data is latched at rising time of the CL signal and increments the Z-address counter at the CL falling time.
95	RS	Input	Data or Instruction. RS=H à DB<0:7>:Display RAM data RS=L à DB<0:7>:Instruction data
94	RW	Input	Read or Write. R/W=H à Data appears at DB<0:7> and can be read by the CPU while E=H, CS1B=L, CS2B=L and CS3=H. R/W=L à Display data DB<0:7> can be written at falling of E when CS1B=L, CS2B=L and CS3=H.
79-86	DB0~ DB7	Input/ Output	Data bus. Three state I/O common terminal.

Appendix

<table>
<tr><th>Pin Number
QFP</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>72-9</td><td>S1-S64</td><td>Output</td><td>LCD segment driver output.
Display RAM data 1:On
Display RAM data 0:Off (relation of display RAM data & M)
<table>
<tr><th>M</th><th>Data</th><th>Output Level</th></tr>
<tr><td rowspan="2">L</td><td>L</td><td>V2</td></tr>
<tr><td>H</td><td>V0</td></tr>
<tr><td rowspan="2">H</td><td>L</td><td>V3</td></tr>
<tr><td>H</td><td>V5</td></tr>
</table></td></tr>
<tr><td>93</td><td>RSTB</td><td>Input</td><td>Reset signal.
When RSTB=L,
-ON/OFF register 0 set (display off)
-Display start line register 0 set (display line from 0)
After releasing reset, this condition can be changed only by instruction.</td></tr>
<tr><td>87
88
89</td><td>NC</td><td></td><td>No connection. (Open)</td></tr>
</table>

OPERATING PRINCIPLES AND METHODS

I/O BUFFER

Input buffer controls the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS1B-CS3.

INPUT REGISTER

Input register is provided to interface with MPU, which is different operating frequency. Input register stores the data temporarily before writing it into display RAM. When CS1B to CS3 are in the active mode, R/W and RS select the input register. The data from MPU is written into input register, then into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

OUTPUT REGISTER

Output register stores the data temporarily from display data RAM when CS1B, CS2B and CS3 are in active mode and R/W and RS=H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W=H, RS=L, status data (busy check) can read out. To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data, which is latched. That is, to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

RS	R/W	Function
L	L	Instruction
	H	Status read (busy check)
H	L	Data write (from input register to display data RAM)
	H	Data read (from display data RAM to output register)

RESET

The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU.

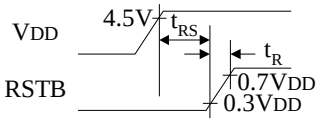
When RSTB becomes low, following procedure is occurred.

- Display off
- Display start line register become set by 0. (Z-address 0)

While RSTB is low, No instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4=0 (clear RSTB) and DB7=0 (ready) by status read instruction. The Conditions of power supply at initial power up are shown in table 2.

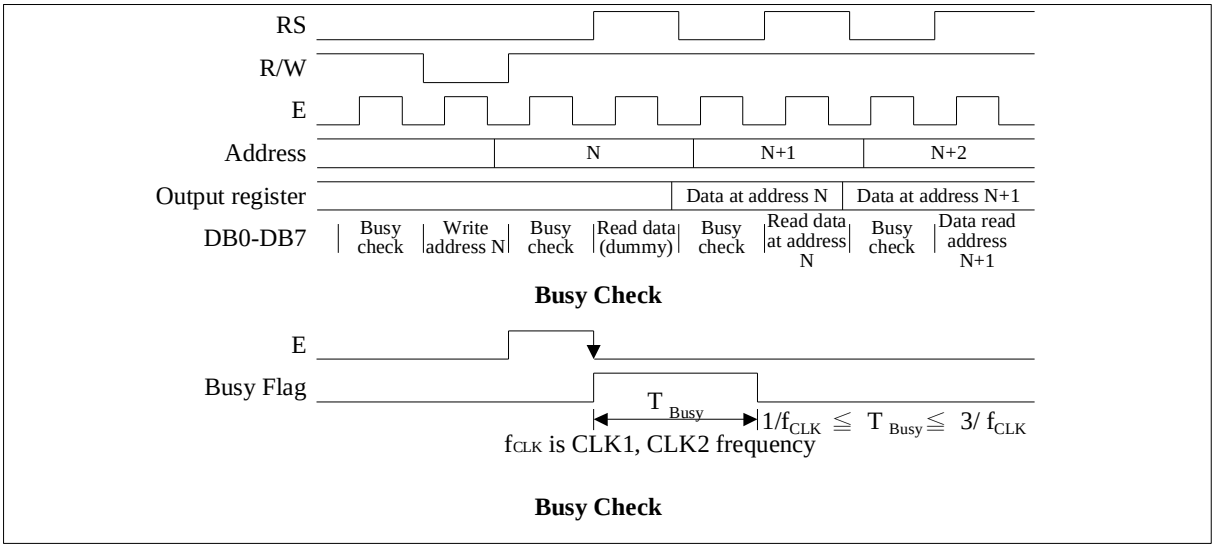
Table 2. Power Supply Initial Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Reset time	tRS	1.0	-	-	μs
Rise time	tR	-	-	200	ns



Busy Flag

Busy Flag indicates the NT7108 is operating or no operating. When busy flag is high, NT7108 is in internal operating. When busy flag is low, NT7108 can accept the data or instruction. DB7 indicates busy flag of the NT7108.



Display ON / OFF Flip-Flop

The display on/off flip-flop makes on/off the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non-selective voltage appears on segment output terminals. When flip-flop is set (logic high), non-selective voltage appears on segment output terminals regardless of display RAM data. The display on/off flip-flop can changes status by instruction. The display data at all segments disappear while RSTB is low. The status of the flip-flop is output to DB5 by status read instruction. The display on/off flip-flop synchronized by CL signal.

X Page Register

X page register designates pages of the internal display data RAM. Count function is not available. An address is set by instruction.

Y Address Counter

An Address is set by instruction and is increased by 1 automatically by R/W operations of display data. The Y address counter loops the values of 0 to 63 to count.

Display Data RAM

Display data RAM stores a display data for liquid crystal display. To indicate on state dot matrix of liquid crystal display, write data 1. The other way, off state, writes 0.

Display data RAM address and segment output can be controlled by ADC signal.

- ADC=H à Y-address 0:S1-Y address 63:S64
- ADC=L à Y-address 0:S64-Y address 63:S1

ADC terminal connects the VDD or Vss.

Display Start Line Register

The display start line register indicates of display data RAM to display top line of liquid crystal display. Bit data (DB<0.5>) of the display start line set instruction is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter. It is used for scrolling of the liquid crystal display screen.

DISPLAY CONTROL INSTRUCTION

The display control instructions control the internal state of the NT7108. Instruction is received from MPU to NT7108 for the display control. The following table shows various instructions.

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Display on/off	L	L	L	L	H	H	H	H	H	L/H	Controls the display on or off. Internal status and display RAM data is not affected. L:OFF, H:ON
Set address (Y address)	L	L	L	H	Y address (0-63)						Sets the Y address in the Y address counter.
Set page (X address)	L	L	H	L	H	H	H	Page (0-7)			Sets the X address at the X address register.
Display Start line (Z address)	L	L	H	H	Display start line (0-63)						Indicates the display data RAM displayed at the top of the screen.
Status read	L	H	Busy	L	On/ Off	Reset	L	L	L	L	Read status. BUSY L: Ready H: In operation ON/OFF L: Display ON H: Display OFF RESET L: Normal H: Reset
Write display data	H	L	Write data								Writes data (DB0: 7) into display data RAM. After writing instruction, Y address is increased by 1 automatically.
Read display data	H	H	Read data								Reads data (DB0: 7) from display data RAM to the data bus.

DISPLAY ON/OFF

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D=0, it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.

SET ADDRESS (Y ADDRESS)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Y address (AC0-AC5) of the display data RAM is set in the Y address counter. An address is set by instruction and increased by 1 automatically by read or write operations of display data.

SET PAGE (X ADDRESS)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	AC2	AC1	AC0

X address (AC0-AC2) of the display data RAM is set in the X address register. Writing or reading to or from MPU is executed in this specified page until the next page is set.

DISPLAY START LINE (Z ADDRESS)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	AC5	AC4	AC3	AC2	AC1	AC0

Z address (AC0-AC5) of the display data RAM is set in the display start line register and displayed at the top of the screen. When the display duty cycle is 1/64 or others (1/32-1/64), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

STATUS READ

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	0	ON/OFF	RESET	0	0	0	0

- BUSY

  When BUSY is 1, the Chip is executing internal operation and no instructions are accepted.

  When BUSY is 0, the Chip is ready to accept any instructions.

- ON/OFF

  When ON/OFF is 1, the display is OFF.

  When ON/OFF is 0, the display is ON.

- RESET

  When RESET is 1, the system is being initialized.

  In this condition, no instructions except status read can be accepted.

  When RESET is 0, initializing has finished and the system is in usual operation condition.

WRITE DISPLAY DATA

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Writes data (D0-D7) into the display data RAM. After writing instruction, Y address is increased by 1automatically.

READ DISPLAY DATA

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Reads data (D0-D7) from the display data RAM. After reading instruction, Y address is increased by 1 automatically.

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit	Note
Operating voltage	VDD	-0.3 to +7.0	V	(1)
Supply voltage	VEE	VDD-19.0 to VDD +0.3		(4)
Driver supply voltage	VB	-0.3 to VDD +0.3		(1),(3)
	VLCD	VEE-0.3 to VDD +0.3		(2)
Operating temperature	TOPR	-30 to +85	℃	
Storage temperature	TSTG	-55 to +125		

NOTES:

1. Based on Vss=0V

2. Applies the same supply voltage to VEE1 and VEE2. VLCD=VDD-VEE.

3. Applies to M, FRM, CL, RSTB, ADC, CLK1, CLK2, CS1B, CS2B, CS3, E, R/W, RS and DB0-DB7.

4. Applies to V0L(R), V2L(R), V3L(R) and V5L(R).

Voltage level: VDD≧V0L=V0R≧V2L=V2R≧V3L=V3R≧V5L=V5R≧VEE.

Appendix

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (VDD=5.0V, Vss=0V, VDD-VEE=8 to 17V, Ta=-30℃ to +85℃)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating Voltage	VDD	-	2.7	-	5.5	V	
Input high Voltage	VIH1	-	0.7VDD	-	VDD		(1)
	VIH2	-	2.0	-	VDD		(2)
Input low Voltage	VIL1	-	0	-	0.3VDD		(1)
	VIL2	-	0	-	0.8		(2)
Output high voltage	VOH	IOH=-200 μA	2.4	-	-		(3)
Output low voltage	VOL	IOL=1.6mA	-	-	0.4		(3)
Input leakage current	ILKG	VIN=VSS-VDD	-1.0	-	1.0	μA	(4)
Three-state(off) input current	ITSL	VIN=VSS-VDD	-5.0	-	5.0		(5)
Driver input leakage current	IDIL	VIN=VEE-VDD	-2.0	-	2.0		(6)
Operating current	IDD1	During display	-	-	100		(7)
	IDD2	During access Access cycle = 1 MHz	-	-	500		(7)
On resistance	RON	VDD-VEE=15V ILOAD= ±0.1mA	-	-	7.5	kΩ	(8)

NOTES:

1. CL, FRM, M RSTB, CLK1, CLK2
2. CS1B, CS2B, CS3, E, R/W, RS, DB0 - DB7
3. DB0 - DB7
4. Except DB0 -DB7
5. DB0 - DB7 at high impedance
6. V0L(R), V2L(R), V3L(R), V5L(R)
7. 1/64 duty, fCLK=250kHz, frame frequency=70HZ, output: no load
8. VDD - VEE =15.5V

V0L(R)>V2L(R)=VDD-2/7(VDD-VEE)>V3L(R)=VEE+2/7(VDD-VEE)>V5L(R)

AC CHARACTERISTICS (VDD=+5V±10%, Vss=0V, Ta=-30℃ to +85℃)

Clock Timing

Characteristic	Symbol	Min	Type	Max	Unit
CLK1, CLK2 cycle time	tCY	2.5	-	20	μs
CLK1 "low" level width	tWL1	625	-	-	ns
CLK2 "low" level width	tWL2	625	-	-	
CLK1 "high" level width	tWH1	1875	-	-	
CLK2 "high" level width	tWH2	1875	-	-	
CLK1-CLK2 phase difference	tD12	625	-	-	
CLK2-CLK1 phase difference	tD21	625	-	-	
CLK1, CLK2 rise time	tR	-	-	150	
CLK1, CLK2 fall time	tF	-	-	150	

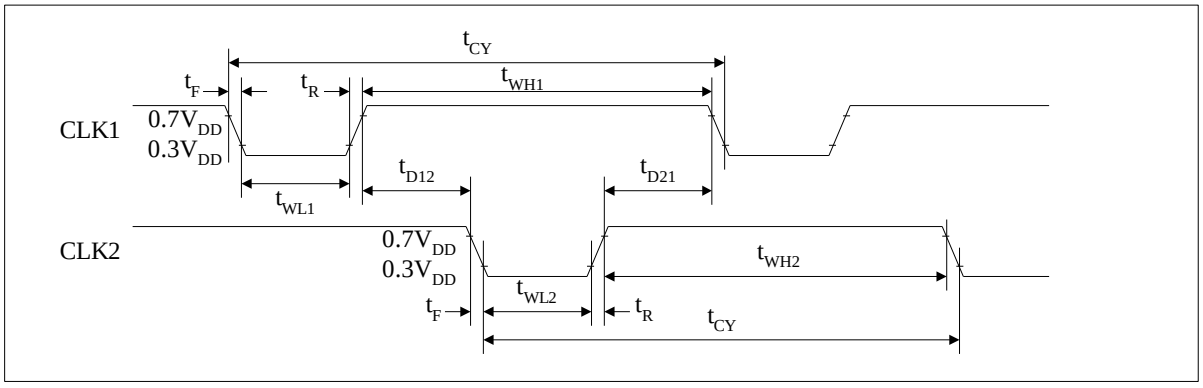


Figure 1. External Clock Waveform

Display Control Timing

Characteristic	Symbol	Min	Type	Max	Unit
FRM delay time	tDF	-2	-	2	μs
M delay time	tDM	-2	-	2	
CL "low" level width	tWL	35	-	-	
CL "high" level width	tWH	35	-	-	

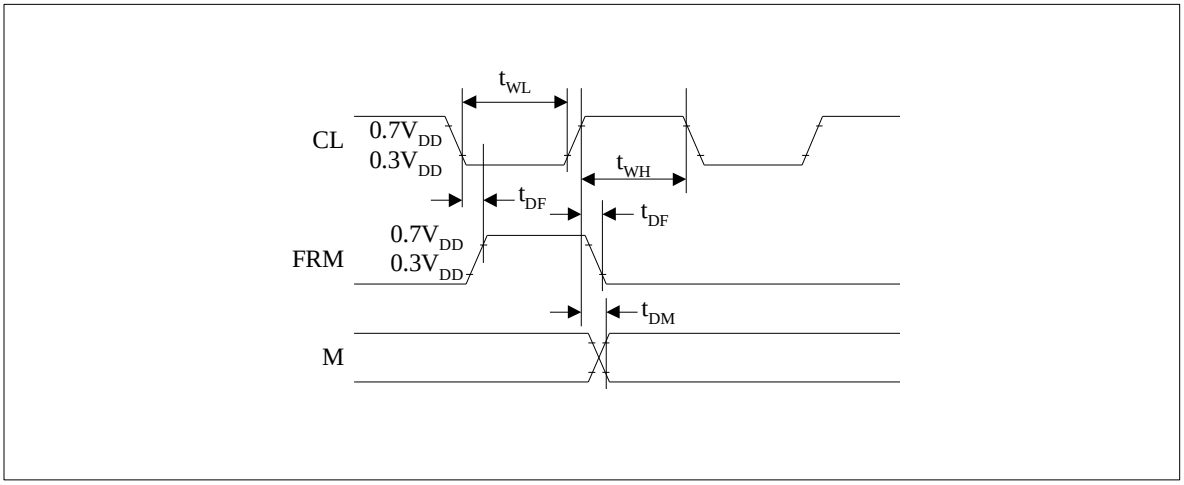


Figure 2. Display Control Waveform

MPU Interface

Characteristic	Symbol	Min	Type	Max	Unit
E cycle	tC	1000	-	-	ns
E high level width	tWH	450	-	-	
E low level width	tWL	450	-	-	
E rise time	tR	-	-	25	
E fall time	tF	-	-	25	
Address set-up time	tASU	140	-	-	
Address hold time	tAH	10	-	-	
Data set-up time	tDSU	200	-	-	
Data delay time	tD	-	-	320	
Data hold time (write)	tDHW	10	-	-	
Data hold time (read)	tDHR	20	-	-	

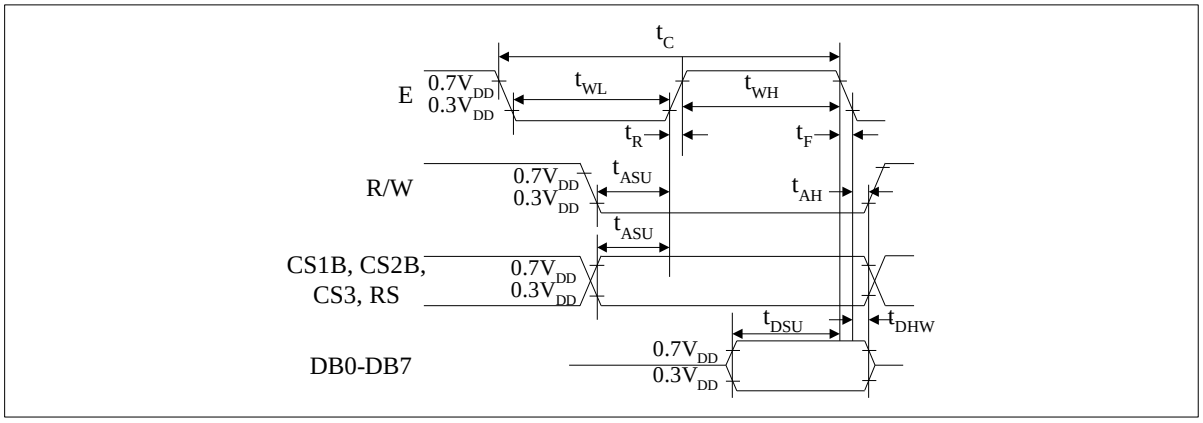


Figure 3. MPU Write Timing

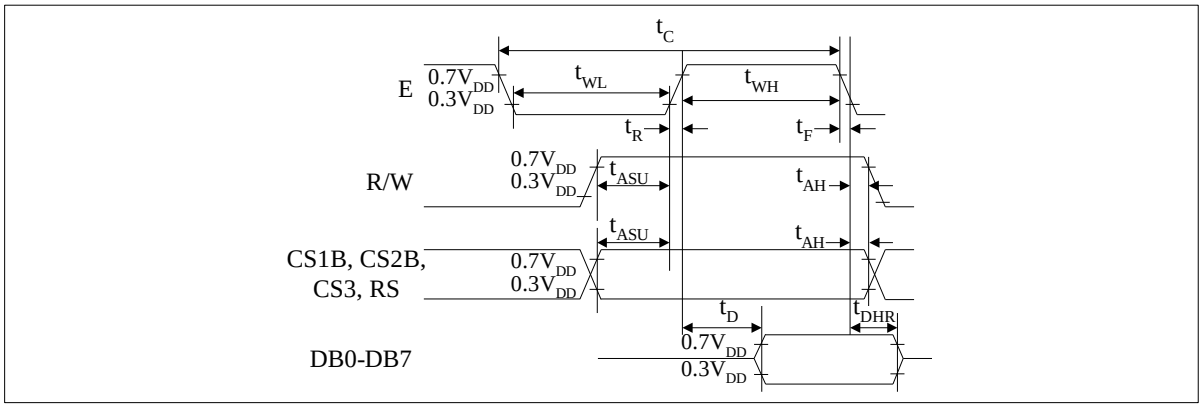
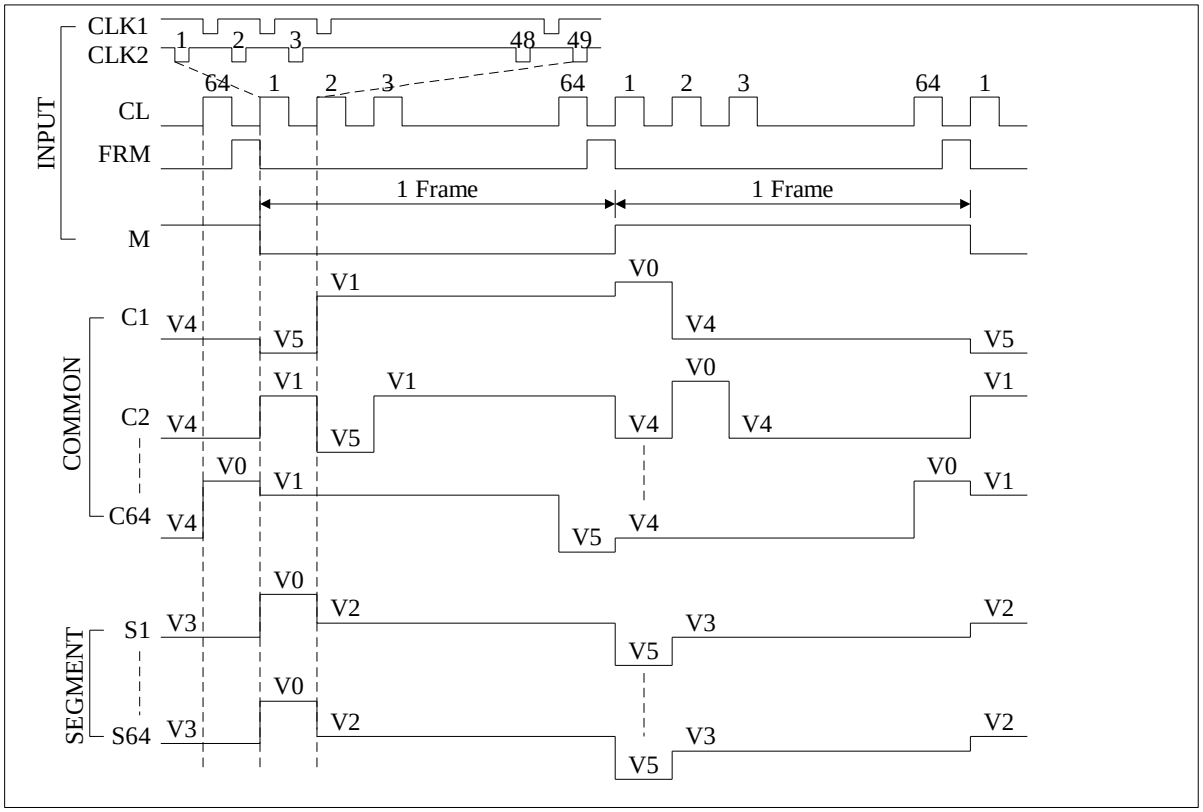


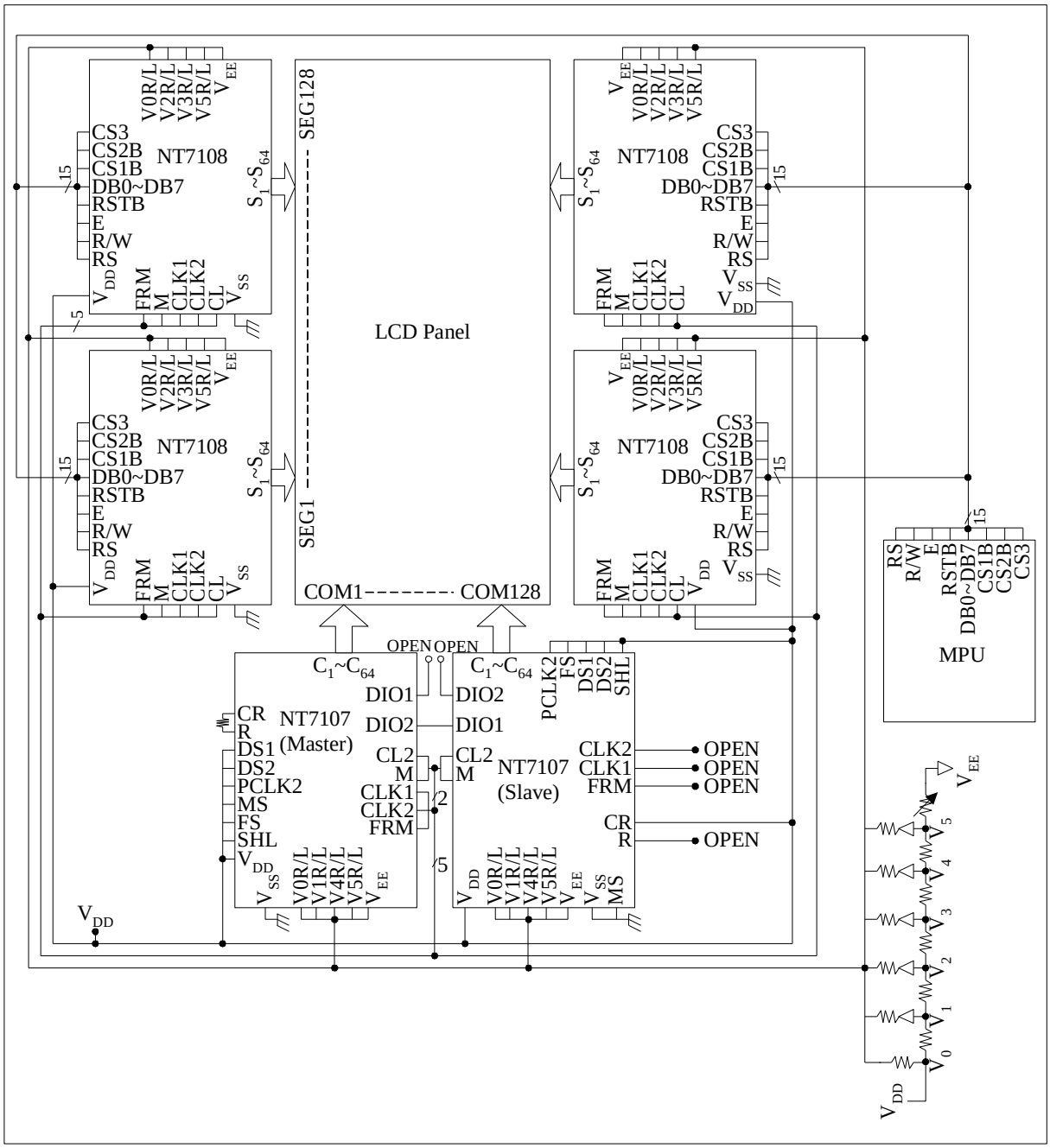
Figure 4. MPU Read Timing

TIMING DIAGRAM (1/64 DUTY)



APPLICATION CIRCUIT

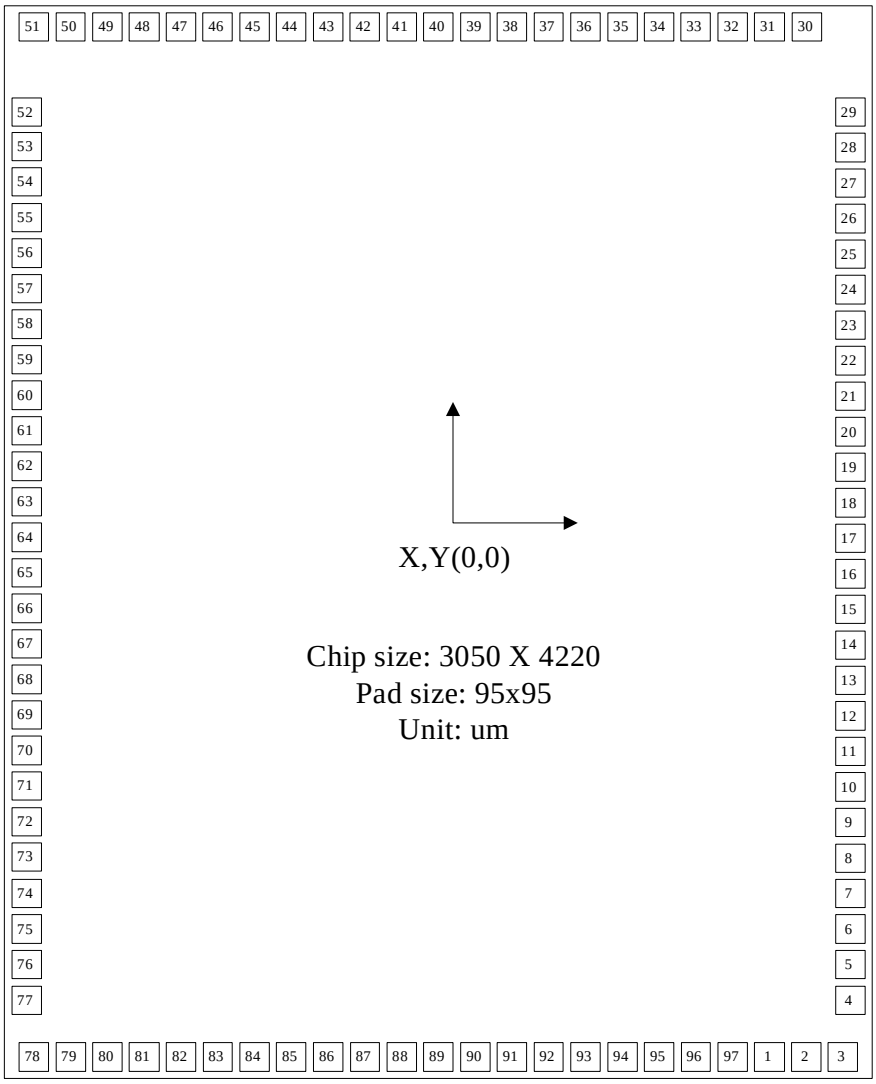
1/128 duty COMMON driver (NT7107) interface circuit



Appendix

PAD DIAGRAM

Note: Please connects the substrate to V_{DD} or floating



PAD DIAGRAM

Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y
1	ADC	1125.000	-1994.198	50	SEG23	-1187.500	1994.200
2	M	1250.000	-1994.198	51	SEG22	-1312.500	1994.200
3	VDD	1375.000	-1994.198	52	SEG21	-1408.098	1399.700
4	V3R	1408.100	-1725.300	53	SEG20		1274.700
5	V2R		-1600.300	54	SEG19		1149.700
6	V5R		-1475.300	55	SEG18		1024.700
7	V0R		-1350.300	56	SEG17		899.700
8	VEE		-1225.300	57	SEG16		774.700
9	SEG64		-1100.300	58	SEG15		649.700
10	SEG63		-975.300	59	SEG14		524.700
11	SEG62		-850.300	60	SEG13		399.700
12	SEG61		-725.300	61	SEG12		274.700
13	SEG60		-600.300	62	SEG11		149.700
14	SEG59		-475.300	63	SEG10		27.700
15	SEG58		-350.300	64	SEG9		-100.300
16	SEG57		-225.300	65	SEG8		-225.300
17	SEG56		-100.300	66	SEG7		-350.300
18	SEG55		24.700	67	SEG6		-475.300
19	SEG54		149.700	68	SEG5		-600.300
20	SEG53		274.700	69	SEG4		-725.300
21	SEG52		399.700	70	SEG3		-850.300
22	SEG51		524.700	71	SEG2		-975.300
23	SEG50		649.700	72	SEG1		-1100.300
24	SEG49		774.700	73	VEE		-1225.300
25	SEG48		899.700	74	V0L		-1350.300
26	SEG47		1024.700	75	V5L		-1475.300
27	SEG46		1124.700	76	V2L		-1600.300
28	SEG45		1274.700	77	V3L		-1725.300
29	SEG44		1399.700	78	GND	-1375.000	-1994.198
30	SEG43	1312.500	1994.200	79	DB0	-1250.000	
31	SEG42	1187.500		80	DB1	-1125.000	
32	SEG41	1062.500		81	DB2	-1000.000	
33	SEG40	937.500		82	DB3	-875.000	
34	SEG39	812.500		83	DB4	-750.000	
35	SEG38	687.500		84	DB5	-625.000	
36	SEG37	562.500		85	DB6	-500.000	
37	SEG36	437.500		86	DB7	-375.000	
38	SEG35	312.500		87	CS3	-250.000	
39	SEG34	187.500		88	CS2B	-125.000	
40	SEG33	62.500		89	CS1B	0.000	
41	SEG32	-62.500		90	RSTB	125.000	
42	SEG31	-187.500		91	R/W	250.000	
43	SEG30	-312.500		92	RS	375.000	
44	SEG29	-437.500		93	CL	500.000	
45	SEG28	-562.500		94	CLK2	625.000	
46	SEG27	-687.500		95	CLK1	750.000	
47	SEG26	-812.500		96	E	875.000	
48	SEG25	-937.500		97	FRM	1000.000	
49	SEG24	-1062.500					

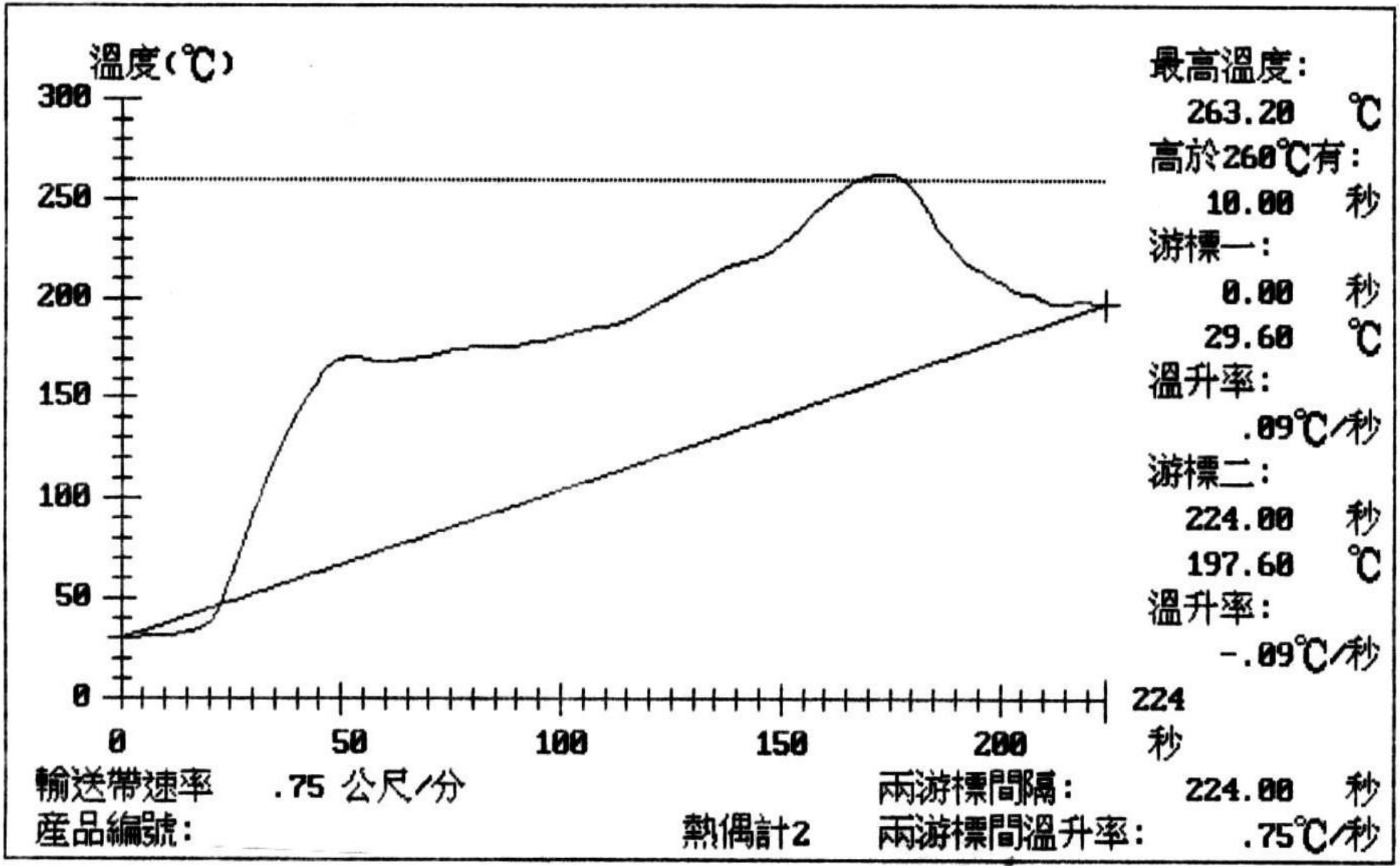
Appendix

VERSION HISTORY

Date	Description
6/5/2002	Add the notice of substrate connection.
12/11/2002	To correct some mistakes at page 5,6,15,19
12/18/2002	To correct some mistakes at page 3,4,7,8,12,16
03/15/2006	Add 100LQFP pin configuration

溫度監控系統V2.52a

新德科技　　無鉛製程　IR Reflow Profile



Crystalfontz America, Incorporated

Crystalfontz Model Number	**CFA10006 Demonstration Board Kits**
Hardware Version	**Revision 1.1, August 2008**
Firmware Version	**Revision 1.0, August 2008**
Data Sheet Version	**Revision 1.0, August 2008**
Product Pages	www.crystalfontz.com/product/CFA10006.html

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REVISION HISTORY

CFA10006 DEMONSTATION BOARD HARDWARE	
2008/08/02	Current demonstration board hardware version: **v1.1** New demonstration board.

CFA10006 DEMONSTRATION BOARD FIRMWARE	
2008/08/02	Current firmware version (series): **v1.0** Initial release.

CFA10006 DEMONSTRATION BOARD KITS USER GUIDE	
2008/08/02	Current Data Sheet version: **v1.0** New Data Sheet.

QUICK START

The CFA10006 demonstration board is shipped with the display of your choice mounted and tested. Simply plug the power supply (included) into an AC outlet. The CFA10006 will initialize the display, turn on the backlight (if the module has a backlight), and run its demonstration program.

INTRODUCTION

The CFA10006 Demonstration Board Kits have everything you need to easily demonstrate and experiment with a Crystalfontz LCD module. The CFA10006 Demonstration Board is compatible with Crystalfontz graphic LCD modules that use a Samsung S6B0107 / S6B0108 controller (formerly KS0107 / KS0108). Samsung's S6B0107 64 CH Common Driver for Dot Matrix LCD and S6B0108 64 CH Common Driver for Dot Matrix LCD specifications are included in a zipped folder that can be downloaded here: www.crystalfontz.com/product/CFA10006.html.

The CFA10006 Demonstration Board can be ordered with the following modules:

CFA10006 DEMONSTRATION KIT	MOUNTED WITH THIS LCD MODULE
DMOG12864ATMI	CFAG12864ATMIVN
DMOG12864AYYHV	CFAG12864AYYHVN
DMOG12864ACFHT	CFAG12864ACFHTA
DMOG12864BTFH	CFAG12864BTFHV
DMOG12864BTMI	CFAG12864BTMIV
DMOG12864BWGHN	CFAG12864BWGHN
DMOG12864BWGH	CFAG12864BWGHV
DMOG12864BYYHN	CFAG12864BYYHN
DMOG12864BYYH	CFAG12864BYYHV
DMOG12864CTMI	CFAG12864CTMITN
DMOG12864CYYH	CFAG12864CYYHTN
DMOG12864EWGH	CFAG12864EWGHTN
DMOG12864ISTI	CFAG12864ISTITN
DMOG12864ITMI	CFAG12864ITMITN
DMOG12864IYYH	CFAG12864IYYHTN

CFA10006 DEMONSTRATION KIT	MOUNTED WITH THIS LCD MODULE
DMOG12864KSTI	CFAG12864KSTITN
DMOG12864KTMI	CFAG12864KTMITN
DMOG12864KYYH	CFAG12864KYYHTN
DMOG12864MTMI	CFAG12864MTMITN
DMOG12864MYYH	CFAG12864MYYHTN
DMOG19264ASTIT	CFAG19264ASTITZ
DMOG19264ATMIT	CFAG19264ATMITZ
DMOG19264AYYH	CFAG19264AYYHTZ
DMOG19264DTFH	CFAG19264DTFHVZ
DMOG19264DTMI	CFAG19264DTMIVZ
DMOG19264DYYH	CFAG19264DYYHVZ

The CFA10006 Demonstration Board Kit may also be used as a reference for your designs that use a Crystalfontz LCD module listed in the table above.

DEMONSTRATION BOARD KIT CONTENTS

- ❑ CFA10006 Demonstration Board
- ❑ Mounted LCD graphics module of your choice. (Selected at time of ordering. See list of choices in table above.)
- ❑ Power adapter (110 VAC).
- ❑ MicroSD memory card, loaded with BASIC demonstration program and bitmap images.
- ❑ USB reader for the microSD memory card.

In addition to the kit contents, a zipped folder of hardware design and program files is available at www.crystalfontz.com/product/CFA10006.html. (Free download.)

HOW TO MAKE A CUSTOM DEMONSTRATION

The CFA10006 is programmed with firmware that will read a BASIC program file from the microSD memory card. The BASIC program can read bitmap image files from the microSD memory card and display them on the LCD module. The BASIC program can also read the four buttons, change the backlight settings, and change the contrast settings.
By using the USB reader, a text editor, and a graphic conversion utility (which we supply), you can customize the demonstration to include your own bitmap images. The large capacity of the microSD card allows you to create complex demonstrations.

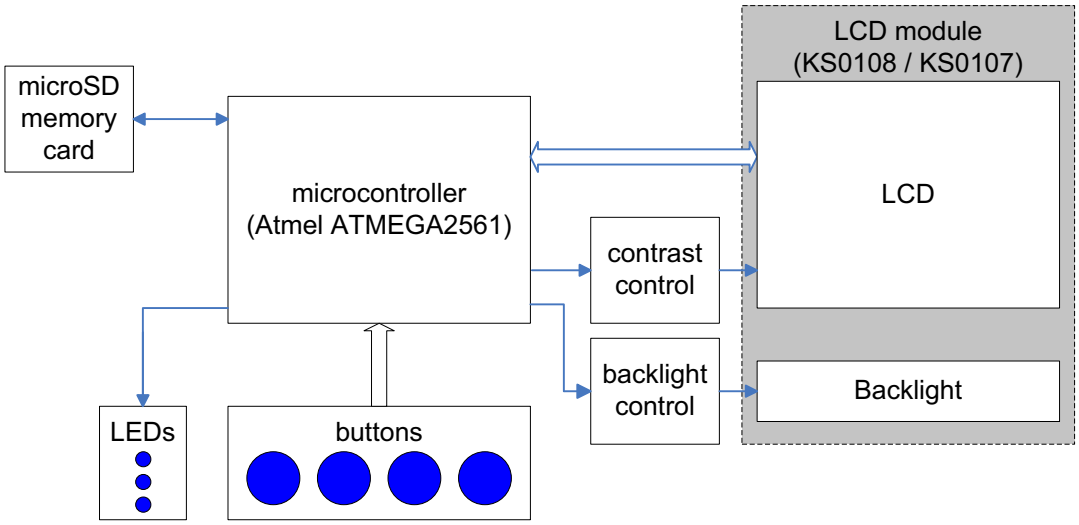
For the most recent version of the graphic conversion utility, sample scripts, and sample images for customizing the

demonstration, download the zipped folder at www.crystalfontz.com/product/CFA10006.html.

Acknowledgement Note: The miniBASIC-AVR is a derivative of this (see www.ericengler.com/Minibasic.aspx), which is a derivative of this (see www.personal.leeds.ac.uk/~bgy1mm/Minibasic/MiniBasicHome.html). The miniBASIC-AVR also includes the EFSL embedded file systems library (see http://efsl.be/ and the Graphic Library for KS0108- (and compatible) based LCDs by Fabian Maximilian Thiele.

HARDWARE DESIGN INFORMATION

Here is a block diagram of the CFA10006 Demonstration Board:



The zipped folder at www.crystalfontz.com/product/CFA10006.html includes the complete hardware design of the CFA10006 Demonstration Board.

- Schematic.
- PCB layout.
- BOM (Bill Of Materials) as an XLS spreadsheet.
- “Super simple” LCD initialization code and bitmap display code.

The schematic and PCB layout were created with CadSoft EAGLE. EAGLE is a capable and low-cost electrical CAD system. You can download EAGLE from http://www.cadsoft.de/ (at no cost for evaluation purposes) to view the schematic and layout files.

CARE AND HANDLING PRECAUTIONS

The kit is sold with a module mounted on it. If you attempt to modify the board to work with other modules, the warranty is void. For optimum operation of the module and demonstration board and to prolong their life, please follow the precautions below.

ESD (ELECTRO-STATIC DISCHARGE)

The circuitry is industry standard CMOS logic and susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other PCB such as expansion cards or motherboards.

AVOID SHOCK, IMPACT, TORQUE, AND TENSION

- Do not expose the module to strong mechanical shock, impact, torque, and tension.
- Do not drop, toss, bend, or twist the module.
- Do not place weight or pressure on the module.

LCD MODULE GLASS

- The exposed surface of the LCD "glass" is actually a polarizer laminated on top of the glass.To protect the soft plastic polarizer from damage, the module ships with a protective film over the polarizer. Please peel off the protective film slowly. Peeling off the protective film abruptly may generate static electricity.
- The polarizer is made out of soft plastic and is easily scratched or damaged. When handling the module, avoid touching the polarizer. Finger oils are difficult to remove.
- If the LCD panel breaks, be careful not to get the liquid crystal fluid in your mouth or eyes. If the liquid crystal fluid touches your skin, clothes, or work surface, wash it off immediately using soap and plenty of water.
- Be very careful when you clean the polarizer. Do not clean the polarizer with liquids. Do not wipe the polarizer with any type of cloth or swab (for example, Q-tips). Use the removable protective film to remove smudges (for example, fingerprints) and any foreign matter. If you no longer have the protective film, use standard transparent office tape (for example, Scotch® brand "CrystalClear Tape"). If the polarizer is dusty, you may carefully blow it off with clean, dry, oil-free compressed air.

OPERATION

- Use only the included AC adapter to power the board.
- Observe the operating temperature limitations: from -20°C minimum to +70°C maximum with minimal fluctuations. Operation outside of these limits may shorten the life and/or harm the display.
  - At lower temperatures of this range, response time is delayed.
  - At higher temperatures of this range, display becomes dark. (You may need to adjust the contrast.)
- Operate away from dust, moisture, and direct sunlight.

STORAGE AND RECYCLING

- Store in an ESD-approved container away from dust, moisture, and direct sunlight.
- Observe the storage temperature limitations: from -30°C minimum to +80°C maximum with minimal fluctuations. Rapid temperature changes can cause moisture to form, resulting in permanent damage.
- Do not allow weight to be placed on the modules while they are in storage.
- Please recycle your outdated Crystalfontz LCD modules at an approved facility.