AN11318

How to implement the PMBus software stack

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Document information

Info	Content
Keywords	PMBus, I2C, SMBus
Abstract	This app note will explain how to implement the PMBus using the LPC microcontroller

Revision history

Rev	Date	Description
1	20130125	Initial version.

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1. Introduction

The Power Management Bus (PMBus) is an open standard protocol used for communication with power conversion and other devices. The PMBus is a superset of the System Management Bus (SMBus). The SMBus is based on the operating principles of the I^{2}C-bus.

The I2C engine found on the LPC11xx, LPC11Axx, LPC13xx, LPC17xx, LPC18xx, and LPC43xx operate in the same manner. The sample software presented in this application note is targeted for the LPC1343, but it can easily be ported to the other microcontrollers.

2. Comparing PMBus, SMBus, and I2C

The SMBus timing parameter is based on the I2C Standard Mode and the PMBus is based on the I2C Fast Mode specification. The major differences between the SMBus and the I^{2}C-bus are highlighted in Table 1.

Table 1. SMBus vs. I2C Standard Mode timing parameters

Symbol	Parameter	SMBus		I2C Standard Mode		Units
		Min	Max	Min	Max	
F_{scl}	Operation frequency	10	100	0	100	kHz
THD:DAT	Data hold time	300	-	0	-	ns
T_{high}	Clock high period	4	50	4	-	µs
I_{OL}	V_{OL} @ 0.4 V	4	-	3	-	mA

The SMBus has two power operating modes: low-power and high-power. In the low-power mode, the IOL is limited from 100 uA to 350 uA. In the high-power mode, the IOL must be able to sink a minimum of 4 mA. For the SMBus to operate on an I^{2}C-bus, the high-power mode must be used.

The major differences between the PMBus and the I^{2}C-bus are highlighted in Table 2.

Table 2. PMBus vs. I2C Fast Mode timing parameters

Symbol	Parameter	PMBus		I2C Fast Mode		Units
		Min	Max	Min	Max	
F_{scl}	Operation frequency	10	400	0	400	kHz
THD:DAT	Data hold time	300	-	0	-	ns
T_{high}	Clock high period	0.6	50	0.6	-	µs

PMBus has a maximum bus speed of 400 kHz while the SMBus has a maximum bus speed of 100 kHz. The PMBus specifies a minimum bus speed of 10 kHz while the I^{2}C-bus does not have a minimum bus speed.

2.1 PMBus Group Command Protocol

The PMBus devices must support the Group Command Protocol. The Group Command Protocol is used to send commands to multiple PMBus devices in one continuous transmission. In a PMBus Group Command Protocol transmission, the master issues a START condition, and then addresses the first slave device. The session to the slave device is not terminated with a STOP condition, but a Repeated START condition is issued and the second slave device is addressed. When all the slave devices have been addressed, a STOP condition is issued. Upon receiving the STOP condition, all slave devices execute its respective command simultaneously. The data format is shown in Fig 1.

The Group Command Protocol can only issue commands which do not require the slave to return any data. For each slave addressed, only one command can be issued.

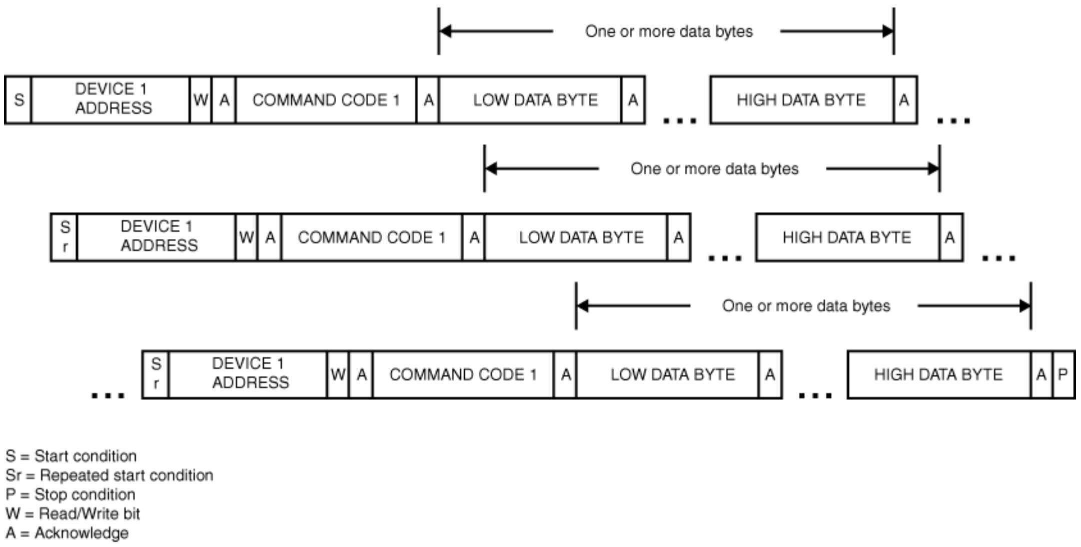

Fig 1. Group Command Protocol

The LPC microcontrollers' I2C engine does not differentiate between a STOP and Repeated Start condition. In the I2C engine, the STOP and Repeated Start condition share the same status code of 0xA0. In this instance, when the Group Command Protocol is issued, the I2C will start execution of the command it received when either a Repeated Start or STOP condition is received.

2.2 Hardware work around to support Group Command Protocol

To allow the LPC microcontrollers to differentiate between a STOP and Repeated Start condition, a hardware workaround can be implemented using a D-Type flip-flop. The schematic for the workaround is shown in Fig 2. The SDA and SCL lines are tied to the CLK and CLR of the D-Type flip-flop, respectively. The Q output is tied to an external interrupt of the LPC GPIO pin.

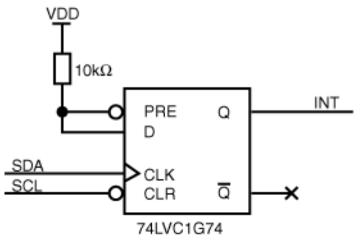

Fig 2. STOP condition detector

The truth table for the D-Type flip-flop, shown in Table 3, is used to illustrate how the STOP condition can be detected. Note that since the PRE and D inputs are both tied high, only three states (2, 4 and 6) will be valid in this configuration, however, state 6 does not cause a change of state in the output, so this can be eliminated.

On a Start condition, the SDA signal is pulled low, followed by a falling edge on the SCL signal. With the SCL signal tied to the CLR line, this causes state 2 to be valid and Q to transition to LOW. After the Start condition, the SCL and SDA lines are both toggling when the address and data are being sent, however, the SDA signal only changes state while the SCL signal is low, which keeps the D-Type flip-flop in state 2 throughout the I2C transmission, even during a Restart condition. However, on a STOP condition, state 4 will occur because SCL is high and SDA will transition to a high state. This will allow Q to transition to HIGH. This low-to-high transition will be used as a STOP condition indicator to the external interrupt pin on the LPC.

Table 3. D-type flip-flop truth table

State	Inputs				Outputs	
	Pre (HIGH)	CLR (SCL)	CLK (SDA)	D (HIGH)	Q (INT)	$\overline{Q}$
1	L	H	X	X	H	L
2	**H**	L	X	**X**	L	H
3	L	L	X	X	H	H
4	**H**	H	↑	**H**	H	L
5	H	H	↑	L	L	H
6	**H**	H	L	**X**	Q_0	$\overline{Q_0}$

The corresponding waveform is shown in Fig 3. For this example, two slave devices are addressed, with a Repeated Start issued between each slave address. The STOP label is the Q output from the D-Type flip-flop.

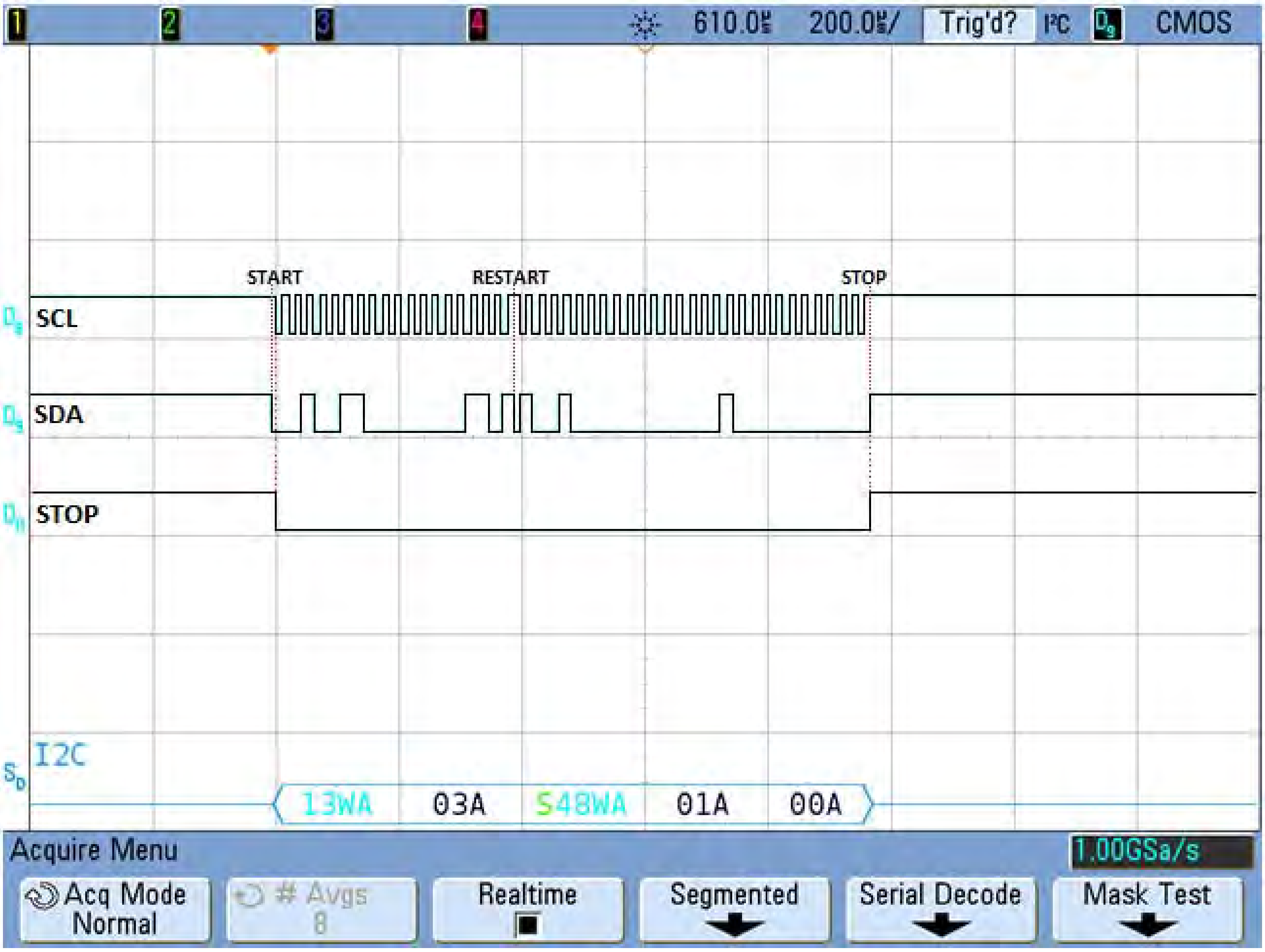

Fig 3. STOP condition detection using D-Type flip flop

2.2.1 Software workaround to support Group Command Protocol

A GPIO pin is configured as an external interrupt pin to accept the Q signal from the D-Type flip-flop. The GPIO is set to trip when a low-to-high transition occurs. The sample code accompanying this application note uses PIO0_7 on the LPC1343 as the external interrupt pin.

To prevent the GPIO ISR from always triggering, the GPIO interrupt is enabled only when its I2C address match is detected. Thus the GPIO interrupt is enabled within the I2C ISR routine.

When a STOP condition is detected, the GPIO ISR will be used to determine if the command received requires returning data. If the command does not require returning data, the detected STOP condition will be set in a status flag indicating this command is part of the Group Command Protocol.

The I2C interrupt has a lower priority than the GPIO interrupt, thus it is necessary to change the interrupt's priority to ensure the GPIO interrupt has a higher precedent than the I2C interrupt.

```
        NVIC_SetPriority(I2C_IRQn, 0);
        NVIC_SetPriority(EINT0_IRQn, 4);
```

3. PMBus software stack

The software code accompanying this application note demonstrates how the LPC microcontroller can be used to implement a PMBus compliant code.

Upon power-up, the device must initialize certain peripheral blocks:

- Configure the I2C to slave mode
- Setup the GPIO pin as an external interrupt
- Setup timer for system up time

3.1 Main loop

The main loop is used to handle commands that do not require the returning of data and updating the system up time. The main loop will determine if a command is available to be processed by checking the status flags I2C_MSG and I2C_STOP.

The timer is set for a 10 ms interval. The up time value is updated every second.

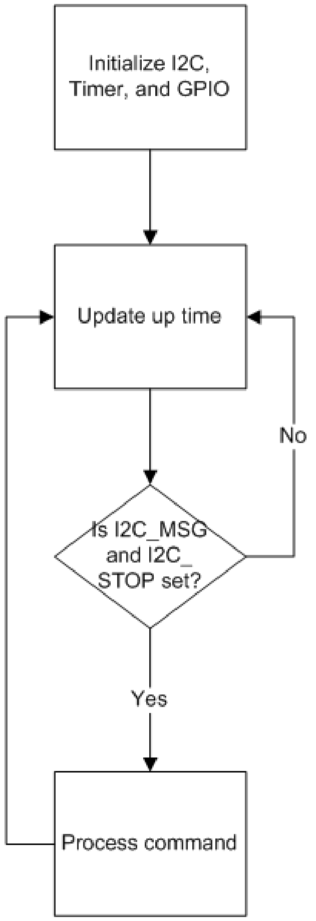
Initialize I2C, Timer, and GPIO
Update up time
No
Is I2C_MSG and I2C_ STOP set?
Yes
Process command

Fig 4. Main loop flow diagram

3.2 I2C ISR

The I2C ISR, in addition to handling the I2C interrupts, is also used to process commands which require returning data bytes. On a slave address match, the GPIO interrupt is enabled.

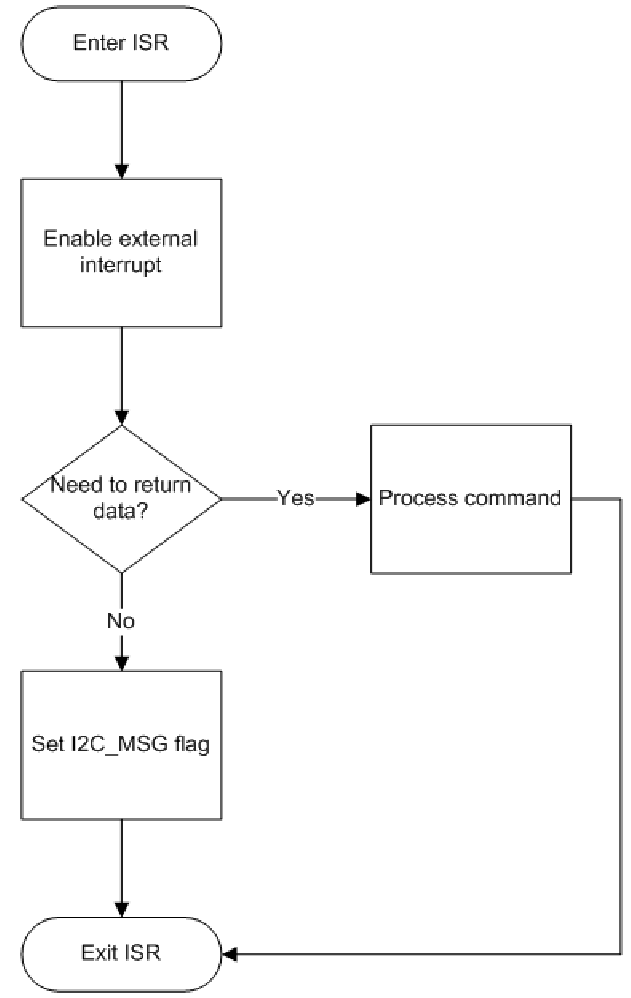

Fig 5. I2C ISR flow diagram

3.3 GPIO ISR

The GPIO ISR is entered when a STOP condition is detected. If the I2C_MSG flag is set, indicating this is part of the Group Command Protocol, the I2C_STOP flag gets set.

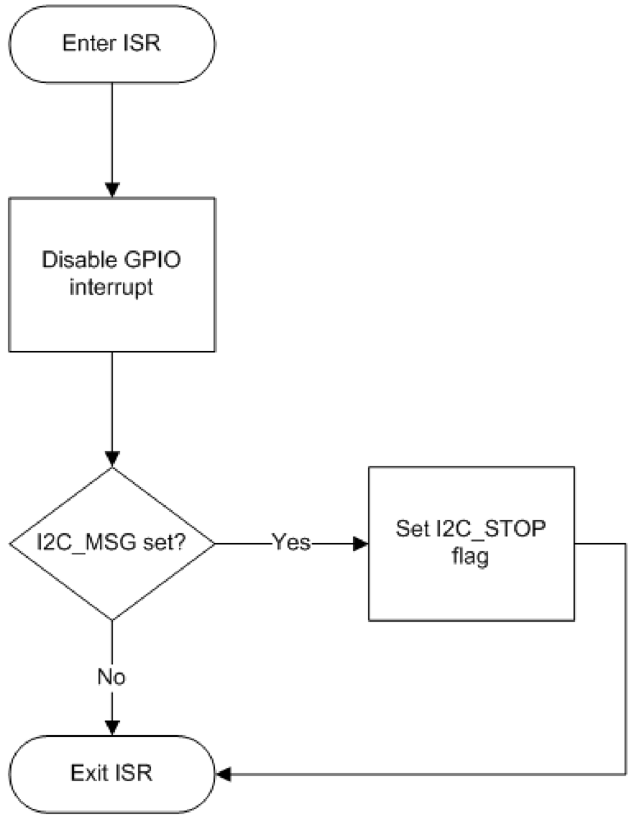

Fig 6. GPIO ISR flow diagram

3.4 CRC checking

The CRC checking is accomplished by a look-up table with pre-calculated CRC values. The CRC values are calculated using the polynomial x^8 + x^2 + x^1 + x^0.

4. Portability of code

The sample code was written for the LPC1343, but it can easily be ported to other LPC microcontrollers. The code portions that need to be modified are as follows:

- Change the timer interval (if the system clock speed is different)
- Change I2C port pins
- Change GPIO port pin

4.1 Timer value

The timer is a counting mechanism dependent on the peripheral clock. The sample code is set to count to 10 ms. On each 10 ms interval, a counter is incremented. Once the counter reaches 100, indicating a second has passed, the up time is updated. The ported code should configure the timer to count to 10 ms.

Alternatively, the systick timer can be used in place of a timer.

4.2 I2C pins

The PMBus requires that the I2C pins be in a high impedance state when the device is unpowered, during startup until fully powered, and during shutdown once the device can no longer assure the proper signal levels. Thus the I2C pins selected must be true open-drain pins.

4.3 GPIO pins

The sample code uses PIO0_7 of the LPC1343 as an external interrupt pin. The targeted LPC should configure a GPIO pin to detect a low-to-high transition.

5. Summary

The LPC microcontroller can be made compliant to the PMBus standard with the addition of a single D-Type flip-flop and using one GPIO pin with interrupt capability. The accompanying sample software can be used as a base to create a PMBus software stack on any LPC microcontroller, with minimal changes.

6. References

[1] SMBus specification, version 2.0 – http://www.smbus.org/specs/

[2] PMBus specification, version 1.2 – http://www.pmbus.org/specs.html

[3] I^{2}C-bus specification, version 2.1 – http://www.nxp.com/documents/other/39340011.pdf

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