
| Tool Version : Vivado v.2023.1 (win64) Build 3865809 Sun May 7 15:05:29 MDT 2023

| Date : Sun Oct 29 23:40:31 2023

| Host : LAPTOP-9LEGU41K running 64-bit major release (build 9200)

| Command : report_power -file counterNoOptimization_power_routed_1.rpt -pb counterNoOptimization_power_summary_routed_1.pb -rpx counterNoOptimization_power_routed_1.rpx

| Design : counterNoOptimization

| Device : xa7a12tcpg238-2I

| Design State : routed

| Grade : industrial

| Process : typical

| Characterization : Production

Power Report

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1. Summary

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| Total On-Chip Power (W) | 3.735 |

| Design Power Budget (W) | Unspecified* |

| Power Budget Margin (W) | NA |

| Dynamic (W) | 3.668 |

| Device Static (W) | 0.067 |

| Effective TJA (C/W) | 6.2 |

| Max Ambient (C) | 76.9 |

| Junction Temperature (C) | 48.1 |

| Confidence Level | Low |

| Setting File | --- |

| Simulation Activity File | --- |

| Design Nets Matched | NA |

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* Specify Design Power Budget using, set_operating_conditions -design_power_budget <value in Watts>

1.1 On-Chip Components

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| On-Chip | Power (W) | Used | Available | Utilization (%) |

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| Slice Logic | 0.044 | 10 | --- | --- |

| LUT as Logic | 0.034 | 2 | 8000 | 0.03 |

| BUFG | 0.006 | 1 | 32 | 3.13 |

| Register | 0.004 | 4 | 16000 | 0.03 |

| Others | 0.000 | 1 | --- | --- |

| Signals | 0.058 | 7 | --- | --- |

| I/O | 3.566 | 6 | 112 | 5.36 |

| Static Power | 0.067 | | | |

| Total | 3.735 | | | |

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1.2 Power Supply Summary

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| Source | Voltage (V) | Total (A) | Dynamic (A) | Static (A) | Powerup (A) | Budget (A) | Margin (A) |

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| Vccint | 1.000 | 0.117 | 0.106 | 0.011 | NA | Unspecified | NA |

| Vccaux | 1.800 | 0.302 | 0.292 | 0.010 | NA | Unspecified | NA |

| Vcco33 | 3.300 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vcco25 | 2.500 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vcco18 | 1.800 | 1.688 | 1.688 | 0.001 | NA | Unspecified | NA |

| Vcco15 | 1.500 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vcco135 | 1.350 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vcco12 | 1.200 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vccaux_io | 1.800 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vccbram | 1.000 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| MGTAVcc | 1.000 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| MGTAVtt | 1.200 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vccadc | 1.800 | 0.020 | 0.000 | 0.020 | NA | Unspecified | NA |

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1.3 Confidence Level

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| User Input Data | Confidence | Details | Action |
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Design implementation state	High	Design is routed	
Clock nodes activity	Low	User specified less than 75% of clocks	Provide missing clock activity with a constraint file, simulation results or by editing the "By Clock Domain" view
I/O nodes activity	Low	More than 75% of inputs are missing user specification	Provide missing input activity with simulation results or by editing the "By Resource Type -> I/Os" view
Internal nodes activity	Medium	User specified less than 25% of internal nodes	Provide missing internal nodes activity with simulation results or by editing the "By Resource Type" views
Device models	High	Device models are Production	

| | | |
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| Overall confidence level | Low | |
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2. Settings

2.1 Environment

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| Ambient Temp (C) | 25.0 |

| ThetaJA (C/W) | 6.2 |

| Airflow (LFM) | 250 |

| Heat Sink | medium (Medium Profile) |

| ThetaSA (C/W) | 4.6 |

| Board Selection | medium (10"x10") |

| # of Board Layers | 12to15 (12 to 15 Layers) |

| Board Temperature (C) | 25.0 |

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2.2 Clock Constraints

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| Clock | Domain | Constraint (ns) |

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3. Detailed Reports

3.1 By Hierarchy

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| Name | Power (W) |

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| counterNoOptimization | 3.668 |

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