
| Tool Version : Vivado v.2023.1 (win64) Build 3865809 Sun May 7 15:05:29 MDT 2023

| Date : Sun Oct 29 22:58:30 2023

| Host : LAPTOP-9LEGU41K running 64-bit major release (build 9200)

| Command : report_power -file CounterWithPowerGating_power_routed.rpt -pb CounterWithPowerGating_power_summary_routed.pb -rpx CounterWithPowerGating_power_routed.rpx

| Design : CounterWithPowerGating

| Device : xa7a12tcpg238-2I

| Design State : routed

| Grade : industrial

| Process : typical

| Characterization : Production

Power Report

Table of Contents

2.2 Clock Constraints

3. Detailed Reports

3.1 By Hierarchy

1. Summary

+-------------------------+--------------+

| Total On-Chip Power (W) | 0.960 |

| Design Power Budget (W) | Unspecified* |

| Power Budget Margin (W) | NA |

| Dynamic (W) | 0.899 |

| Device Static (W) | 0.061 |

| Effective TJA (C/W) | 6.2 |

| Max Ambient (C) | 94.1 |

| Junction Temperature (C) | 30.9 |

| Confidence Level | Low |

| Setting File | --- |

| Simulation Activity File | --- |

| Design Nets Matched | NA |

+-------------------------+--------------+

* Specify Design Power Budget using, set_operating_conditions -design_power_budget <value in Watts>

1.1 On-Chip Components

+----------------+-----------+----------+-----------+-----------------+

| On-Chip | Power (W) | Used | Available | Utilization (%) |

+----------------+-----------+----------+-----------+-----------------+

| Slice Logic | 0.017 | 10 | --- | --- |

| LUT as Logic | 0.010 | 3 | 8000 | 0.04 |

| BUFG | 0.006 | 1 | 32 | 3.13 |

| Register | 0.001 | 4 | 16000 | 0.03 |

| Signals | 0.023 | 10 | --- | --- |

| I/O | 0.859 | 8 | 112 | 7.14 |

| Static Power | 0.061 | | | |

| Total | 0.960 | | | |

+----------------+-----------+----------+-----------+-----------------+

1.2 Power Supply Summary

+-----------+-------------+-----------+-------------+------------+-------------+-------------+------------+

| Source | Voltage (V) | Total (A) | Dynamic (A) | Static (A) | Powerup (A) | Budget (A) | Margin (A) |

+-----------+-------------+-----------+-------------+------------+-------------+-------------+------------+

| Vccint | 1.000 | 0.058 | 0.052 | 0.006 | NA | Unspecified | NA |

| Vccaux | 1.800 | 0.079 | 0.069 | 0.010 | NA | Unspecified | NA |

| Vcco33 | 3.300 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vcco25 | 2.500 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vcco18 | 1.800 | 0.402 | 0.401 | 0.001 | NA | Unspecified | NA |

| Vcco15 | 1.500 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vcco135 | 1.350 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vcco12 | 1.200 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vccaux_io | 1.800 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vccbram | 1.000 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| MGTAVcc | 1.000 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| MGTAVtt | 1.200 | 0.000 | 0.000 | 0.000 | NA | Unspecified | NA |

| Vccadc | 1.800 | 0.020 | 0.000 | 0.020 | NA | Unspecified | NA |

+----------+----------+----------+----------+----------+----------+----------+----------+

1.3 Confidence Level

+----------+----------+----------+----------+
| User Input Data | Confidence | Details | Action |
+----------+----------+----------+----------+
Design implementation state	High	Design is routed	
Clock nodes activity	Low	User specified less than 75% of clocks	Provide missing clock activity with a constraint file, simulation results or by editing the "By Clock Domain" view
I/O nodes activity	Low	More than 75% of inputs are missing user specification	Provide missing input activity with simulation results or by editing the "By Resource Type -> I/Os" view
Internal nodes activity	Medium	User specified less than 25% of internal nodes	Provide missing internal nodes activity with simulation results or by editing the "By Resource Type" views
Device models	High	Device models are Production	

| | | |
|

| Overall confidence level | Low | |
|

+---------------------------+-----------+---+----------------------------
---+

2. Settings

2.1 Environment

+----------------------+-------------------------+

| Ambient Temp (C) | 25.0 |

| ThetaJA (C/W) | 6.2 |

| Airflow (LFM) | 250 |

| Heat Sink | medium (Medium Profile) |

| ThetaSA (C/W) | 4.6 |

| Board Selection | medium (10"x10") |

| # of Board Layers | 12to15 (12 to 15 Layers) |

| Board Temperature (C) | 25.0 |

+----------------------+-------------------------+

2.2 Clock Constraints

+-------+--------+-----------------+

| Clock | Domain | Constraint (ns) |

+-------+--------+-----------------+

3. Detailed Reports

3.1 By Hierarchy

+------------------------+-----------+

| Name | Power (W) |

+------------------------+-----------+

| CounterWithPowerGating | 0.899 |

+------------------------+-----------+