169202, ALLGER MIGIDE SYMLES.

ICS 3111: MICROPROCESSOR ASSIGNMENT II ANSWERS.

1) Design and explain a microprocessor-based solution using the 8255 Programmable Peripheral Interface (PPI) in BSR mode to alternately set and reset pins PC7 and PC0 with a 1-second interval, maintaining this pattern for approximately five seconds. Your response should include:

a. The rationale for selecting BSR mode for this task.

The BSR (Bit Set/Reset) mode of the 8255 PPI is used to individually control the bits of Port C, without affecting other bits or needing full port configurations. It is useful since we only need to manipulate PC7 and PC0 individually. It simplifies control logic when only specific bits are involved.

b. A breakdown of the control word(s) required to manipulate the specified pins.

D7	D6	D5	D4	D3	D2	D1	D0
0	x	x	x	B2	B1	B0	S/R

D7=0: BSR mode identifier

D3-D1 (Bit select): Binary code for the target pin (PC0=000, PC7=111)

D0 (S/R): Set (1) or Reset (0)

The required control words are;

Set PC7: 0000 1111 = 0Fh

(D7=0, Bits=111 for PC7, S/R=1)

Reset PC7: 0000 1110 = 0Eh

(D7=0, Bits=111, S/R=0)

Set PC0: 0000 0001 = 01h

(D7=0, Bits=000 for PC0, S/R=1)

Reset PC0: 0000 0000 = 00h

(D7=0, Bits=000, S/R=0)

c. A complete program (in assembly) that implements this behavior, with appropriate timing considerations.

```
ORG 0000H
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```
MVI B, 05H
LOOP:
MVI A, 0Fh
OUT 83H
MVI A, 00h
OUT 83H
CALL DELAY_1S
MVI A, 0Eh
OUT 83H
MVI A, 01h
OUT 83H
CALL DELAY_1S
DCR B
JNZ LOOP
HLT
DELAY_1S:
  MVI D, 0FFH
DELAY_LOOP1:
  MVI E, 0FFH
DELAY_LOOP2:
  NOP
  NOP
  DCR E
  JNZ DELAY_LOOP2
  DCR D
  JNZ DELAY_LOOP1
```

RET

END

d. A brief analysis of how the program ensures timing accuracy and correct pin behavior.
10mks
For timing accuracy, the 1-second delay is implemented using nested loops with a known clock speed. This ensures approximate timing is achieved in the program. For the pin behaviour, PC7 and PC0 are alternately set/reset in 1-second intervals for 5 seconds , which is done by the nested loops. Since its BSR mode, no other pins are affected by the toggling hence ensuring perfect isolation of the pins.

2) Given that ports A and B of the 8255 PPI are configured as input ports in Mode 1, analyze the role and behavior of the control signals involved in the strobed input process.
In your response:
a. Explain how the control signals (STB, IBF, INTR,INTE) facilitate data transfer from peripheral devices to the microprocessor.

STB (Strobe Input) -Generated by the peripheral to indicate valid data is available on Port A or B. It's an active low signal.

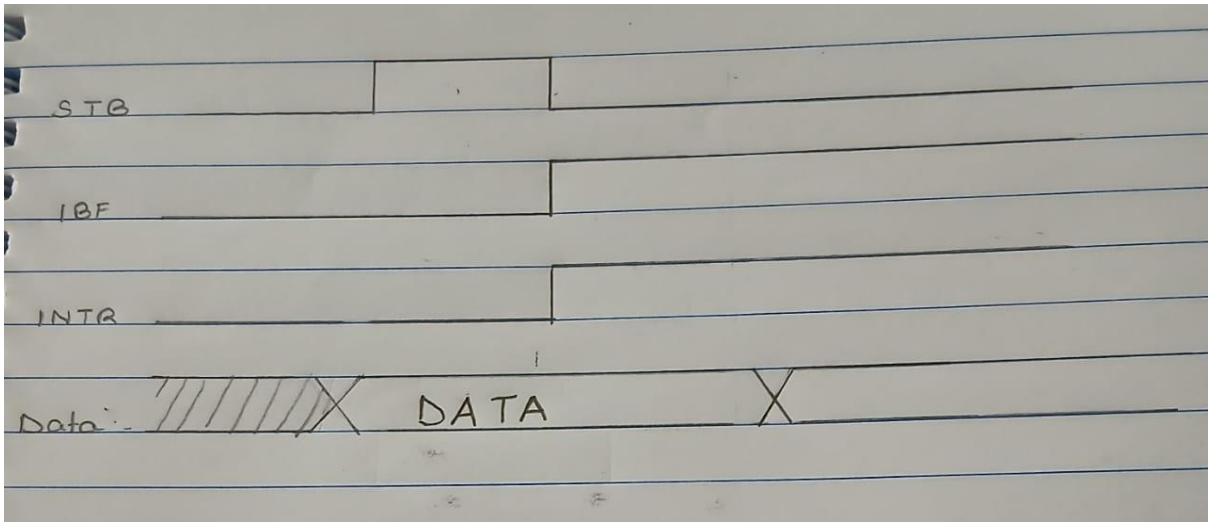
IBF (Input Buffer Full) -Set by 8255 when data latches into the input port (after STB goes low). Cleared when the microprocessor reads the port.

INTR (Interrupt Request) - Activated (high) when data is ready to be read by the microprocessor. It goes high only if INTE = 1 and IBF = 1.

INTE (Interrupt Enable) - A flip-flop controlled by the microprocessor using the BSR mode. If INTE = 1, INTR will be activated when IBF is set.

BSR mode. If INTE = 1, INTR will be activated when IBF is set.

b. Discuss how the timing and coordination of these signals affect the system performance and reliability.
Early STB might latch incorrect or invalid data.
Late read by the CPU might risk data being overrun if the peripheral sends new data.
Missed INTR causes input data loss unless polling is used.
c. Draw and interpret the timing waveforms for a typical strobed input operation. clearly labelling all relevant signals and transitions.



d. Evaluate the advantages and potential limitations of using Mode 1 for input operations in real-world interfacing scenarios.

10mks

Advantages

1. Handshake Reliability: Prevents data loss via IBF/ST$\overline{B}$ synchronization.
2. CPU Efficiency: Interrupt-driven transfers reduce polling overhead.
3. Synchronization allows safe data sharing between asynchronous systems.

Disadvantages

1. Port C Utilization: Dedicates 3 Port C lines per port (e.g., PC4-PC6 for Port A), limiting the use of general-purpose I/O.
2. Interrupt Overhead: Frequent INTRs may saturate the CPU in high-speed systems.