**CAT II.**

**MIGIDE ALLGER SYMLES.**

**169202.**

**ICS 3.1 D.**

1. Write a BSR control word to set bits PC7 and PC0 and to reset them a er 1 1-second delay. Include an assembly language program to perform the above task. 4marks

JMP START

; data

; code

START:NOP

;Start writing code here

; -------------------------------

; Program to:

; - Set PC0

; - Set PC7

; - Wait ~1 second

; - Reset PC0

; - Reset PC7

; -------------------------------

; Set PC0

MVI A, 08H

OUT 83H

; Set PC7

MVI A, 0F8H

OUT 83H

; Delay loop

; Simple nested loop for approx 1 second

; (Adjust constants for your clock speed)

MVI B, 0FFH

MVI C, 0FFH

DELAY\_OUTER:

MVI D, 0FFH

DELAY\_INNER:

NOP

DCR D

JNZ DELAY\_INNER

DCR C

JNZ DELAY\_OUTER

DCR B

JNZ DELAY\_OUTER

; Reset PC0

MVI A, 00H

OUT 83H

; Reset PC7

MVI A, 0F0H

OUT 83H

; Infinite loop

HERE:

JMP HERE

2. Write down the mode 0 control words for the following two cases:

(a) Port A = Input port, Port B = not used, Port CU = Input port and Port CL = Output port.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | 1 | 0 | 1 | 1 | x | 0 | x |

Control Word is therefore D8H.

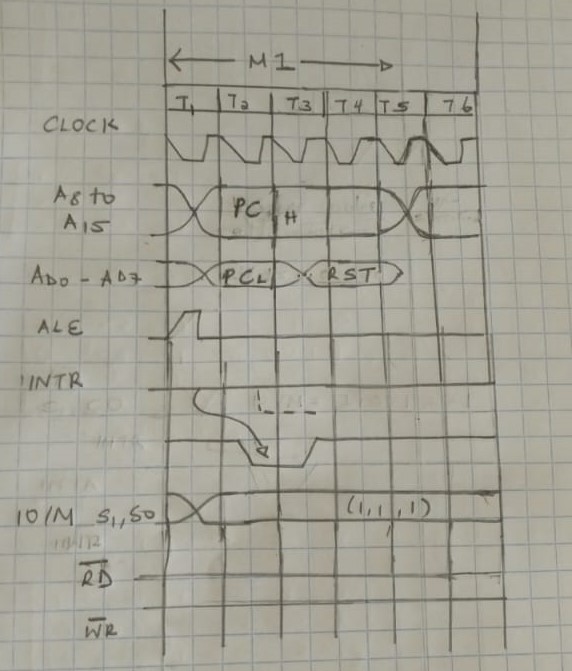
(b) Port A = Output port, Port B = Input port, Port C = Output port

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | 0 | 0 | 0 | 1 | x | 0 | x |

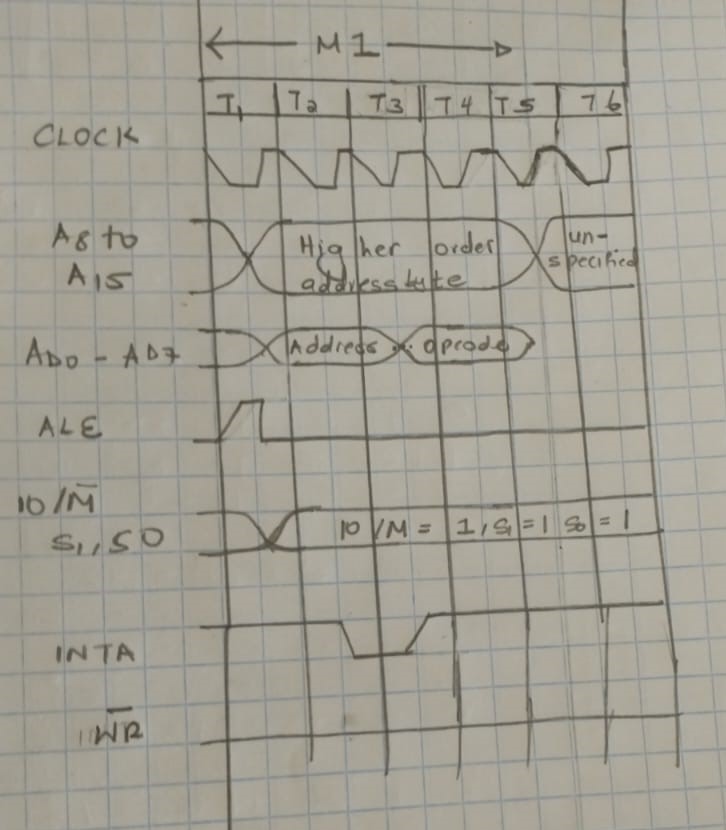
Control Word is therefore 88H.

3. Draw the Interrupt Acknowledge cycles for

(a) RST instruction



(b) CALL instruction



4. Show how the MEMR and MEMW signals are derived from IO/ M , RD and WR signals of PP 8085

When IO/M̅ = 0 (memory operation), MEMR̅ and MEMW̅ become active low during read or write operations respectively.

5. Design a memory having size 16k × 8 from 4k × 4 memory modules

