Using Calibre with DESIGNrev

Student Workbook

May 2006

Trademark Information

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About This Training Workbook

This document is the *Using Calibre* training workbook, which instructs in the concepts necessary for efficient use of the Mentor Graphics Calibre layout verification tool set when verifying an IC design.

Audience

The information in this course is intended for IC Layout Engineers/Specialists who will use the Calibre tools to check the design of Very Large Scale Integration (VLSI) layout and who have the prerequisite knowledge specified below.

What this course is not

- *xCalibre* or *xRC* (the Mentor Graphics parasitic analysis tools) is not taught in this course.

- Creation of the *rule file* (a control file that directs the Calibre verification tool) is not taught in this course.

However, because persons who write rule files should also know the *user* aspects of Calibre, they too might wish to participate in this course.

Prerequisite Knowledge

- Students should have knowledge of IC layout techniques and procedures.

- The user should have pre-existing knowledge of an IC layout tool and an understanding of Spice netlists.

- Knowledge of verification concepts and techniques is not required, but is helpful.

DESIGNrev as a Background Process

DESIGNrev is the layout viewing/editing tool of choice for this class. To guarantee smooth operation, never launch DESIGNrev as a background process or even type in the invoking shell window.

Slide Numbers in the Workbook

Not all slides are published in all workbooks. It may appear from the slide numbers that some slides have been skipped. They have not. Every slide the Instructor will show as part of the class (except for the Title and Objective slides) are re-printed in this workbook for you convenience.

Custom Class Lab Numbering

If you are taking a Custom Class the numbering of the Labs may not directly correspond to the lab number itself. For example, you may be working on Lab 2 but you will find the data in a directory called "lab3". Please take care to follow the Lab instructions for which directory you will find the data for a given Lab.

Module 1
Introduction

Objectives

Upon completion of this module, you will be able to:

- Explain how Calibre fits into an IC design flow

- Select which Calibre tool to use for which job

- Name the Calibre inputs and outputs for DRC and LVS checks

- Perform simple tasks using Calibre Interactive User Interface launched from Calibre DESIGNrev

Course Objectives

Course Objectives

At the completion of this course you will be able to:

♦ **Run DRC checks using Calibre DRC.**

♦ **Run LVS checks using Calibre LVS.**

♦ **Read and understand various Calibre reports.**

♦ **Use DRC RVE and LVS RVE to help find discrepancies in the layout.**

♦ **Explain some of Calibre extended capabilities.**
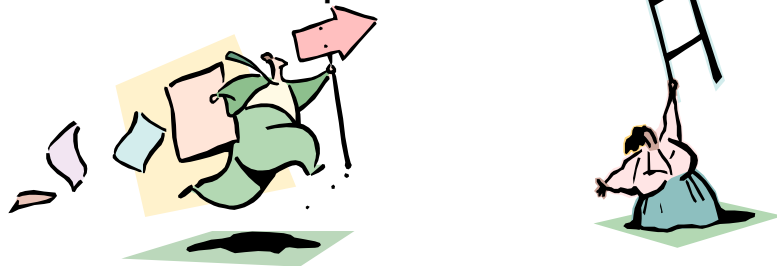
DESIGNrev

Notes:

DRC: Design Rule Checking

RVE: Results Viewing Environment

References:

There are several on-line manuals that you will find useful throughout this class. The file name is in parentheses after the title:

- *Calibre Verification Bookcase* (_bk_calbr.pdf)

- *Calibre Verification User's Manual* (calbr_user.pdf)

- *Standard Verification Rule Format (SVRF) Manual* (svrf_ur.pdf)

- *Calibre DESIGNrev User's Manual* (calbr_drv_user.pdf)

All these manuals are located in the $MGC_HOME/shared/pdfdocs/ directory.

Objectives for This Module

Objectives for This Module

At the completion of this lecture and lab you will be able to:

◆ **Explain how Calibre fits into an IC design flow**

◆ **Select which Calibre tool to use for which job**

◆ **Name the Calibre inputs and outputs for DRC and LVS checks**

◆ **Perform simple tasks using the Calibre Interactive User interface launched from Calibre DESIGNrev**

Notes:

What Flows Include Calibre?

- ◆ **IC Design and Layout Verification Flow**
  - ● **Layout Verification Process Flow for DRC**
  - ● **Layout Verification Process Flow for LVS**
- ◆ **Mask Manipulation and Mask Data Prep Flow**

The details for the layout verification process flow for DRC and LVS are given in the next few slides.

Notes:

IC Design and Layout Verification Flow

IC Design and Layout Verification Flow

```
        ┌──────────────┐
        │   Netlist    │
        └──────────────┘
               ↕
        ┌──────────────┐
        │  Simulation  │
        └──────────────┘
          ↙          ↘
┌──────────────┐  ┌──────────────────┐
│Automated Layout│◄─►│Full Custom Editing│
└──────────────┘  └──────────────────┘
        ┌──────────────────┐
        │ Completed Layout │
        └──────────────────┘
               ↓
        ┌──────────────────┐
        │Layout Verification│
        └──────────────────┘
```
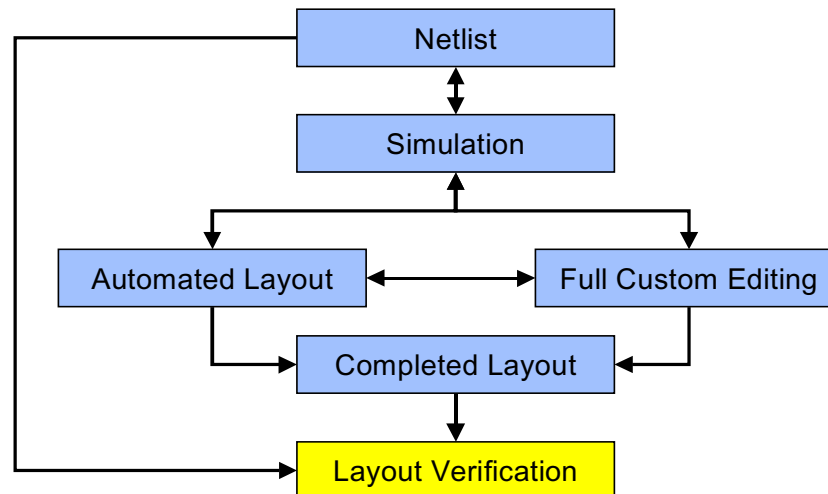
Notes:

Netlist is normally in SPICE format but is can also be VHDL, Verilog, or any other format that formally defines the intent of a design. Note that Calibre will currently only accept SPICE and Verilog formats.

Completed layout is not necessarily "completely" complete. You may choose to verify a design when only part of it is complete. Calibre provided methods to verify partially completed layouts.

Layout Verification Process Flow for DRC

Layout Verification Process Flow for DRC

```
   ┌───────────┐    ┌───────────┐
   │ Rule File │    │ Completed │◄──────────────────────┐
   └───────────┘    │  Layout   │                        │
         │          └───────────┘                        │
         │                │                               │
         ▼                ▼                               │
   ┌──────────────────────────────┐                      │
   │         Calibre DRC          │                      │
   └──────────────────────────────┘                      │
         │                │                               │
         ▼                ▼                               │
   ┌───────────┐    ┌───────────┐                        │
   │   ASCII   │    │DRC Results│                        │
   │  Report   │    │ Database  │                        │
   └───────────┘    └───────────┘                        │
                          │                               │
                          ▼                               │
   ┌──────────────────────────────┐     ┌──────────────┐ │
   │      Locate Errors using     │────►│Correct Layout│─┘
   │  Calibre RVE and Layout Tool │     │    Errors    │
   └──────────────────────────────┘     └──────────────┘
```

Notes:

Using Calibre with DESIGNrev
June 2004
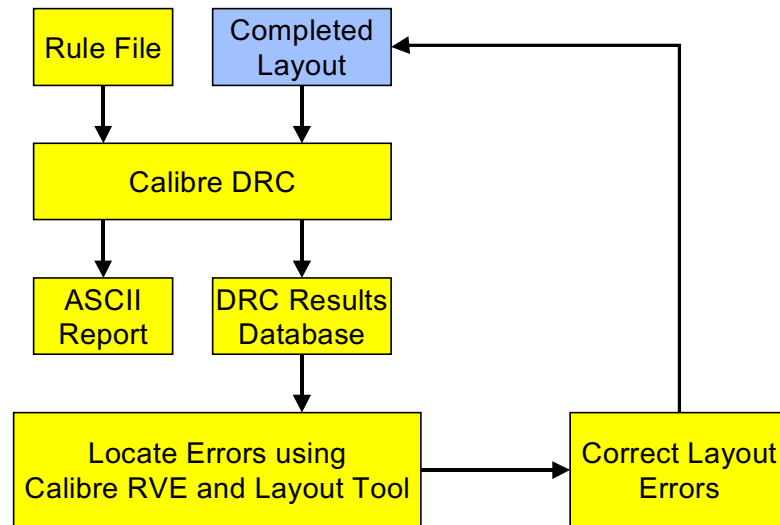
Layout Verification Process Flow for LVS

Layout Verification Process Flow for LVS

```
┌──────────────┐   ┌──────────────┐   ┌──────────────┐
│  Completed   │   │  Rule File   │   │  Completed   │◄─────┐
│   Source*    │   │              │   │   Layout     │      │
└──────┬───────┘   └──────┬───────┘   └──────┬───────┘      │
       │                  │                  │              │
       ▼                  ▼                  ▼              │
┌───────────────────────────────────────────────────┐      │
│                   Calibre LVS                       │      │
└──────┬───────────────────┬──────────────────┬──────┘      │
       │                   │                  │             │
       ▼                   ▼                  ▼             │
┌──────────────┐   ┌──────────────┐   ┌──────────────┐      │
│    ASCII     │   │  Extracted   │   │ LVS Results  │      │
│   Report     │   │   netlist    │   │ Database(s)  │      │
└──────┬───────┘   └──────┬───────┘   └──────┬───────┘      │
       │                  │                  │              │
       ▼                  ▼                  ▼              │
┌──────────────┐   ┌──────────────┐   ┌──────────────┐      │
│   Determine  │   │ Locate Errors│   │              │      │
│ Errors from  │──►│ using Calibre│──►│Correct Layout│──────┘
│    Report    │   │   RVE and    │   │    Errors    │
│              │   │ Layout Tool  │   │              │
└──────────────┘   └──────────────┘   └──────────────┘
```
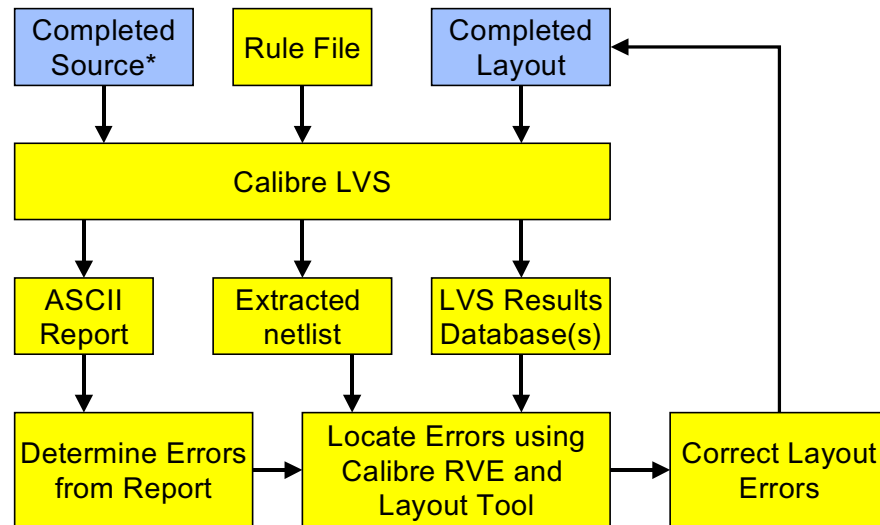
*Schematic netlist for the completed source

Notes:

Mask Manipulation Process Flow

Mask Manipulation Process Flow

```
┌──────────┐   ┌──────────┐
│ Rule File│   │ Completed│
│          │   │  Layout  │
└────┬─────┘   └────┬─────┘
     │              │
     ▼              ▼
┌────────────────────────┐
│      Calibre DRC       │
└────┬──────────────┬────┘
     │              │
     ▼              ▼
┌──────────┐   ┌──────────┐
│  ASCII   │   │Final Mask│
│  Report  │   │  GDSII   │
└──────────┘   └────┬─────┘
                    │
                    ▼
┌────────────────────────┐
│ Final Layout Verification │
└────────────────────────┘
```
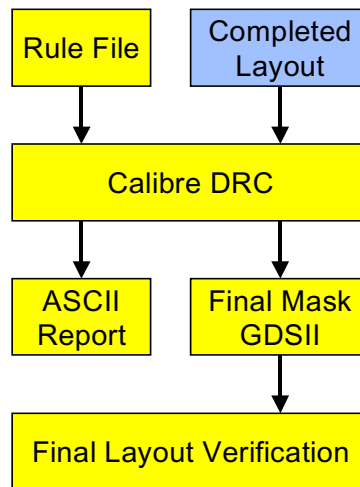
Notes:

What are the Various Calibre Tools?

What are the Various Calibre Tools?

Covered in this class:	Not covered in this class:
♦ **Calibre RVE/QDB-H**	♦ **Calibre xRC (xCalibre)**
♦ **Calibre LVS and Calibre LVS-H**	♦ **Calibre Cell/Block**
♦ **Calibre DRC and Calibre DRC-H**	♦ **Calibre MDP**
♦ **Calibre Interactive**	♦ **Calibre RET tools**
♦ **Calibre DESIGNrev (optionally)**	

Notes:

QBD-H: Query Database -Hierarchical

Useful Abbreviations

Useful Abbreviations

- ♦ **SVRF—Standard Verification Rule Format**
- ♦ **PVX—Physical Verification and Extraction**
- ♦ **RVE—Results Viewing Environment**
- ♦ **SVDB—Standard Verification Database (LVS results)**
- ♦ **DRC—Design Rule Checking**
- ♦ **LVS—Layout Versus Schematic**
- ♦ **ERC—Electrical Rule Checking**

Notes:

What is the Difference Between Hierarchical and Flat? (and Why Should I Care?)

What is the Difference Between Hierarchical and Flat? (and Why Should I Care?)

♦ **Flat: Looks at every geometry in every cell**

♦ **Hierarchical: Only looks at a single instance of any cell**

♦ **Benefits of using Hierarchical:**

- **Minimizes redundant processing
  Stores, analyzes, and processes data once per cell instead of once for every cell placement**

- **Uses design database hierarchy to reduce processing time, memory usage, and DRC result counts**

- **Does not lose lower level to upper level interactions**

♦ **If you have the license, you can use hierarchy all the time.**

Notes:

What are I/Os for DRC and LVS?

What are I/Os for DRC and LVS?

◆ **Inputs**

- **Layout**
- **Logic (for LVS)**
- **Rules**

◆ **Outputs**

- **DRC Results**
- **SVDB (LVS results database)**
- **Report**
- **Log (Transcript)**

Notes:

Using Calibre with DESIGNrev
June 2004

What are the Various I/O Formats?

What are the Various I/O Formats?

♦ **Inputs**

- **Layout (Typically GDSII)**

- **Rule Files (ASCII)**

- **Schematic or Netlist (SPICE or Verilog)
  (LVS only)**

♦ **Outputs**

- **Layout (with results flagged)**

- **Transcript (ASCII)**

- **Results databases (ASCII and binary)**

Notes:

Methods for Invoking Calibre Tools

Methods for Invoking Calibre Tools

♦ **Directly from the command line**
  - **$MGC_HOME/bin/calibre -drc my_file**
  - **Specify run information on the command line or in the rule file**

♦ **From Calibre Interactive GUI**
  - **$MGC_HOME/bin/calibre -gui**

  - **Select which Calibre you want to use**

♦ **From within other tools**

From DESIGNrev:
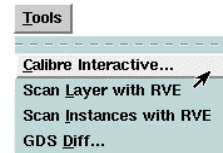
Notes:

What is Calibre DESIGNrev?

What is Calibre DESIGNrev?

- ♦ **Rapid display/edit for GDSII layouts**
- ♦ **Launch Calibre DRC, LVS, and RVE (Calibre Interactive)**
- ♦ **Display results on the layout**
- ♦ **Make simple layout changes**

Notes:

How to Invoke Calibre DESIGNrev—calibredrv
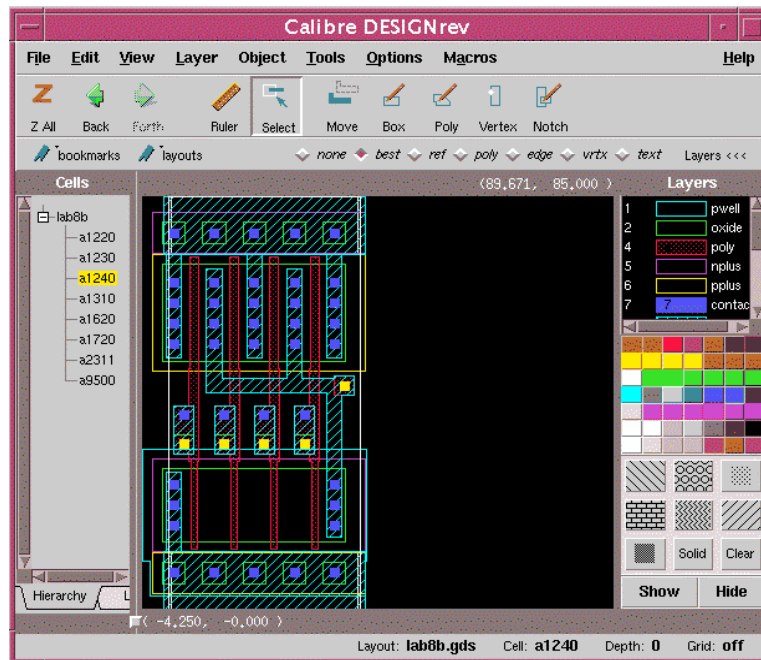
Notes:

How to Find Help

How to Find Help

♦ **Online help / manuals**

♦ **Supportnet**

♦ **White papers**

♦ **Application Notes**

Notes:

What is the Command Line Format?

What is the Command Line Format?

♦ **You can run all Calibre operations directly from the command line**

♦ **Example**

- **calibre -drc my_drc_rules_file**

- **calibre -lvs my_lvs_rules_file**

♦ **Rule files contain more setup information than when using Calibre Interactive**

♦ **Covered in the last Module**

Notes:

Lab Information

Lab Information

In this lab you will:

- ♦ **Invoke DESIGNrev**

- ♦ **Launch Calibre Interactive**

- ♦ **Review the DRC, LVS, and RVE interactive windows**

- ♦ **Run a completely setup DRC run**

- ♦ **Use the Help to find information**

- ♦ **Display the DRC results**

Notes:

Lab: Introduction to Calibre

Introduction

In this lab, you will learn how to invoke DESIGNrev and launch the various Calibre Interactive tools from DESIGNrev. You will run "pre-set" LVS and DRC learning how to view a discrepancy using Calibre RVE. You will also explore how to obtain help for the various Calibre tools. Finally you will be encouraged to experiment with polygon creation in DESIGNrev to enable you to edit layout designs in future labs.

Several concepts and procedures have not yet been thoroughly explained in the lecture, but you will be given enough information to perform the necessary tasks. You will obtain a deeper understanding of these concepts in later lectures and labs.

In this first lab, all procedural steps contain full step-by-step instructions and information. As you gain practice in performing common procedures, the labs will provide less instruction on those procedures. The labs will inform you when they will no longer give detailed step-by-step instructions for a procedure and they will reference the most recent lab step that provided those instructions.

Lab Conventions

In order to make labs as simple and clear as possible, the instructions use the following conventions:

- You usually just click mouse buttons unless specifically told to do otherwise.

    o LMB: left mouse button (default)

    o RMB: right mouse button

    o MMB: middle mouse button

- Numbered or lettered steps have you perform some action. Paragraphs without numbers only provide supplemental information or ask questions for you to think about.

- Numbered steps are a "base" action. If there are lettered steps below a number, these lettered steps provide all the details of how to perform the numbered step. Therefore, if you already know how to do the numbered step you may safely skip the lettered steps, unless you are specifically told otherwise. (It would be a good idea to at least skim the lettered steps, even if you already know how to perform the base operation.)

  For example:

  1. Go outside.

     a. Exit the room through the rear door of the classroom.

     b. Walk left down the hall.

     c. Turn right at the "T".

     d. Make a right at the elevators.

     e. Exit through the front doors of the building.

  If you already know how to "go outside", you can just "go outside". If you do not know or remember how to get outside, you could follow the lettered steps to get there. Notice that even though you know how to get outside you might not have gone out through the front doors, so it would still be a good idea to skim the lettered steps to make sure you end up at the expected place.

- In the early exercises, all steps are provided. Once you have done a task, you will simply be told to do it, with maybe a little reminder of how it was done.

- You should leave the tools up and running as you move from exercise to exercise. The exercises usually build on each other. On the other hand, you can close the tools after a lab (full block of exercises). If you are

specifically told to close a tool or application between exercises you should do so.

- If you ever have any problems or questions about a lab, feel free to ask your instructor for help.

List of Exercises

Exercise 1-1: Invoke DESIGNREV

Exercise 1-2: Launch Calibre DRC and LVS Interactive

Exercise 1-3: View a Discrepancy with Calibre RVE

Exercise 1-4: Get Help

Exercise 1-5: Experiment with DESIGNrev

Exercise 1-1: Invoke DESIGNREV

In this exercise you will invoke DESIGNrev from the command line, load the palette, and load a GDSII design.

1. From a UNIX shell, change your directory to "lab1".
   ```
   cd $HOME/using_calbr/lab1
   ```

2. List the contents of the lab1 directory.
   ```
   ls
   ```

   You should see at a minimum the following files:

   - golden_rules

   - lab1.gds

   - lab1_rules

   - lab1_runset.txt

   - layer_props.txt

   If any of these files are missing, please double check that you are in the correct directory, and then notify your instructor.

3. Launch DESIGNrev.
   ```
   $MGC_HOME/bin/calibredrv
   ```

   🚫
   Warning　Do not launch DESIGNrev as a background process! Also do not type in the DESIGNrev shell window once the application is invoked until you close it.

   This will open the initial DESIGNrev window.

   Now you will load the GSDII file.

4. Choose **Menu: File > Open Layout**.

5. Select lab1.gds, by double-clicking.

   This loads the layout design you will be using for the first parts of this lab.

   Next you load the layer properties file. This file gives the various layers names (rather than just numbers) and gives the layers their "expected" colors.

6. Load the layer properties. (**Menu: Layer > Load Layer Properties**)

   This opens the Load Layer Properties dialog box.

7. Select the layer_props.txt file.

8. Choose **OPEN** to execute the dialog box.

   This loads the layer properties.

The DESIGNrev window should look similar to below.

Select Mode Options
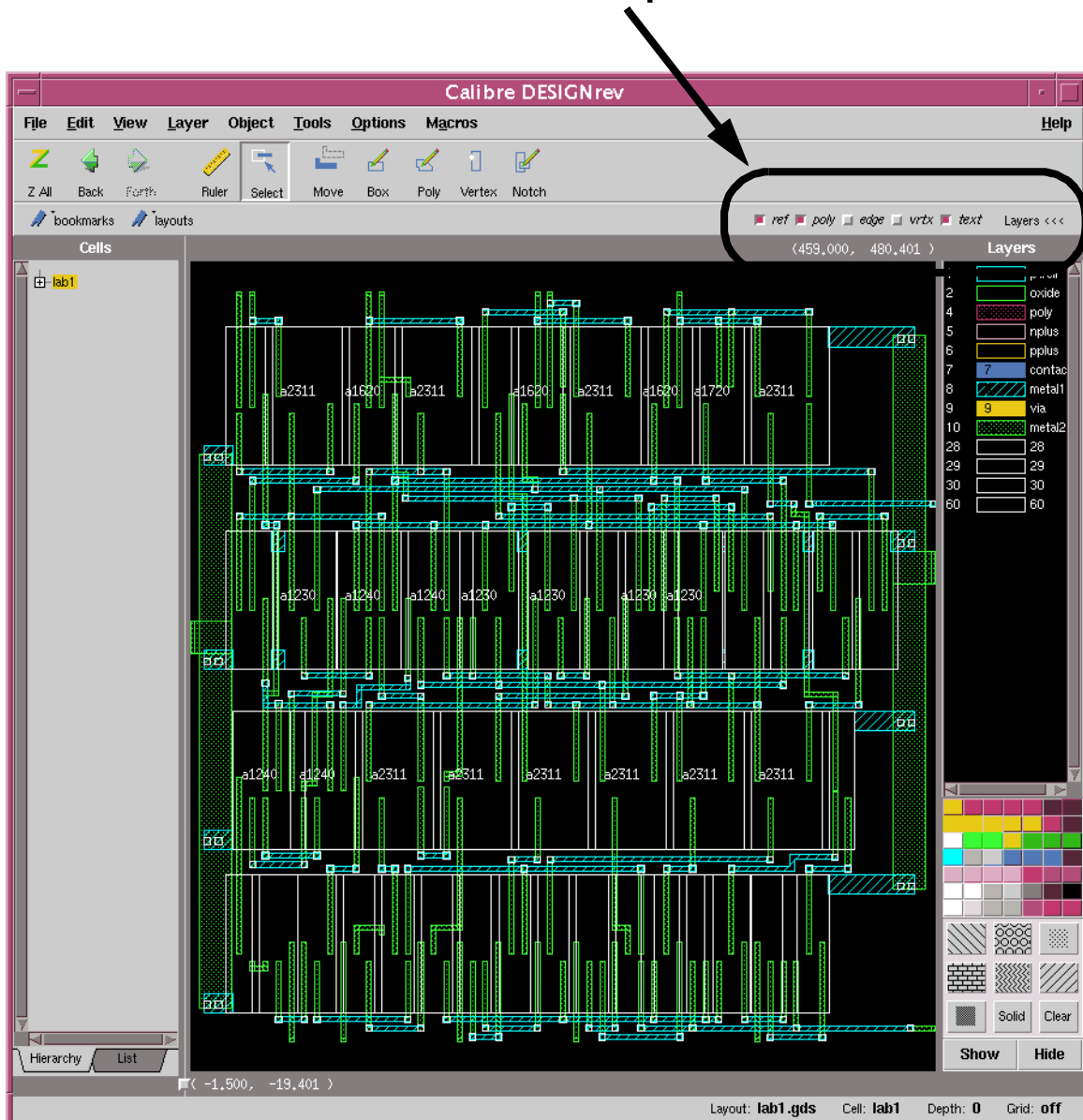
In a later exercise, you will review how to work in the DESIGNrev environment, for now you are ready to launch Calibre Interactive.

Exercise 1-2: Launch Calibre DRC and LVS Interactive

In this exercise you will launch Calibre DRC Interactive from within the layout viewer. You will briefly review the Calibre Interactive LVS application window. You will then load a runset containing all the information required for a DRC run. You will then review all the various menus and options available from Calibre Interactive.

1. From DESIGNrev, choose **Menu: Tools > Calibre Interactive**.

    This opens the Calibre Interactive Server dialog box.

2. Display the **Server** tab.
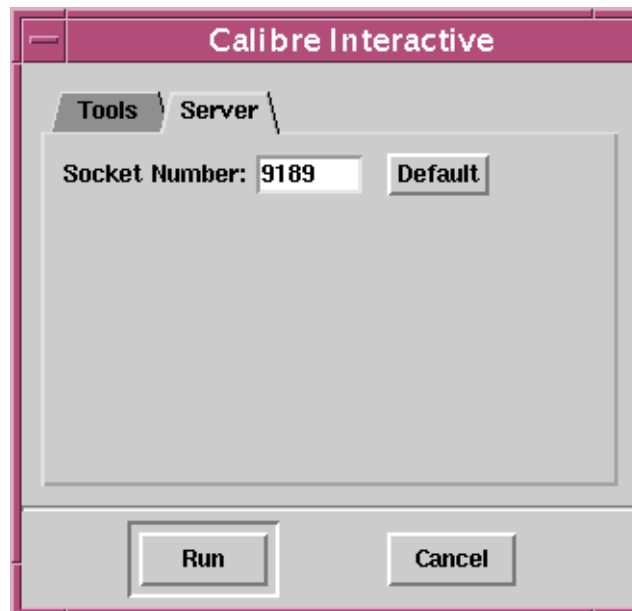
NOTE: Under the **Server** tab is the socket number[1]. The socket number determines which TCP-IP socket DESIGNrev will use to communicate

---

1. Additional socket information: Sharing data between Calibre DESIGNrev and any other application requires establishing a connection between them using sockets and TCP-IP protocol. Sockets are essentially addresses to which messages and data can be sent. One application, the server, owns the address. The other, the client, sends messages to that address. The Calibre DESIGNrev revision tool selects a default socket for communicating with other applications. If that socket is busy, it finds an available one. However, if you intend to share data with another application that is already running, you must know the socket number that application is using.

with Calibre Interactive and Calibre RVE. In general, the socket number should not require editing.

3. Leave the socket as the default number (unless the instructor tells you otherwise).

4. Display the **Tools** tab.
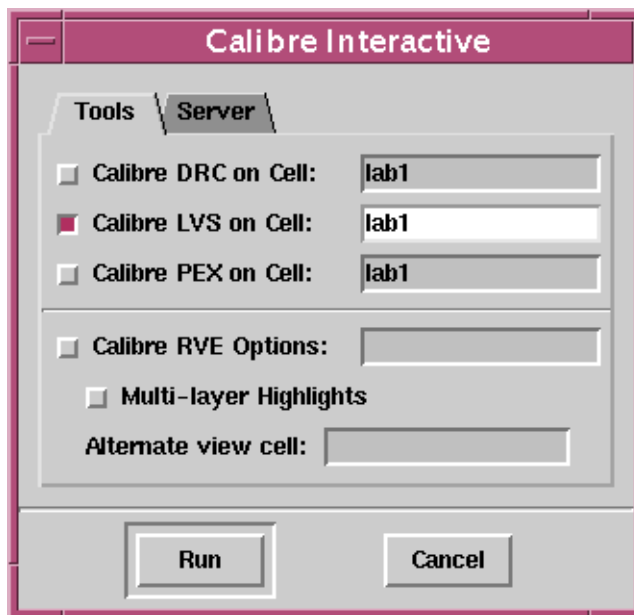
The Multi-layer highlight option allows multiple layers to be created for highlighting RVE geometries. (A single layer is enough for this lab.)

The Calibre Interactive section determines which Calibre interactive tools will be launched. In this class, we are only covering DRC and LVS. The cell names are automatically filled-in from the cell selected in DESIGNrev. (In this case it is the top-level cell, since you did not select anything.)

The last section covers Calibre RVE. For most of this class, we will allow RVE to launch automatically after a DRC run, so we will not select it at this point. Types of RVE options include:

o specifying the results databases (not necessary)

o -64 if you need to run in 64 bit mode

o   -nowait if you do not want to wait for a license

o   other licensing options

5. In the dialog box, select **LVS**.

6. Check that the cell name is "lab1".

7. Choose **Run** to execute the dialog box.

This launches Calibre LVS.
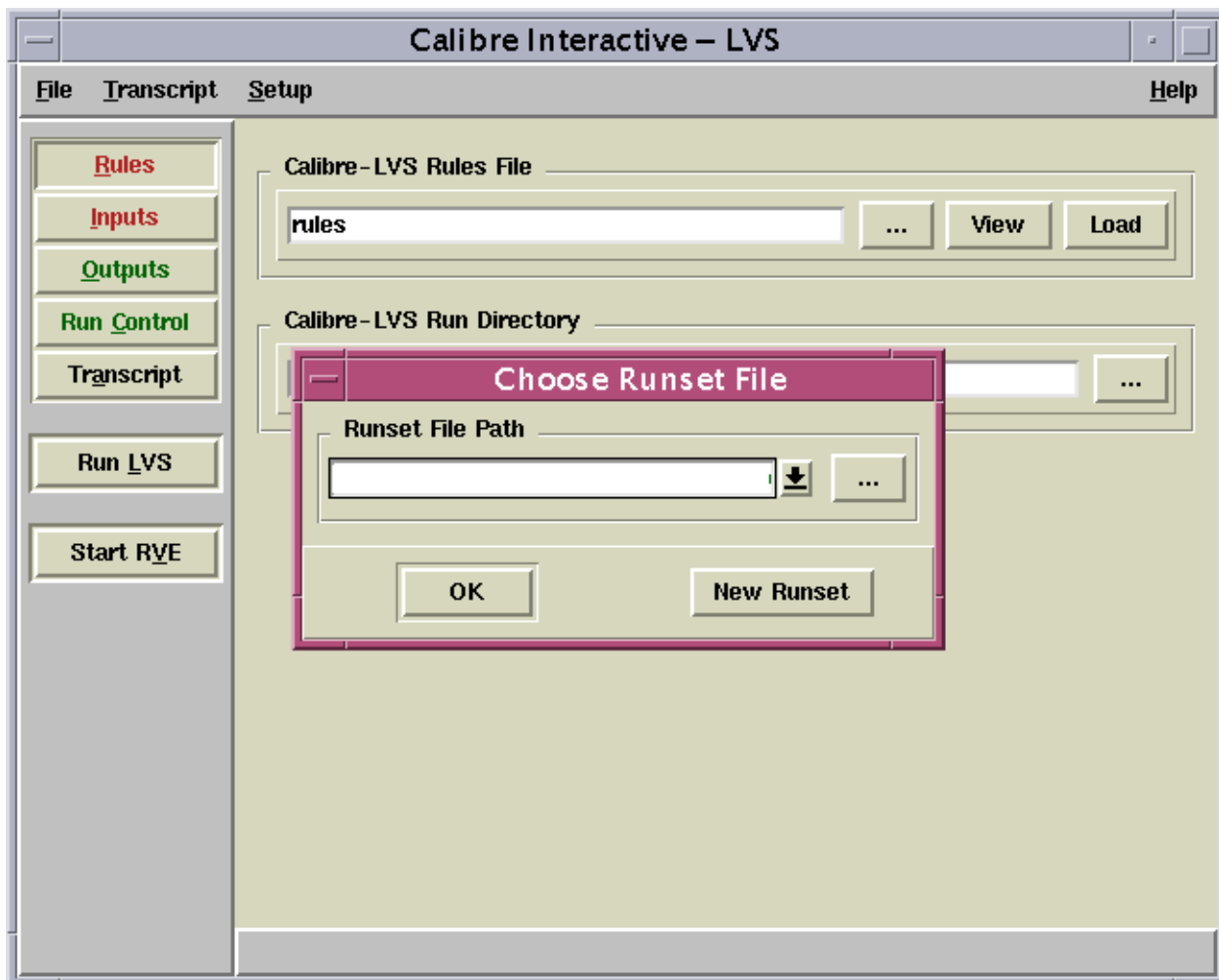
Initially Calibre Interactive LVS asks you to choose a runset. A runset is a default setting so you can have consistent settings between Calibre runs. For this exercise, you will not load a runset.

8. Choose **New Runset** in the Choose Runset File dialog box.

This will make the Calibre Interactive - LVS dialog box active. We will spend a minute reviewing this window.

First, you will notice there are command buttons in three different colors running down the left side of the dialog box. These are called Menu buttons. Red Menu buttons display windows that do not have complete/valid information. Green Menu buttons display windows with

complete/valid information. Black Menu buttons perform an operation or their information is optional.

Pulldown Menus
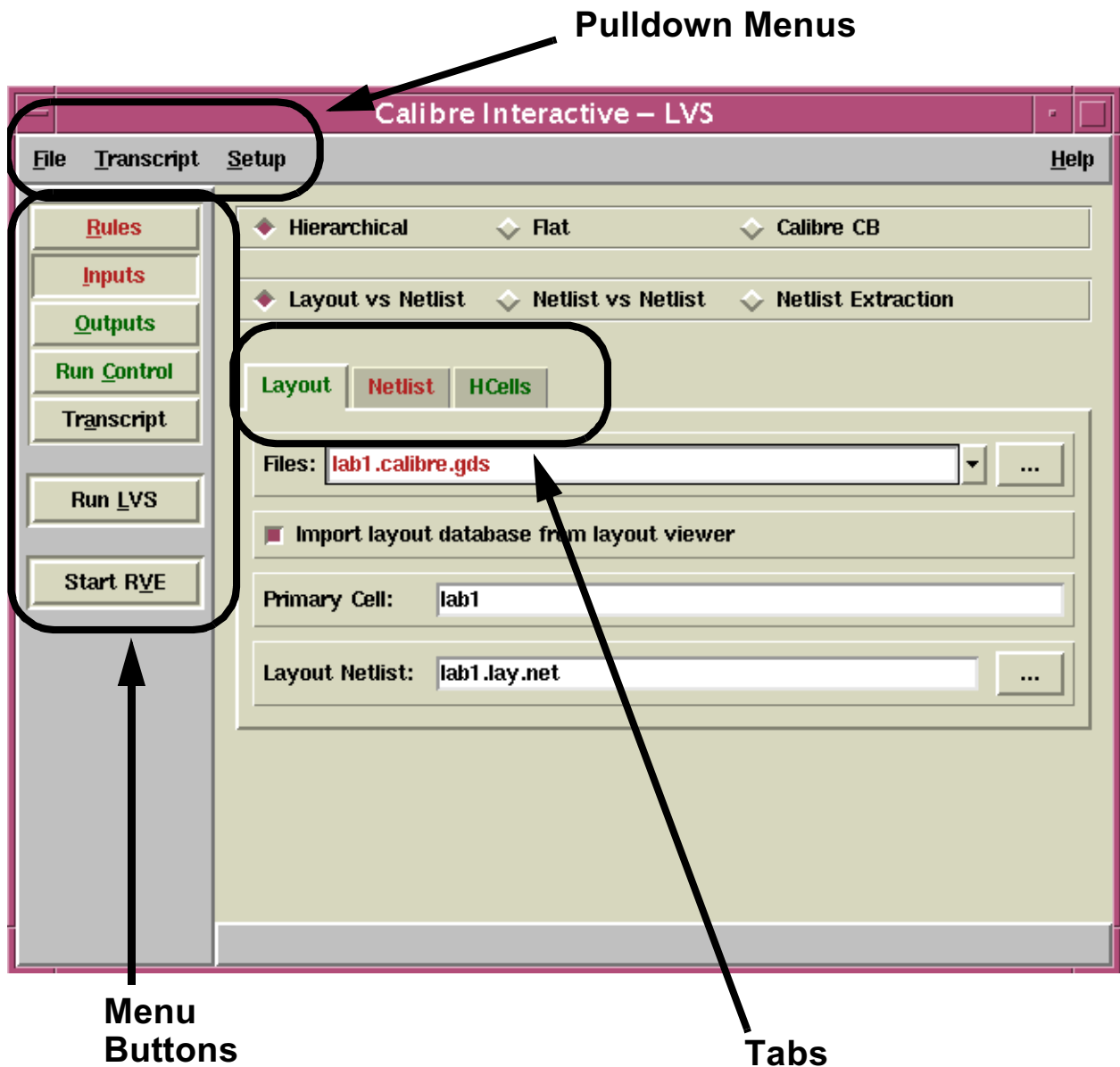
Menu Buttons

Tabs

Pulldown menus are similar to any other application.

Tabs will vary by window. They also use the same color coding as the Menu buttons.

9. Select the various Tabs and Menu buttons to review the types of options available.

   You will be told exactly were to look in the future, but this is just to familiarize yourself with the basic layout of the tool.

10. Close the Calibre Interactive - LVS window (**Menu: File > Exit**). (Choose **NO** to the Save runset dialog box.)

11. Return to the layout viewer.

    Next you will open a Calibre Interactive DRC window.

12. From DESIGNrev, choose **Menu: Tools > Calibre Interactive**.

13. Leave the socket as the default number (unless the instructor tells you otherwise).

14. In the dialog box, select DRC.

15. Unselect LVS.

16. Check that the cell name is "lab1".
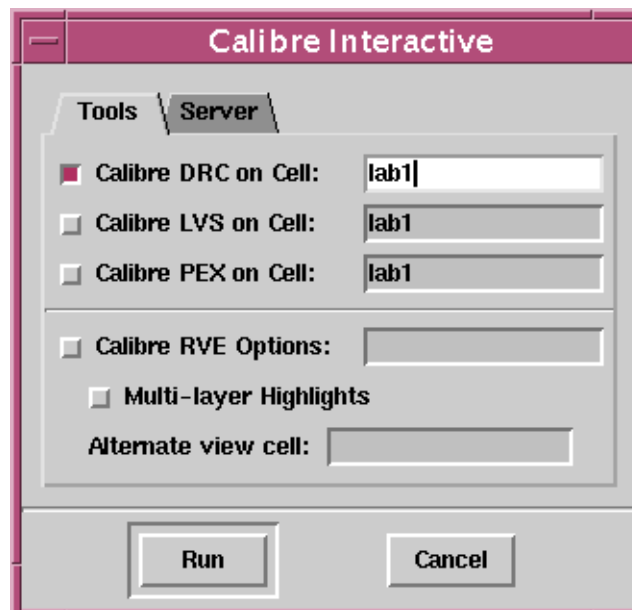
17. Choose **Run** to execute the dialog box.

    The Calibre Interactive - DRC window and Load Runset File dialog box should now be displayed.

18. Choose the **Browse** button ... in the Load Runset File dialog box.

    This opens the Choose Runset dialog box.

19. Making sure you are in the lab1 directory, select lab1_runset.txt.

20. Choose **OK** to execute the Choose Runset dialog box.

    This will return you to the Load Runset File dialog box with lab1_runset.txt entered in the text box. The text should be green, indicating a valid (existing) file.

21. Choose **OK** to execute the Load Runset File dialog box.

    This will make the Calibre Interactive - DRC window active and load all pre-set information into the dialog box. **Inputs** should be the active Menu Button.

    You now have all the information loaded required to perform a DRC run.

22. Choose **Outputs**.

    This window displays the information you want Calibre to output from this run and the format you expect. Notice that RVE will start and the DRC report will automatically display at the end of a DRC run.

23. Choose **Transcript**.

    This window will display the transcript while Calibre DRC runs.

24. Choose **Run DRC**.

When the run completes, the Transcript window will look similar to below:

```
Calibre Interactive – DRC : [lab1_rules.txt]

File   Transcript   Setup                                           Help

  Rules          --- CALIBRE::DRC-H EXECUTIVE MODULE COMPLETED.  CPU TIME = 0  REAL
                 --- TOTAL RULECHECKS EXECUTED = 11
  Inputs         --- TOTAL RESULTS GENERATED = 1 (1)
                 --- DRC RESULTS DATABASE FILE = lab1.drc.results (ASCII)
  Outputs
                 --- CALIBRE::DRC-H COMPLETED - Mon Feb 24 10:04:41 2003
  Run Control    --- TOTAL CPU TIME = 0  REAL TIME = 0
                 --- PROCESSOR COUNT = 2
  Transcript     --- SUMMARY REPORT FILE = lab1.drc.summary

                 // Calibre v9.1_9.3    Fri Dec 13 15:05:27 PST 2002
                 // Litho Libraries v9.1_9.2  Fri Dec  6 12:47:01 PST 2002
  Run DRC        //
                 //             Copyright Mentor Graphics Corporation 2002
                 //                     All Rights Reserved.
                 //        THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMAT
  Start RVE      //          WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
                 //            OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
                 //
                 // Mentor Graphics software executing under Sun SPARC Solaris
                 //
                 // Running on SunOS sundown 5.7 Generic_106541-08 sun4u
                 //
                 // Starting time: Mon Feb 24 10:04:41 2003
                 //
                 // Graphical User-Interface startup.... Complete.
                 //
```

Notice the top set of lines. They tell you that the DRC run completed and the number of discrepancies found.

25. Spend a second scrolling through the transcript, taking note of the type of information available.

26. Make the DRC Summary Report window active by selecting it.

```
====================================================================================
=== CALIBRE::DRC-H SUMMARY REPORT
===
Execution Date/Time:     Mon Feb 24 10:04:40 2003
Calibre Version:         v9.1_9.3   Fri Dec 13 15:05:27 PST 2002
Rule File Pathname:      _lab1_rules_
Rule File Title:
Layout System:           GDS
Layout Path(s):          lab1.gds
Layout Primary Cell:     lab1
Current Directory:       /user/sallyw/calibre/using_calbr/lab1
User Name:               sallyw
Maximum Results/RuleCheck: 1000
Maximum Result Vertices: 4096
DRC Results Database:    lab1.drc.results (ASCII)
Layout Depth:            ALL
Text Depth:              PRIMARY
Summary Report File:     lab1.drc.summary (REPLACE)
Geometry Flagging:       ACUTE = NO   SKEW = NO   OFFGRID = NO
                         NONSIMPLE POLYGON = NO   NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:       COMMENT TEXT + RULE FILE INFORMATION
Layers:                  MEMORY-BASED
Keep Empty Checks:       YES
------------------------------------------------------------------------------------
--- RUNTIME WARNINGS
---
------------------------------------------------------------------------------------
--- ORIGINAL LAYER STATISTICS
---
LAYER pwell ..... TOTAL Original Geometry Count = 7    (48)
LAYER contact ... TOTAL Original Geometry Count = 238 (1587)
LAYER poly ...... TOTAL Original Geometry Count = 26   (324)
LAYER oxide ..... TOTAL Original Geometry Count = 70   (472)
LAYER metal1 .... TOTAL Original Geometry Count = 119 (517)
LAYER metal2 .... TOTAL Original Geometry Count = 189 (487)
------------------------------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS
```

This window displays the results of the DRC check in text format. In later modules, you will cover how to read the report, for now you may what to just skim the report to see the type of information available.

27. When you are finished viewing the report, close the report window. (Choose **Menu: File > Close**.)

The other application launched at the end of the DRC run is Calibre RVE.

Exercise 1-3: View a Discrepancy with Calibre RVE

In the exercise, you will learn how to use RVE to view discrepancies and highlight them in the layout.

1. Make the RVE window active.
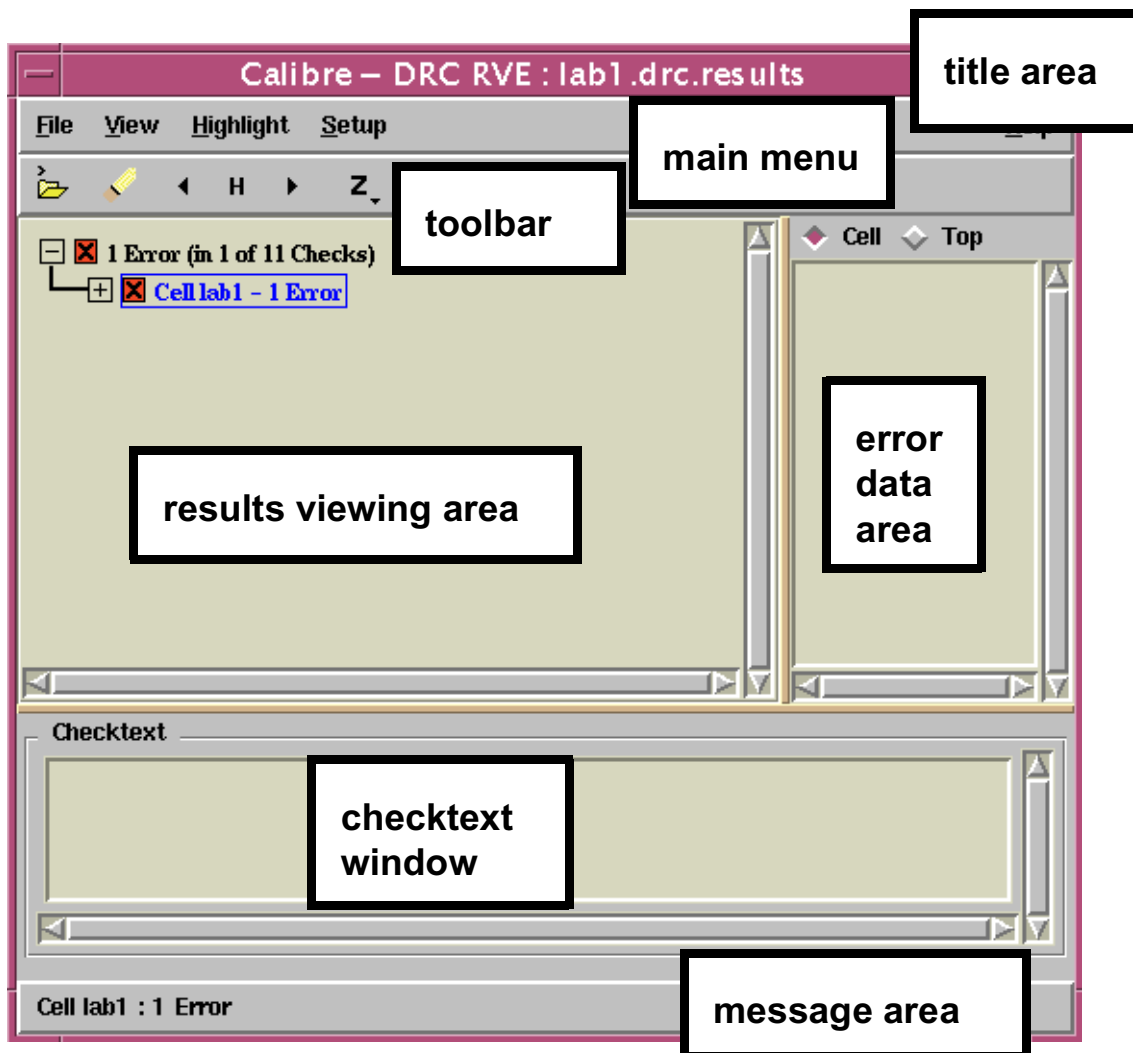
This window has pulldown Menus that are similar to any application.

It also has a Toolbar for the commands used most frequently. The icons from left to right are:

o   Open Database

o Erase Highlights

o Highlight Previous Discrepancy

o Highlight Current Discrepancy

o Highlight Next Discrepancy

o Set Highlight Zoom.

The Results Viewing Area contains a "tree" structure of the DRC results.

To the right of the Results Viewing Area is Error Data Area. This area provides the layout coordinates for the discrepancies. (Useful to manually track the location in the layout.)

Below the Results Viewing Area is the Checktext Window. This area displays the information provided from the rule file about the current discrepancy.

2. Click on the "+" in the Cell lab1 - 1 Error in the Results viewing area.
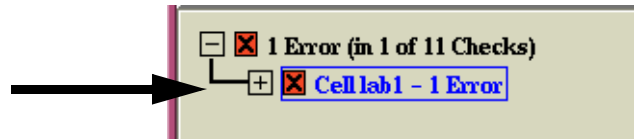
This expands the errors tree to tell you which rule has the discrepancy.

What is the name of the rule with the discrepancy?

_____

3. Click on the "+" for the rule.

What do you see now?

_____

4. Click on the "01".

What do you see now?

In the Error Data Area: _____

In the Checktext Window: _____

This is the type of information you will find for each discrepancy.

In future labs, you will trace the error back to the layout. For now you are finished using RVE.

5. Close the RVE window. (**Menu: File > Exit**)

Exercise 1-4: Get Help

In this exercise, you will learn the basics of where and how to find help on the various Calibre applications you will be using in this class. There are basically two types of Help documentation available for Calibre. Tool Tips which just gives you a brief description of a particular button or field and Manuals which will give you all the printed information available on a given topic.

1. Make the Calibre Interactive - DRC window active again.

2. Choose **Menu: Setup > Show Tool Tips**.
    (Make sure the selection box is highlighted.)

    This enables Tool Tips.

    When you place the cursor over a button or field that has a Tool Tip available, a brief description of the button or the required input displays after about 2 seconds.

3. Make the Inputs window active.

4. Display the Tool Tip for the Files field.

    What is this Tool Tip?

    _____

    What interesting thing did you learn about this field from the Tool Tip?

    _____

5. Try the Tool Tip for the [...] button at the end of the Files field.

    What is the Tool Tip?

    _____

    You can leave the Tool Tips on or turn them off for the rest of the labs.

    Now you will learn how to display the Help information in Manual format.

6. Choose **Menu: Help > Open Bookcase**.

   (If this is the first time Acrobat has run on this workstation, you will need to accept the license agreement when it appears.)

   This launches Adobe Acrobat and automatically loads the Calibre Verification Bookcase.
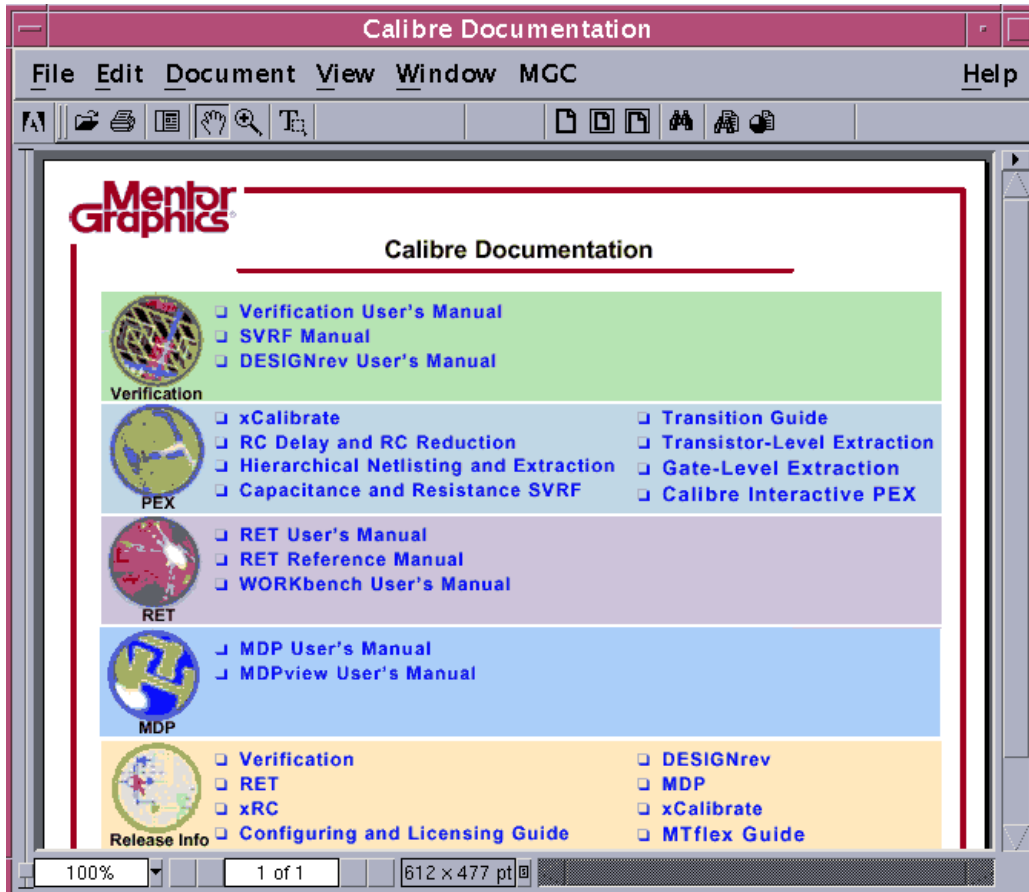
From this document you can find information on all the Calibre applications. The top three items in the list are direct links to manuals documenting the Calibre features we will use in this class. Just click on the manual's name and the document will open in an Acrobat window. The upper three bullets are links to the documentation for this class. All the rest of the bullets are for documentation for Calibre products that are outside the scope of this class.

7. Open the *Verification User's Manual* by clicking on it.

You will notice that down the left side is a Table of Contents-like list of all the Chapters in this manual. These are called Bookmarks.

8. Click on the "arrow" icon ▷ just before Chapter 5 DRC Execution.

   This expands the Bookmarks to include lower level topics in Chapter 5.

9. Click on the word "Chapter 5 DRC Execution".

   This will jump to the beginning of Chapter 5.

   This is useful if you have a good idea of exactly what you are looking for, but what happens if you have no idea where to start? In this case, you can start by searching for a word or phrase. In the next several steps you will look for information on the DRC results database.

10. Click on the Find icon in the Acrobat toolbar.

    This opens the Find dialog box.

11. Enter "drc database" in the Find What text box.

12. Choose **Find**.

    Acrobat will search through the document until it finds that particular string of words.

13. Choose **Find Again** to search for additional occurrences of the word.

14. When you are done experimenting with the search feature close the Find dialog box.

15. Experiment searching for other words or phrases until you are comfortable with the basics of the documentation Viewer tool.

16. When you are done, close all Acrobat windows.

17. Close all Calibre windows except DESIGNrev.
    (You do not need to save the runset.)

Exercise 1-5: Experiment with DESIGNrev

In this exercise, you will learn how to perform some very simple operations in Calibre DESIGNrev. There are multiple ways to perform any task in DESIGNrev. In this lab, most tasks will be done using the Toolbar or mouse button (RMB or LMB) commands whenever possible.

In this exercise, nothing you are going to do is "exacting". You are just to experiment with the tool. You may view any area, select any polygon, change or move any shape. All illustrations are just references to how your layout might look. Anything you do in this exercise will have no bearing on future labs.

1. Make the DESIGNrev window active.

2. Click on the **Z All** toolbar icon.

   This displays the whole design and places you at a good starting point.

3. Displaying the contents of a cell:

   a. Click on the "+" by lab1 in the Cells tree.
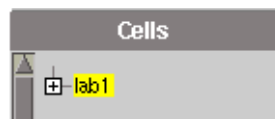
   This expands to give the hierarchy list of all the cells in the lab1 cell.
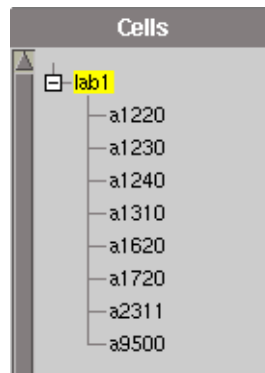
b. Click on a1720 in the cell hierarchy list.
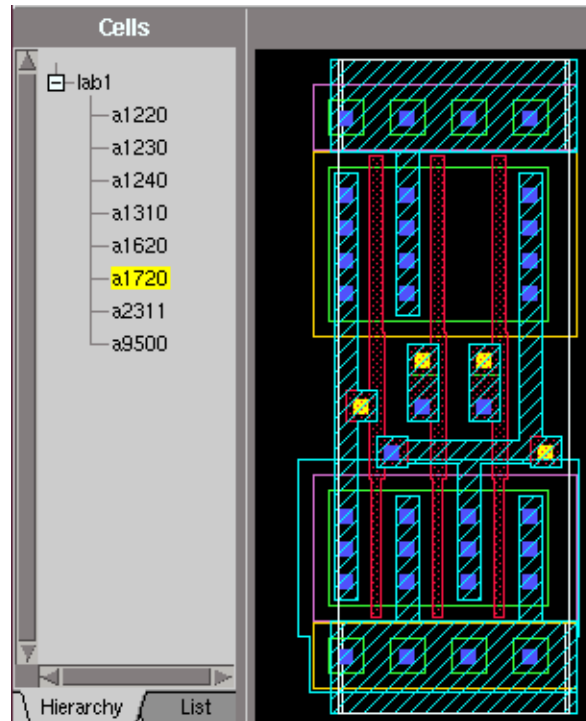
This jumps you into cell a1720, where you can both view and edit the cell's internal layout.

c. Click on lab1 in the cell hierarchy list to return to the full design.

4. Displaying lower/higher in the context:

a. Choose **Menu: View > Change Hierarchy Depth > Increase To Depth**.
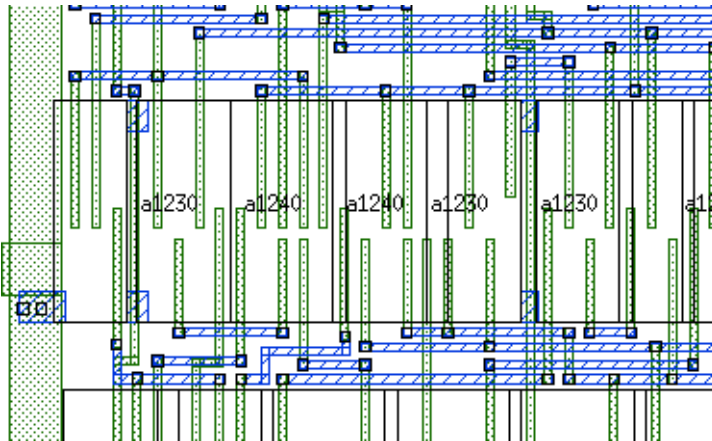
Default
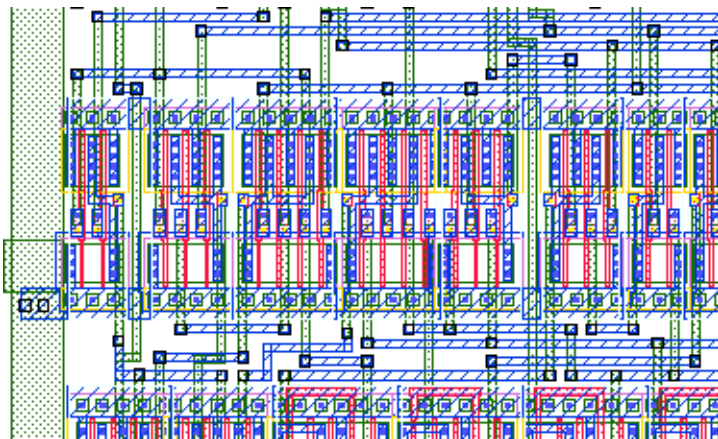
Depth Increase

This displays the layout structures one level lower in the hierarchy. You cannot edit the contents of cells at this level, but you can see the underlying structure and avoid creating shorts, etc.

b. Choose **Menu: View > Change Hierarchy Depth > Decrease To Depth**.

This returns to only displaying the structures at the upper level of the hierarchy.

Note Go directly to a level in the hierarchy by typing the desired level number. For example, "0" is the top level and "1" is the level just below the top level. Do not use the 10-key numeric pad. Only use the regular alphanumberic keys when typing these numbers.

5. Zooming Into an Area:

 a. Hold down the right mouse button (RMB).

 b. Draw a rectangle from upper left to lower right around the area you want to display.

c. Release the RMB.
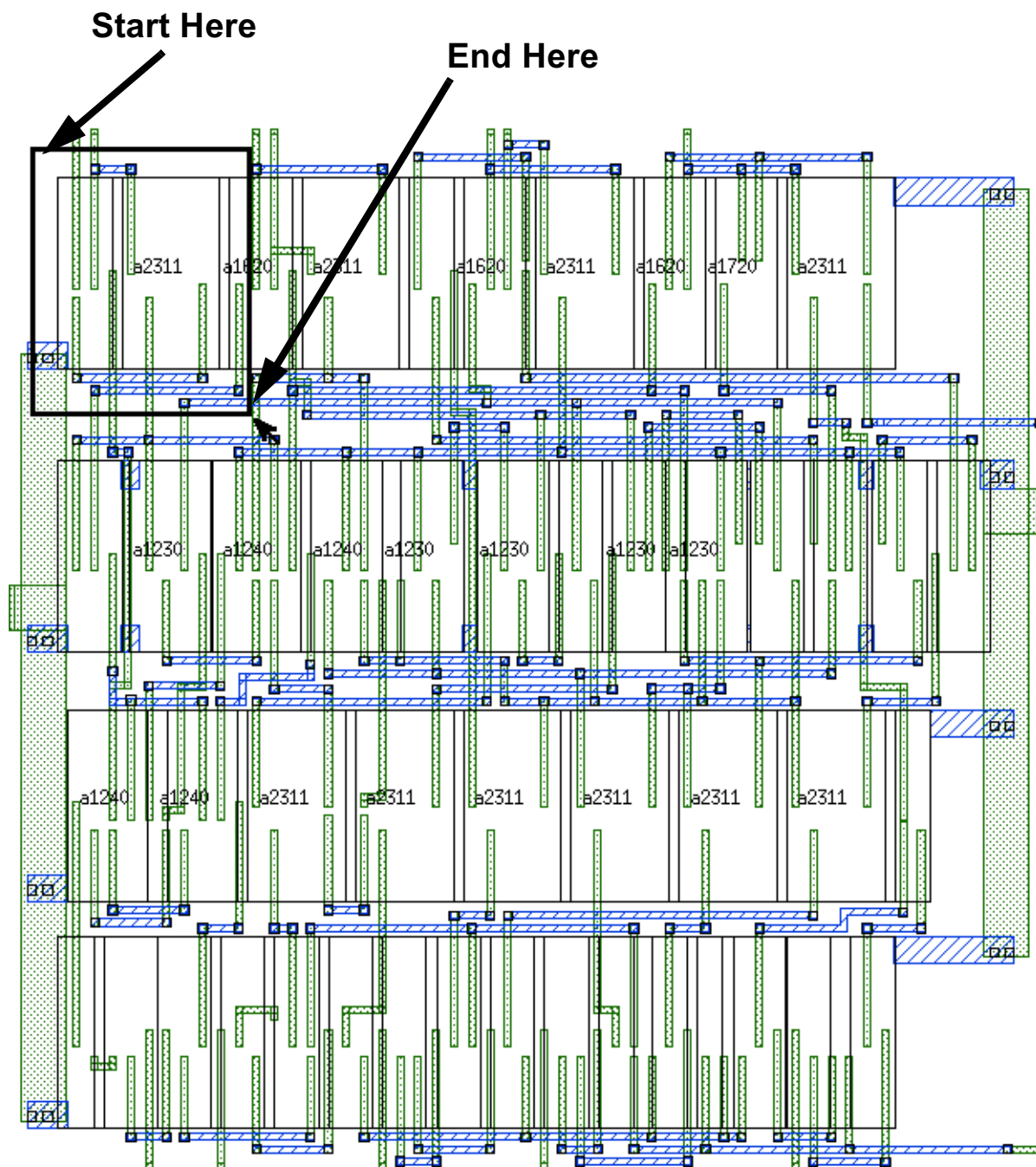
When you release the mouse button, the surrounding area zooms in to fill the display window.

a1220 a2311 a1620
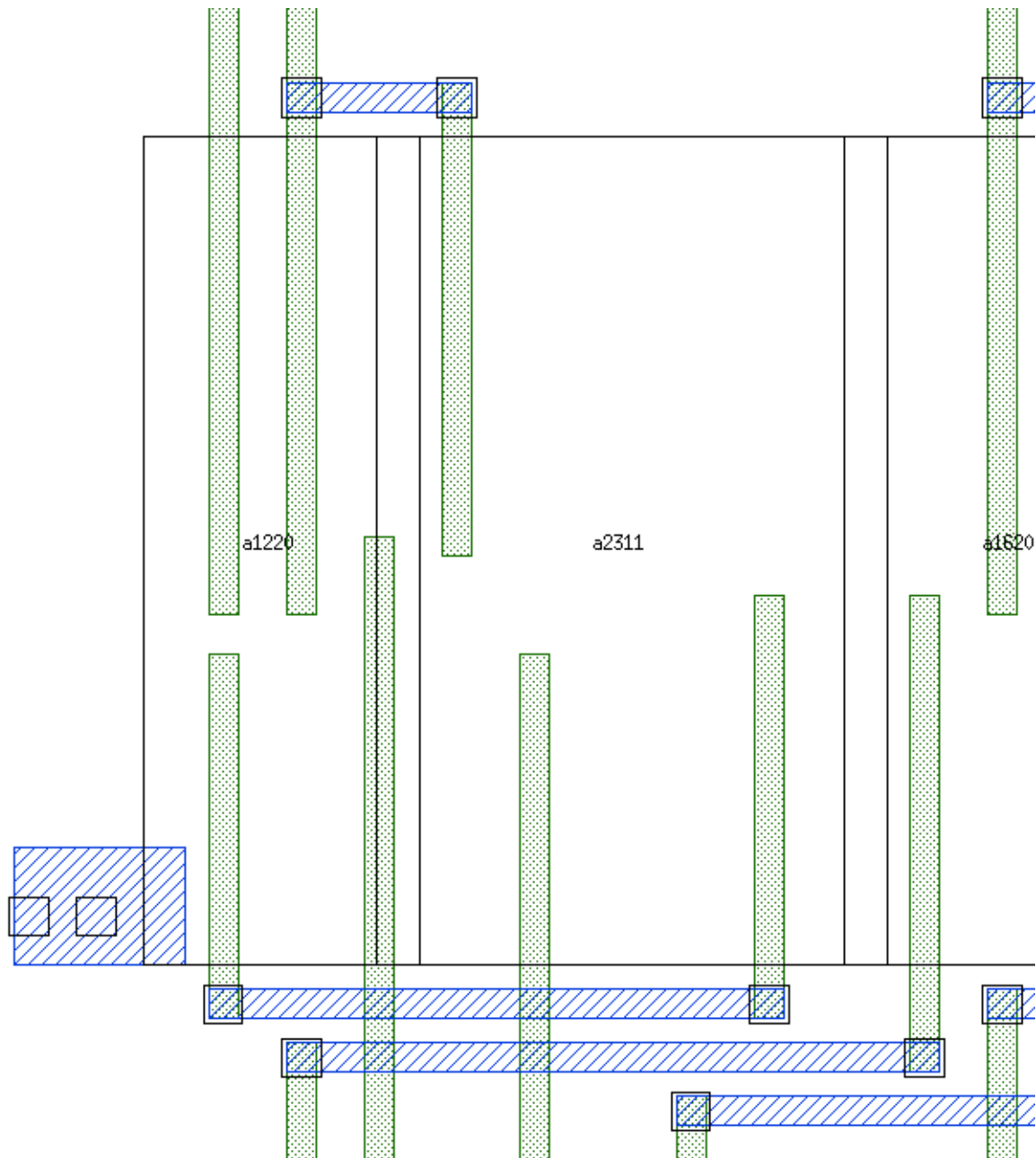
6. Zooming Out of an Area:

   a. Hold down the RMB.

b. Draw a rectangle from the lower right to the upper left, centering around the area that you would like centered in the new display

c. Release the RMB.

End Here

Start Here

a1220

a2311

a1820
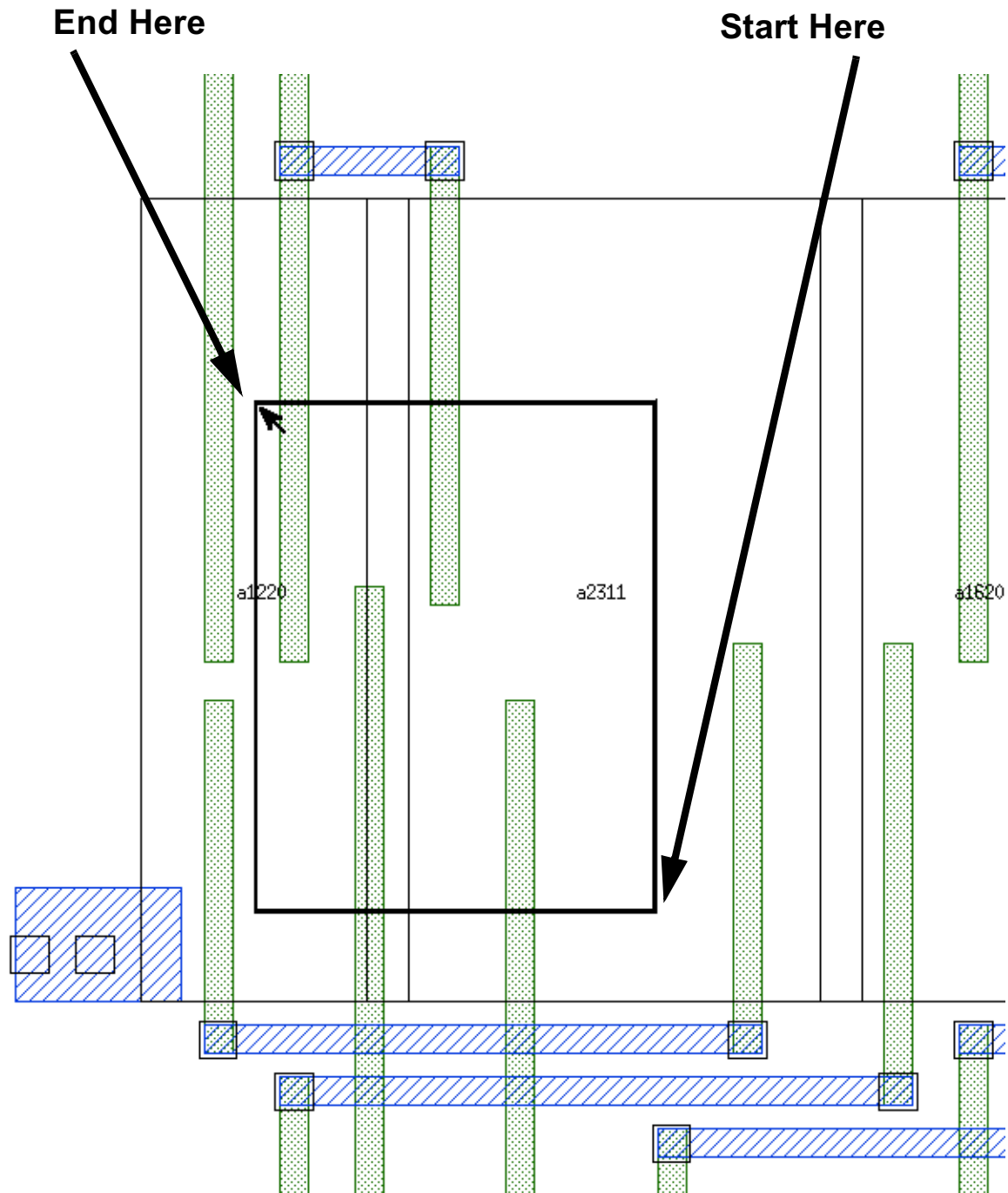
The size of the rectangle will determine how far the display zooms out. The smaller the rectangle, the more the display will zoom out.

The results may be similar to below.
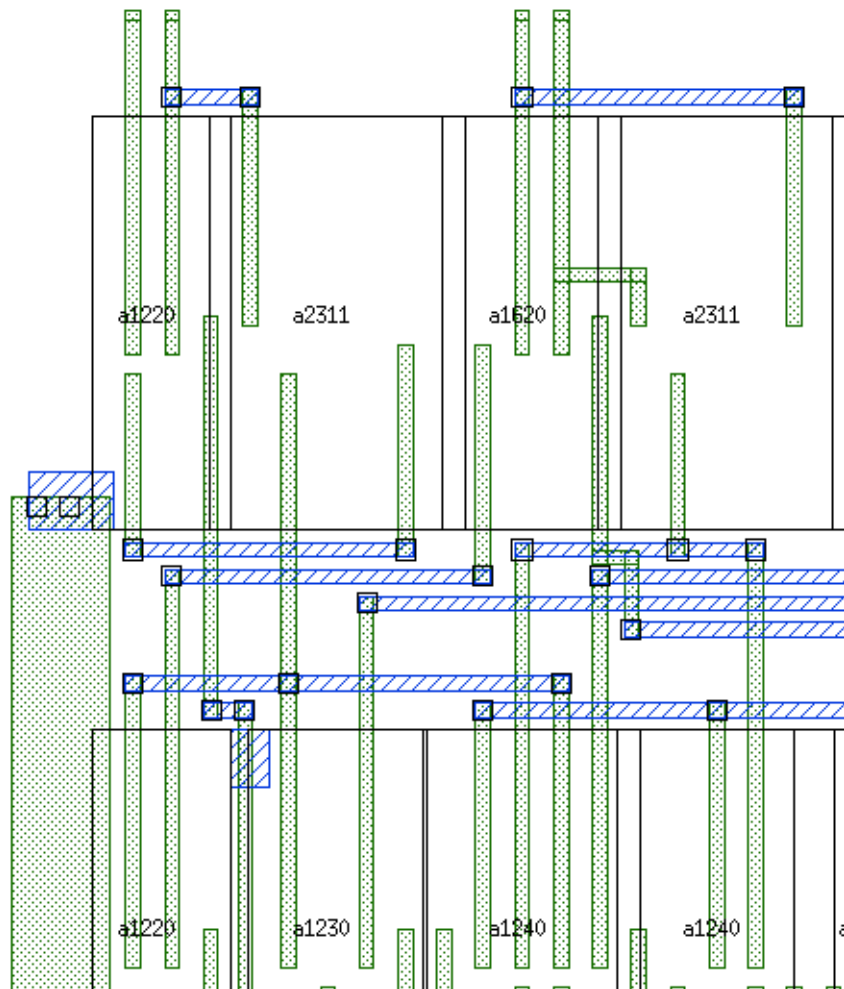
7. Centering the display:

    a. Place the cursor over the area you want to be the new center of the display.

    b. Click the MMB.
(If you only have a two-button mouse, click both buttons at the same time.)

The layout display re-centers itself around the new center.

8. Selecting Polygons:

    a. Choose the **Select** icon from the Toolbar Menu.
(Make sure the **Select** icon is selected.)

    b. Unselect all selection types except poly.

    c. Select any single item in the layout by clicking on it with the LMB.

The selected polygon will highlight.

9. Unselecting polygon(s):

    a. Choose the **Select** icon from the Toolbar Menu.
(Make sure the **Select** icon is selected.)

    b. Click the LMB in an empty area of the layout.

The unselected polygon will loose its highlight.

10. Selecting more than one polygon:

    a. Choose the **Select** icon from the Toolbar Menu.
(Make sure the **Select** icon is selected.)

    b. Hold down the CTRL key and click the LMB on the desired polygon.

The selected polygon will highlight.

    c. Repeat until you have selected all the desired polygons.

    The selected polygons will highlight as they are selected.

11. Unselecting just one polygon from a group of selected polygons:

    a. Choose the **Select** icon from the Toolbar Menu.
    (Make sure the **Select** icon is selected.)

    b. Hold down the CTRL key and click the LMB on the undesired polygon.

    The unselected polygon will loose its highlight.

12. Moving Polygons:

    a. Select the polygon(s).

    b. Choose the **Move** icon from the Toolbar Menu.

    c. Hold down the LMB.

    d. Drag the polygon(s) to their new location.

Note You do not need to have the cursor directly over the selected items to move them. The selected items will move relative to the cursor. Please experiment with this feature, so you understand how the move function operates.

    e. Release the LMB.
    Notice that your polygon(s) are still selected after the move operation.

    f. Undo the move by selecting Menu: Edit > Undo: Move.

For the rest of the steps in this exercise, you may want to work in an empty area of the layout.

13. Making a box:

    a. Choose the **Box** icon from the Toolbar Menu.

b. Select the desired layer from the layer palette.
   (The layer number highlights when selected.)

c. Click at a starting point for the box.

Start Here → □ ← **End Here**
45.200 by 28.900
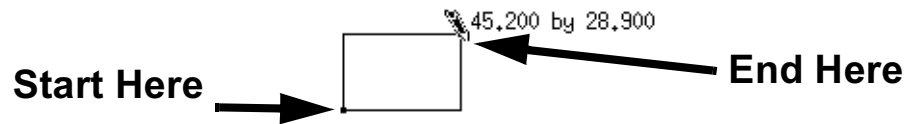
d. Click at the ending point. (Opposite diagonal)
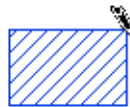
14. Making a polygon:

a. Choose the **Poly** icon from the Toolbar Menu.

b. Select the desired layer from the layer palette.
   (The layer number highlights when selected.)

c. Click at the starting point.

d. Click at each vertex.

End Here

95.600

Start Here
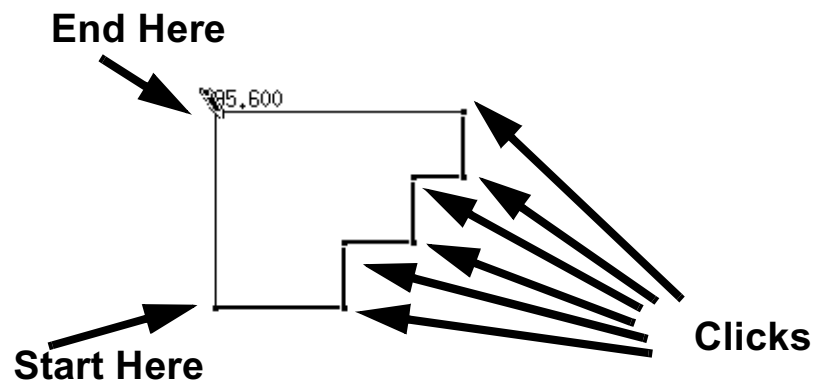
Clicks

e. Double-click to complete the polygon.

15. Making a new vertex:

   a. Choose the **Select** icon.

   b. Select the polygon.

   c. Choose the **Vertex** icon from the Toolbar Menu.

   d. Click on the desired segment.

      This highlights a segment of the polygon.

   e. Double-click in the location for the new vertex.
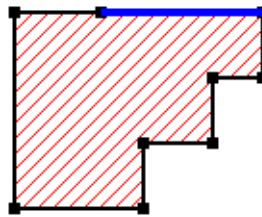
16. Change a shape by moving a segment (edge) of a polygon:

   a. Unselect everything.
      (Type "**u**".)

   b. Set the Select Mode Options so only **Edge** is selected.

   c. Select the **Move** icon from the Toolbar Menu.

   d. Click the LMB on the desired edge.

      The edge will highlight.

   e. Hold down the LMB.

   f. Drag the segment to the new location.
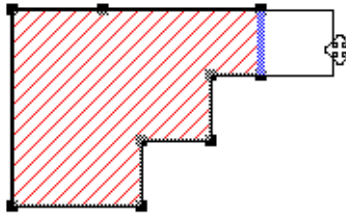
   g. Release the mouse button.

   h. Type "u" to unselect the edge.

17. Notching in an existing shape:

   a. Choose the **Select** icon.

   b. Set the select mode to **poly**.

   c. Select the polygon.

   d. Choose the **Notch** icon from the Toolbar Menu.

   e. Hold down the mouse button and draw a rectangle from RIGHT TO LEFT.

**Notch In
Right to Left**
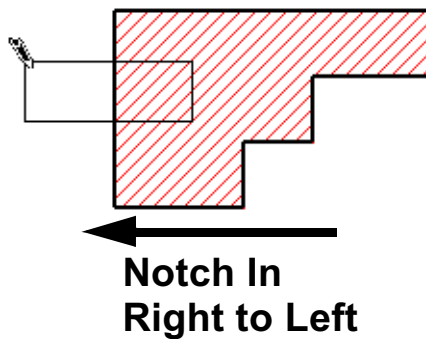
f. Release the mouse button.
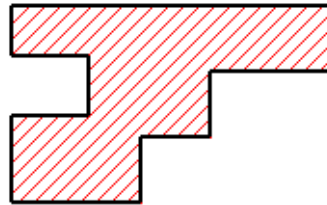
g. Unselect everything.

18. Notching out an existing shape:

a. Select the polygon.

b. Choose the **Notch** icon from the Toolbar Menu.
    (Should already be selected from the previous step.)

c. Hold down the mouse button and draw a rectangle from LEFT TO
    RIGHT.

**Notch Out
Left to Right**
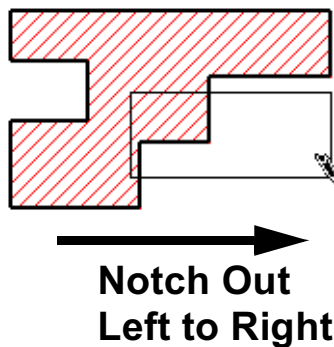
d. Release the mouse button.
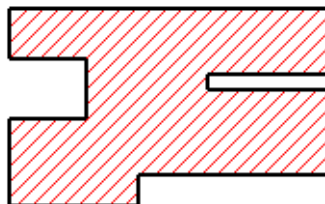
    e. Unselect everything.
       (Type "**u**".)

19. Changing the Grid.

    a. Choose **Menu: Options > Grid Settings**.

    b. Change the grid spacing to 0.001.

    c. Choose **Apply**.

    d. Choose **OK**.

20. Changing the Ruler.

    a. Choose **Menu: Options > Ruler**.

    b. Select Manhattan.

    c. Select Snap: Vertex/Edge.

       This will cause the ruler to "snap" to the edges and make it easier to measure polygons. You may want to change it to snap to grids when you are editing polygons to a certain size.

    d. Choose **Apply**.

    e. Choose **OK**.

21. Close all Calibre windows, so you will be ready for the next lab.
    (Do not save any files.)

Module 2
Calibre Rules 101: The SVRF

Objectives

At the completion of this lecture and lab you should be able to:

- Explain the SVRF format

- Explain basic DRC-type rules

- Explain basic LVS-type rules

- Identify the other types of rules and their function

- Use "golden" rule files

- Use conditional rules

What Does the SVRF Do?

What Does the SVRF Do?

Controls the following activities:

♦ **Provides specifications for run (data file names, etc.)**

♦ **Defines layers**

♦ **Generates derived layers**

♦ **Defines design RuleChecks**

♦ **Defines devices**

♦ **Defines/extracts connectivity**

♦ **Drives Layout vs. Schematic comparisons (using device recognition)**

♦ **Drives Parasitic Extraction (not covered in this class)**

♦ **Drives OPC/ORC (not covered in this class)**

Notes:

Defines layers: Allows you to assign a name to a layer number. A name makes troubleshooting easier.

One rule file can drive all Calibre applications, thus the addition of PEX and OPC/ORC information

What is the Syntax for Rule Statements?

Varies depending on operation:

- **Layer Definition**
  Example:
  LAYER metal1 10   // LAYER *name original_layer*

- **Layer Operation (DRC Check)**
  Example:
  INTERNAL oxide > 12 < 14

- **Specification Statement**
  Example:
  LVS REPORT name

- **Connectivity Definition/Extraction**
  Example:
  CONNECT layer1 layer2

Notes:

What is the Syntax for Rule Statements? (Cont.)

What is the Syntax for Rule Statements? (Cont.)

- **Design RuleChecks**

  EXAMPLE:
  MY_RULECHECK {
        @ Check for METAL1 line width < 5 um
        INTERNAL metal1 < 5
  }

- **Device Recognition**

  Example: Resistor named "res"

  DEVICE R res metal1 (pos) metal2 (neg) [1.1]
    // Resistor with resistivity defined at 1.1 Ohms/square

Notes:

Notice the two different types of comments.

// comments are "regular" comments.

@ comments will also appear in the Check Text window of RVE.

What about Case Sensitivity?

What about Case Sensitivity?

- ◆ **By default, all uppercase letters are converted to lowercase for internal purposes (you can define as needed)**
- ◆ **Keywords are always case-insensitive**
- ◆ **Names are case-insensitive unless used for cell or file names**
- ◆ **Layer names, RuleCheck names, etc., are always case-insensitive**
- ◆ **File names are always case-sensitive (UNIX)**
- ◆ **User defines case sensitivity in Calibre**
  - ● **LAYOUT CASE
    Specifies whether the layout should be processed in a case-sensitive manner**
  - ● **SOURCE CASE
    Specifies whether the source should be processed in a case-sensitive manner**
  - ● **LVS COMPARE CASE
    Controls case sensitivity in the LVS circuit comparison stage**

Notes:

SOURCE CASE Example:

- Original name: Reset

- If SOURCE CASE yes, then Reset.

- If SOURCE CASE no, then reset.

Is Rule Order Important?

Is Rule Order Important?

♦ **Rules are order-independent**

♦ **Most operations within rules are order independent**

♦ **All of the following statements are equivalent:**
  ● **area < 4 contact**
  ● **contact area < 4**
  ● **area contact < 4**
  ● **< 4 area contact**
  ● **< 4 contact area**
  ● **contact < 4 area**

♦ **A few operations are order dependent**
  (The SVRF Manual will always flag order-dependence)

♦ **The following statements are NOT equivalent:**
  ● **contact inside metal**
  ● **metal inside contact**

Notes:

Using Calibre with DESIGNrev
June 2004

What are Conditional Rules?

What are Conditional Rules?

- ◆ **Rules are only run if a "condition" is met**

- ◆ **Can "loosen" or "tighten" specifications**

- ◆ **For Example:**
  How can I make different metals the top layer depending on the process?

- ◆ **Rule execution can be controlled via environment variables**

- ◆ **Generally, don't use conditional rules for the final tape out**

Notes:

How to use Conditional Rules

How to use Conditional Rules

- ♦ **Example: P1, P2, and P3 are different processes.**
- ♦ **Only one is defined as an environment variable at a time.**
- ♦ **Different metal layers become the "top_layer" depending on the process.**
- ♦ **If no process is defined, P3 is the default.**

```
#ifdef $P1
LAYER top_metal metal6
#else
        #ifdef $P2
        LAYER top_metal metal5
        #else
                LAYER top_metal metal4      // implies using P3
        #endif
#endif
```

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Notes:

It is not the value of an environment variable that is important, it is if the environment variable is set at all. Using the above example, setting $P1 to "off" or "no" will not change to process 2 or 3.

Rule Efficiency

Rule Efficiency

- ◆ **As in programming, DRC rules can be written in several ways, leading to more or less efficiency.**
- ◆ **Rule efficiency can be achieved through various means:**
  - ● **Data reduction (minimize data "fed into" a RuleCheck)**
  - ● **Concurrency**
  - ● **Using unique rule features**
  - ● **Other techniques (conditional execution, rule sequencing, etc.)**
- ◆ **Concurrency example:**

OK	**Better**
regular_contact = **contact** outside **pad**	regular_contact = **contact** outside **pad**
pad_contact = **contact** not **regular_contact**	pad_contact = **contact** not outside **pad**

Different layers used in each rule: Rules run sequentially

Same layers used in both rules: Rules run concurrently

Notes:

Unique Features Example

Unique Features Example

OK
ENCLOSURE Cont M1 < 2
NOT INSIDE Cont M1

BETTER
ENCLOSURE Cont M1 < 2 OUTSIDE ALSO

Poly

M1

Cont

Notes:

Using Calibre with DESIGNrev
June 2004
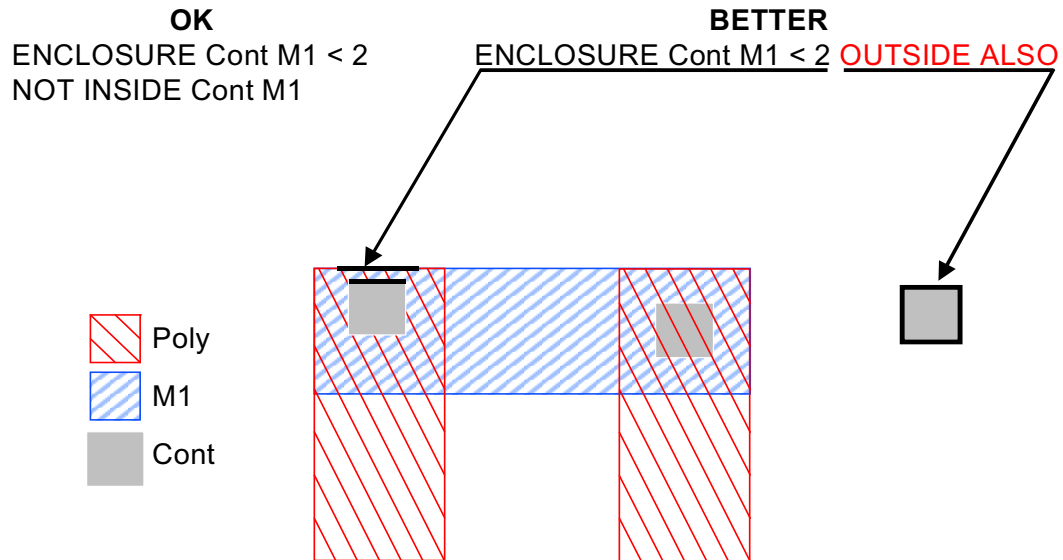
Data Reduction Example

Data Reduction Example

Speed up DRC by reducing data fed into individual checks

OK:

```
A = SIZE M1 BY -5
WIDEM1 = SIZE A BY 5
B = SIZE M1 BY -40
PADM1 = SIZE B BY 40
```

Process
all of M1 twice

Better:

```
A = SIZE M1 BY -5
WIDEM1 = SIZE A BY 5
B = SIZE WIDEM1 BY -40
PADM1 = SIZE B BY 40
```

Process all
of M1 once

Process a
subset of M1
(WIDEM1)
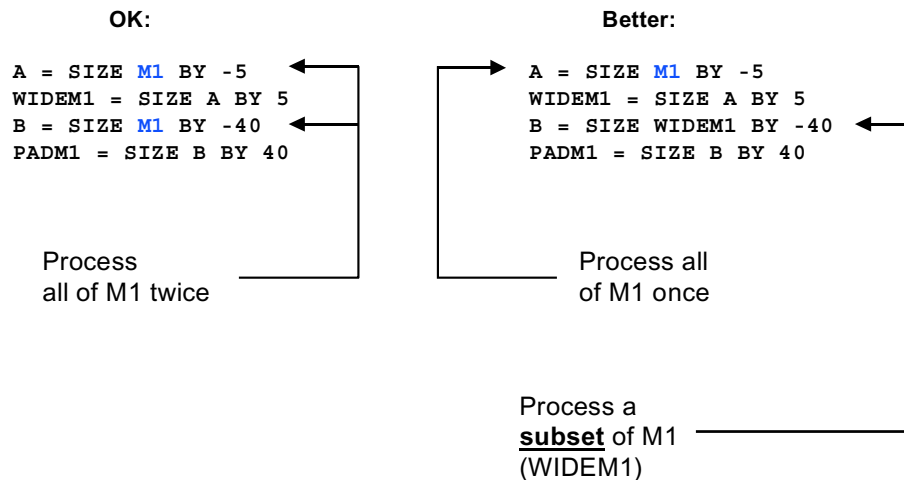
Notes:

This example is not a trade off between rule concurrency and rule efficiency. Size
is not one of the operations that can run concurrently.

Combining Data Reduction and Unique Features Example

Combining Data Reduction and Unique Features Example

Can get even better results by using all available techniques

OK:

```
A = SIZE M1 BY -5
WIDEM1 = SIZE A BY 5
B = SIZE M1 BY -40
PADM1 = SIZE B BY 40
```

Better:

```
A = SIZE M1 BY -5
WIDEM1 = SIZE A BY 5
B = SIZE WIDEM1 BY -40
PADM1 = SIZE B BY 40
```

Best:

```
WIDEM1 = SIZE M1 BY 5 UNDEROVER
PADM1 = SIZE WIDEM1 BY 40 UNDEROVER
```

Notes:

Using Calibre with DESIGNrev
June 2004

Including Other Rule Files

Including Other Rule Files

♦ **Why would I have more than one rule file?**

- ● **Should not edit "golden" rule file from the factory**

- ● **Want to check beyond factory spec**

♦ **INCLUDE statement allows you to use rules from the factory and include your own checks in one file**

♦ **For example:**

```
SOURCE PATH D3.spi
LAYOUT PATH D3.gds
LVS REPORT lvs.rpt
MASK SVDB DIRECTORY svdb QUERY
My_Rule_1 {
 .
 }
.
.
INCLUDE "/factory/ruleset_1.1"
```

2-15 • Using Calibre: Calibre Rules 101: The SVRF   Copyright © 2004 Mentor Graphics Corporation

Notes:

What Does it Mean that Calibre is an "Edge-Based" Tool?

What Does it Mean that Calibre is an "Edge-Based" Tool?

- **Calibre DRC uses edges, not polygons**

- **Edges with the violation highlight in the layout**

Error is between these edges

Notes:

Using Calibre with DESIGNrev
June 2004
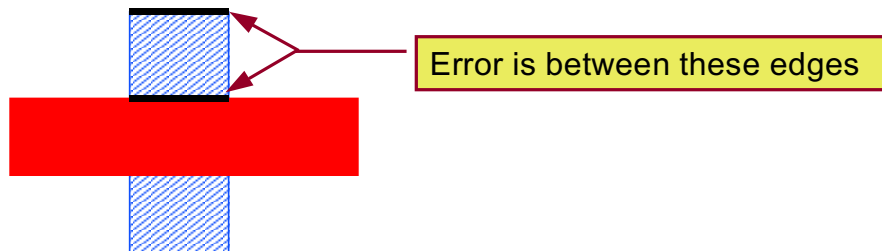
Why Does Calibre Only Highlight Part of an Edge?

Why Does Calibre Only Highlight Part of an Edge?

♦ **Calibre only highlights the part of the edge in violation**
♦ **You specify the edge checking option**
  ● **Euclidean (default)**
  ● **Square**
  ● **Opposite**

`INT OXIDE POLY < 3 OPPOSITE`

`INT OXIDE POLY < 3`
`//EUCLIDEAN METRIC`

`INT OXIDE POLY < 3 SQUARE`

3

Notes:

What are Typical DRC Rules?

What are Typical DRC Rules?

- ◆ **Internal**
  - ● **Width**
  - ● **Overlap**
- ◆ **External**
- ◆ **Enclosure**
- ◆ **Extension**

NOTE: The above are dimensional RuleChecks.
   There are other types.

Notes:

Using Calibre with DESIGNrev
June 2004

Width Checks

Width Checks

♦ **Width checks are internal checks on polygons on a single input layer**

♦ **Width checks are measured between interior-facing edge pairs on the same polygon**
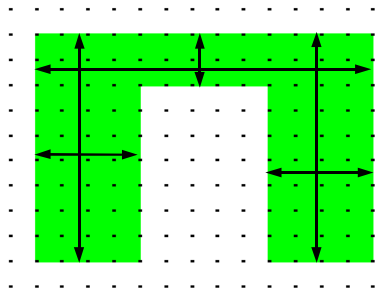
Notes:

Interior-Facing Edge Checks

Interior-Facing Edge Checks

Internal RuleChecks apply only to interior-facing edge pairs

interior-facing edge pair (two layer)

interior-facing edge pair (single layer)

Notes:

Using Calibre with DESIGNrev
June 2004
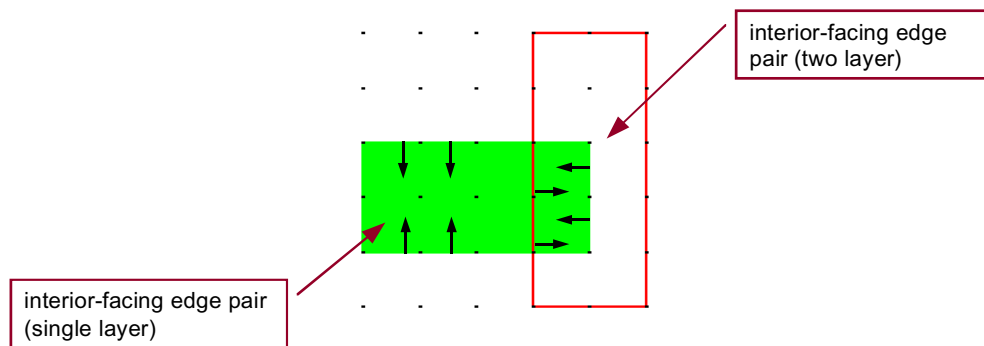
Overlap Checks

Overlap Checks

Overlap checks are checks between interior-facing edge pairs of polygons on two different layers

```
OXIDE



POLY
```
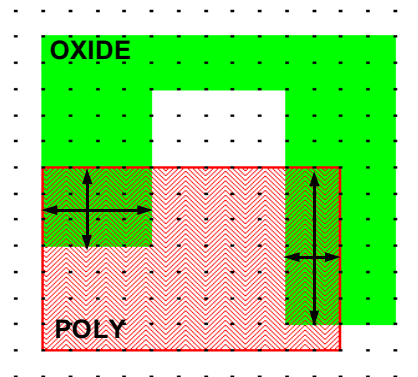
`INT OXIDE POLY <=3`

Notes:

Exterior-Facing Edge Checks

Exterior-Facing Edge Checks

External RuleChecks apply only to exterior-facing edge pairs

exterior-facing edge
pair (two layers)

exterior-facing edge
pairs (single layer)

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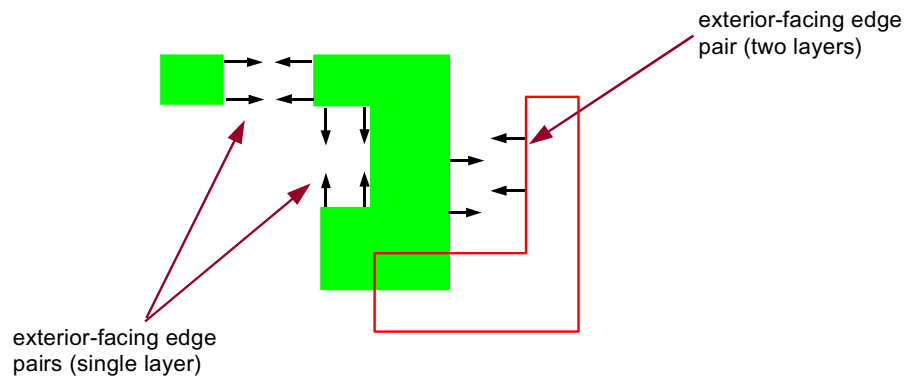
Notes:

External Checks

External Checks
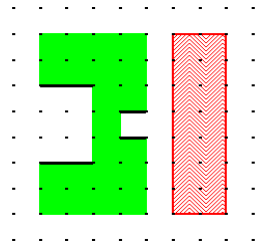
EXT OXIDE <= 3
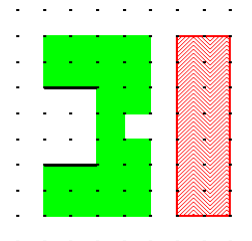
EXT OXIDE > 1 <= 3
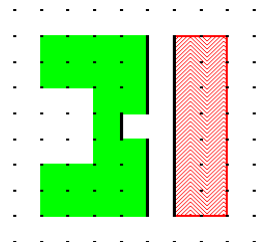
EXT OXIDE POLY <= 2
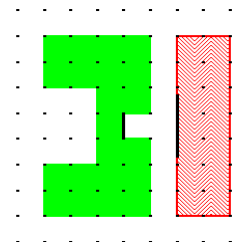
EXT OXIDE POLY >1 <= 2

Notes:

Enclosure and Extension Checks

Enclosure and Extension Checks

extension edge pairs
of poly over oxide

enclosure edge pairs
of oxide over poly

Notes:

Using Calibre with DESIGNrev
June 2004
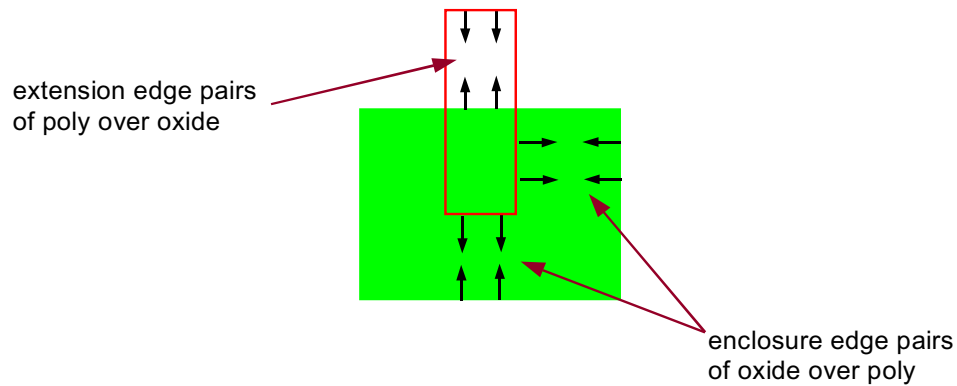
Examples of Enclosure Checks

Examples of Enclosure Checks

- ♦ **Notice the significance of switching the layer order in the first two examples**

ENC OXIDE POLY < 4   ENC POLY OXIDE < 4   ENC METAL1 POLY < 2

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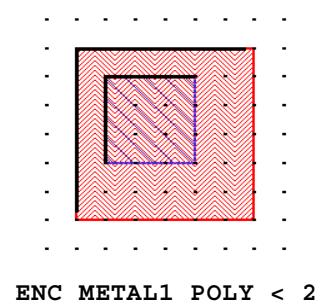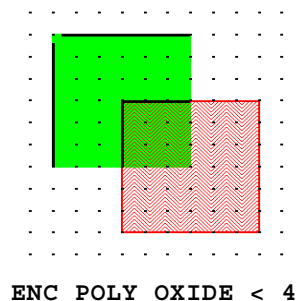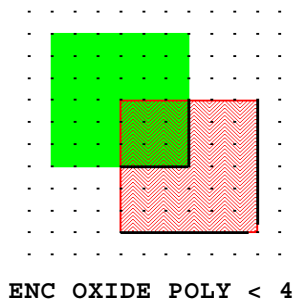
Notes:

What are Typical LVS Rules?

What are Typical LVS Rules?

- **Device Statements**
  - **device mn ngate ipoly nsd nsd s_pwell [0]**
  - **device r(pl) rpoly ipoly ipoly [20000]**
- **Gate Recognition Statements**
  - **LVS GROUND NAME VSS VSS1**
  - **LVS POWER NAME VDD VCC**
  - **LVS RECOGNIZE GATES ALL**

Notes:

Using Calibre with DESIGNrev
June 2004

Fundamental Ideas of Device Recognition

Fundamental Ideas of Device Recognition

Device recognition:

♦ **Identifies instances of devices from layout geometry**

♦ **Computes specified properties of device instances**

♦ **Prepares results of device computations for other processes such as LVS comparison or parasitic extraction**

References:

More information on device recognition is covered in Module 9 Device Recognition.

Notes:

Built-In Device Definitions

Built-In Device Definitions

The following devices have built-in device definitions:

- ♦ **MOS Transistor (M MN MP MD ME)**
- ♦ **Diode (D)**
- ♦ **Capacitor (C)**
- ♦ **Resistor (R)**
- ♦ **Bipolar Transistor (Q)**

Notes:

CMOS Device Example

CMOS Device Example

total perimeter of
NSD pins
touching the
gate region

gate

NSD   NSD
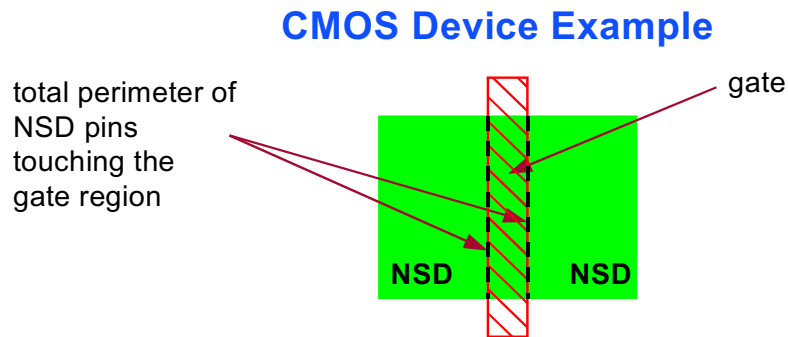
DEV MN (NMOS) GATE GATE(G) NSD(S) NSD(D) PWELL(B) [0.5]

//N-TYPE TRANSISTOR OF MODEL NMOS

//weffect PROPERTY SPECIFICATION OF 0.5 FOR BENT GATES

- ♦ **Length and width are properties computed for MOS transistors by default (in meters)**

- ♦ **Width, "W", is taken as half the total perimeter of NSD pins touching the gate region**

- ♦ **Length, "L", is calculated as gate area divided by width**

Notes:

What Other Types of Rules are There?

What Other Types of Rules are There?

- **Specification**
  LAYOUT SYSTEM, LAYOUT PATH, LAYOUT PRIMARY

- **Connectivity**
  STAMP, CONNECT, SCONNECT, TEXTING

- **Hierarchical**
  FLATTEN CELL, INSIDE CELL

- **Control**
  INCLUDE, Conditional Rules, Grouping Rules

Notes:

Lab Information

Lab Information

In this lab you will:

- **See how various Calibre DRC rules operate**
  - **Width**
  - **Internal**
  - **External**
  - **Enclosure**
- **Learn how to use Calibre RVE and DESIGNrev**
- **Learn how to highlight errors in DESIGNrev**
- **Learn how to use conditional rules**

Notes:

Lab: Calibre Rules 101

Introduction

In this lab, you will take a closer look at the rules in a rule file, view the results generated, and even write some rules of your own.

Imagine you have been assigned the task to verify the layout of the "a1220" NAND cell used in the lab1 chip. Your starting point is the GDS file containing the layout data for the cell and a "golden" rule file which contains the DRC rules specific to the processing technology that will be used to fabricate the design. In the first exercise, you will invoke Calibre DRC from within the layout editor after loading the nand cell layout. At the completion of the DRC run, you will invoke RVE to cross-probe the DRC results into the layout. In the second exercise, you will change the failure criteria for one of the rules by setting an environment variable and then re-run the DRC check to see the impact of the change. In the third exercise, you will write two DRC rules related to minimum transistor size and then run Calibre DRC one more time, noting the results and cross-probing them into the layout.

List of Exercises

Exercise 2-1: Load a Design & Prepare for DRC

Exercise 2-2: Run DRC

Exercise 2-3: Write Transistor Checks

Exercise 2-1: Load a Design & Prepare for DRC

In this exercise you will invoke DESIGNrev from the command line, load the palette, load a GDSII design and review the rule file which will be used for the DRC run.

1. From a UNIX shell, change your directory to "lab2".
   ```
   cd $HOME/using_calbr/lab2
   ```

2. List the contents of the lab2 directory.
   ```
   ls
   ```

   You should see at a minimum the following files:

   - a1220.gds

   - lab2_rules

   - lab2_runset.txt

   - layer_props.txt

   If any of these files are missing, please double check that you are in the correct directory, and then notify your instructor.

3. Launch DESIGNrev.
   ```
   $MGC_HOME/bin/calibredrv
   ```

   This will open the initial DESIGNrev window.

   Next you will load the GSDII file.

4. Choose **Menu: File > Open Layout**.

5. Select file **a1220.gds**.

6. Choose **OPEN**.

   This loads the layout design you will be using for this lab.

7. Load the layer properties. (**Menu: Layer > Load Layer Properties**)

8. Select the **layer_props.txt** file.

9. Choose **Open** to execute the dialog box.

   This loads the layer properties.

   The DESIGNrev window should look similar to below.
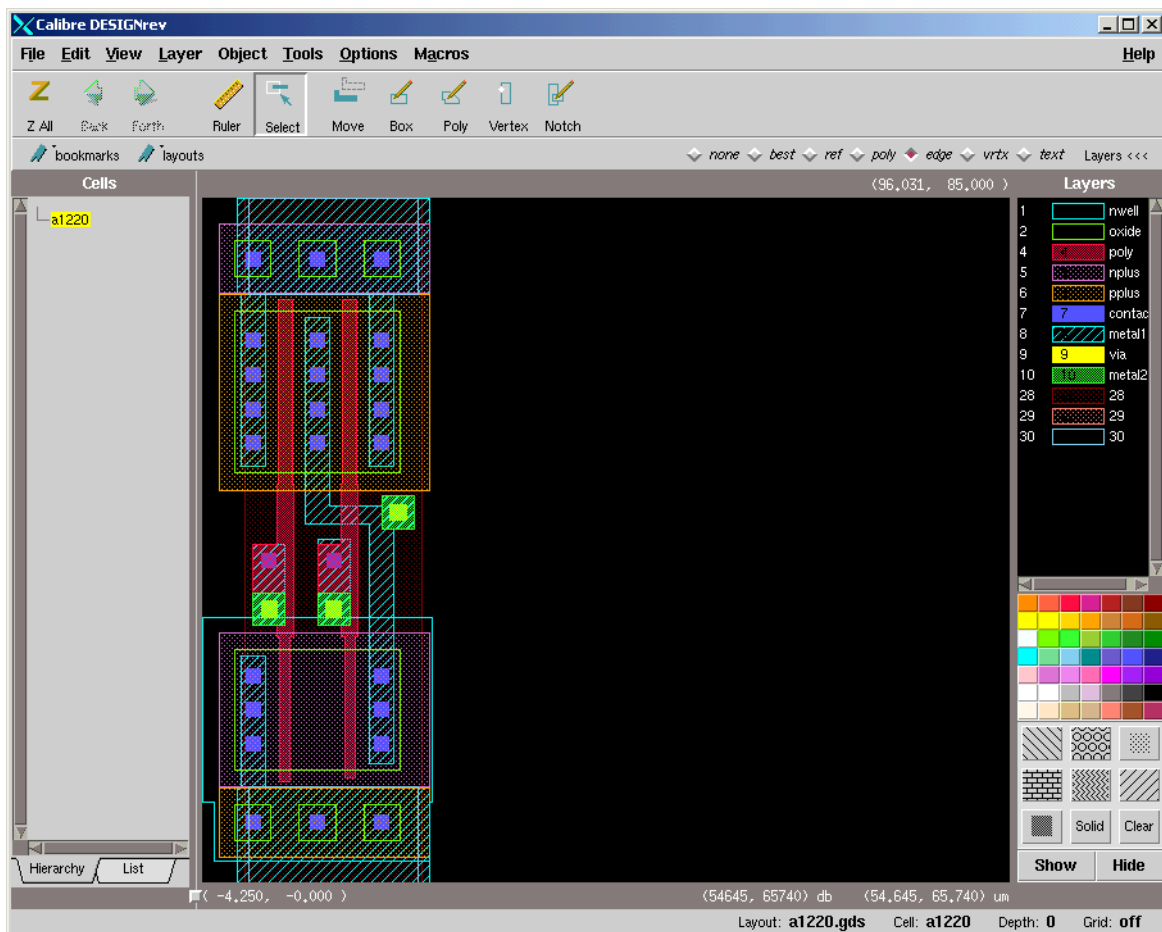
10. From DESIGNrev, choose **Menu: Tools > Calibre Interactive**.

This opens the Calibre Interactive Server dialog box.
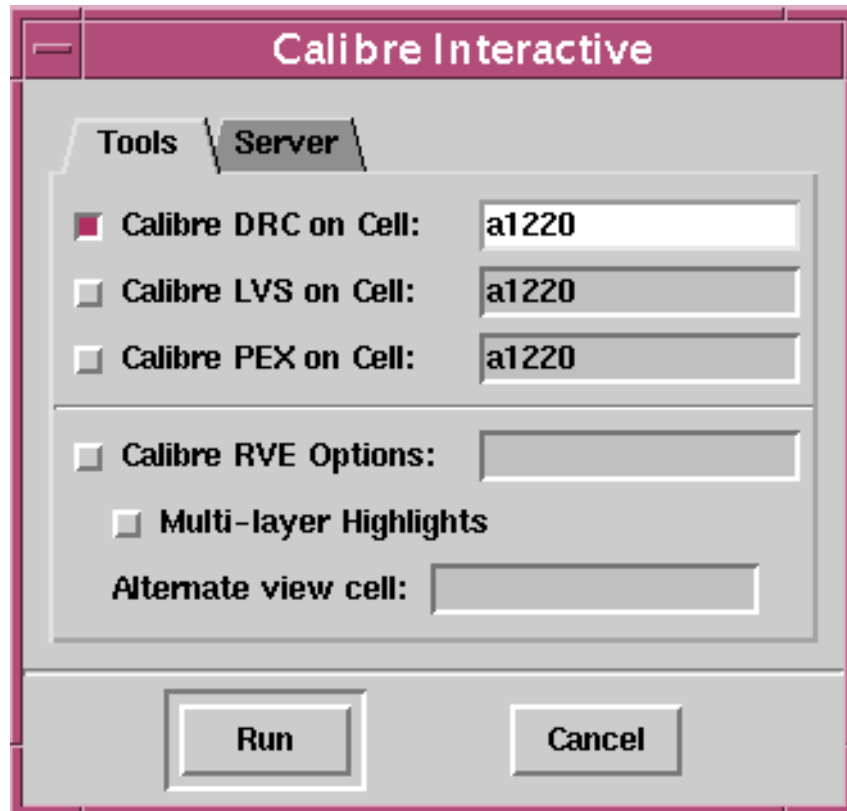
11. Select **Calibre DRC**.

12. Leave the socket as the default number (unless the instructor tells you otherwise).

13. Check that the cell name is "a1220".

14. (Optional) Select Multi-layer Highlights.
    If you choose this option each of your "Discrepancy" highlights will appear on a different layer (a different color) in the GDS file.

15. Choose **Run** to execute the dialog box.

    Both the Calibre Interactive - DRC window and the Choose Runset File dialog box open.

16. Enter "lab2_runset.txt" as the runset file path.
    (You can use the **"..." Browse** button to locate the file name in the lab2 directory.)

17. Choose **OK** to execute the dialog box.

    The Calibre Interactive DRC window opens with the **Inputs** menu button selected. The Calibre Interactive DRC window will now look like this:
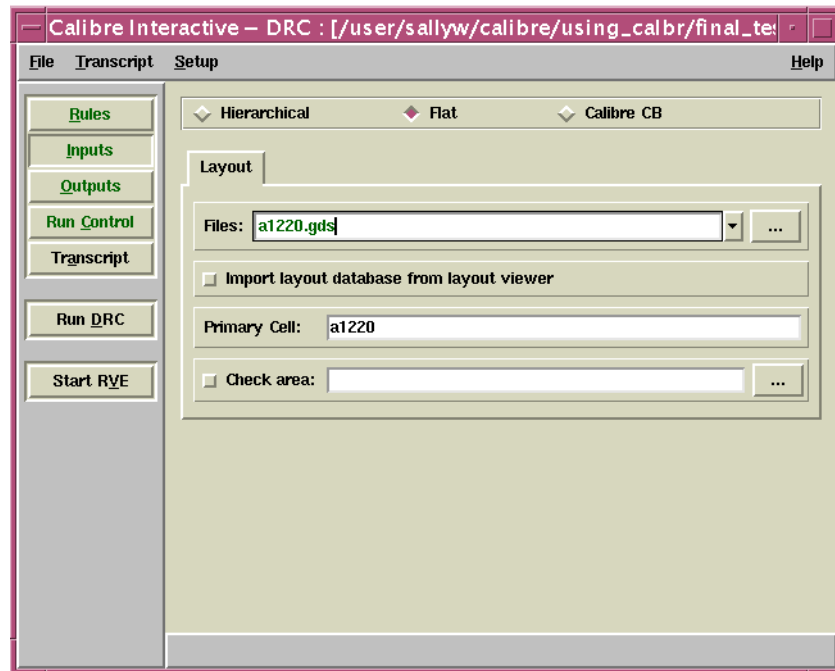
    We will now take a closer look at the rule file.

18. Click on the **Rules** menu button.

    This will display the Rules frame in the Calibre Interactive window. File "lab2_rules" should already be specified in the "Calibre-DRC rule file" field (if not, use the browser to select the file).

19. Choose **View**.
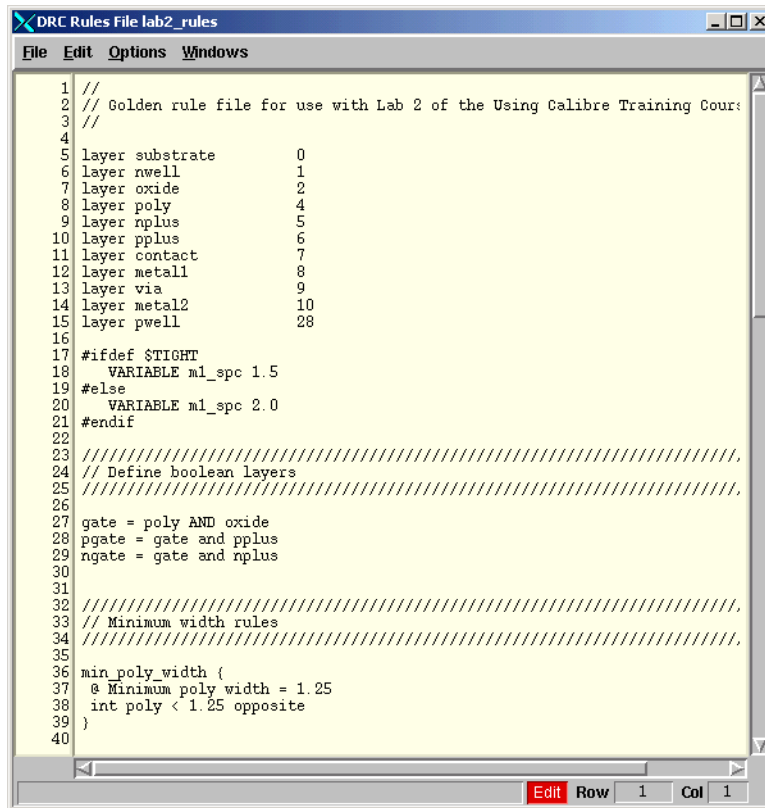
    This will open a text window displaying the lab2_rules file.

20. In the text window, choose **Menu: > Options > Line Numbers**.

This will add line numbers to the text display. The text window will now look like this:

```
X DRC Rules File lab2_rules                                    _ □ X
File  Edit  Options  Windows
     1 //
     2 // Golden rule file for use with Lab 2 of the Using Calibre Training Cours
     3 //
     4
     5 layer substrate        0
     6 layer nwell            1
     7 layer oxide            2
     8 layer poly             4
     9 layer nplus            5
    10 layer pplus            6
    11 layer contact          7
    12 layer metal1           8
    13 layer via              9
    14 layer metal2           10
    15 layer pwell            28
    16
    17 #ifdef $TIGHT
    18     VARIABLE m1_spc 1.5
    19 #else
    20     VARIABLE m1_spc 2.0
    21 #endif
    22
    23 //////////////////////////////////////////////////////////////////////
    24 // Define boolean layers
    25 //////////////////////////////////////////////////////////////////////
    26
    27 gate = poly AND oxide
    28 pgate = gate and pplus
    29 ngate = gate and nplus
    30
    31
    32 //////////////////////////////////////////////////////////////////////
    33 // Minimum width rules
    34 //////////////////////////////////////////////////////////////////////
    35
    36 min_poly_width {
    37  @ Minimum poly width = 1.25
    38  int poly < 1.25 opposite
    39 }
    40
                                                Edit  Row  1    Col  1
```

Study the rule file carefully to answer the following questions.

Which line numbers provide names for original GDS layers?

_____

If the environment variable $TIGHT is not defined, what is the minimum allowed metal1 external spacing?

_____

How many overlap checks appear in this rule file?

_____

What do you think the derived boolean layers will ultimately be used for?

_____

21. Choose **Menu: File > Close** to close the rule file text window.

Exercise 2-2: Run DRC

We will now run the DRC check and cross-probe the results into the layout viewer (DESIGNrev).

1. In the Calibre Interactive DRC window, choose the **Run DRC** menu button.

   When the run completes, the Transcript window will look similar to below:
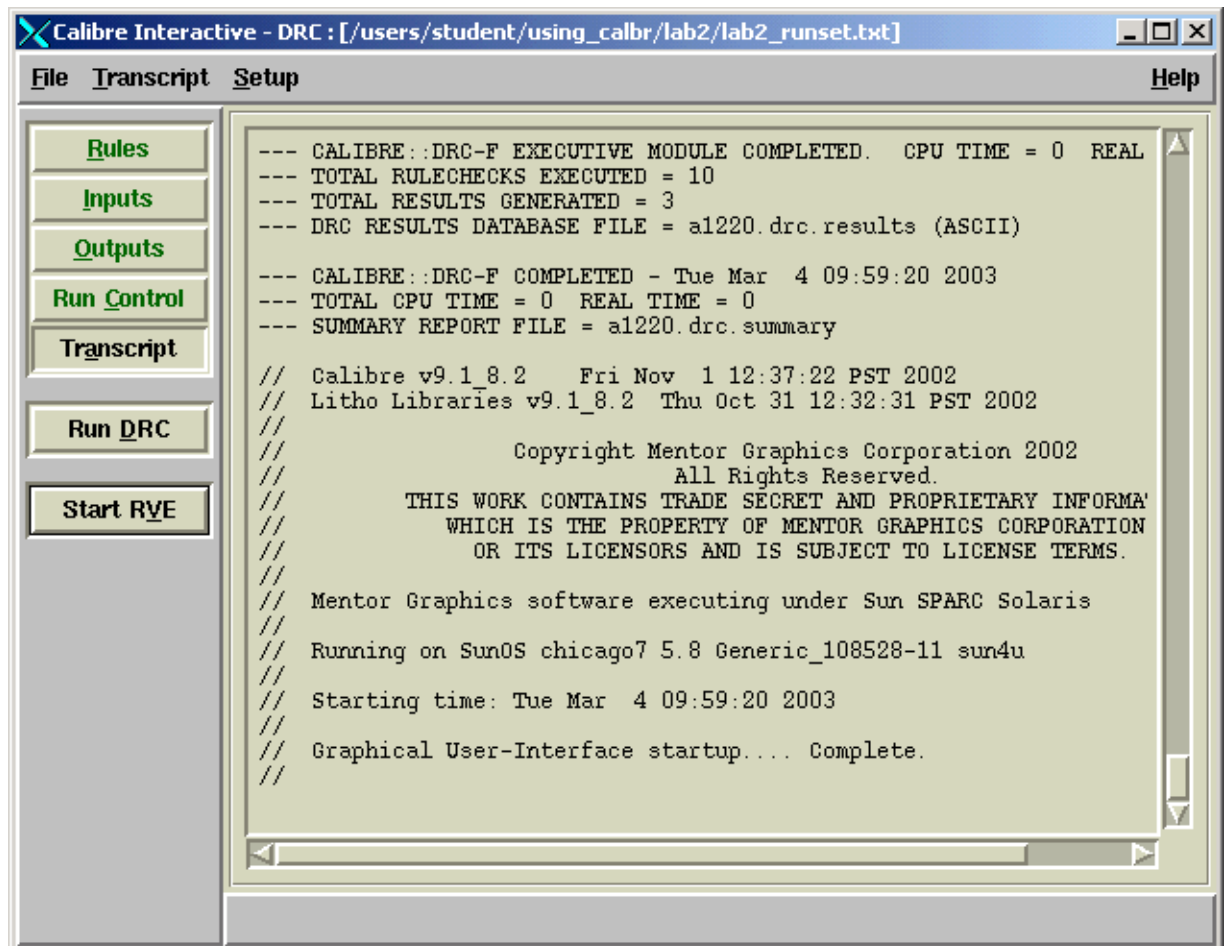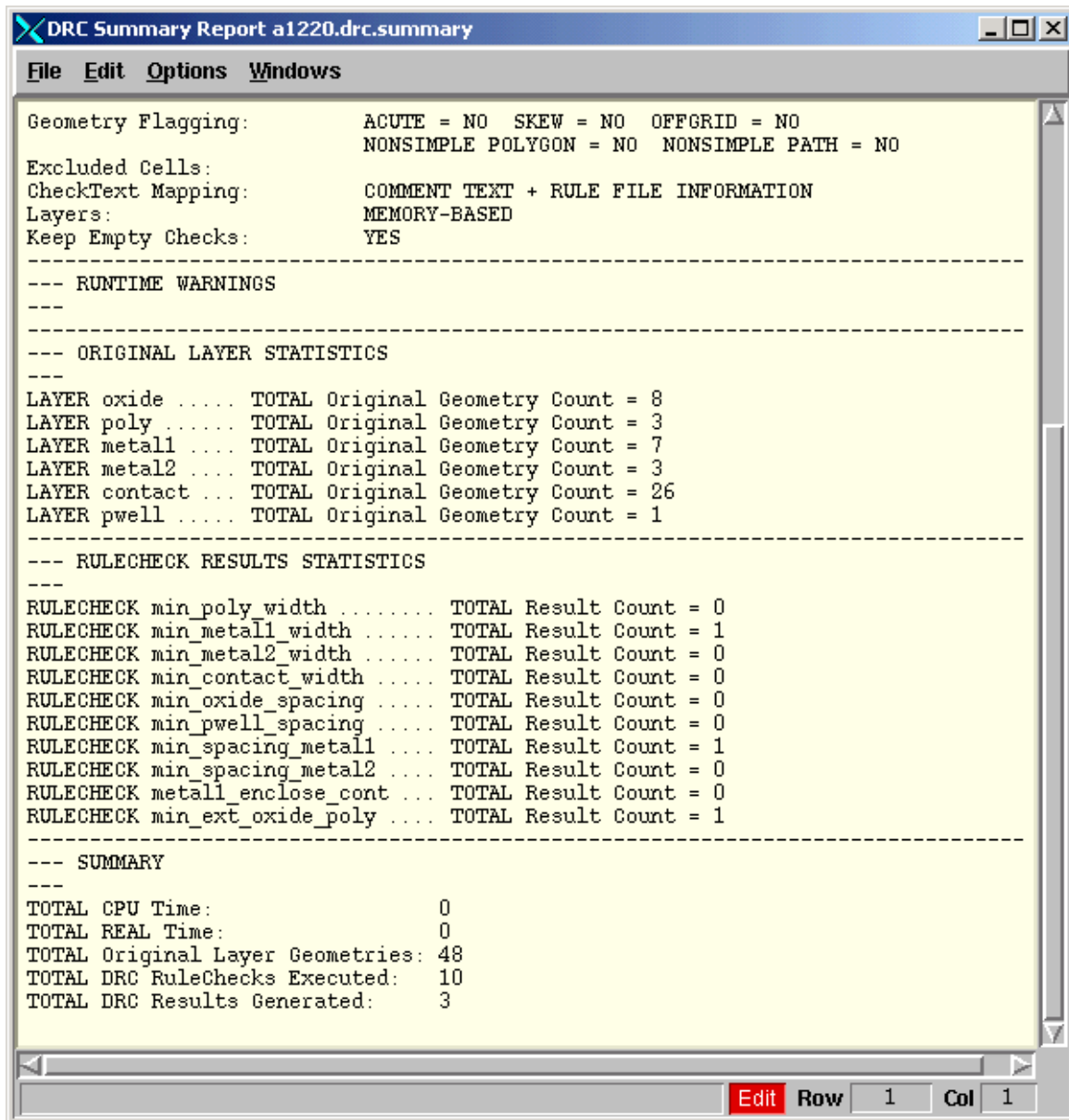
   The top several lines indicate successful DRC completion and document the number of discrepancies found.

2. Make the DRC Summary window active by selecting it.

3. Scroll down to the end of the report to display the "RULECHECK RESULTS STATISTICS" section.

The report window should look similar to below:

```
DRC Summary Report a1220.drc.summary                              _ □ ×

File  Edit  Options  Windows

Geometry Flagging:          ACUTE = NO   SKEW = NO   OFFGRID = NO
                            NONSIMPLE POLYGON = NO   NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:          COMMENT TEXT + RULE FILE INFORMATION
Layers:                     MEMORY-BASED
Keep Empty Checks:          YES
-----------------------------------------------------------------------
--- RUNTIME WARNINGS
---
-----------------------------------------------------------------------
--- ORIGINAL LAYER STATISTICS
---
LAYER oxide .....  TOTAL Original Geometry Count = 8
LAYER poly ......  TOTAL Original Geometry Count = 3
LAYER metal1 ....  TOTAL Original Geometry Count = 7
LAYER metal2 ....  TOTAL Original Geometry Count = 3
LAYER contact ...  TOTAL Original Geometry Count = 26
LAYER pwell .....  TOTAL Original Geometry Count = 1
-----------------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK min_poly_width ........  TOTAL Result Count = 0
RULECHECK min_metal1_width ......  TOTAL Result Count = 1
RULECHECK min_metal2_width .....   TOTAL Result Count = 0
RULECHECK min_contact_width .....  TOTAL Result Count = 0
RULECHECK min_oxide_spacing .....  TOTAL Result Count = 0
RULECHECK min_pwell_spacing .....  TOTAL Result Count = 0
RULECHECK min_spacing_metal1 ....  TOTAL Result Count = 1
RULECHECK min_spacing_metal2 ....  TOTAL Result Count = 0
RULECHECK metal1_enclose_cont ...  TOTAL Result Count = 0
RULECHECK min_ext_oxide_poly ....  TOTAL Result Count = 1
-----------------------------------------------------------------------
--- SUMMARY
---
TOTAL CPU Time:             0
TOTAL REAL Time:            0
TOTAL Original Layer Geometries: 48
TOTAL DRC RuleChecks Executed:   10
TOTAL DRC Results Generated:     3

                                            Edit  Row  1   Col  1
```

Note that rules "min_metal1_width," "min_spacing_metal1" and "min_ext_oxide_poly" all had one violation each.

4. When you are finished viewing the report, close the report window.
   (Choose **Menu: File > Close**.)

   We will now open Calibre RVE to cross-probe these results into the layout.

5. Make the RVE window active.

6. Choose **Menu: View > By Check**.

   The RVE window will look similar to below:
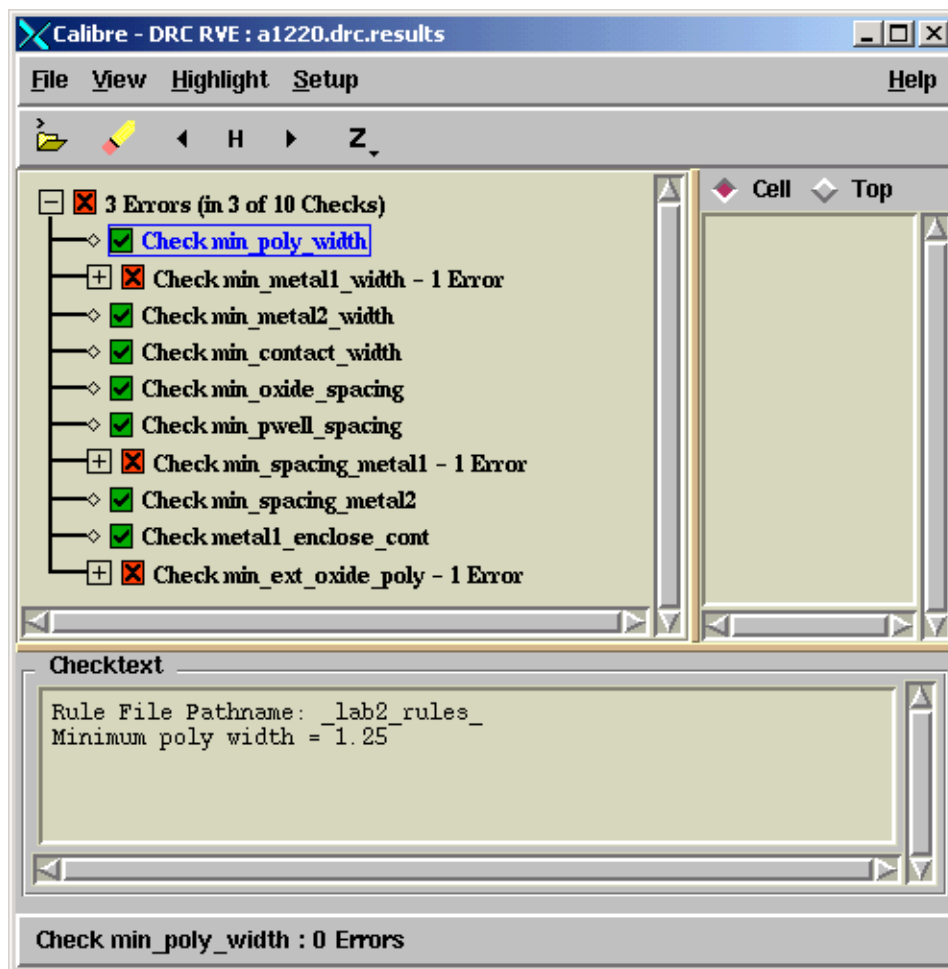
   Note that all rules are listed and the ones involved in violations are
   preceded by a red "X." Since the cell layout fits completely within the
   DESIGNrev edit window, we are going to instruct RVE to maintain our
   DESIGNrev window size as we display each of the violations. In larger

designs, we would take advantage of RVE's ability to zoom a viewing window around each violation as it is displayed.

Note If you would prefer to only see rulecheck that have errors (rather than all rulechecks that were run), you can choose **Menu: View > Error Checks Only**.

7. Choose **Toolbar: Z > No view change**.

8. Choose **Toolbar: Z > Clear existing highlights** in the RVE window:
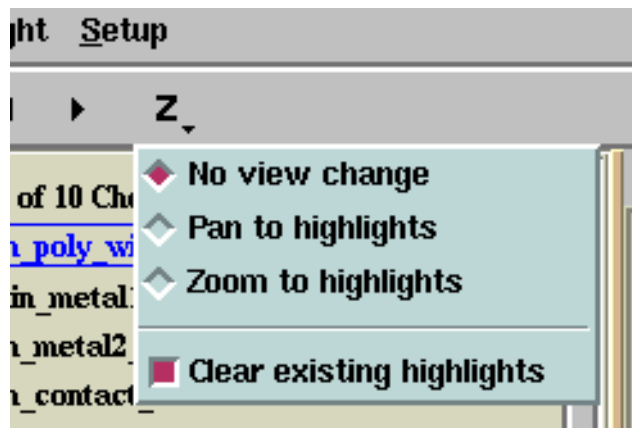
Now we are ready to cross-probe the results into the layout viewer. In preparation for this step, grab the RVE window by its title bar and position the window to the right of the cell layout display in the layout edit window so that you have a clear view of all cell geometries.

9. Click on the "min_metal1_width" RuleCheck.

The text will turn blue to indicate that this rule has been selected. You'll also see a description of this rule appear in the Checktext frame at the bottom of the RVE window.

10. Choose **Toolbar: H** to highlight the minimum metal1 width violation in the layout.

Two highlight bars will appear in the layout documenting the location of the violation.
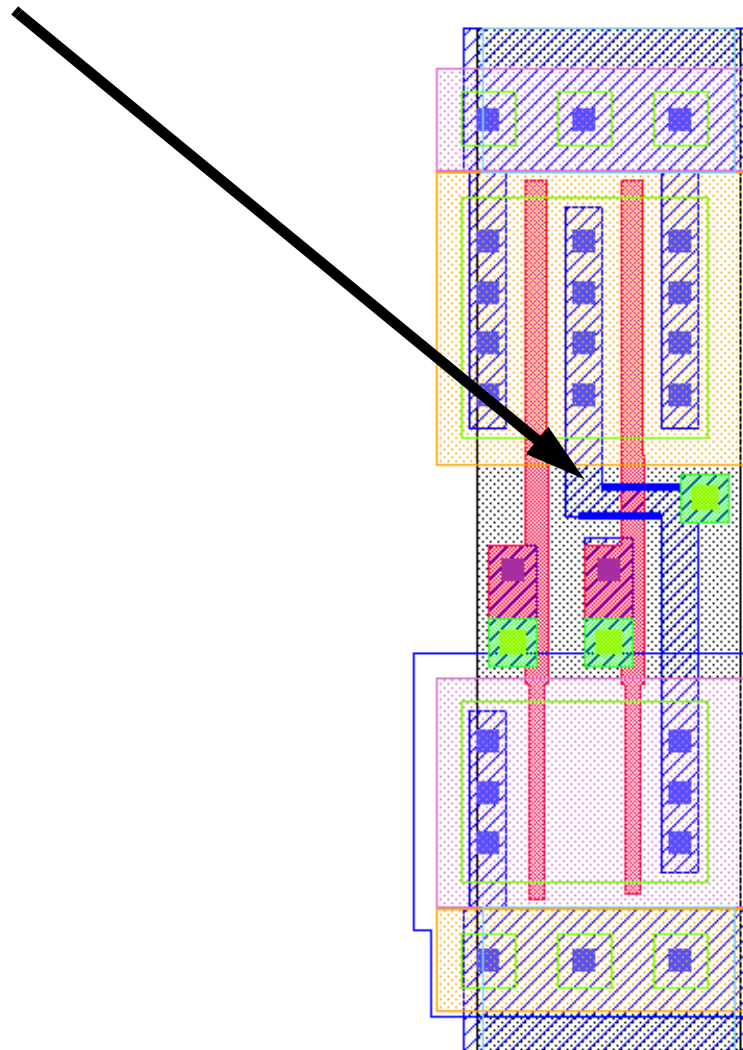
Why doesn't the lower highlight bar cover the entire metal edge it lies on?

_____

11. Follow the procedure outlined above to highlight the minimum metal1 spacing and minimum poly-oxide extension violations.

12. Click on the **eraser icon** in the toolbar to clear all highlights.

Now that we've seen an overview of where all of our violations are, we'll use RVE's ability to zoom the viewing window to take a closer look at the minimum metal1 spacing violation.

13. Choose **Menu: Setup > Options**.

    This will open the "Setup DRC - RVE Options" window.

14. In the options window, choose the **Highlight** tab.

15. Select the **Zoom cell view to highlights by** option button.

16. Enter 0.5 as the zoom factor.

    The options window will now look like this:
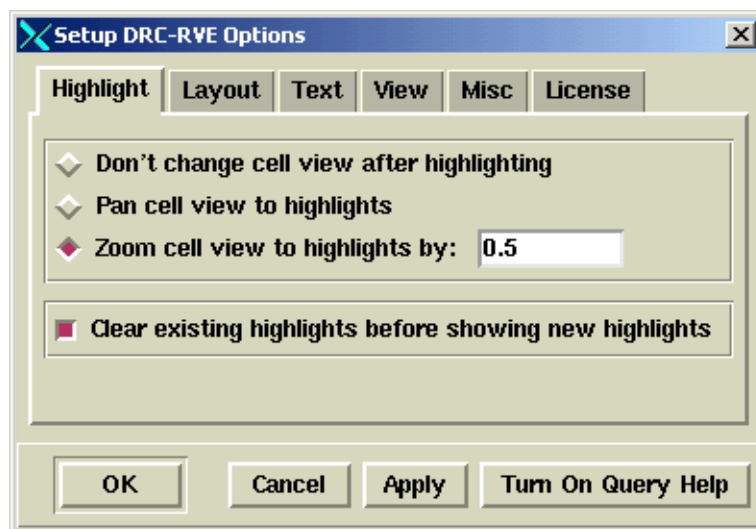
17. Choose **Apply**.

18. Choose **OK** to execute the dialog box.

19. Select the minimum metal1 spacing RuleCheck. (min_spacing_metal1)

20. Choose the **H** icon.

The spacing violation is again highlighted and now the edit window has been zoomed in such that the extent of the highlight bars fills half of the edit window width:
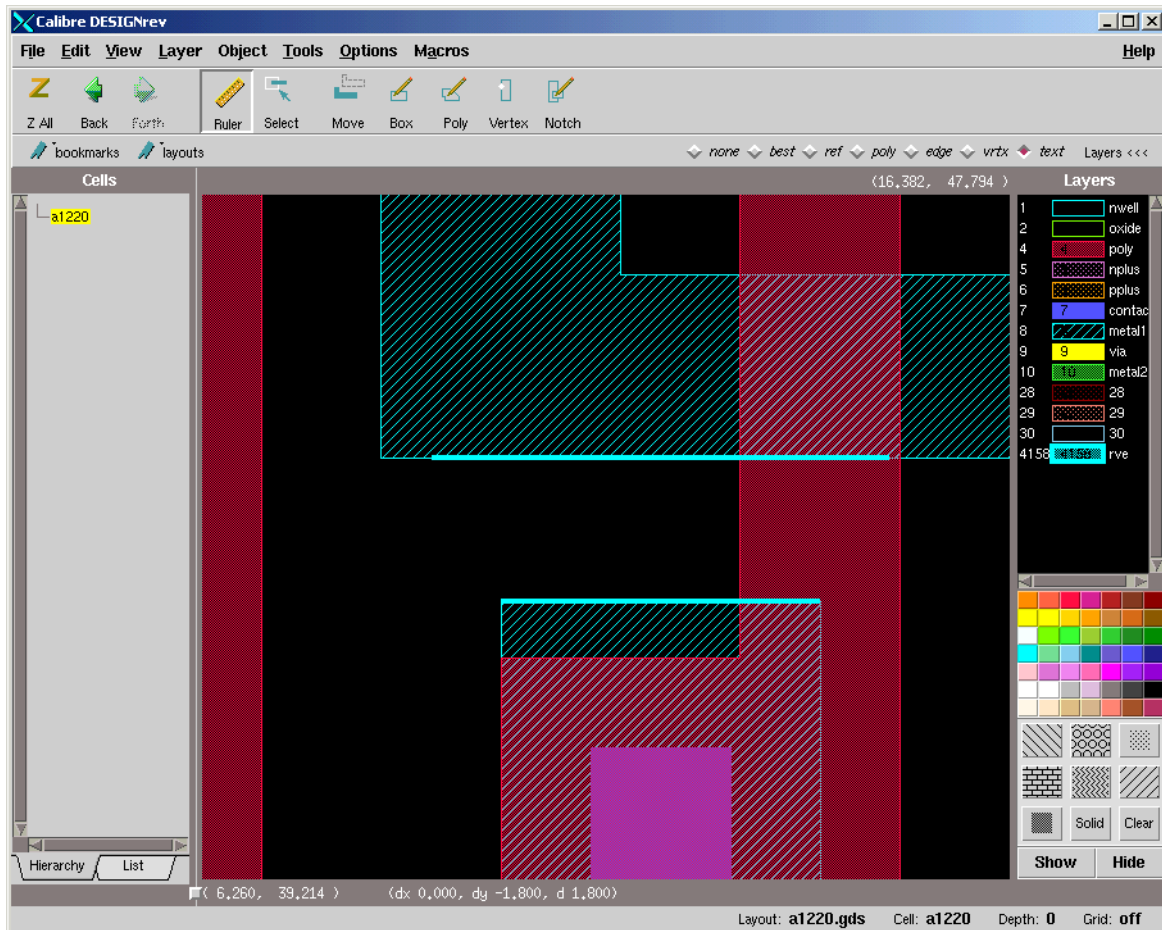
21. Choose the **Ruler** icon in the layout editor.
    (Make sure Ruler Options are set to Manhattan and snap to grid.)

22. Use the Ruler to measure the spacing between the highlighted edges.

    What is the measured spacing between the metal edges?

    _____

What minimum spacing is required by the rule (look in the CheckText frame)?

_____

23. In DESIGNrev, select **Menu: Options > Ruler**

    This opens the Preferences dialog box.

24. In the Preferences box, select **ALL** in the "Clear Rulers" section.

25. Choose **OK** in the Preferences dialog box.

26. In RVE, click the Eraser icon to clear the highlights.

27. In RVE, choose **Menu: File > Exit**.

28. Choose **YES** to confirm the exit.

    Now we will allow tighter metal1 spacing by defining the Unix environment variable "TIGHT."

29. Re-activate the Calibre DRC window.

30. Choose **Menu: Setup > Environment**

    This will open the Set Rules Environment dialog box.

    Note the environment variable TIGHT is not defined.

31. Type "**yes**" in the Value field of the dialog box.

Note that the variable name changes color from red to green indicating that the variable is now defined. The dialog box will look like this:
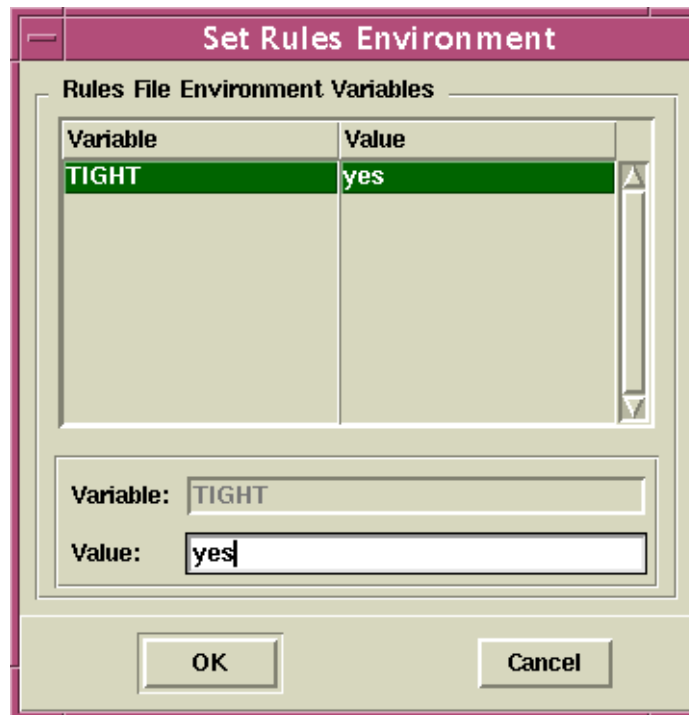
32. Choose **OK** to execute the dialog box.

33. Choose the **Run DRC** Menu button.

34. Review the DRC summary report and the RVE results display to verify that now only two DRC violations are found, minimum metal1 width and minimum poly extension over oxide.

    Why did the original metal1 spacing violation disappear?

    _____

35. Click on the **Eraser** icon in the RVE window to clear all highlights.

36. Close the RVE and summary report windows.

37. Follow the procedure outlined above to open the Set Environment dialog box.

38. Unset the TIGHT environment variable by deleting its value.
    (The variable name will turn back to red.)

39. Choose **OK** to close the dialog box.

40. In DESIGNrev, click on the "**Z All**" icon to view the entire layout.

    In the next exercise we will write two rules to verify transistor lengths.

Exercise 2-3: Write Transistor Checks

In this exercise, you will write two rules to check for minimum transistor lengths in the layout. This exercise will demonstrate how derived layers can be used to focus a RuleCheck on a specific subset of layout data.

For this exercise, transistor length is defined as the width of a poly shape that overlaps oxide in the presence of a pplus or nplus shape. PMOS transistors are found where poly, oxide and pplus coincide, NMOS transistors are found where poly, oxide and nplus coincide.

You will complete two rules which are in the rule file. Rulecheck "min_pgate_length" will highlight all PMOS transistor gates whose length is less than 1.75 microns; RuleCheck "min_ngate_length" will do the same for all NMOS lengths less than 1.25 microns. Both rules will utilize derived layers already defined in the rule file.

1. Make the Calibre Interactive - DRC window active again.

2. Click on the **Rules** menu button.

3. Click on the **View** button next to the rule file name.

    This will open a text edit window containing a copy of the rule file.

4. In the text window, choose **Menu: > Options > Line Numbers**.

5. If necessary, re-position the text edit window so that the red "**Edit**" button located at the bottom of the window is visible.

6. Click on the red "**Edit**" button.

    The button will turn green, indicating that you may now edit the file.

    Find the three layer derivation statements in the rule file (lines 27 - 29). Each derived layer will consist of a collection of shapes copied from the input layers based on the derivation rule. For example, "m1_cont = metal1 AND contact" would create a derived layer of shapes that were copies of all areas overlapped by both a contact shape and a metal1 shape.

Briefly describe the contents of each derived layer in the rule filer:

_____

_____

_____

7. Scroll to the bottom of the rule file and delete the two lines that read "REMOVE THIS LINE TO ACTIVATE TRANSISTOR RULES."

    These two lines were originally placed in the rule file to comment out the incomplete transistor rules.

8. Insert an appropriate internal spacing statement into the two transistor RuleChecks to verify minimum transistor lengths.

    HINT: Refer to the minimum poly width rule in line 38 for the internal statement format - use the appropriate derived gate layer in each of your statements.

9. Choose **Menu: File > Save**.

10. In the Calibre Interactive DRC window, choose the **Load** button next to the rule file name to load the updated rule file.

11. Choose **Menu: File > Close** to close the rule file text edit window.

12. Choose the **Run DRC** menu button.

    If you wrote the transistor length rules correctly (and you did not fix any of the errors in the previous exercises), you should now see four violations reported as results in the RVE window. The fourth violation involves an incorrect PMOS gate length (rule "min_pgate_length"). Select this

RuleCheck in the RVE window and click on the "**H**" icon to highlight the violation in the layout. Your display should look like this:
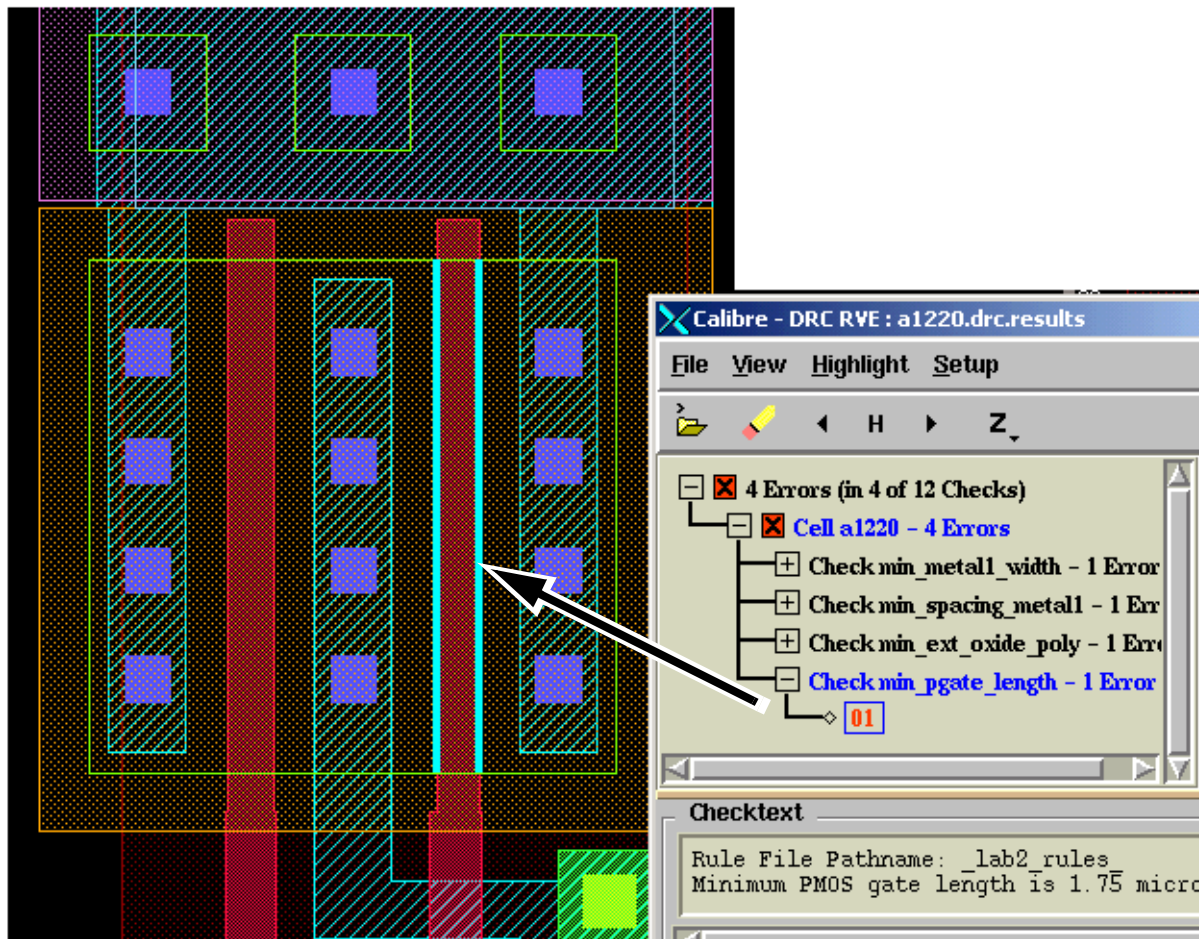
13. (Optional) If there is time, using the Layout Editor correct any of the identified layout rule violations and re-run DRC to verify your fix.
    Hint is for DESIGNrev only.
    Hint: Edge selection is useful here.

When you are finished with this lab, close all Calibre related windows. (Including DESIGNrev, Calibre Interactive DRC, RVE, and Summary Report.)

Module 3
Basic DRC

Objectives

At the completion of this lecture and lab you should be able to:

- List the files required for a Calibre DRC run

- Perform a simple Calibre DRC run

- Identify width and spacing discrepancies from a DRC report

- Identify width and spacing discrepancies in a layout using Calibre DRC RVE

What is the DRC Process?

What is the DRC Process?

Process for Finding, Correcting, and Viewing DRC Results
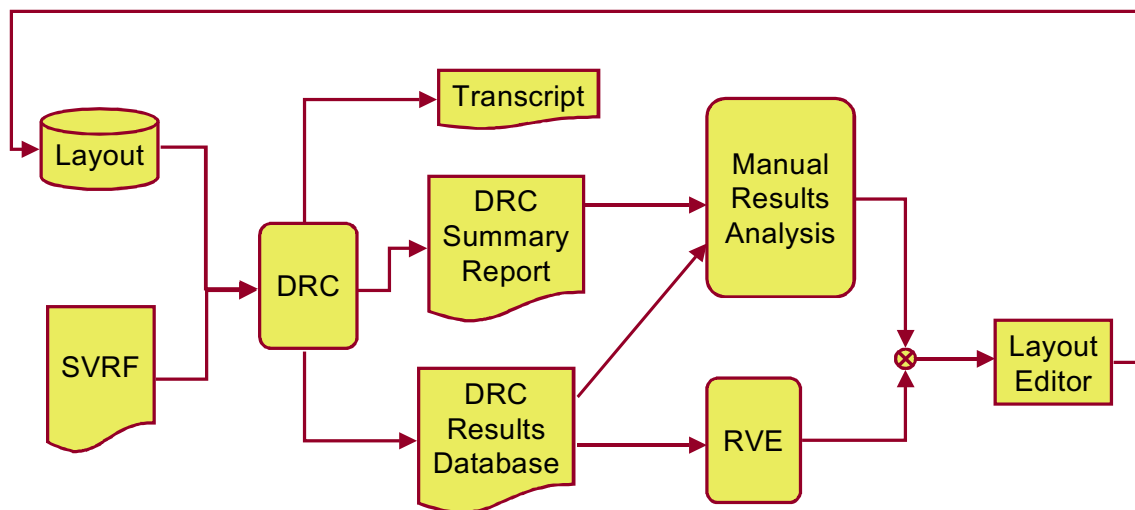
Notes:

What Types of DRC Problems Can Calibre Find?

What Types of DRC Problems Can Calibre Find?

- ◆ **Exterior spacing between objects on the same layer**

- ◆ **Interior dimensions of an object**

- ◆ **Extension of one geometry layer across another**

- ◆ **Overlap of polygons on different layers**

- ◆ **Other special checks**
  (For example: metal density)

Notes:

Example: Exterior Spacing Problem

Inadequate space between paths

metal2 path too close to other metal2 path
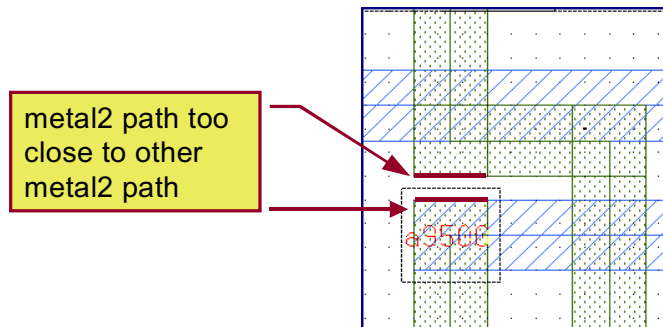
Example Rule:
min_space_metal2 {
@Minimum external space between metal2 is 3 microns
external metal2 < 3
}

Notes:

Example: Interior Spacing Problem

Polygon is too narrow
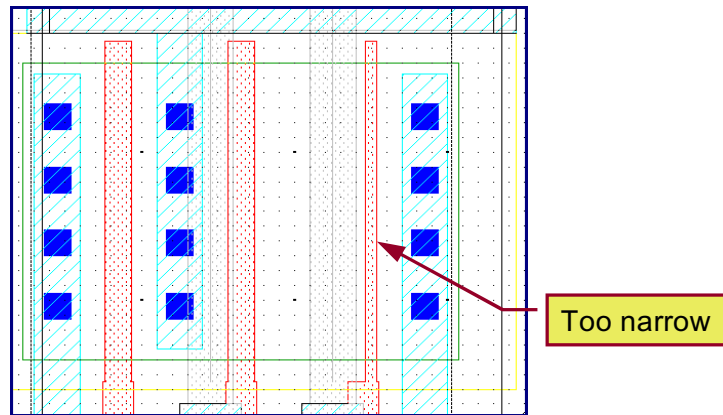
Example Rule:
min_poly_width {internal poly < 1.25 opposite}

Notes:

Example: Extension Spacing Problem

Example: Extension Spacing Problem

Polygon extension is too small

Extension too small
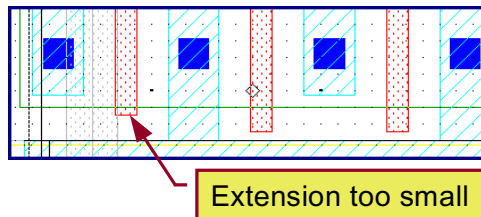
Example Rule:

min_ext_oxide_poly {enclosure oxide poly < 1.25}

Notes:

Using Calibre with DESIGNrev
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Example: Overlap of Polygons on Different Layers

Example: Overlap of Polygons on Different Layers

Not enough overlap

Not enough distance between outside and inside edges
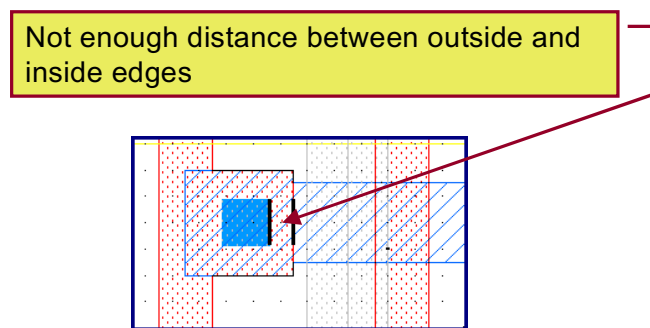
Example Rule:
poly_enclose_cont { enclosure contact poly < 1.0 opposite }

Notes:

What Files Does a DRC Run Require?

- ◆ **Layout file**
  Any of these formats are acceptable:
  - ● **ASCII**
  - ● **GDSII**
  - ● **CIF**
  - ● **Oasis**
- ◆ **Rules File**
  - ● **ASCII**
  - ● **SVRF format**

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Notes:

Calibre Output Files

Calibre Output Files

- ♦ **DRC summary report in ASCII format**

- ♦ **Data files:**

  - ● **DRC Results database**

    - – **ASCII:**
      for Calibre RVE, IC Station Editor, DESIGNrev

    - – **Binary:**
      **used for as an intermediary step to translation for third party tools'
      databases when file size in an issue**

  - ● **GDSII**
    **used for changing the database using Calibre or as the input to
    other editors**

Notes:

How to Set Up a Calibre DRC Run—Load Layout

Using Calibre DESIGNrev and Calibre Interactive:

♦ **Launch DESIGNrev**

   $MGC_HOME/bin/calibredrv

♦ **Open the cell in DESIGNrev**

   MENU: File > Open GDS

Open GDS		
Directory:	/user/sallyw/calibre/using_calbr/lab2	
📄 lab2.gds		
File name:	lab2.gds	Open
Files of type:	GDS (*.gds,*.db,*.sf,*.str,*.stm,*.strm,*.STR,*.GDS,*.GDS2,*.GDSII,*.gds2,*.gdsii)	Cancel

3-12 • Using Calibre: Basic DRC   Copyright © 2004 Mentor Graphics Corporation
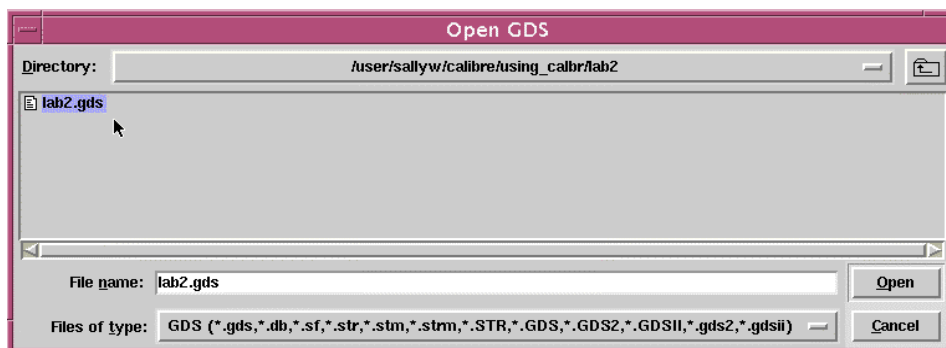
Notes:

How to Set Up a Calibre DRC Run— Launch Calibre Interactive

- ◆ **Launch Calibre Interactive DRC**
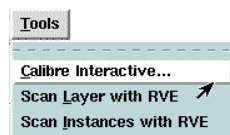
- ◆ **Create new runset (or load runset)**
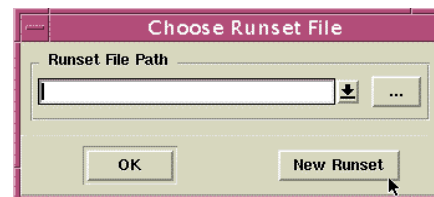
Notes:

What is a runset? A runset is a text file created by Calibre Interactive that stores the settings you specify in the Calibre DRC and LVS windows. Runset files only show the settings you make that are different from the default settings. Runsets increase the reusability and repeatability of Calibre runs by "guaranteeing" consistent inputs.

How to Set Up a Calibre DRC Run—Enter Layout Information

How to Set Up a Calibre DRC Run— Enter Layout Information

- ◆ **Hierarchical**
- ◆ **GSDII file**
- ◆ **Import layout**
- ◆ **Primary cell name**

Notice when input turns from red to green
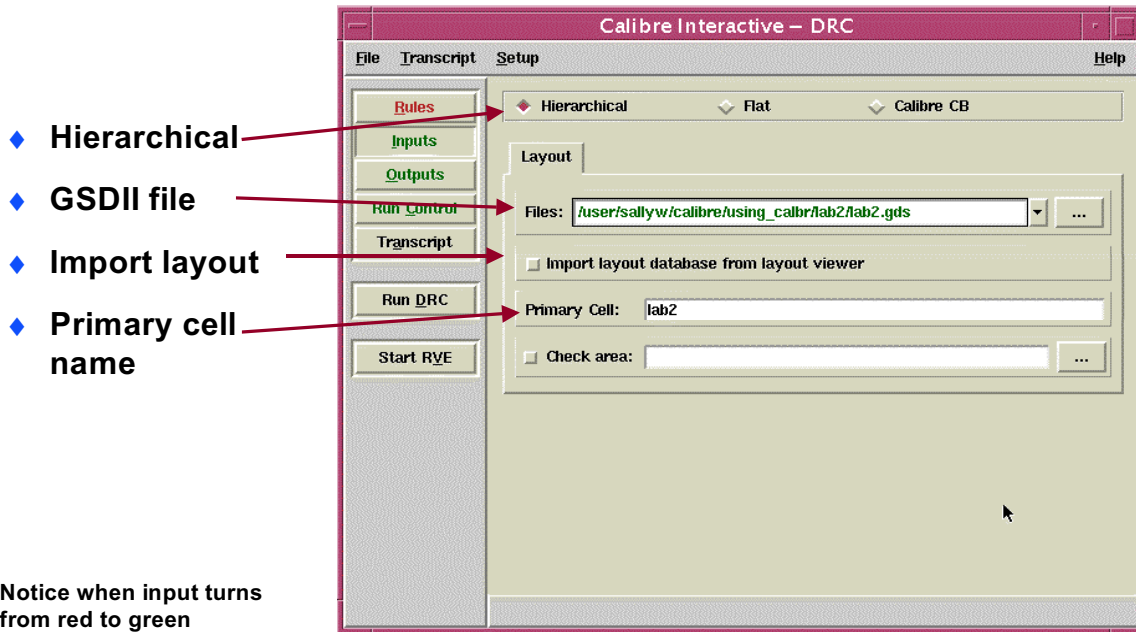
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Notes:

Import layout database from layout viewer option discussion.

If this option is checked, Calibre will take a snapshot of contents of the database viewer and write a "new" GDSII file to the filename specified in the Files text box. (Thus is acceptable for this field to be "red" before running the design.) This works well for the check-fix-check-fix cycle without requiring you to save your work. You should NOT have the name of the GDSII file you have open in DESIGNrev in the File text box. Since this file is open for edits in DESIGNrev, Calibre will not be able to over-write your existing file.

All of the labs use existing files rather than importing the file from the layout viewer.

How to Set Up a Calibre DRC Run—Rule File Information

♦ **Enter the Rule File**

♦ **Enter Run Directory**
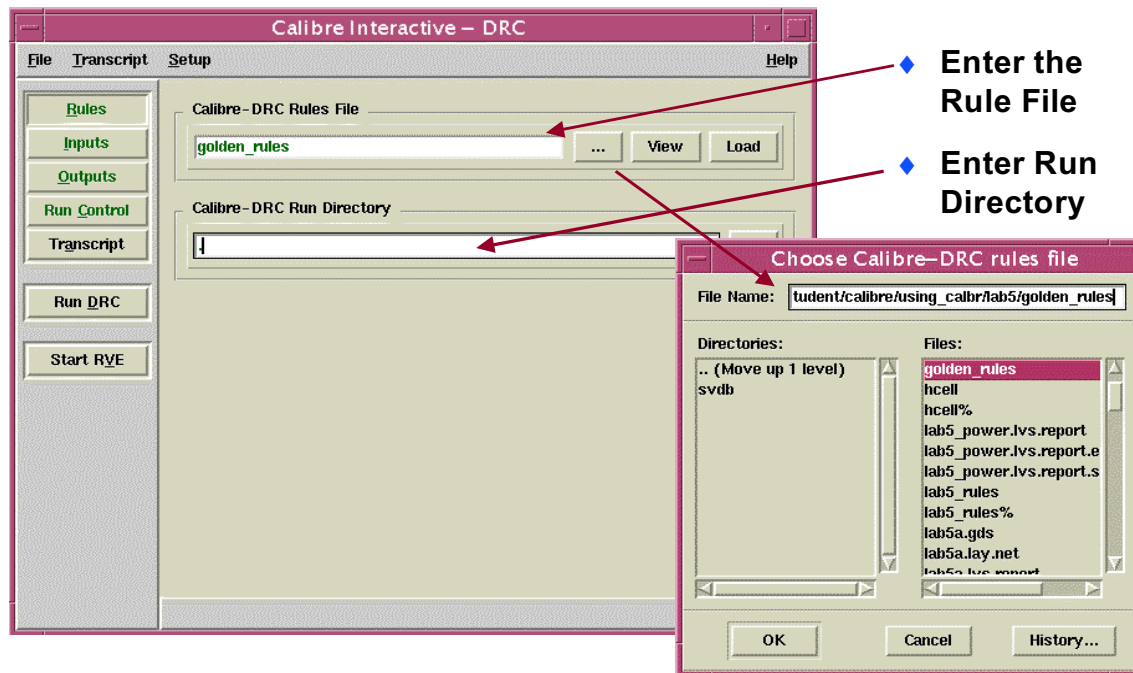
3-17 • Using Calibre: Basic DRC

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Notes:

The **Load** button will parse/check the rule file in preparation for a Calibre run. It is not necessary to use the Load button unless you would like a quick syntax check for your rule file or have changed the file name since the last DRC run.

How to Set Up a Calibre DRC Run— Define Outputs

How to Set Up a Calibre DRC Run—Define Outputs

- ◆ **Specify Results Database Information**

- ◆ **Launch RVE after DRC run**

- ◆ **Define DRC Summary Report Information**

- ◆ **View Summary Report after DRC run**
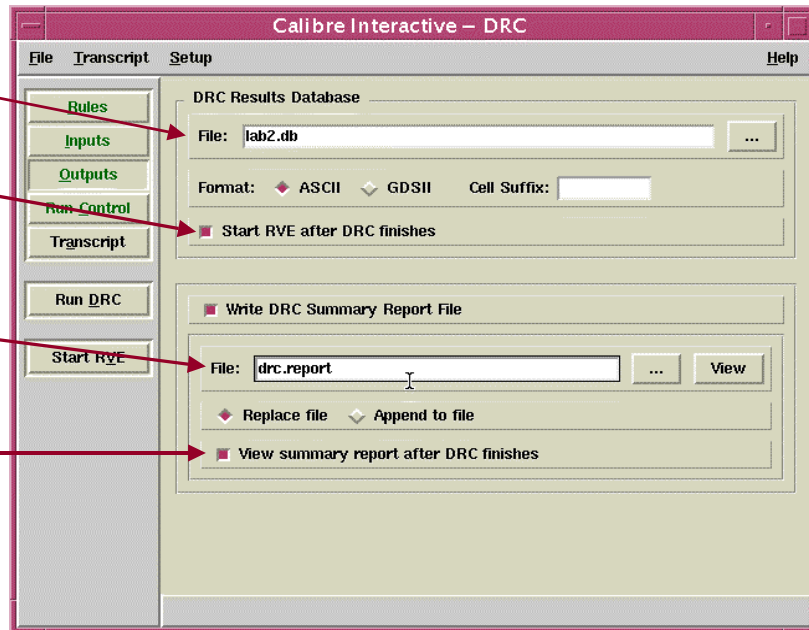
Notes:

How to Set Up a Calibre DRC Run—Define Run Control

How to Set Up a Calibre DRC Run—Define Run Control

As needed:

- **Queue for license**
- **Run 64-bit version**
- **Run multi-threaded**
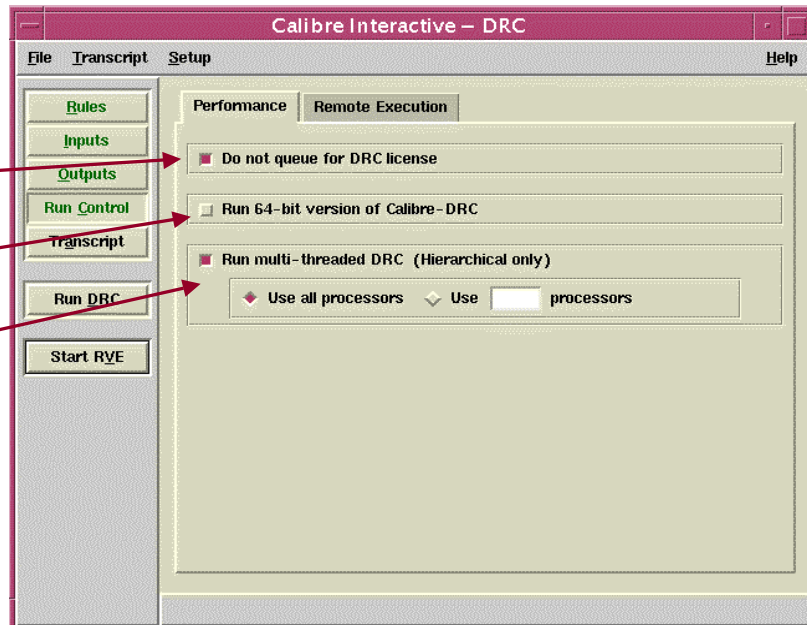
Notes:

How to Set Up a Calibre DRC Run— Define Options

DRC Options Menu:
Setup >
DRC Options

Notes:

How to Set Up a Calibre DRC Run—Define Options (Cont.)

DRC Options:

◆ **Output**

◆ **Connect**

◆ **Area DRC**

◆ **Includes**

Calibre Interactive – DRC

File   Transcript   Setup   Help

| Rules |
| Inputs |
| Outputs |
| Run Control |
| DRC Options |
| Transcript |

| Run DRC |

| Start RVE |

Output   Connect   Area DRC   Includes

☐ **Output cell errors in cell space (Hierarchical DRC only)**

Max. errors generated per check: ◇ All   ◆ Count: 1000

Max. vertices in output polygons: ◇ All   ◆ Count: 4096

Notes:

Using Calibre with DESIGNrev
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How to Set Up a Calibre DRC Run—Define Options (Cont.)

DRC Options:

- ♦ **Output**
- ♦ **Connect**
- ♦ **Area DRC**
- ♦ **Includes**

Calibre Interactive – DRC

File Transcript Setup   Help

Rules
Inputs
Outputs
Run Control
DRC Options
Transcript

Run DRC

Start RVE

Output | Connect | Area DRC | Includes

☐ Connect nets with colon (:)

♦ Don't connect nets by name
◇ Connect all nets by name
◇ Connect nets named: [   ]

☐ Report connections made by name

Notes:

How to Set Up a Calibre DRC Run— Define Options (Cont.)

How to Set Up a Calibre DRC Run—Define Options (Cont.)

DRC Options:

♦ **Output**

♦ **Connect**

♦ **Area DRC**

♦ **Includes**

Notes:

Using Calibre with DESIGNrev
June 2004

How to Set Up a Calibre DRC Run— Define Options (Cont.)

How to Set Up a Calibre DRC Run—Define Options (Cont.)

DRC Options:

- ◆ **Output**
- ◆ **Connect**
- ◆ **Area DRC**
- ◆ **Includes**

Notes:
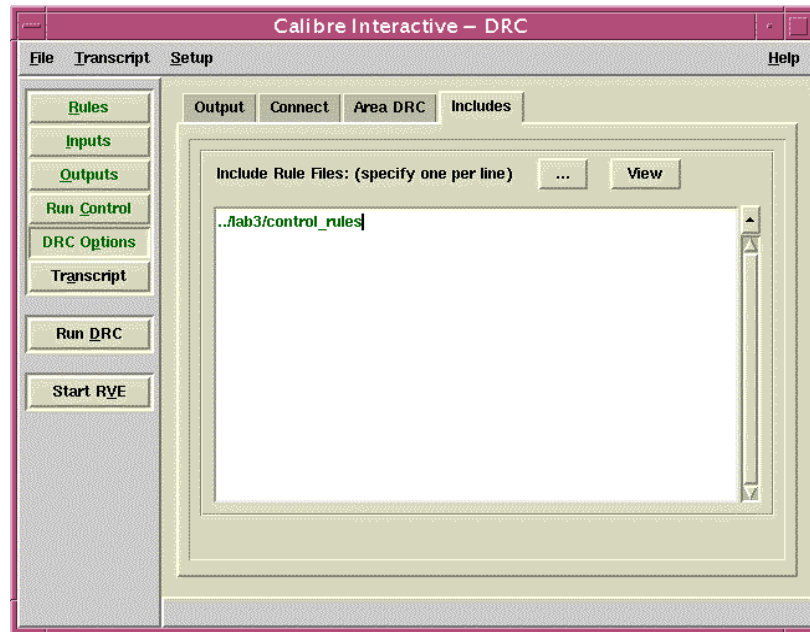
How to Set Up a Calibre DRC Run—Launching a Run

◆ **Save the runset (optional)**

◆ **Choose Run DRC**

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Notes:

How to Read the DRC Transcript

Note: Bottom of the transcript.

Notes:

How to Read the DRC Transcript— LVHEAP Statistics

Notes:

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Using Calibre with DESIGNrev
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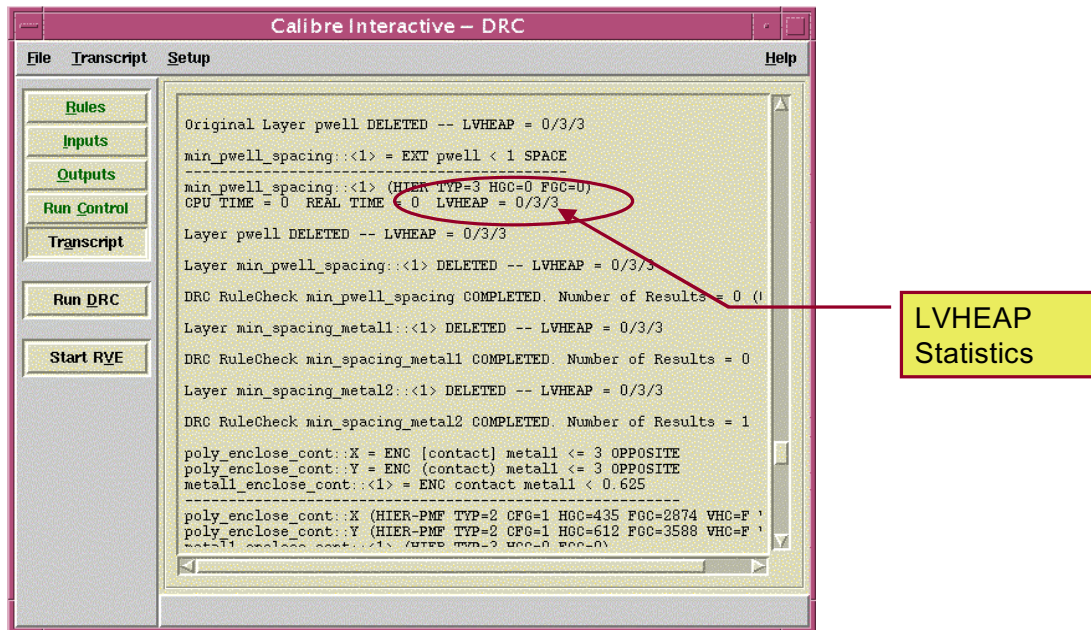
What are LVHEAP Statistics?

♦ **LVHEAP Statistics**

  ● **Reports current memory usage for Calibre DRC/DRC-H**

  ● **Numbers are in megabytes**

<div align="center">

`LVHEAP = 28/47/49`

</div>

Memory being used

Memory allocated

Maximum memory ever allocated
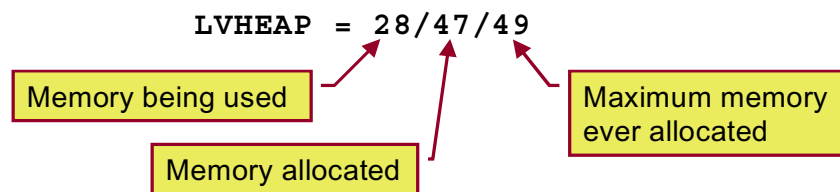
  ● **The maximum memory requirement ("high water mark") of Calibre up to that point in the run is the third number**

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Notes:

What Information is in the DRC Summary Report?

What Information is in the DRC Summary Report?

- ♦ **RuleCheck results**
- ♦ **Number and types of layers checked**
- ♦ **Are the violations in cells or at the top level?**

Notes:

Using Calibre with DESIGNrev
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How to Read the DRC Summary Report—RuleCheck Results

How to Read the DRC Summary Report— RuleCheck Results

♦ **Which rules have violations?**
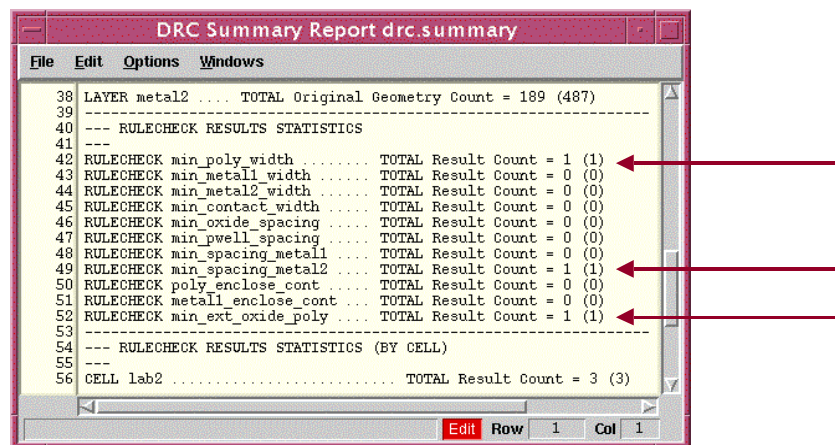
Line numbers on the report are optional.

Notes:

How to Read the DRC Summary Report—Layer Statistics

♦ **What layers were checked?**

```
         DRC Summary Report drc.summary

 File   Edit   Options   Windows

 26  Keep Empty Checks:          YES
 27  ----------------------------------------------------------------
 28  --- RUNTIME WARNINGS
 29  ---
 30  ----------------------------------------------------------------
 31  --- ORIGINAL LAYER STATISTICS
 32  ---
 33  LAYER pwell ..... TOTAL Original Geometry Count = 7    (48)
 34  LAYER contact ... TOTAL Original Geometry Count = 238 (1587)
 35  LAYER poly ...... TOTAL Original Geometry Count = 26  (324)
 36  LAYER oxide ..... TOTAL Original Geometry Count = 70  (472)
 37  LAYER metal1 .... TOTAL Original Geometry Count = 119 (517)
 38  LAYER metal2 .... TOTAL Original Geometry Count = 189 (487)
 39  ----------------------------------------------------------------
 40  --- RULECHECK RESULTS STATISTICS
 41  ---
 42  RULECHECK min_poly_width ........ TOTAL Result Count = 1 (1)
 43  RULECHECK min_metal1_width ...... TOTAL Result Count = 0 (0)
 44  RULECHECK min_metal2_width ...... TOTAL Result Count = 0 (0)

                                          Edit  Row  1   Col  1
```

♦ **Calibre ignores layers that are not involved in a check**

Notes:

How to Read the DRC Summary Report—Cell Statistics

♦ **What cells have discrepancies?**

```
                    DRC Summary Report drc.summary

 File   Edit   Options   Windows

 46  RULECHECK min_oxide_spacing ..... TOTAL Result Count = 0 (0)
 47  RULECHECK min_pwell_spacing ..... TOTAL Result Count = 0 (0)
 48  RULECHECK min_spacing_metal1 .... TOTAL Result Count = 0 (0)
 49  RULECHECK min_spacing_metal2 .... TOTAL Result Count = 1 (1)
 50  RULECHECK poly_enclose_cont ..... TOTAL Result Count = 0 (0)
 51  RULECHECK metal1_enclose_cont ... TOTAL Result Count = 0 (0)
 52  RULECHECK min_ext_oxide_poly .... TOTAL Result Count = 1 (1)
 53  ------------------------------------------------------------
 54  --- RULECHECK RESULTS STATISTICS (BY CELL)
 55  ---
 56  CELL lab2 ....................... TOTAL Result Count = 3 (3)
 57      RULECHECK min_poly_width ....... TOTAL Result Count = 1 (1)
 58      RULECHECK min_spacing_metal2 ... TOTAL Result Count = 1 (1)
 59      RULECHECK min_ext_oxide_poly ... TOTAL Result Count = 1 (1)
 60  ------------------------------------------------------------
 61  --- SUMMARY
 62  ---
 63  TOTAL CPU Time:              0
 64  TOTAL REAL Time:             0

                                        Edit  Row   1    Col   1
```

Notes:

How to Read the DRC Summary Report—Hierarchical and Flat Counts

How to Read the DRC Summary Report— Hierarchical and Flat Counts

♦ **What do the numbers in ( ) mean?**
For hierarchical runs, the number in ( ) is the equivalent count for a flat run

```
        DRC Summary Report drc.summary

 File   Edit   Options   Windows

 26 Keep Empty Checks:        YES
 27 ------------------------------------------------------------
 28 --- RUNTIME WARNINGS
 29 ---
 30 ------------------------------------------------------------
 31 --- ORIGINAL LAYER STATISTICS
 32 ---
 33 LAYER pwell ..... TOTAL Original Geometry Count = 7    (48)
 34 LAYER contact ... TOTAL Original Geometry Count = 238 (1587)
 35 LAYER poly ...... TOTAL Original Geometry Count = 26  (324)
 36 LAYER oxide ..... TOTAL Original Geometry Count = 70  (472)
 37 LAYER metal1 .... TOTAL Original Geometry Count = 119 (517)
 38 LAYER metal2 .... TOTAL Original Geometry Count = 189 (487)
 39 ------------------------------------------------------------
 40 --- RULECHECK RESULTS STATISTICS
 41 ---
 42 RULECHECK min_poly_width ........ TOTAL Result Count = 1 (1)
 43 RULECHECK min_metal1_width ...... TOTAL Result Count = 0 (0)
 44 RULECHECK min_metal2_width ...... TOTAL Result Count = 0 (0)

                                        Edit  Row   1   Col  1
```

♦ **Flat DRC runs do not have data in ( )**

Notes:

How to Use the DRC Results Database—ASCII

♦ **You can manually read the results database.**

Minimum metal2 spacing violation

Minimum enclosure of poly by oxide violation


```
File Viewer — /user/sallyw/calibre/using_ca
File  Edit  Options  Windows
27 | Rule File Pathname: __golden_rules__
28 | Minimum pwell spacing = 1
29 | min_spacing_metal1
30 | 0 0 2 Nov 21 09:27:13 2002
31 | Rule File Pathname: __golden_rules__
32 | Minimum metal1 spacing = 1.0
33 | min_spacing_metal2
34 | 1 1 2 Nov 21 09:27:13 2002
35 | Rule File Pathname: __golden_rules__
36 | Minimum metal2 spacing = 3.0
37 | e 1 2
38 | 122500 347500 126500 347500
39 | 123000 348000 129458 348000
40 | poly_enclose_cont
41 | 0 0 5 Nov 21 09:27:13 2002
42 | Rule File Pathname: __golden_rules__
43 | Enclosure of contact by poly must be 1 micron.
44 | Exception: enclosure in direction of current flow
45 | Direction of current flow is defined as any direc
46 | in which metal encloses a contact edge by more th
47 | metal1_enclose_cont
48 | 0 0 2 Nov 21 09:27:13 2002
49 | Rule File Pathname: __golden_rules__
50 | Minimum enclosure of contact by metal1 = .625
51 | min_ext_oxide_poly
52 | 1 1 2 Nov 21 09:27:13 2002
53 | Rule File Pathname: __golden_rules__
54 | Minimum enclosure of poly by oxide = 1.25
55 | e 1 2
56 | 317875 369000 319125 369000
57 | 317875 368500 319125 368500
58 |
                                    Edit  Row  1    Col  1
```

Notes:

How to Use the DRC Results Database— RVE

How to Use the DRC Results Database—DRC RVE

- ♦ **RVE uses the results database to display the results in graphical form**

- ♦ **RVE can be invoked automatically at the end of a DRC run**
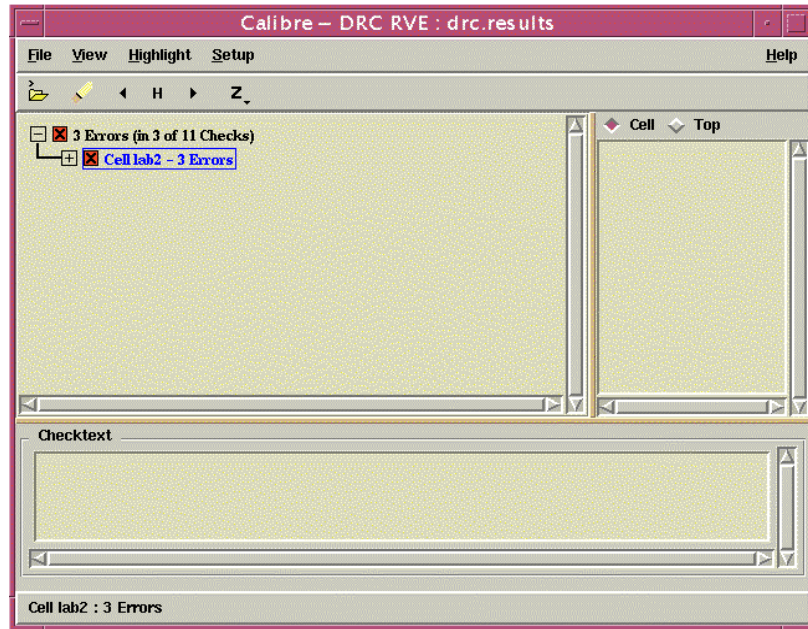
Notes:

DRC RVE GUI Callout
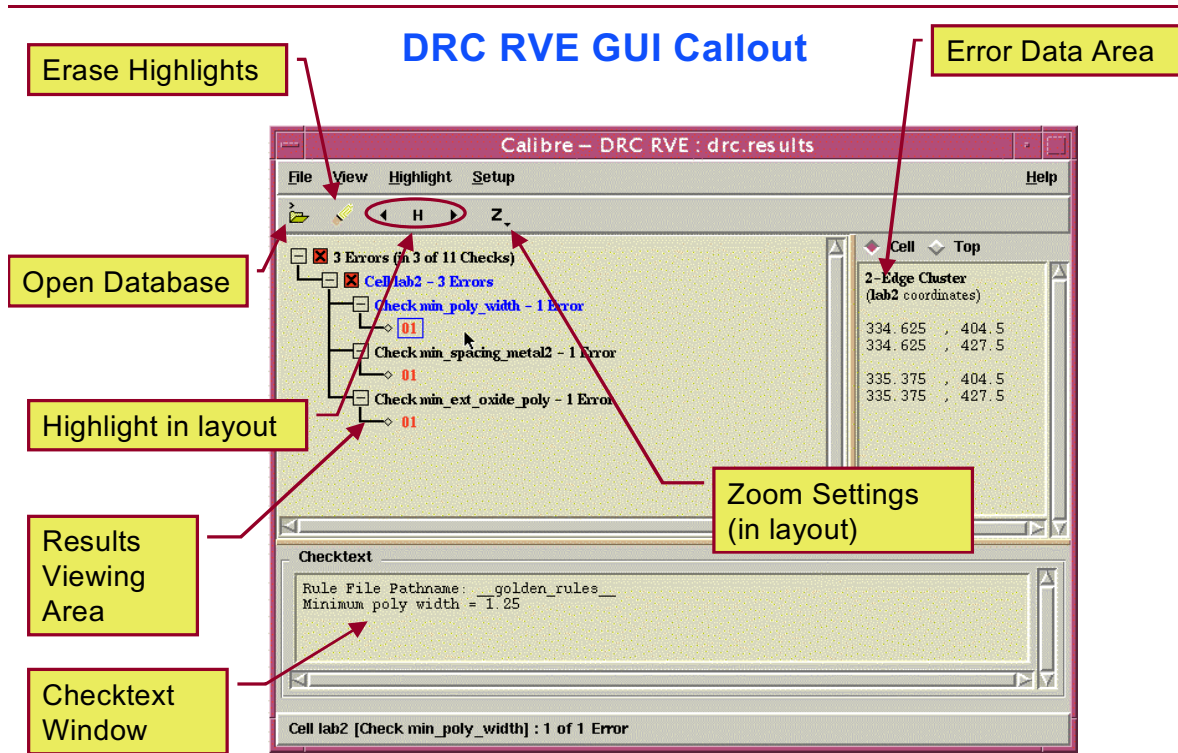
3-36 • Using Calibre: Basic DRC

Notes:

Zoom Factor: Default is 0.7. This means that the highlight will fill 0.7 of the display area. 1.0 would cause the highlight error to completely fill the display.

How to View the Discrepancies by RuleCheck

How to View the Discrepancies by RuleCheck

♦ **Menu:
View >
By Check**

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Notes:

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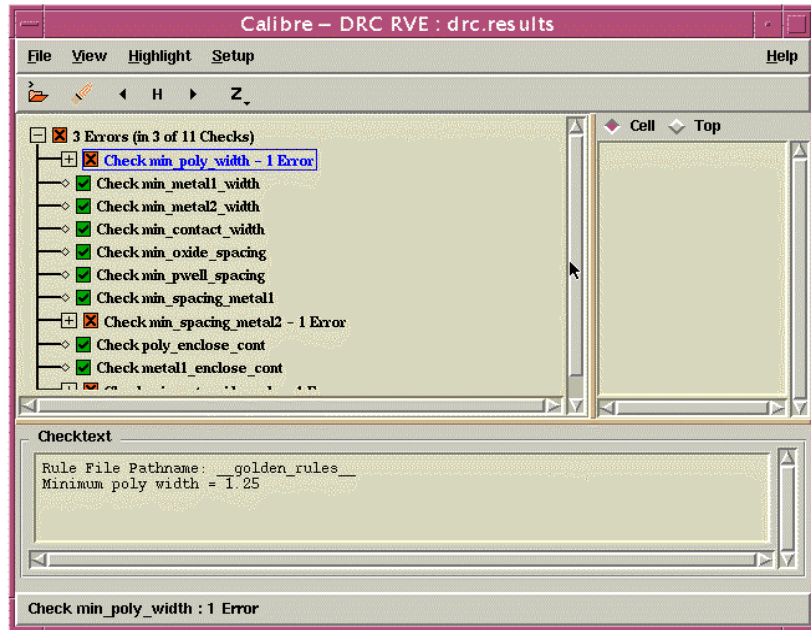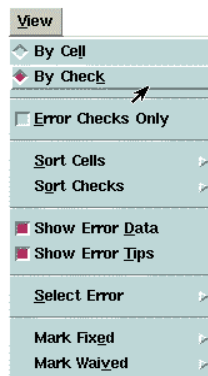
How to Flag the Status of Discrepancies

How to Flag the Status of Discrepancies
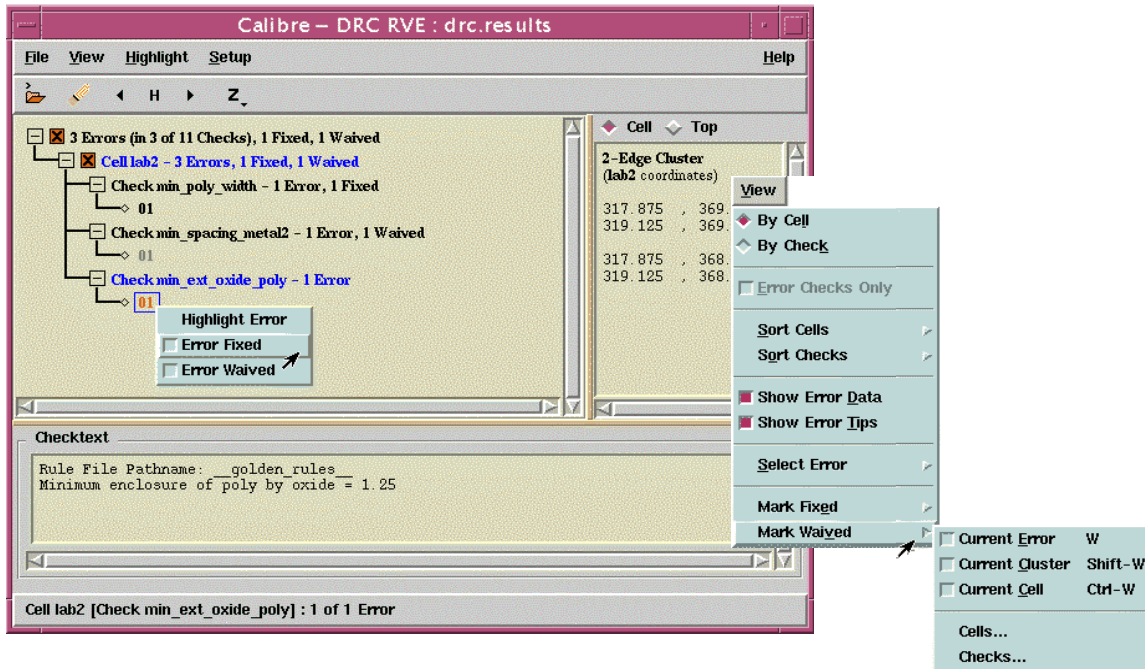
Notes:

How to Use RVE to Locate Discrepancies in the Layout

How to Use RVE to Locate Discrepancies in the Layout

♦ **Set the desired Highlight Zoom.**
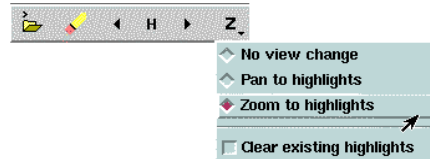
♦ **Select the error to display.**

♦ **Choose H.**

Notes:

Using Calibre with DESIGNrev
June 2004
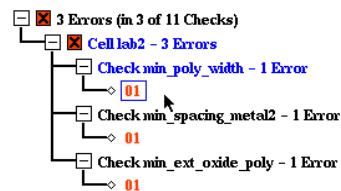
Displaying the Error in the Layout

Displaying the Error in the Layout

Calibre RVE jumps to DESIGNrev and highlights the error
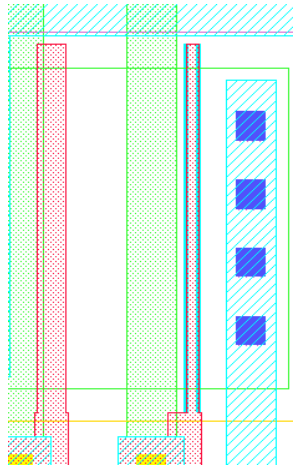
Notes:

Displaying Errors Hierarchically

Displaying Errors Hierarchically

- Display errors at the top level of the hierarchy or at the level in the hierarchy where the error occurs (in context)
- Default is displaying at the top level of the hierarchy
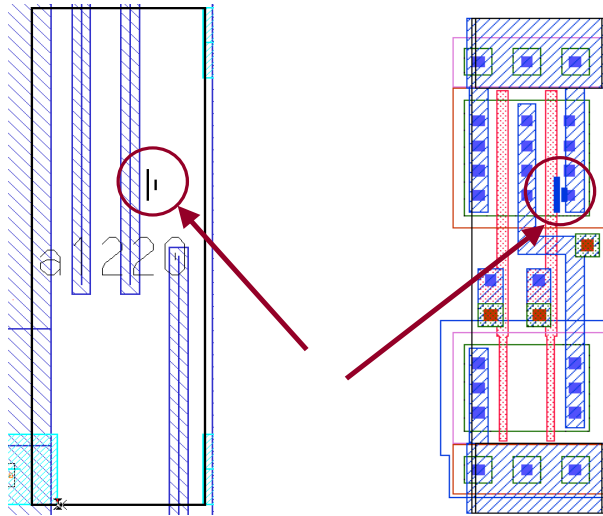
Notes:

Displaying Errors in Context

Displaying Errors in Context

- ◆ **Choose from DRC Option Menu: Output tab**

  | Output | Connect | Area DRC | Includes |

  ■ Output cell errors in cell space (Hierarchical DRC only)
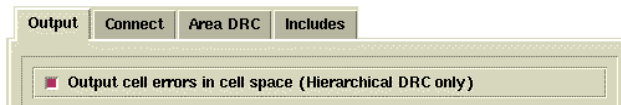
- ◆ **Set RVE to view in context**
  Menu: Highlight > Highlight in Context

  File View Highlight Setup

  ■ Highlight in Context

  ☐ Skip Fixed
  ☐ Skip Waived

  Set Highlight Layers...

  Clear Highlights   F4
  Zoom To Last Highlight F5

  Highlight Error
  Highlight Range...
  Highlight All

  Export to Layout...

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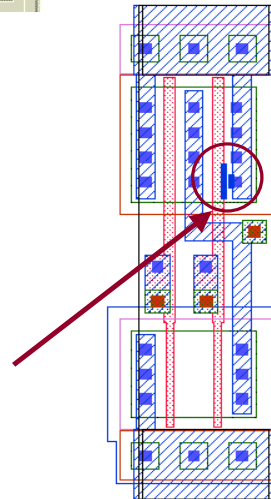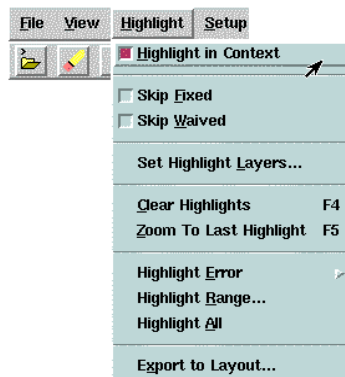
Notes:

Lab Information

Lab Information

In this lab you will:

- **Run Calibre DRC**

- **View a summary report**

- **Invoke RVE**

- **Highlight discrepancies**

- **Correct errors**

- **Check the corrections (import data from layout editor)**

Notes:

Lab: Basic DRC

Introduction

Several of the procedural steps in this lab contain more simplified instructions because you have performed similar steps in the first lab. New procedures will be fully explained.

In this lab, you will you will again run a flat Calibre DRC verification of a layout. This time, Calibre DRC will find several results (errors). When the verification completes, you will view the results by reading the ASCII DRC Summary Report file and using Calibre RVE to highlight the error in a layout tool.

After you find all the errors in the layout, you will correct at least one of the errors, run Calibre DRC on the modified layout, and again check the results with Calibre RVE.

By doing this lab, you perform an entire iteration of checking a layout, making corrections, and verifying the corrections.

List of Exercises

Exercise 3-1: Setup and Run Calibre DRC

Exercise 3-2: Check the Results

Exercise 3-3: Correct Errors in the Layout

Exercise 3-4: Run Calibre DRC on the New Layout

Exercise 3-1: Setup and Run Calibre DRC

In this exercise you will set up a DRC run without help from a runset.

1. Make sure you are still logged in to the workstation.

2. Open a UNIX shell and change your directory to the location of the lab 3 training files as follows:
   ```
   cd $HOME/using_calbr/lab3
   ```

3. List the contents of the lab3 directory.

   You should see at a minimum these the three files:

   - lab3.gds

   - golden_rules

   - layer_props.txt

   If any of these files are missing, please double check that you are in the correct directory, and then notify your instructor.

4. Launch DESIGNrev.
   ```
   $MGC_HOME/bin/calibredrv
   ```

   Now you will load the GSDII file.

5. Choose **Menu: File > Open Layout**.

6. Select lab3.gds by double-clicking.

7. Load the layer properties file, layer_props.txt.
   (**Menu: Layer > Load Layer Properties**)

8. Launch Calibre Interactive DRC on cell lab3.

   a. Choose **Menu: Tools > Calibre Interactive**.

   b. Select Calibre DRC.

    c. Check that lab3 is entered in the Cell text box.

    d. Choose **Run** to execute the dialog box.

This launches Calibre Interactive DRC, displaying the Choose Runset dialog box.

In the previous two labs, you used a runset to load all the required information. In this lab you will create your own runset and initially enter all the information by hand.

9. Choose **New Runset** in the Choose Runset dialog box.

This makes the Calibre Interactive DRC dialog box active with the **Inputs** Menu button active.
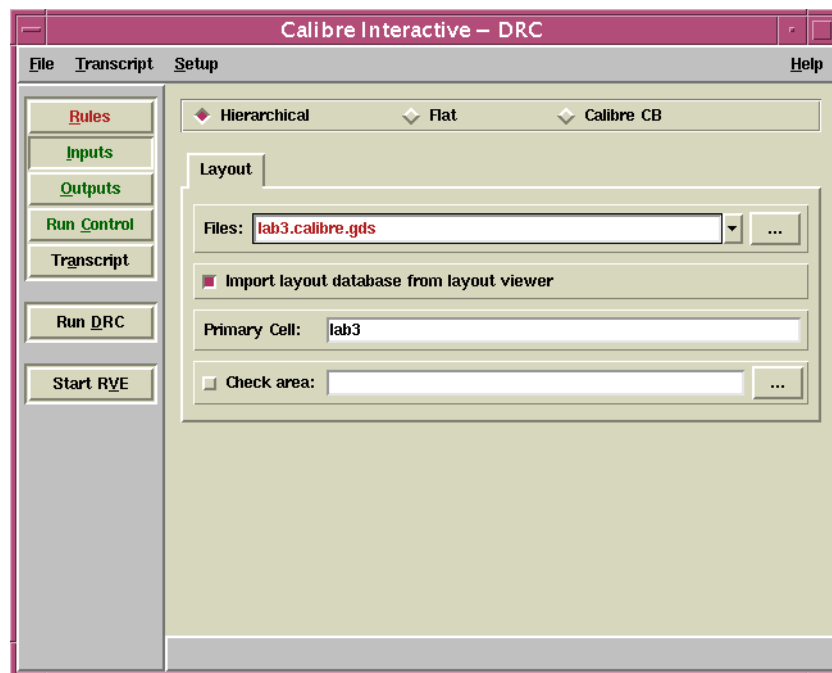
Notice that the Layout file name is in red. You will need to enter the correct data.

10. Select Hierarchical.

11. Enter "lab3.gds" in the Files text box.

Is is green?

If it is not green, try re-entering the GDSII file name using the ⸢ ⋯ ⸣ button.

12. Unselect **Import layout database from layout viewer**.

> **Note** When you unselect this option, you are telling Calibre to use the file you provided in the Files text box.
>
> When you select this option, you are instructing Calibre to create the file in the Files text box from the current layout in the layout viewer. If the GSDII file already exists, Calibre will ask you to overwrite the existing file.

13. Check the name of the Primary cell.

Is it lab3?

If not, correct it, so lab3 is in the primary cell text box.

The dialog box should look similar to below. (You may have the full path for the GDSII file.)
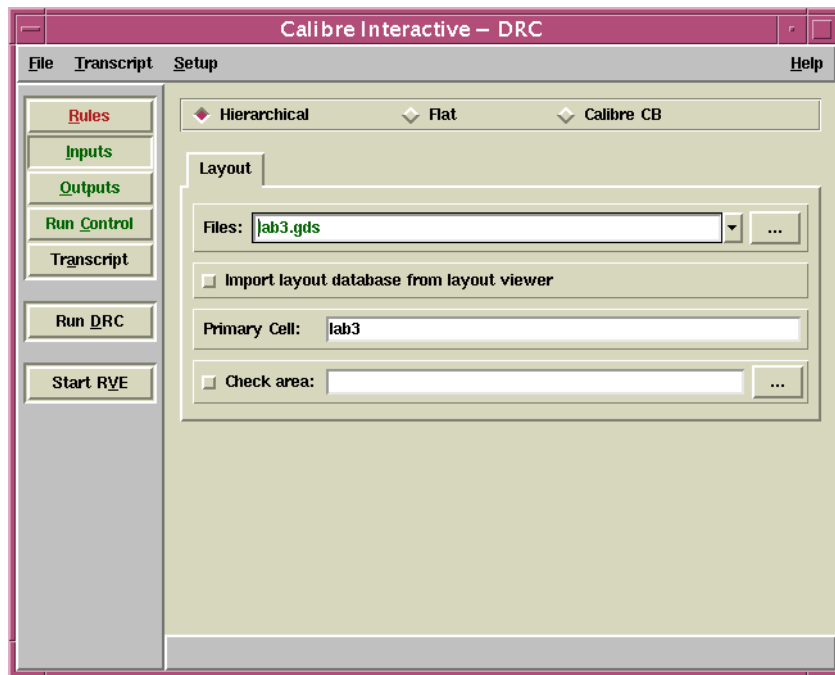
You now have all the required inputs, time to load the rule information.

14. Choose the **Rules** Menu Button.

This displays the Rules information needed for a DRC run.
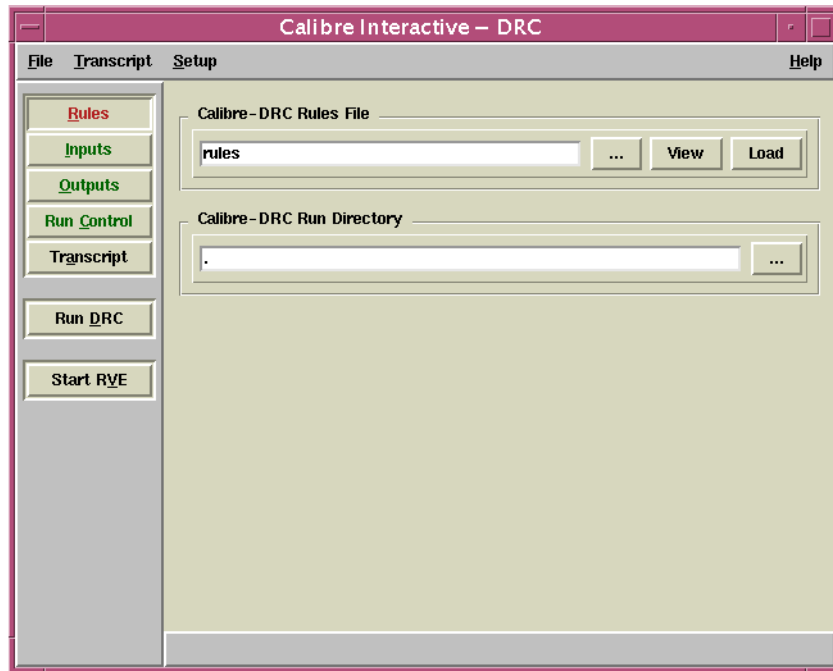
15. Enter golden_rules in the Calibre DRC Rules File text box.

16. Make sure the text turns green, indicating this is an acceptable file.

17. Choose **Load** to load the rule file.

18. Enter (or leave) "." in the Calibre DRC Run Directory.
    (Remove the quotes.)

    This will place all the resulting files in the current directory,
    $HOME/using_calbr/lab3.

The dialog box should now look similar to the one illustrated below. (Again, you may have the full path names in the text boxes.)
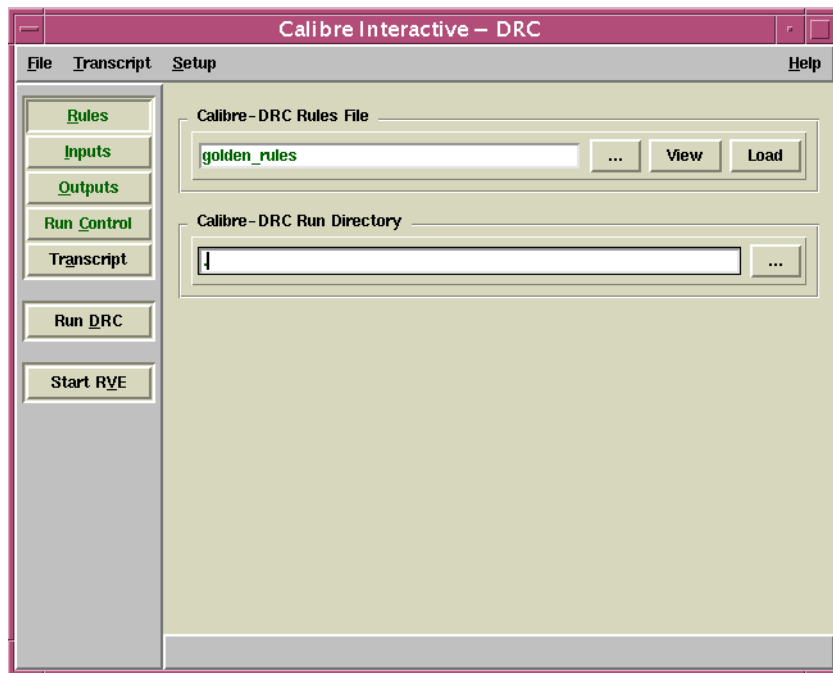
19. Choose the **Outputs** Menu Button.

This displays the dialog box where you will set the names of the output files.
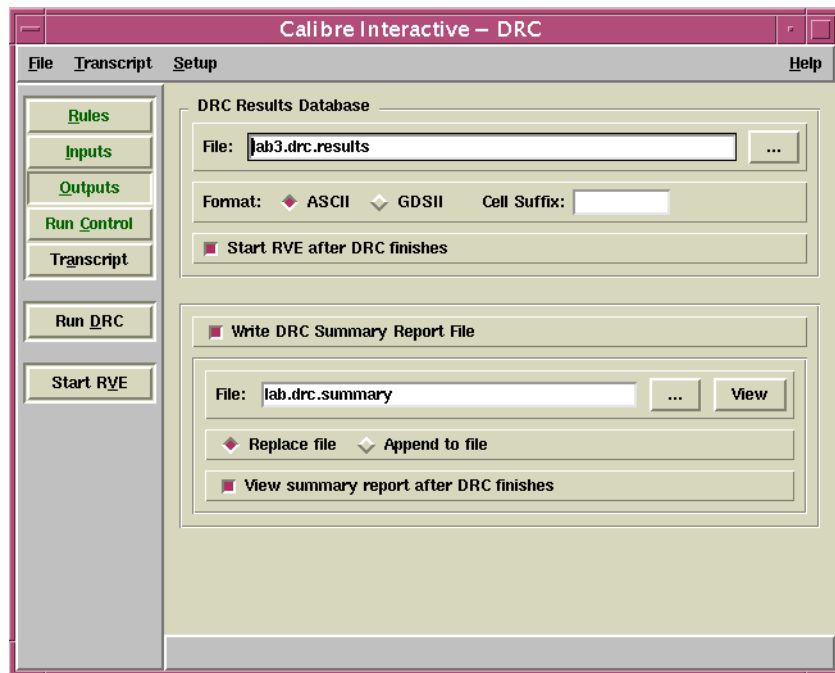
20. Enter lab3.db as the DRC Results Database filename.

21. Select ASCII as its format.

22. Select Start RVE after DRC Finishes.

23. Select Write DRC Summary Report File.

24. Enter drc_report as the DRC Summary Report filename.

25. Select Replace File.

26. Select View summary report after DRC finishes.

In summary, you are creating files, lab3.db (the DRC Results Database) and drc_report (the DRC Summary Report). You want RVE the start as soon as the DRC run completes. You also want the DRC Summary Report to appear

in a text editor when DRC completes. The dialog box should look similar to below.
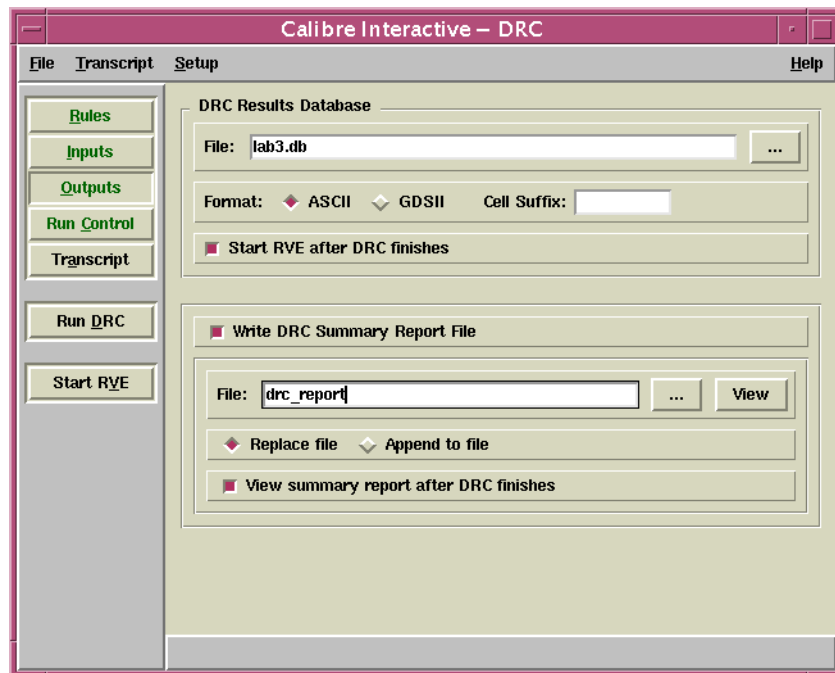
27. Choose the **Transcript** Menu Button.

    This displays the Transcript during the DRC run. From here you can quickly note any problems that may occur during the run.

28. Choose **Run DRC** to start the run.

When the run completes: RVE launches, the DRC Summary Report displays, and the Transcript Window should look similar to below.
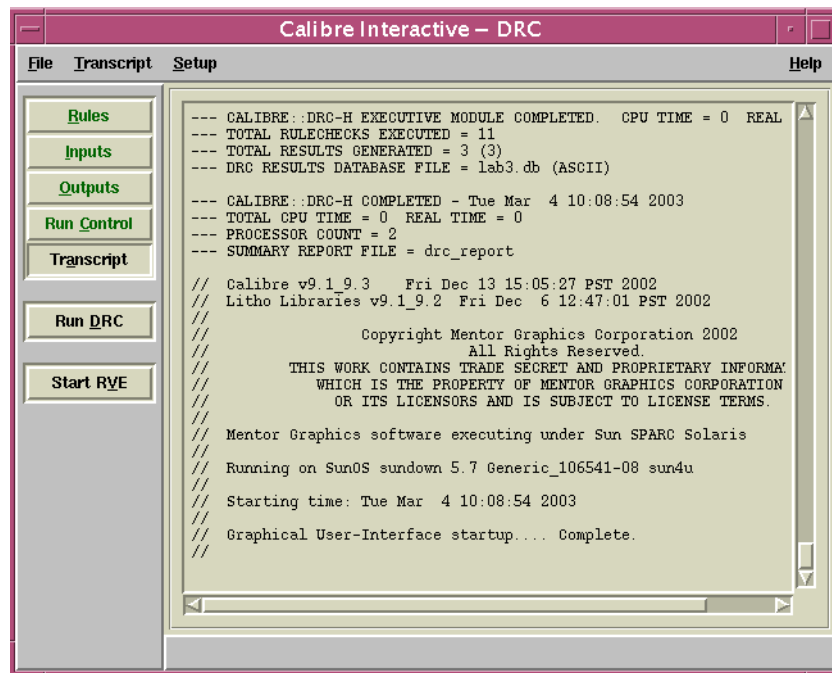
You will analyze the results in the next exercise.

Exercise 3-2: Check the Results

In this exercise, you will review the error messages found in the transcript, summary report, and RVE. You will also highlight the errors in the layout.

1. Look at the transcript window and answer the following questions:

   How many rules were checked?

   _____

   How many discrepancies (results) were found?

   _____

2. Scan the Summary Report and answer the following questions: (Hint: This information is towards the bottom of the report.)

   Which rules have discrepancies?

   _____

   _____

   _____

   How many of these errors occurred multiple times due to being in a cell that has several instances in the layout?

   _____

   Which cell(s) have discrepancies?

   _____

   Notice that you can get increasing more details as you step through the various output files available.

3. Close the DRC Summary Report Window.

4. Make the RVE window active.
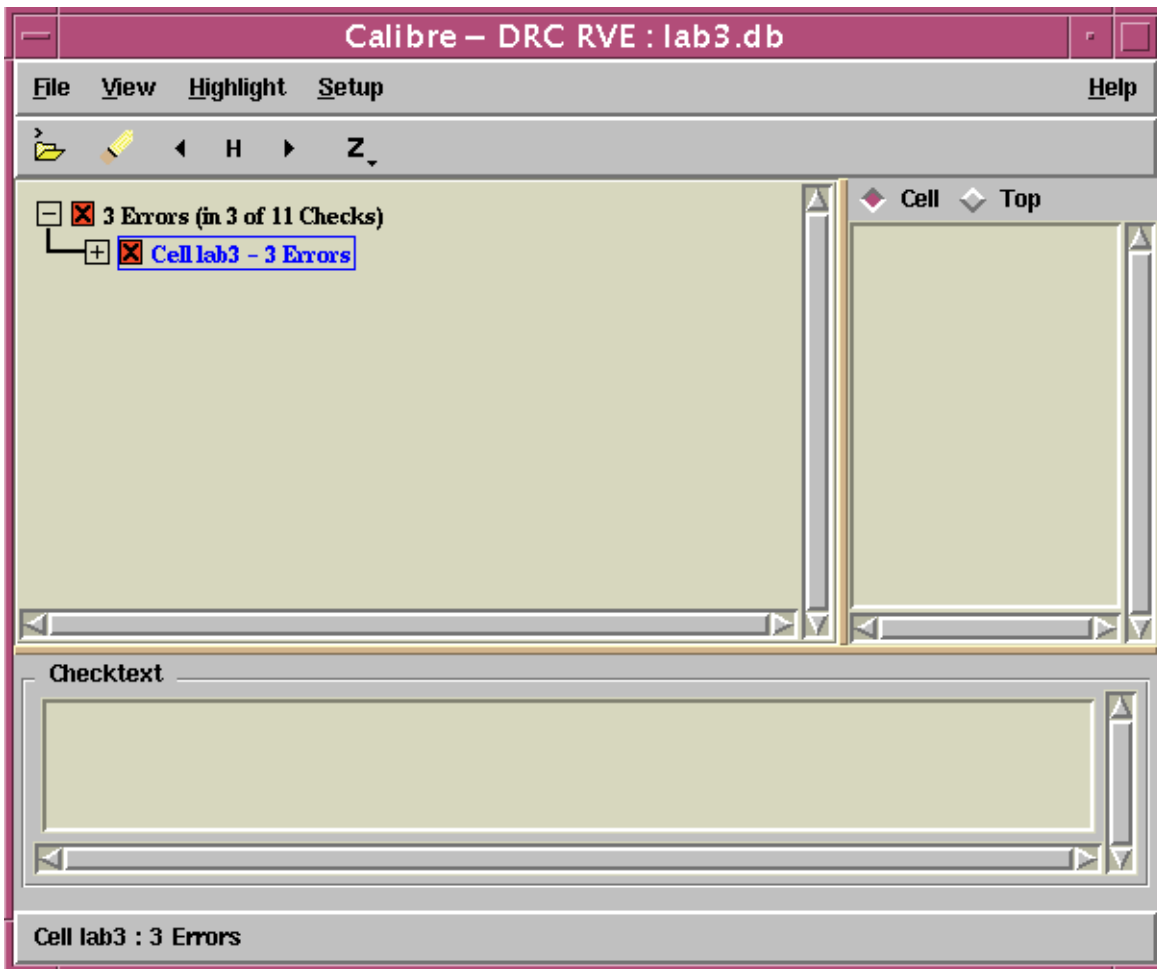
5. Display the full results by clicking on the "+'s" until fully expanded.
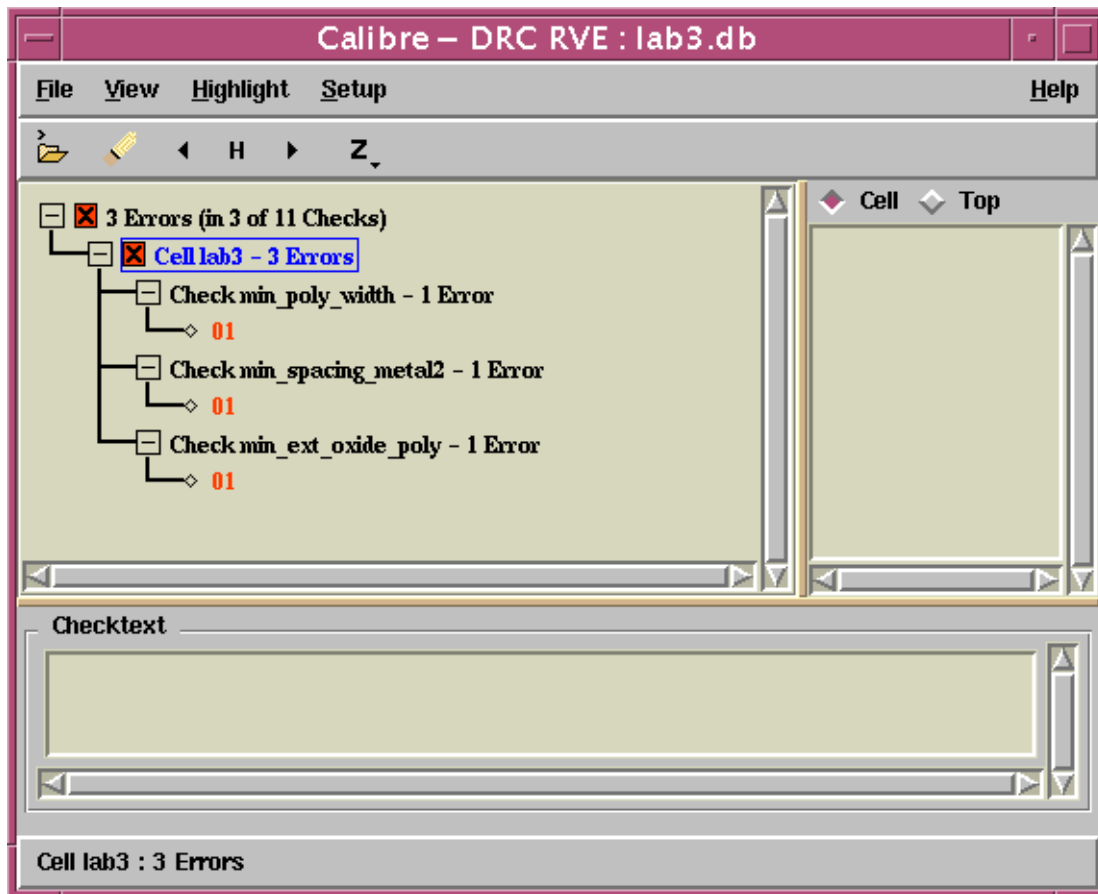
Does the information in this display correspond with the knowledge you already gained from the transcript and the Summary Report?

_____

Next, you will set up the highlight options for displaying the discrepancies in the layout.

6. Choose **Menu: Setup > Options**.

This opens the Setup DRC-RVE Options dialog box.
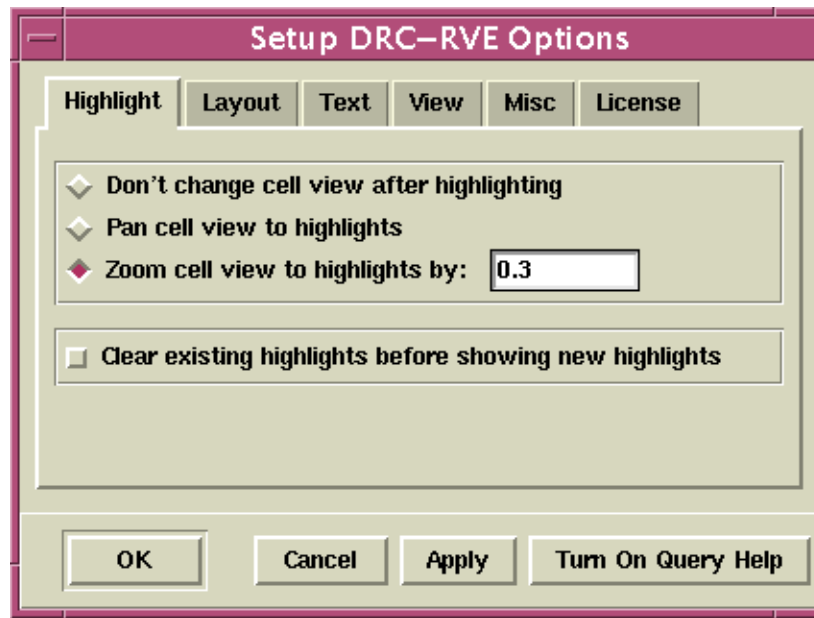
7. Make sure the **Highlight** tab is displayed.

8. Select **Zoom cell view to highlight by**.

9. Enter 0.3 in the text box.
   (This zoom works well for the errors in the current layout.)

10. Make sure the **Clear existing highlights option** is unselected.

11. Choose **Apply**.

12. Choose **OK** to execute the dialog box.

    Next you will find out a little more information about one of the discrepancies.

13. Click on the RuleCheck "min_poly_width -1 Error".
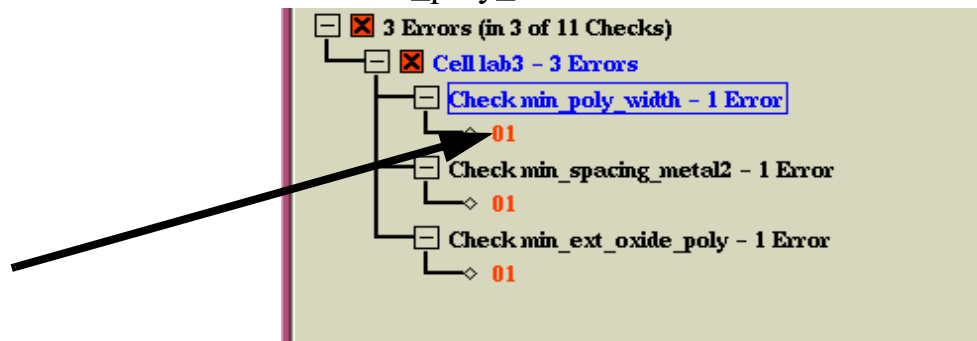
This displays additional information about the rule, itself.

14. Read the contents of the Checktext window.

What is the rule specification?

_____

Interesting side note: what is the name of the rule file?

_____

Is that the name of the rule file you specified?

_____

Why do you think Calibre Interactive changed the name of your rule file?

_____

This is not obvious! You may need to look this up in the documentation.

HINT: Look in the *Calibre Verification User's Manual* and search for "_rule".

Next, you will highlight the error in the layout.

15. Move the layout Window so you can view both RVE and the Layout Viewer (DESIGNrev) at the same time.

16. Select the 01 below the Checkmin_poly_width error.

17. Choose **H** from the toolbar.

The layout viewer pans and zooms into the display to highlight the discrepency.
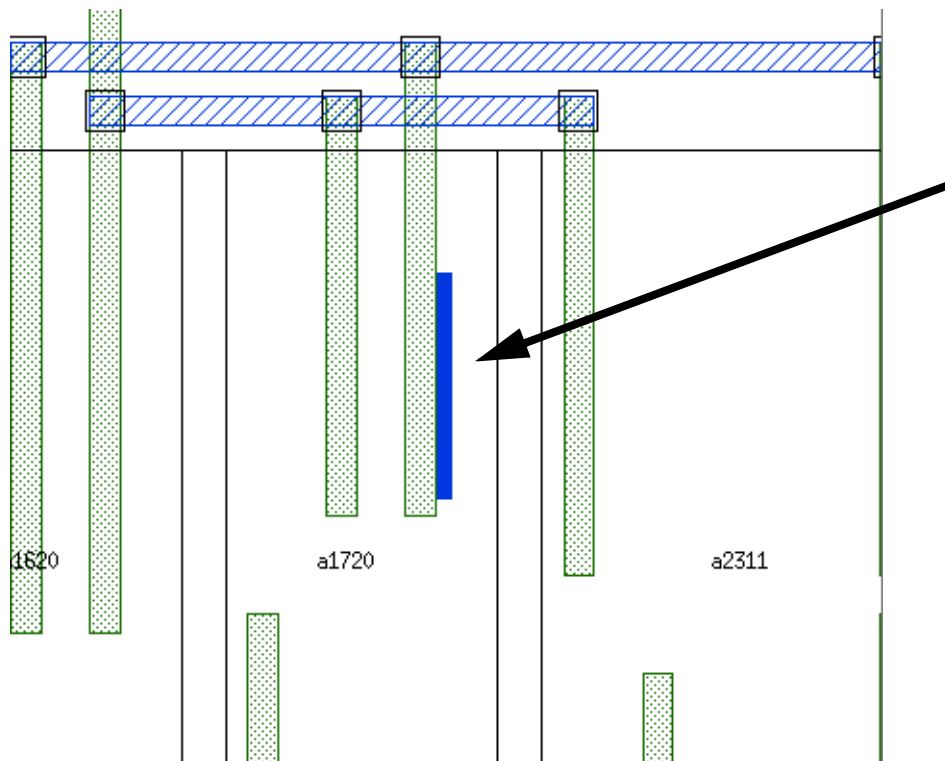
Notice that the error is centered in the display. It is also in an empty area of the display. This indicates that it is inside cell a1720.

You ran the DRC check in hierarchical mode, why do you think the error appears in the top cell (lab3) in the reports?

_____

_____

Now you will display the underlying structure of the cell.

18. Choose **Menu: View > Change Hierarchy Depth > Increment To Depth**.

This displays all the polygons in the next level of the hierarchy.
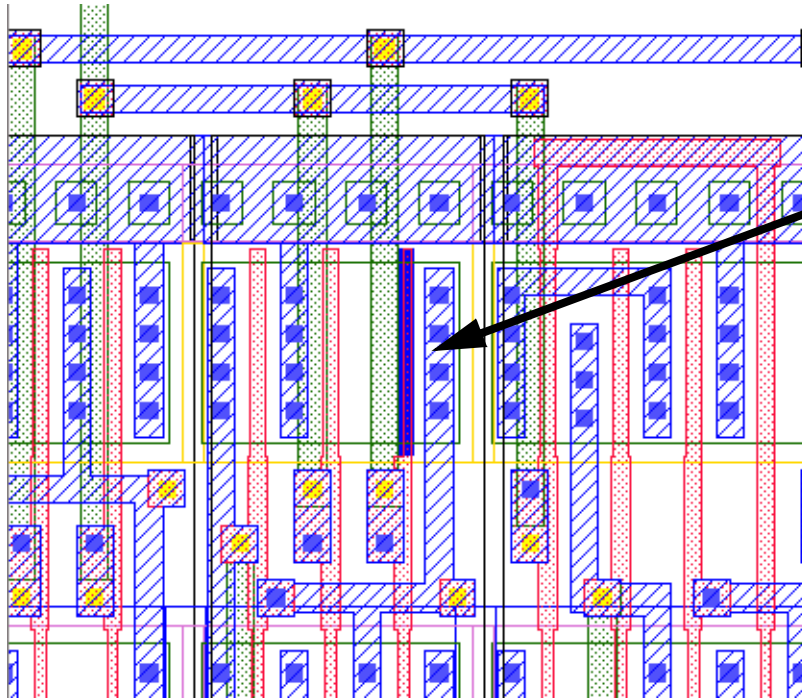
If you want to fix the problem, you would need to display just the cell with the error.

19. Note the exact location of the error.
(The highlight will not display when you go into the cell.)

20. Choose a1720 from the list of cells in the left window.

This opens down into cell a1720.
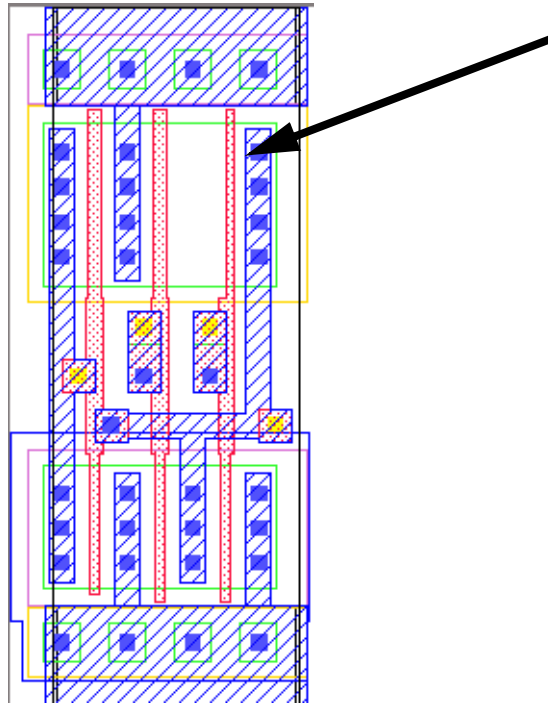
You can use the Back arrow in the Toolbar to view the highlight, if you cannot remember its location.

The Checktext window in Calibre RVE states that this violates the rule where minimum poly width is 1.25. To correct the error, you would widen the poly that was highlighted to match the adjacent pieces of poly.

You will fix this error in the next exercise.

Next you will look at another error.

21. Return to the Calibre RVE window.

22. Choose the   ▶   button (Highlight Next Error) from the Toolbar.

This displays the next error in the layout window.
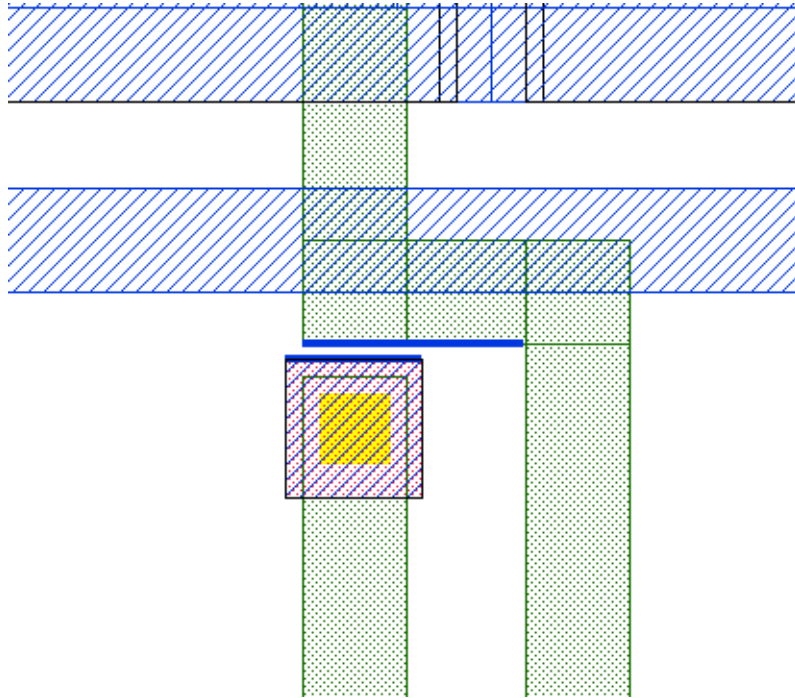
What is the problem with this part of the layout?

_____

_____

23. Display the last discrepancy, using RVE.
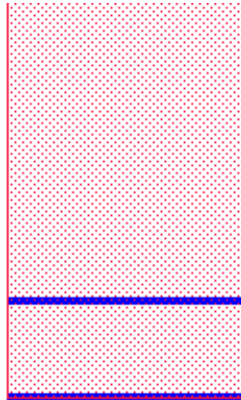
This time you are a little too zoomed in to really see the problem.

24. Choose **Menu: View > Zoom Out** at least twice to display another poly run.
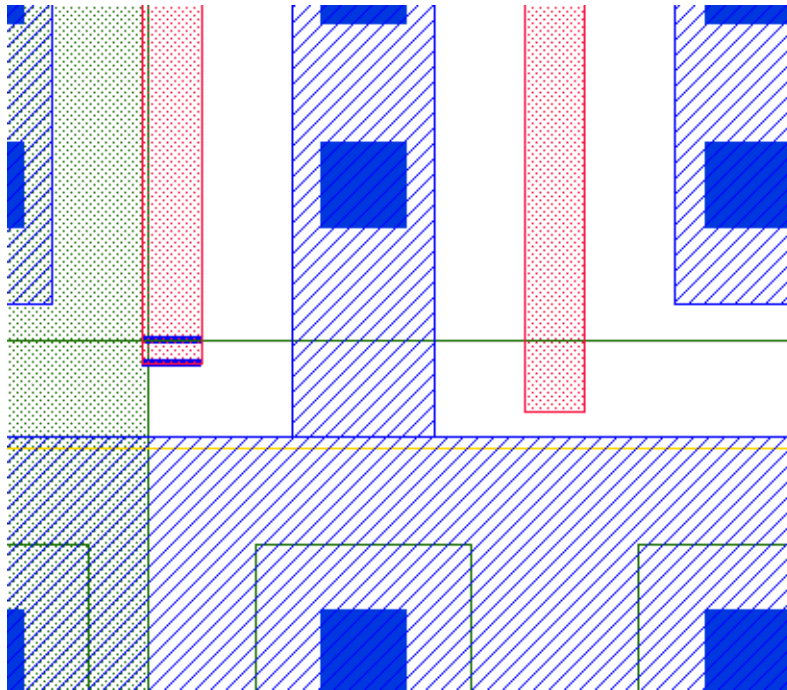
What appears to be the problem?

_____

_____

Exactly where (and what cell) is the problem?
HINT: You may need to continue to zoom and change the view so you are only looking at the polygons in the top hierarchy to find the answer.

_____

In the next exercise you will correct this error.

Exercise 3-3: Correct Errors in the Layout

In this exercise, you will be given step by step instructions to correct the problems in a1720. You know there are two problems. The first is a narrow poly in the upper right of the cell and the second is an overlap that is too small in the lower left of the cell.

First we need to establish a common display (since you needed to do different amounts of zooming, etc. to answer the last question in the previous exercise).

1. Turn on all highlights in the layout from RVE using **Menu: Highlight > Highlight All**.

   In the layout viewer, set the view to only display the contents of the top cell.

2. Choose **Menu: View > Change Hierarchy Depth > Decrement To Depth**.

   i   To change the view to only display the contents of the next cell up in the hierarchy you can also just type: "<". (Do not type the quotes.) Conversely, to display one step lower in the hierarchy, type: ">".

   You should now be able to see the highlights and just the contents of the top cell.

3. Zoom and pan as needed to display the a1720 cell.

4. Select the a1720 cell.

Your display should look similar to the illustration below.
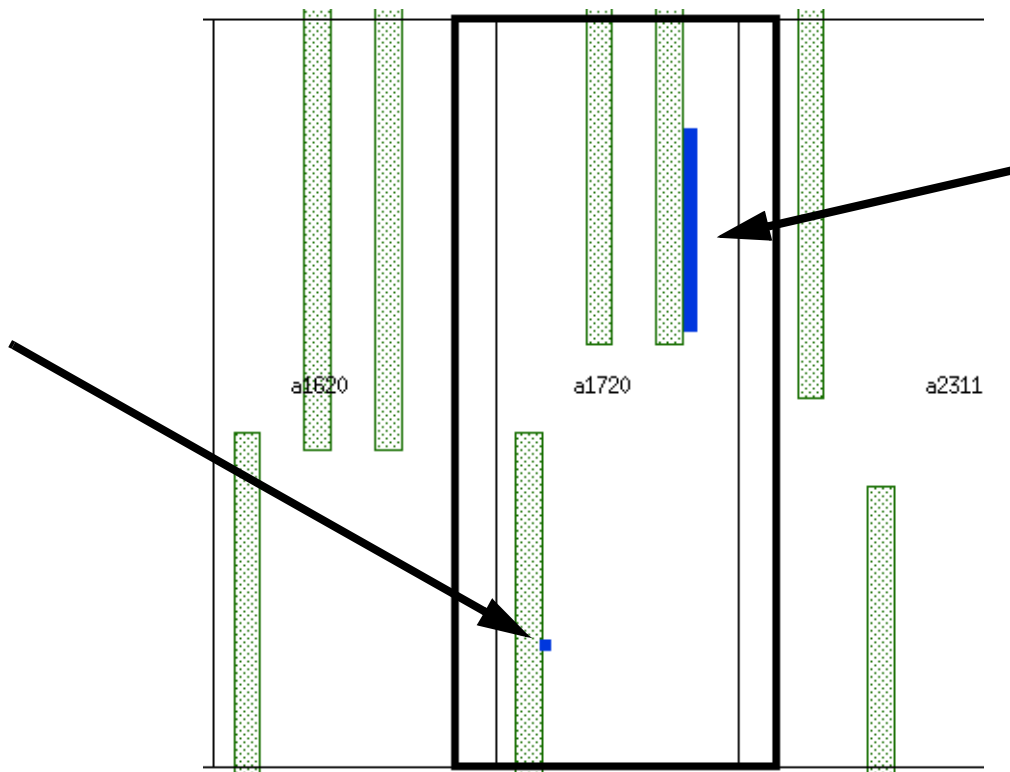
Note the location of the two highlights. When you begin editing the cell these highlights will no longer be visible.

5. Choose a1720 from the Cell window.

This opens down into the cell in a separate area.
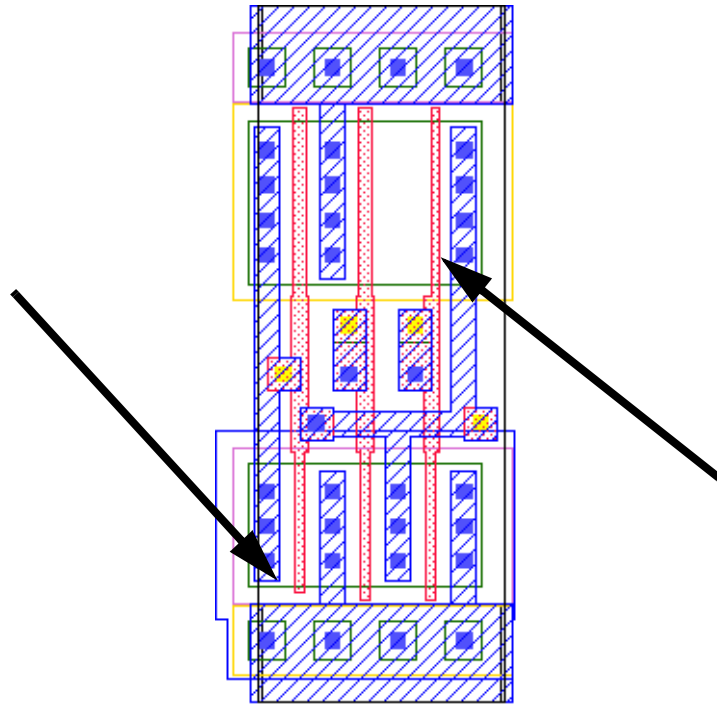
Can you find the two pieces of poly that need to be fixed?

We will start with error 3, the poly in the lower left.

6. Zoom in to display a close up around this poly.

    You know you need to extend the poly 1.25 beyond the oxide layer. You will need something to act as a reference so you will know when you have extended the poly the correct distance.

    📄 **Note**   You may need to change the Ruler options from "Vertex/Edge" to "Grid". Change the options using **Menu: Options > Ruler**.

7. Choose **Ruler** from the Toolbar.

8. Click on the bottom edge of the oxide layer.

9. Draw a straight line down approximately 1.25.

Your display should look similar to below. (Notice that this ruler is 1.258.)
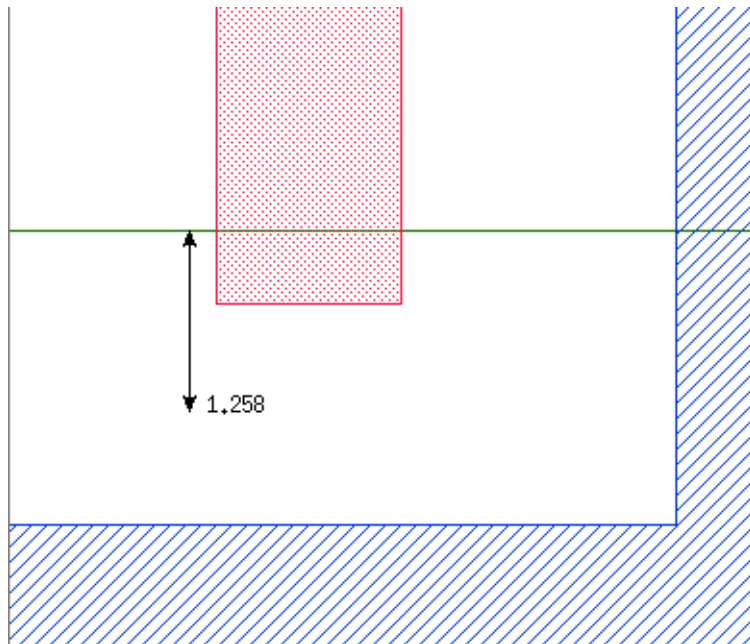
10. Select the poly.

11. Select the edge that needs stretching.

   a. Choose **Vertex** from the Toolbar.

   b. Click in the middle of the lower edge.

      The selected line segment should change to "yellow" to indicate selection.

12. Choose **Move** from the Toolbar.

13. Stretch the segment until it is as long as your ruler indicates.
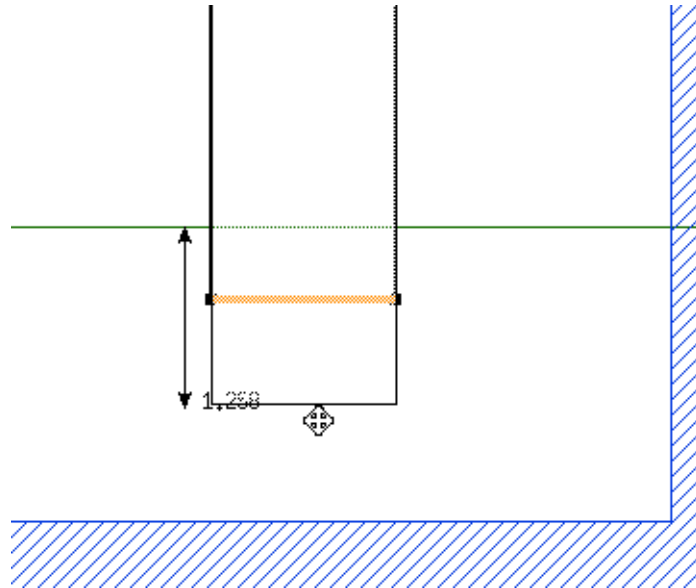
14. Release the mouse button to complete the stretch.

15. Type "**u**" to unselect everything.

    You should have corrected the first error. Now you will correct the second error.

16. Display the part of the cell with the other error.

17. Use the same methods (ruler, select vertex, stretch) to correct this error.

    Although the rule states that the minimum poly width is 1.25, measure the width of the other similar poly lines and make the narrow poly line the same width.

Before:

After:
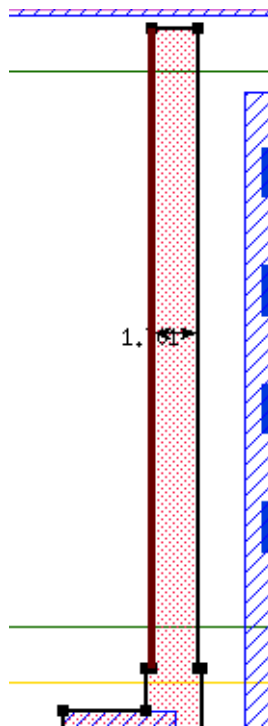
You are now ready to save the file and see if you fixed the problems.

18. In RVE, choose the Eraser icon to erase all current error highlights.

Exercise 3-4: Run Calibre DRC on the New Layout

In this exercise, you will run DRC on the new layout and check your fixes. You will use the Calibre feature which reads the layout directly from the layout editor rather than needing to write the edited file out to GDSII before making the Calibre run.

1. Close the RVE window.

2. Return to the Calibre Interactive DRC Window.
   (You do not need to re-launch Calibre Interactive. You can use the existing window.)

3. Change the following information:

   • [**Outputs**] DRC Results Database File: lab3_fixed.db

   • [**Outputs**] DRC Summary Report File: drc_report_fixed

   • [**Inputs**] Layout File: lab3_fixed.gds

   • [**Inputs**] Import layout database from layout viewer: selected

The Inputs tab of the Calibre Interactive DRC window should look similar to below.
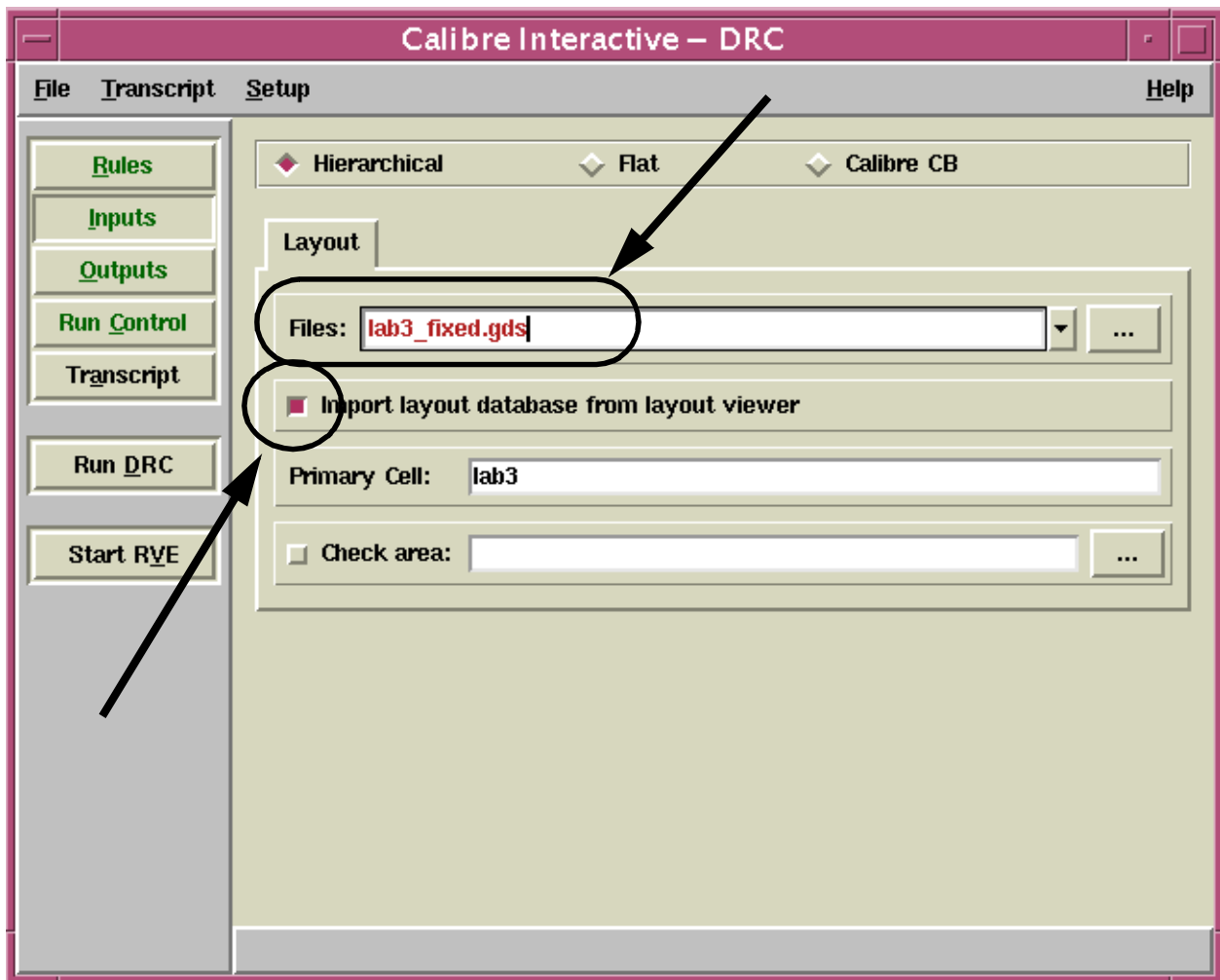
Notice that the **Files** text is in red, but the **Inputs** tab is green. This indicates that the lab3_fixed.gds file does not currently exist, but Calibre has enough information to perform a DRC run. When you selected the "Import layout database from layout viewer" option, you instructed Calibre to create the GDSII file before it starts the actual verification.

4. Choose **Transcript** to display the transcript.

   You are now ready to run DRC on the new data.

5. Choose **Run DRC**.

What results do you expect?

_____

6. Use the Transcript, Summary Report, and RVE to check your results.

What results did you get?

_____

If you have any errors, other than the expected one, you may want to go back and try to fix the discrepancies again. If this is the case, you will get a message asking if it is OK to overwrite the "lab3_fixed.gds" file when you re-run the DRC to check your results.

This concludes Lab 3. You may try to fix the other error on your own and re-run DRC. When you are finished, please exit all Calibre windows (RVE, Summary Report, Calibre Interactive, and the layout viewer) so you will be ready to begin the next lab.

Module 4
Advanced DRC Topics

Objectives

At the completion of this lecture and lab you should be able to:

- Use hierarchical runs effectively

- Debug effectively using:

    o Rule check grouping

    o Database window specification

    o Cell exclusion

    o Maximum results reporting

What are the Differences between Hierarchical and Flat DRC Runs?

What are the Differences between Hierarchical and Flat DRC Runs?

♦ **Flat:**
Looks at every geometry in every cell

♦ **Hierarchical:**
Only looks at the geometries in a single instance of a cell

♦ **Benefits of Hierarchical:**

● **Minimizes redundant processing:**
Stores, analyzes, and processes data once per cell instead of once for every placement of the cell

● **Uses design database hierarchy to reduce processing time, memory usage, and DRC result counts**

♦ **Can use hierarchical for every verification run**

Notes:

When Should I use Hierarchical Runs?

When Should I use Hierarchical Runs?

- ♦ **Multiple occurrences of cells**
- ♦ **If you have a hierarchical license available**
- ♦ **Every run (never a bad time)**

Notes:

DRC Debugging Techniques

DRC Debugging Techniques

The following tools/techniques make DRC debugging easier:

- ♦ **RuleCheck selection**

- ♦ **RuleCheck grouping**

- ♦ **Database window specification**

- ♦ **Cell exclusion**

- ♦ **Maximum results reporting**

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Notes:

How to Select Rules

From within Calibre Interactive:

♦ **Menu: Setup > Select Checks**
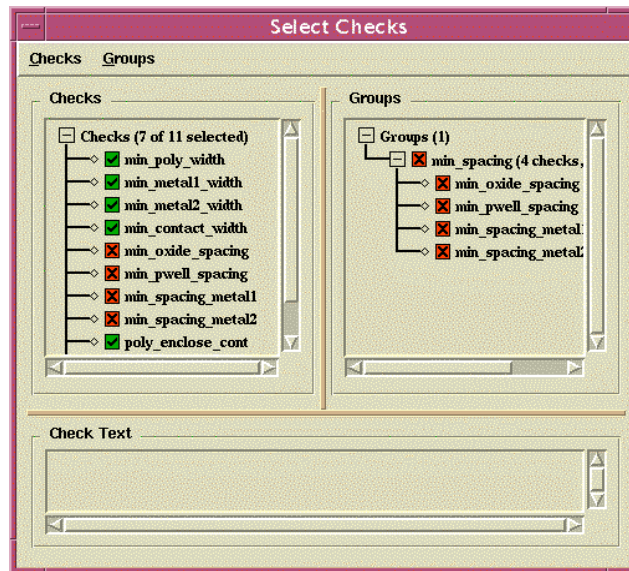
Notes:

How to Group Rules

How to Group Rules

- ♦ **Check just a certain group of rules
  (speed up verification time and minimize results on reports)**
- ♦ **Group rules according to type**
- ♦ **Very useful in combination with DRC (UN)SELECT CHECK**
- ♦ **Create RuleCheck groups inside the rules file using:**

  GROUP *name rule_check1… rule_checkN*

- ♦ **Use the "?" wildcard to match zero or more characters.**

- ♦ **Examples:**
  - **GROUP poly_layer_rules min_poly_width poly_over_metal2 metal1_over_poly**
  - **GROUP min_metal min_metal? metal3_min
    //includes min_metal1, min_metal2, and metal3_min**

Notes:

How to Check Just a Selected Area of the Layout—From Calibre Interactive

How to Check Just a Selected Area of the Layout— From Calibre Interactive

- ◆ **Select Check Area option**
- ◆ **Choose [. . .] button to enter the area using the layout editor**
- ◆ **Select area in the layout -- by creating a rectangle using the LMB**

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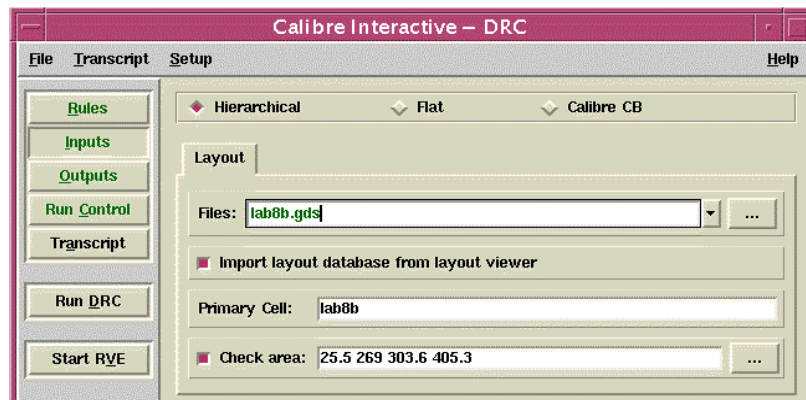
Notes:

How to Check Just a Selected Area of the Layout—From the Rule File

How to Check Just a Selected Area of the Layout— From the Rule File

LAYOUT WINDOW x1 y1 x2 y2 … nx ny

- ♦ **x1 y1 x2 y2 are the opposite coordinates of a rectangle (minimum requirements)**

- ♦ **May define a shape other then a rectangle by using more coordinates**

- ♦ **May have multiple LAYOUT WINDOW commands in the rule file**

Notes:

How to Check Just a Selected Area of the Layout—Boundary Crossing

How to Check Just a Selected Area of the Layout — Boundary Crossing

How are geometries that cross the boundary handled?

♦ **Default: Checks all polygons that cross boundary**

♦ **To clip it at the boundary: LAYOUT WINDOW CLIP yes**

♦ **Halo (only available from gui): Additional area region around selected area**

- **automatic:** the width is computed as half of the lesser of the width and height of the specified area
- **values:** user defined value
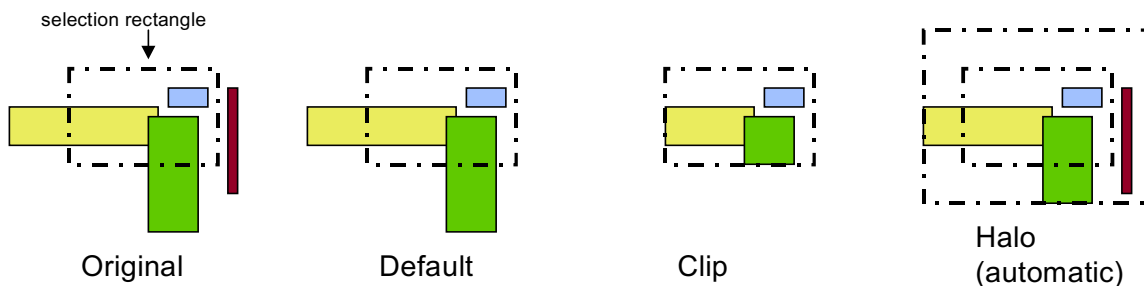
selection rectangle

Original   Default   Clip   Halo (automatic)

Notes:

Halo will clip. Halo will also "change" the coordinates displayed in the Summary Report.

How to Check Everything in the Layout *Except* a Specified Area

♦ **Need to define area in the rule file**

♦ **Unselect areas using this command in the rule file:**

LAYOUT WINDEL *x1 y1 x2 y2… xN yN*

- **Exclude a simple closed polygon window from DRC checking**
- **Window vertex coordinates are with respect to the top cell**
- **Polygons outside of or crossing the window border get processed**
- **May be specified multiple times**
- **Numeric variables may be passed as arguments**
- **Specifying only two pairs of non-collinear coordinates is interpreted as a rectangle**
- **Boundary crossing same behavior as LAYOUT WINDOW**

Notes:

How to Skip Cells During the DRC Check

How to Skip Cells During the DRC Check

- ◆ **Calibre normally checks every cell**

- ◆ **Cells can be skipped via the EXCLUDE CELL statement**

- ◆ **Allows you to ignore non-functional cells (for example, trademark and copyright information) or incomplete cells**

- ◆ **Add the following to the rules file:**

  EXCLUDE CELL *cell_name*

  - ● **Calibre will not process any objects from any placement of the excluded cell - including all hierarchical instances**
  - ● **Cell names can include wildcard characters: ***
  - ● **Not supported for binary and ASCII input database formats**

Notes:

How to Limit the Number of Discrepancies in the Report

How to Limit the Number of Discrepancies in the Report

To control the total number of results generated per RuleCheck, add the following to the rules file:

DRC MAXIMUM RESULTS *max | ALL*

- **Specifying ALL means that every result (error) for each RuleCheck gets reported and sent to the DRC Results Database. Use this setting for GDS database manipulation.**

- **The default is 1000 results per RuleCheck, after which a warning is issued and results output is suspended.**

- **If the default value is excessive, choose a smaller number.**

- **Avoid using ALL or numbers greater than 1000 for everyday use; the output becomes too great to manage efficiently.**

Notes:

Lab Information

Lab Information

In this lab you will:

- ◆ **Create a rule group**

- ◆ **Run DRC checks using only selected rules/groups**

- ◆ **Run DRC checks on specific areas of a layout**

- ◆ **Run DRC checks skipping cells**

Notes:

Lab: Advanced DRC Skills

In this lab you will experiment with various advanced DRC skills. These skills range from observing the value of hierarchical vs. flat DRC runs to learning the mechanics of creating and using Rule Groups to applying DRC checking to only certain areas of the cell.

Since you have made several DRC runs, the instructions for this lab assume you know the basics. New concepts are completely described, but tasks you have done several times before you are simply told to do. If you cannot remember exactly how to perform a task, look back at previous Labs.

List of Exercises

Exercise 4-1: Hierarchical vs. Flat DRC Runs

In all the previous labs, there have only been a few errors inside cells with only one instance in the design. In this lab, you will clearly see the benefits of running hierarchical DRC for tracking down where the discrepancies are really happening.

1. Change to the lab4 directory.
   ```
   cd $HOME/using_calbr/lab4
   ```

2. List the files in the directory.

   There should be the following four files in the directory:

   o golden_rules

   o lab4.gds

   o lab4_rules

   o layer_props.txt

   If any of these files are missing, please double check that you are in the correct directory, and then notify your instructor.

3. Launch DESIGNrev.
   ```
   calibredrv
   ```

4. Open the GDSII file, lab4.gds.

5. Load the layer properties file, layer_props.txt. (**Menu: Layer > Load Layer Properties**)

6. Launch Calibre Interactive DRC on cell lab4.

7. Tell Calibre Interactive that you will create a new runset.

   You should now have the layout viewer open displaying lab4.gds and the Calibre Interactive DRC window open with the default data loaded.

8. Enter the following **Inputs** data:

   Hierarchical, Flat or Calibre CB   Flat

   Layout Files: lab4.gds

   Import layout database from layout viewer: unselected

   Primary Cell: lab4

   Check Area   unselected

9. Enter the following **Rules** data:

   Calibre - DRC Rules File: lab4_rules

   Calibre - DRC Run Directory: .

10. Enter the following **Outputs** data:

    DRC Results Database File: lab4_flat.db

    Format: ASCII

    Start RVE after DRC finishes: selected

    Write DRC Summary Report: selected

    File: lab4_flat_report

    Replace File: selected

    View summary report after DRC finishes: selected

11. View the Transcript.

12. Choose **Run DRC**.

    How many discrepancies did you have?

    _____

    This layout has quite a few errors.

Do you think running in Hierarchal mode would help?

_____

Is this the type of design where you could gain benefits from hierarchy?

_____

13. Close the RVE and Summary Report windows.

14. Change the following DRC parameters:

    [Inputs] Hierarchical, Flat or Calibre CB: Hierarchical

    [Outputs] DRC Results Database File: lab4_hier.db

    [Outputs] DRC Summary Report File: lab4_hier_report

15. View the Transcript.

16. Run DRC again.

    How many errors do you have this time?

    _____

    What happened to the rest of the errors?

    _____

    This seems like a much more "fixable" amount of discrepancies than your first run.

    Now that you have seen the value of hierarchy, you are ready to learn how to use additional debugging concepts.

17. Close the RVE and Summary Report windows.

18. Leave Calibre Interactive DRC open.

Exercise 4-2: Create and Use Rule Groups

In this exercise you will edit the rule file to create groups of rules. You will then use these groups to aid in categorizing the type of discrepancies you are encountering.

1. Return to the Calibre Interactive Window - Rules.

2. View the lab4_rules file.

> What is in the file?

> _____

> Since it is a good practice to never edit your "golden" rule file, we will follow this practice in the lab. You will edit the lab4_rules file to create the Rule groups.

> First, what is the syntax for grouping commands using the rule file?

> _____

> (The answer was in the lecture or you can look it up in the *Standard Verification Rule Format (SVRF) Manual*.)

3. Open the golden_rule file in a new window.

    a. In the text window displaying the lab4_rules file, choose **Menu: File > Open**.

    b. Select "golden_rules" from the list of files.

    c. Choose **OK**.

    d. In the resulting Open File dialog box, choose **New Window**.

You will notice that the golden_rule file naturally groups the rules by three categories. What are they?

_____

_____

_____

What rules are under each group?

Group 1:

_____

_____

_____

_____

Group 2:

_____

_____

_____

_____

_____

_____

Group 3:

_____

Now you have enough information to write the rule groups.

4. Click on the Edit button in the lower right of the lab4_rules window.

    This changes the Edit button from red to green, indicating that the file is editable.

5. Using the group names: "min_width", "min_spacing", and "min_extent" write the "rule grouping" rules in the lab4_rule file.

6. Save the lab4_rules file.

7. In the Calibre Interactive Window, choose **Load** to load the edited rule file.

    Note   If you have an error in the syntax or a non-existent rule (typo in the rule name), you will receive an error message when you try to load the new rule file. Correct any problems and try to load the rules again.

8. Close the lab4_rules window and the golden_rules window.

9. Choose **Menu: Setup > Select Checks**.

This opens the Select Checks window. It should look similar to below.
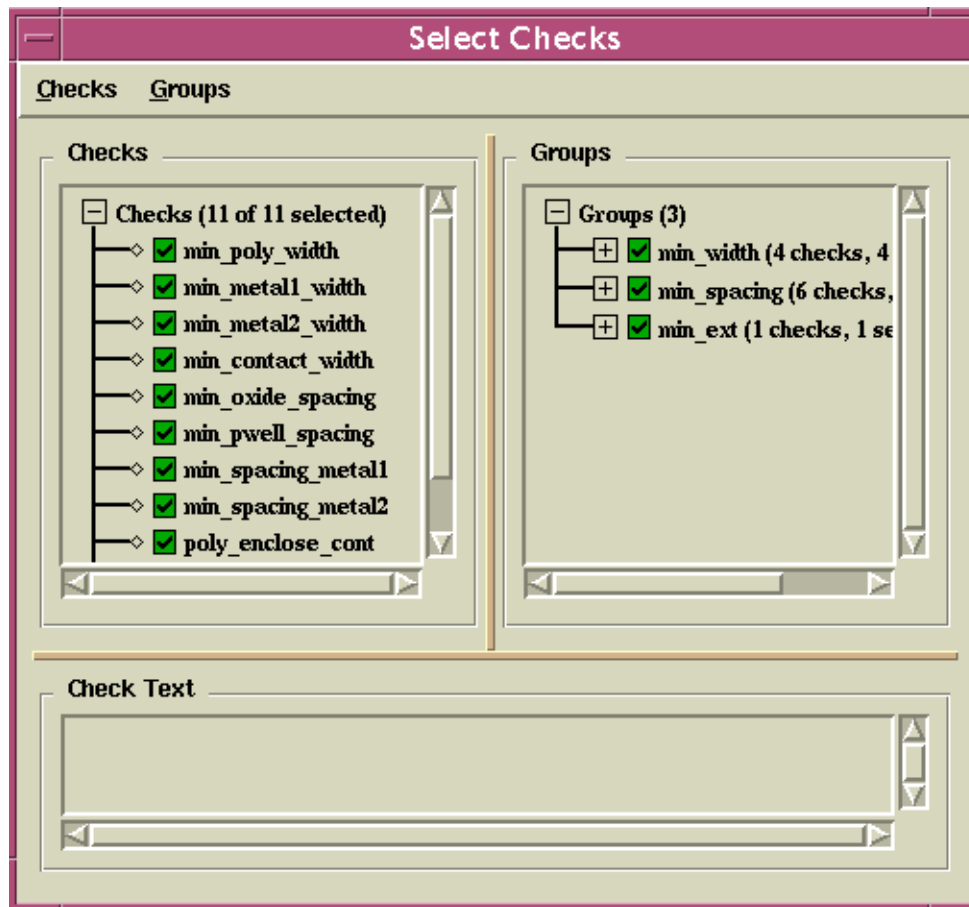
Take note of the Groups and the number of rules in each group. Make sure that your groups match those in the illustration. If not, go back and edit your rule file to make them match.

First you are only going to run min_width checks.

10. Choose **Menu: Checks > Unselect All Checks**.

Notice that all the rules now have a red "x" in front of them. This is a flag that this rule will not be checked.

11. Click on the min_width name in the Groups list box.

This toggles the rules selection back to green. It also changes the rules in that group back to green in the Checks list box. The window should look similar to below.
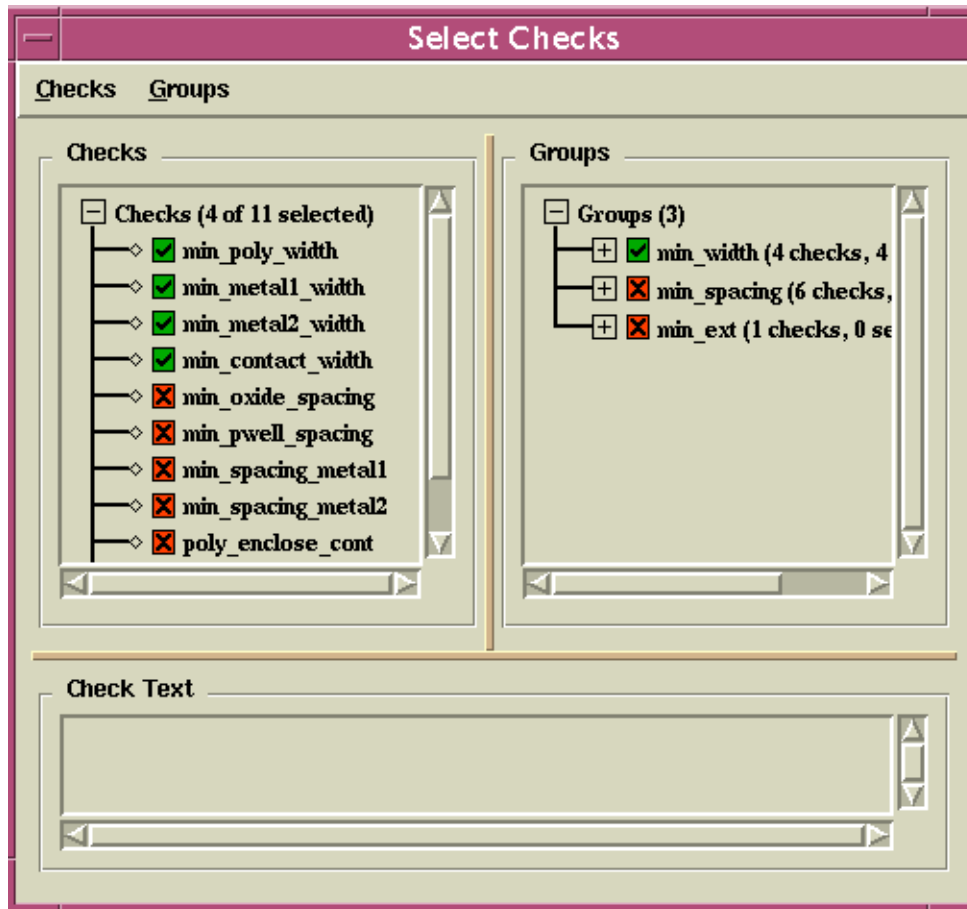
12. Run DRC again.
    (Notice it is not necessary to close the Select Checks window.)

    How many errors do you have this time?

    _____

    Are these errors only from the rules in the selected group?

    _____

13. Close the RVE and Summary Report windows.

14. Spend some time experimenting with the rules selection feature.

15. When you are done experimenting, make sure all rules are selected, close the Select Rules window, and close any open RVE or Summary report windows you may have opened during your experiments.

Exercise 4-3: Run DRC Checking on a Select Area

In this exercise you will run the DRC checks on just a selected area in the layout.

1. Make the Calibre Interactive DRC window active.

2. Display the Inputs.

3. Select the Check Area option button.

     What happens?

     _____

     You need to define the area you wish to check.

4. Choose the [...] button from the end of the Check Area text box.

   This gives you an information box telling you that it is waiting for input.
   Ignore this message for now.

   Waiting for layout

   ⓘ   Waiting for DRC area coordinates from layout viewer

   [Cancel]

   ---
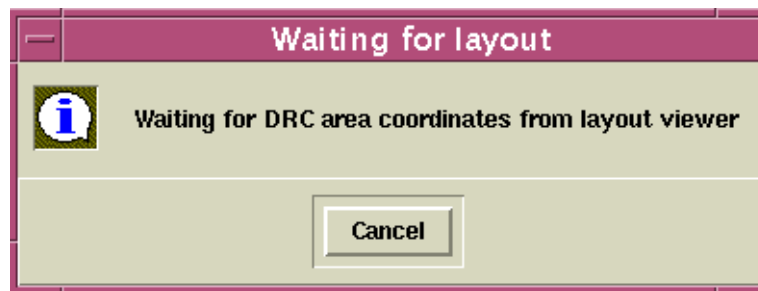
5. Make the Layout Viewer window active.

6. Hold down the LMB and draw a rectangle around the desired area.
   (Any area in the layout will do for this step.)

7. Release the LMB.

What happened in the Calibre Interactive window?

_____

_____

8. Run DRC.

    What kind of results do you get?

    _____

9. Close the DRC Summary Report and RVE windows.

10. Experiment several times with making area DRC runs until you are comfortable with the process.

11. Answer the following questions.

    Can you tell in RVE that you only checked part of the layout?

    _____

    Can you tell in the Summary Report that you only checked part of the layout?

    _____

    Can you tell in the Transcript that you only checked part of the layout? Hint: Use **Menu: Transcript > Search** in Calibre Interactive and look for the phrase "LAYOUT WINDOW".

    _____

    When would this be a useful tool?

    _____

12. Close any open RVE and Summary Report windows.

13. Unselect Check Area in the Calibre Interactive DRC Inputs window.

Exercise 4-4: Run DRC Skipping Cells

Often you will want to start running DRC before a design is completely finished. To avoid sorting out the errors in incomplete cells, it is easier to just skip them. In this exercise, you will learn how to skip cells.

1. Make the Calibre Interactive DRC window active.

2. Display the lab4_rules file for edit.

3. Find the command syntax you would add to a rule file to exclude a cell. Hint: Look either in the lecture or in the *SVRF Manual*.

    What is it?

    _____

    What would the command to exclude cell a2311 look like?

    _____

4. Enter this command to the lab4_rules rule file.

5. Save the file.

6. Load the rule file.

7. Run DRC.

    What kind of results did you get?

    _____

    Does this give you an idea where a large number of the problems are located?

    _____

8. Close any RVE and Summary Report windows.

9. Re-edit the lab4_rules file to comment out the EXCLUDE CELL statement. (Add // to the beginning of the line.)

10. Save the rule file.

11. Load the rule file.

Exercise 4-5: Displaying Hierarchical Results in Different Ways

In this exercise you will display hierarchical results in two different ways:

- Displaying errors on the top level of the hierarchy

- Displaying errors within the child cell with the error

1. Return to the Calibre Interactive—DRC window.

2. Choose **Menu: Setup > DRC Options**.

    This adds an additional menu button, DRC Options, to the left side of the window.

3. Choose the **DRC Options** menu button.

4. Choose the **Output** tab.

5. Select "Output cell errors in cell space" option.

The Calibre Interactive window should look similar to below.
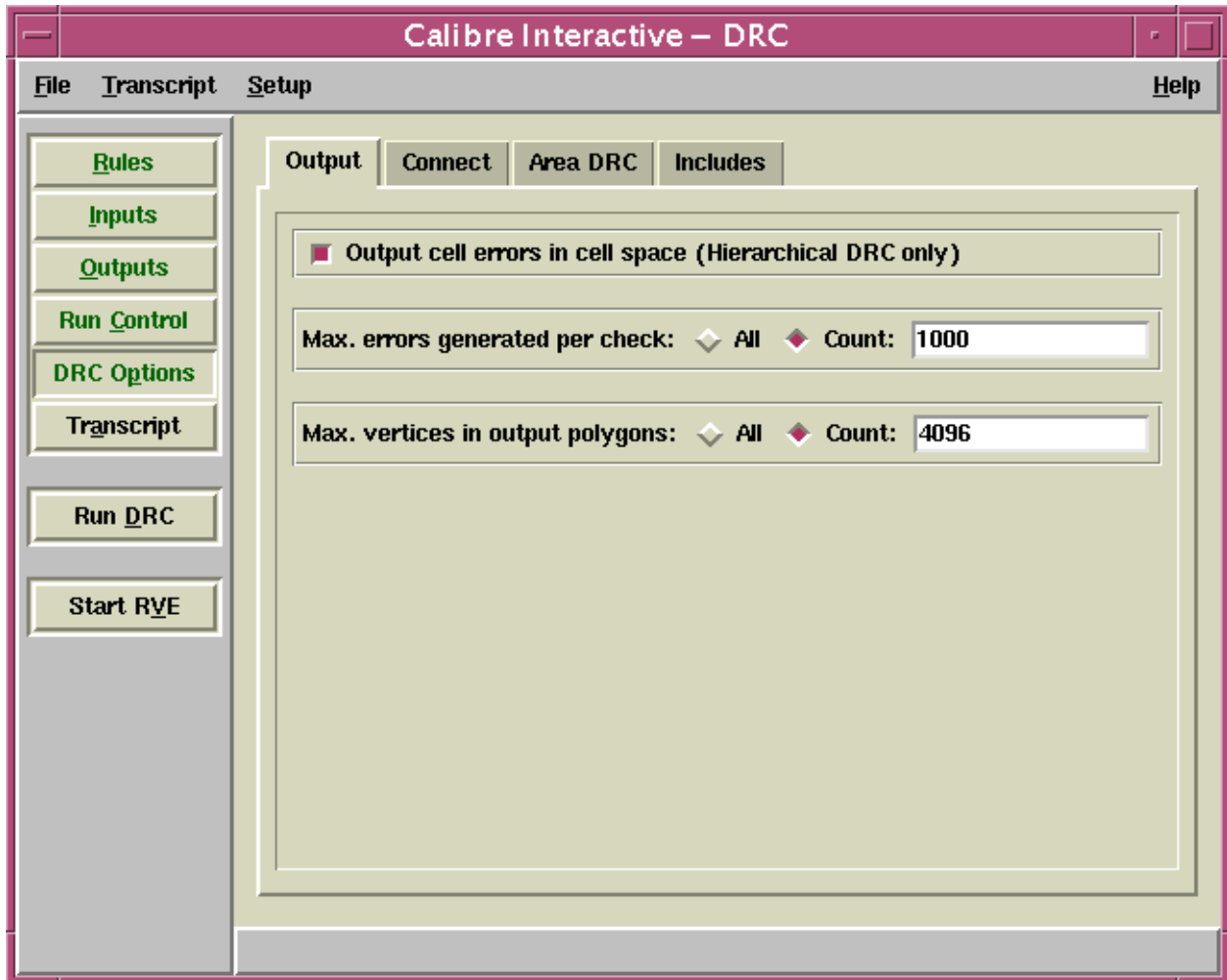
Older versions of Calibre Interactive do not offer the "Output cell errors in cell space" option. If your version of Calibre does not have this option, you will need to add the line:

Note

```
DRC CELL NAME YES CELL SPACE XFORM
```

to the lab4_rule file.
(You will also need to save and load the updated rule file.)

6. Choose **Run DRC**.

The error tree should look similar to below.
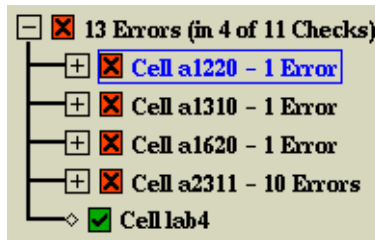
How is this display different from the previous error trees?

_____

To make all your viewing options available all the time, you need to make highlighting in context the default. (You can then turn it off when desired.)

7. In RVE, choose **Menu: Setup > Options**.

   This opens the Setup DRC—RVE Options dialog box.

8. Choose the **View** tab.

9. From the Highlight menu settings drop down menu, select **Highlight in Context**.

10. Choose **Apply**.

11. Choose **OK** to close the Setup DRC—RVE Options dialog box.

12. In the RVE window, select **Menu: Highlight > Highlight in Context**.

13. Open the RVE error tree for cell a1310.

14. Select the error.
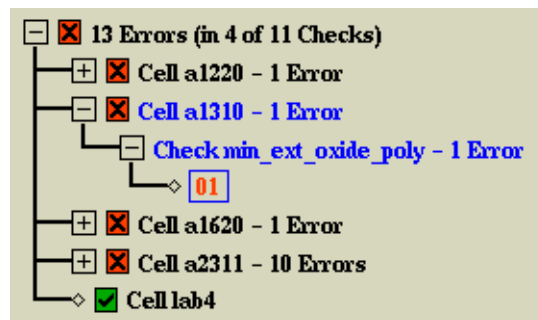
15. Highlight this error by choosing the **Highlight** icon. ⬛ H

    This opens the a1310 cells and zooms into the error.
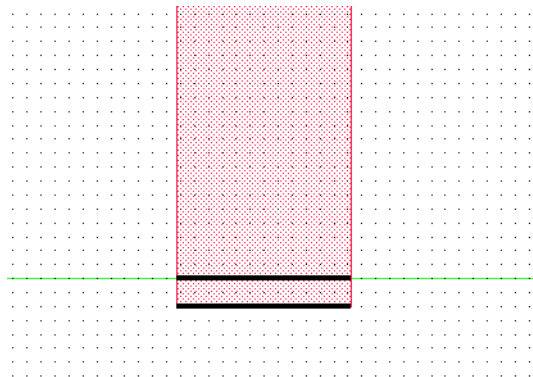
16. Return to the RVE window and erase the highlight.

17. In the RVE window, unselect **Menu: Highlight > Highlight in Context**.

18. Choose **Highlight** again.

This displays the error in the context of the top cell (lab4).
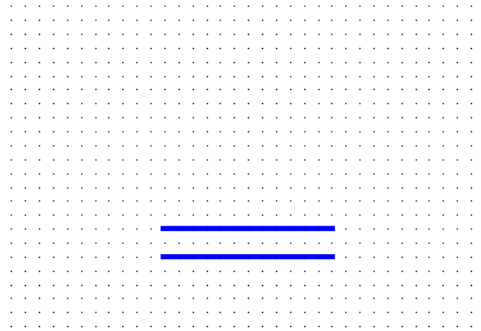
Depending on your editing needs or preferred editing style, you can display the results either way to fit your needs.

19. If you have time, experiment displaying the other errors in various ways.

20. When you are ready to go to the next exercise, erase all highlights.

Exercise 4-6: Correcting Errors

This is a free-form exercise. There are 13 errors in the layout. Using the skills you learn in this lab (and all the previous ones) see how many of the errors you can correct in the time remaining.

Don't forget to change the layout file to a new name and select "Import layout database for layout viewer" in the Calibre Interactive [Inputs] window so changes are reflected in the DRC run.

Good Luck!

When you are finished with this lab, close all Calibre related windows. (Including DESIGNrev, Calibre Interactive DRC, RVE, and Summary Report.)

Module 5
Texting

Objectives

At the completion of this lecture and lab you should be able to:

- Use text to provide initial correspondence points for LVS

- Identify and correct the following texting problems:

    o Net or port names that are difference from the source

    o Identically named objects with different connectivity

    o Text annotations in lower-level cells that are not present in the source

    o Multiple names on the same layout net

    o Text placed in the wrong location in the layout

    o Text placed in the wrong layer in the layout

- Describe a port and its use

How to Place Text into the Layout

How to Place Text into the Layout

♦ **Place free-standing text directly with the layout editor**

New Text
Layer 50   Text VSS
◇ Use Location ->   X Y, dbu 0 0   Place
◆ Place Manually   ▪ Repeat   Cancel
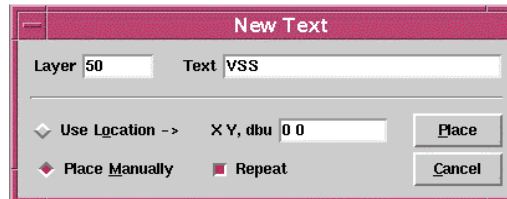
♦ **Place text objects indirectly using Rule file statements**

- **LAYOUT TEXT** *name location layer cell_name*

- **TEXT** *name location layer*

♦ **The TEXT statement always places text in the top cell**

Notes:

LAYOUT TEXT creates objects in both the intermediate GDSII and in the Calibre database. (Good for generation of new GDSII data.)

TEXT just adds the information to the Calibre Database.

You may need to add text using Calibre rules rather than directly to the layout because the layout needs to stay clean.

What are Initial Correspondence Points?

What are Initial Correspondence Points?

- ♦ **Pairs of nets or ports which have identical user-given names in the source and the layout**

- ♦ **Good practice to name the ports of the top-level cell and the major nets in the design**

- ♦ **"Information and Warning" section of the LVS report lists the Initial Correspondence Points**

- ♦ **Do not confuse with matching cell names**

- ♦ **Use the report to resolve circuit ambiguities between the source and the layout**

- ♦ **Improves processing performance**

Notes:

Example of Initial Correspondence Points Report

Example of Initial Correspondence Points Report

LVS Report

```
**********************************************************************
                    INFORMATION AND WARNINGS
**********************************************************************
```

```
// SPECIFY INITIAL CORRESPONDENCE POINTS
LAYOUT TEXT VDD  80.0   3.0 50 top_cell
LAYOUT TEXT VSS  60.0  10.0 50 top_cell
LAYOUT TEXT SEL 120.0 260.0 50 top_cell
        •
        •
        •
```

Excerpt from rule file

```
                        1        1         0        0    a1720
                       10       10         0        0    a2311
                    -------  -------  ---------  --
        Total Inst:      48       48         0
```

LVS reports the names of user-given correspondence points

```
o Initial Correspondence Points:

    Nets:       VDD VSS SEL D0 D1 D2 D3 Q0 Q1
```

Notes:

How to Use Text to Establish Initial Correspondence Points

How to Use Text to Establish Initial Correspondence Points

Prerequisites for successful texting of nets and ports:

♦ **Specify which layers are valid text layers**

♦ **Establish connectivity of target object layers**

♦ **Attach the text labels to target objects**
- **Via text layout objects or SVRF statements**
- **Apply syntax rules to user-given text names**

Notes:

What Syntax Rules Apply to Text Names?

What Syntax Rules Apply to Text Names?

- ◆ **For layout databases apply these rules:**
    - ● **Name cannot begin with n$, N$, or l$**
    - ● **Names can only contain one leading "/" character**
- ◆ **For a user-given name to be valid in SPICE netlists:**
    - ● **Name must contain at least one Non-numeric character**
    - ● **Name can only contain one leading "/" character**

Notes:

When to Use LAYOUT TEXT Placements

When to Use LAYOUT TEXT Placements

♦ **Places text using rule file statements**

♦ **LAYOUT TEXT Placements**

- **Behave exactly as if the designer placed text with the layout editor**

- **Attach to the cell using cell-space coordinates**

- **Obey TEXT LAYER and TEXT DEPTH statements**

♦ **Example**

LAYER M2_TXT 50   // Define the layer

TEXT LAYER M2_TXT   // Define layer as a text layer

LAYOUT TEXT CLOCK 10.5 16.8 M2_TXT NAND2   // place text

Notes:

When to Use TEXT Placements

When to Use TEXT Placements

♦ **TEXT Objects**

- **Can edit (overwrite) existing database text**
- **Attach only to top-level cell using top-cell coordinates**
- **Do not obey TEXT LAYER or TEXT DEPTH statements**

♦ **Example:**

TEXT RESET 20.0 12.5 METAL1

Notes:

How to Specify Which Layers are Valid Text Layers

How to Specify Which Layers are Valid Text Layers

♦ **To designate a layer to contain free-standing text objects:**

- **TEXT LAYER layerN**

- **Example:**

  LAYER m_txt 50   // assign label "m_txt" to layer 50

  TEXT LAYER m_txt   //m_txt contains text objects

♦ **To designate a layer to contain port text objects:**

- **PORT LAYER TEXT layerN**

- **Example:**

  LAYER p_txt 51   //assign label "p_txt" to layer 50

  PORT LAYER TEXT p_txt   //p_txt contains port text

Notes:

How to Filter Unwanted Text Objects

How to Filter Unwanted Text Objects

♦ **Specify hierarchical depth for text recognition**

TEXT DEPTH ALL | PRIMARY | *number*

- **ALL uses text from all levels of the hierarchy (default)**

- **PRIMARY only uses text from the top-level cell**

- *number* **specifies recognition of all text from top level through level** *number*, **where 0 equals the top level**

- **This does not apply to text placed with the TEXT statement, which is read only from the top-level cell**

♦ **Example:**

TEXT DEPTH PRIMARY   **// ignore superfluous text**
                          // in the low-level cells

Notes:

How to Attach Text Labels to Target Objects

How to Attach Text Labels to Target Objects

- ♦ **Choose one of the following methodologies:**
  - ● **Explicit Attachment (highest priority) — requires an ATTACH statement**
  - ● **Implicit Attachment (lower priority) — requires text layer and target layer to be the same**
  - ● **Free Attachment (lowest priority) — requires a LABEL ORDER statement**
- ♦ **Target object layers must appear directly in or be derived (with net preserving operations) from one of these**
  - ● **CONNECT**
  - ● **SCONNECT**
  - ● **STAMP**
  - ● **POLYNET**

Notes:

Example of Explicitly Attached Text

Example of Explicitly Attached Text
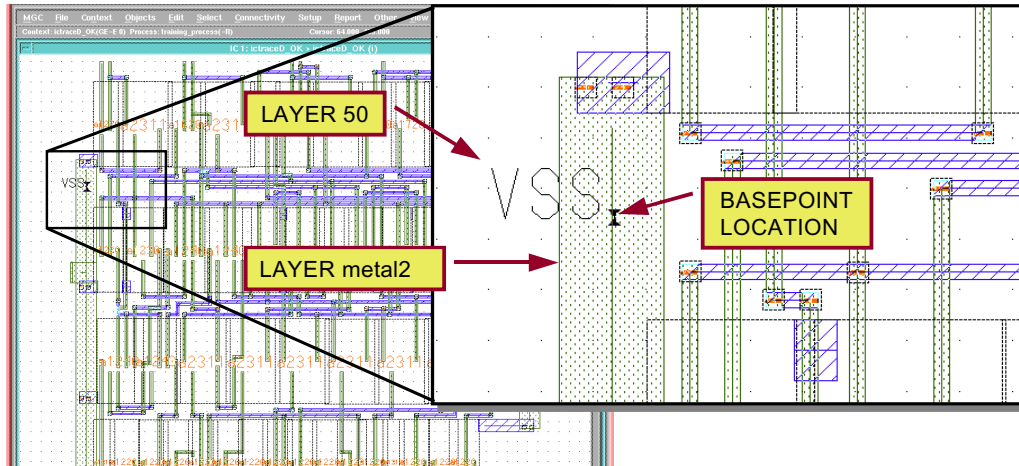
CONNECT metal1 metal2 BY via	// ESTABLISH CONNECTIVITY
TEXT LAYER 50	// SPECIFY LAYER 50 AS A TEXT LAYER
ATTACH 50 metal2	// ATTACH TEXT TO TARGET LAYER

Notes:

Example of Implicitly Attached Text

Example of Implicitly Attached Text

TEXT LAYER metal2	//specify metal2 as a text layer
CONNECT metal1 metal2 BY via	//establish connectivity
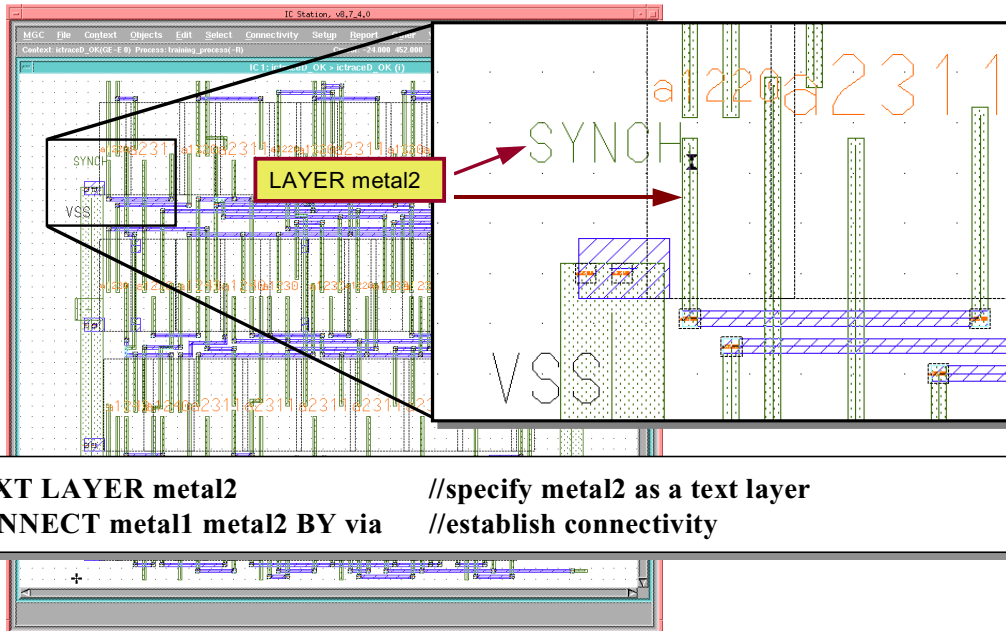
Notes:

Example of Freely Attached Text

Example of Freely Attached Text
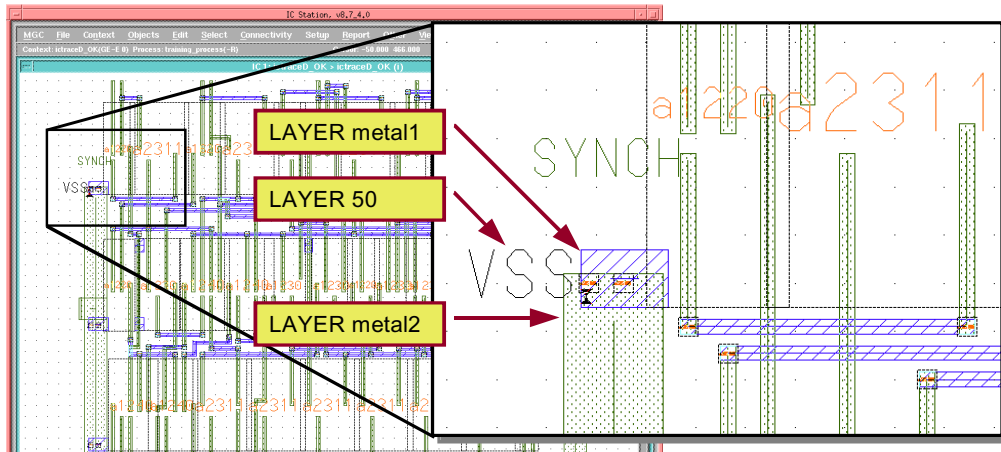
CONNECT metal1 metal2 BY via	**// ESTABLISH CONNECTIVITY**
TEXT LAYER 50	**// SPECIFY LAYER 50 AS A TEXT LAYER**
LABEL ORDER metal1 metal2	**// SPECIFY ATTACHMENT PRIORITY**

Notes:

What about Case Sensitivity?

What about Case Sensitivity?

♦ **Calibre treats all SPICE netlist names as case insensitive by default**

♦ **You can control case sensitivity through rules file commands**

♦ **Similar to other rule statements**

Notes:

How to Control Case Sensitivity

How to Control Case Sensitivity

♦ **Controlled by statement in rules file**

♦ **Applies to model names, node names, subcircuit names, and user-defined parameter names**

LAYOUT CASE NO | YES

SOURCE CASE NO | YES

● **NO (default) — Calibre treats names as case-insensitive**

● **YES — Calibre treats names as case-sensitive**

♦ **Calibre applies case sensitivity when the source or layout netlists are read into the application**

♦ **LAYOUT CASE and SOURCE CASE statements are independent and do not need to be specified together**

♦ **These statements only apply to SPICE netlists**

Notes:

How to Control Case Sensitivity During LVS

How to Control Case Sensitivity During LVS

♦ **Controlled by statement in rules file**

LVS COMPARE CASE YES | NO [NAMES] [TYPES] [SUBTYPES]

- **YES — all comparisons are case sensitive
  (LAYOUT CASE and SOURCE CASE should also be set to YES)**

- **NO — all comparisons are case-insensitive**

- **NAMES — net, instance, and port names are case-sensitive**

- **TYPES — components types are case-sensitive**

- **SUBTYPES — component subtypes are case-sensitive**

♦ **If you are using case sensitivity, the Hcell list automatically becomes case-sensitive**

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Notes:

How to Identify Unmatched Text Names

How to Identify Unmatched Text Names

- ◆ **LVS generates a warning if the connectivity of a layout net matches the source, but the two net names do not match**
  - ● **This behavior also applies to ports**
  - ● **LVS reports no discrepancies if the circuit connectivity matches regardless of incorrect user-given names**
- ◆ **EXAMPLE:**
  - ● **A net is named RESET in the source circuit but is named RST in the layout. Calibre issues a warning message, but does not generate any error messages.**
    (The connectivity does match the source!)
  - ● **How to fix the problem — correct the name in the layout**

Notes:

Example: Report of Unmatched Text Names

LVS Report

```
**************************************************************************
                    INFORMATION AND WARNINGS
**************************************************************************


              Matched    Matched    Unmatched    Unmatched    Component
              Layout     Source      Layout       Source       Type
              -------    -------    ---------    ---------    ---------
Ports:              0          0            0            0

Nets:              63         63            0            0

Instances:         22         22            0            0        a1220
                    5          5            0            0        a1230
                    4          4            0            0        a1240
                    3          3            0            0
                    3          3            0            0
                    1          1            0            0
                   10         10            0            0
              -------    -------    ---------    ---------
Total Inst:        48         48            0            0

o Layout Names That Are Missing In The Source:

   Nets:        RST
```

LVS warns that the net names do not match

Notes:

How to Identify Incorrectly Placed Text in the Layout

How to Identify Incorrectly Placed Text in the Layout

- ◆ **Incorrectly placed text may cause one of these results:**

  - ● **LVS Generates a warning if two or more different names are found on a single net**
    Calibre LVS chooses a power/ground name if found, otherwise it will choose the first name alphabetically and discard any other names it finds

  - ● **LVS generates a warning if you attempt to assign the same name to two or more nets**
    Calibre LVS arbitrarily chooses one net and leaves the other net unnamed

  - ● **LVS generates a discrepancy if the misplaced text name matches a valid source net name**

- ◆ **To resolve these errors, check the following:**

  - ● **Text location, layer, and cell parameters**

  - ● **Text label attachments rules (priority, LABEL ORDER, etc.)**

Notes:

How to Identify when LVS does not Recognize Text

How to Identify when LVS does not Recognize Text

♦ **Text not found in the layout may cause one of these results:**

- **Features dependent on power/ground names will not work**

    – **Short-circuit isolation on the power/ground nets**

    – **Logic gate recognition**

    – **LVS ABORT ON SUPPLY ERROR specification**
        Good idea to use this feature to avoid billions and billions of errors

- **Lose all benefits of initial correspondence points**

    – **Circuit ambiguity resolution is lost**

    – **Improved run-time execution is lost**

♦ **To resolve these issues, check the following:**

- **Text location, layer, and cell parameters**

- **Text layer assignment rules**

Notes:

How to Identify Power/Ground Texting Problems

How to Identify Power/Ground Texting Problems

Incorrectly named power/ground nets may cause one of these results:

♦ **LVS reports "Badly formed power/ground net name" error if the name violates the syntax rules**

♦ **LVS reports "Contradictory power/ground net name" error if the same name is used for both a power and a ground net**

♦ **LVS aborts with the OVERALL COMPARISION RESULTS listed as "NOT COMPARED"**

This is overridden by LVS ABORT ON SUPPLY ERROR NO

Notes:

What is a Port?

What is a Port?

♦ **Ports of a cell form the external interface of the cell**

♦ **A port can consist of any number of shapes and paths on any number of layers**

♦ **Top-level layout ports must be labeled with port text to insure correct generation of the extracted netlist**

♦ **Initial Correspondence Points and Ports**
- ● **Specify initial correspondence points on ports of the top level cell in the source and layout by adding port text to the input pins**
- ● **Add port text objects in layout**
- ● **Use LAYOUT TEXT and PORT LAYER TEXT statements in Rule file as appropriate**

Notes:

How to Use Port Texting

How to Use Port Texting

- ◆ **Defining Ports**
  - ● **Ports are specified for the top level cell using PORT LAYER TEXT and PORT LAYER POLYGON specification statements in the rule file**
- ◆ **Port Text and Polygon Objects**
  - ● **Text and polygons on port layers are read and treated as ports**
  - ● **Port Layer Text supports text objects where the port's layer, location, and name are the same as the layer, location, and value of the text object**
  - ● **Text and geometries defined in the rule file with the TEXT and POLYGON statements cannot become ports**
- ◆ **What if Port Texting is incorrect:**
  - ● **Shorts**
  - ● **Opens**
  - ● **Wrong connections**

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Notes:

Lab Information

Lab Information

In this lab you will:

- ◆ **Find mismatched text names**
- ◆ **Find badly placed text**
- ◆ **Find non-functional text labels**
- ◆ **Review the Initial Correspondence report**

Notes:

Lab: Texting

In this lab, you will explore three different types of texting problems using Calibre LVS. Since you have not been "formally" introduced to LVS, much of the data will be loaded via runsets. This will allow you to concentrate on the main focus of this lab, texting.

List of Exercises

Exercise 5-1: Find a Misspelled Layout Text Label

Exercise 5-2: Find a Badly Placed Layout Text Label

Exercise 5-3: Find Non-functional Text Annotations

Exercise 5-1: Find a Misspelled Layout Text Label

In this lab you will learn how Calibre deals with a misspelled text label.

1. Change to the lab5 directory.
   ```
   cd $HOME/using_calbr/lab5
   ```

2. List the files in the directory.

   There should be the following 14 files in the directory:

cell_file	lab5a_runset	lab5b_runset	lab5d_runset
golden_rules	lab5a_source.spi	lab5b_source.spi	lab5d_source.spi
lab5_rules	lab5b.gds	lab5d.gds	layer_props.txt
lab5a.gds	lab5b_rules		

   If any of these files are missing, please double check that you are in the correct directory, and then notify your instructor.

3. Launch DESIGNrev.

4. Open lab5a.gds.

5. Load the layer properties. (layer_props.txt)

6. Launch Calibre Interactive LVS on cell, lab5.

7. Use lab5a_runset as the runset.

The Calibre Interactive LVS window should look similar to below.
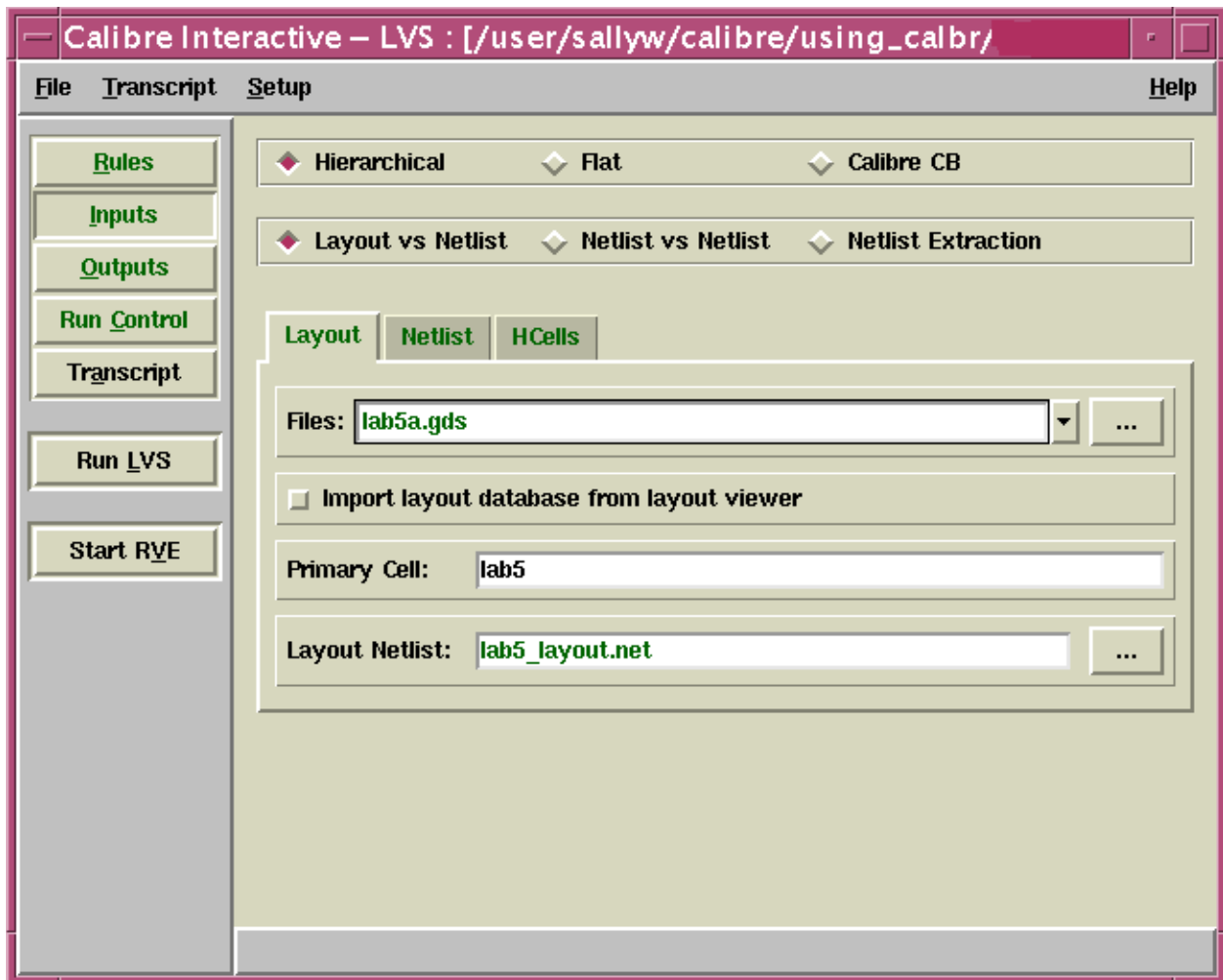
You will cover the details of this window in future Modules, for now you will only deal with texting and that information is contained in the rule file.

8. View the rule file. (Under the **Rules** tab.)
    (It should be lab5_rules.)

    What layer is the text layer?

    _____

What layers are connected to the text layer?

_____

What LAYOUT TEXT exists in the rule file?

_____

9. Leave the rule file open.

10. Choose Menu Button, **Run LVS**, to perform an LVS run.

   At the end of the LVS run, Calibre opens the LVS Report and opens RVE.

   What are the results? Did it pass LVS?

   _____

   Calibre sucesfully matched all the instances and nets. The next couple of step will show you how Calibre helped you match all the nets.

11. Find the Initial Correspondence section for cell lab5 in the report.

   Based on the LAYOUT TEXT in the rule file, what would you expect to find in the Initial Correspondence Report?

   _____

   What is in the Report?

   _____

   Why are you missing one of the Initial Correspondence points?

   _____

   How would you verify this?

   _____

You are going to open the Source Netlist to see if RESETT exists.

12. Return to the LVS RVE window.

    In the left column, there are two groups of information: Input Files and Output Files.

13. Click on "Source Netlist" to open a copy of the source netlist.
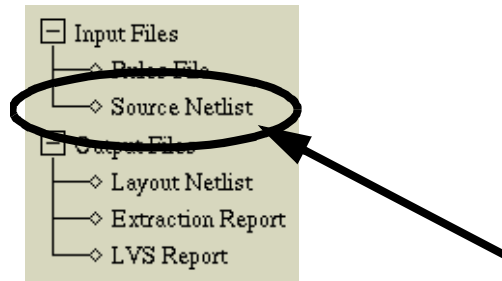
    This opens a new window with the source netlist loaded. Again, we will cover how to use this window's more powerful features in future labs. Right now you just need to find if RESETT exists.

14. In the Source Netlist window, Choose **Menu: Go > Search**.

    This opens the Text Search dialog box.

15. Enter RESETT.

16. Choose **Find from Top**, to begin the search.

    Did you find it?

    _____

17. Try search for just part of the word, RESE.

    Did you find anything?

    _____

What did you find?

_____

It appears that you have a typo in the lab5_rules file.

18. Correct the error in the rule file.

19. Re-run LVS.

What does the Initial Correspondence section for cell lab5 of the report contain now?

_____

What did you learn in this exercise?

_____

_____

20. Close the rule file.

21. Close all Calibre windows except DESIGNrev.

Exercise 5-2: Find a Badly Placed Layout Text Label

In this lab, you will see the results of a badly place text label. You will also learn two ways to fix the problem.

1. Make DESIGNrev active.

2. Open the layout for this exercise, lab5b.gds.

3. Load the layer properties. (layer_props.txt)

4. Launch Calibre Interactive LVS.

5. load lab5b_runset as the runset.

    This prepares you for the next LVS run.

6. Choose **Run LVS**.

    What are the results?

    _____

7. Using information you can find in RVE (you may need to expand trees or open windows), answer the following questions:

    What cell(s) have the discrepancies?

    _____

    What kind of discrepancy?

    _____

    What are the names of the two layout nets with the problem?

    _____

    _____

8. Open the Source Netlist.

9. Open the Layout Netlist.

10. Close the LVS Report.

11. Adjust all your windows so you can see the DESIGNrev, RVE, Source Netlist, and Layout Netlist.
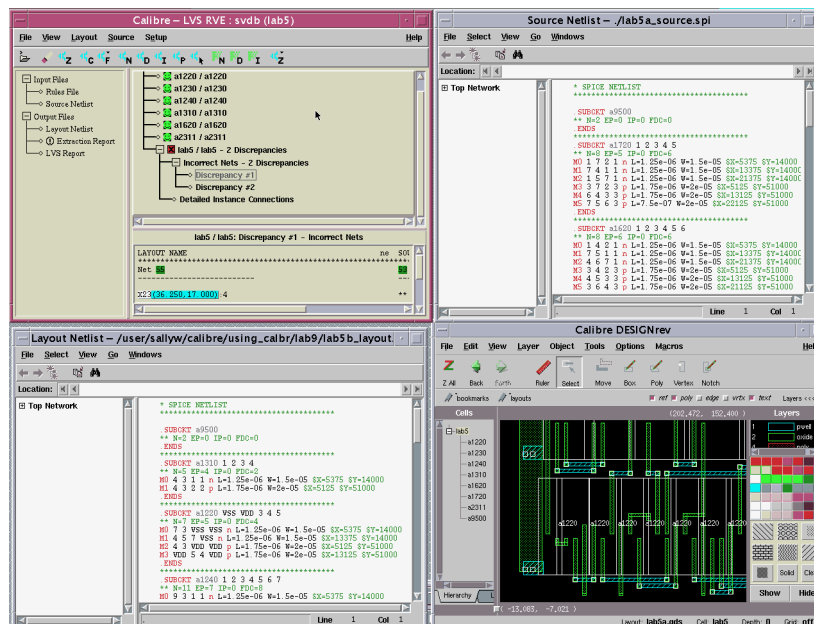
12. Set the RVE Zoom settings to 0.4 and unselect the clear previous highlights option.

13. Using RVE, display all the information for discrepancy 1.

14. Double-click on the layout net 55.

     Notice that the net highlights in the Netlist and in the layout viewer.

15. Display the details for the second discrepancy.

16. Double-click on layout net RESET.

     The problem should be somewhere within these highlights.

What are the Layout and Source Netlist lines containing RESET?

Source: _____

Layout: _____

There is a problem, the layout instance does not even have the correct number of pins.

17. Double-click on X17 in the Source netlist.

    This will highlight its "match" in the Layout netlist and in the layout itself.

    Which instance "matches" X17 in the layout?

    _____

    Since RESET is common to both the Source and the Layout, finding RESET is a good starting point.

    Next you will return to the layout and see if you can find where RESET is currently attached. First you will need to erase the highlights to make it easier to see what you are doing.

18. Choose the **Eraser** icon from the RVE Toolbar.

19. Make the DESIGNrev window active.

20. Zoom into the display so it is easy to see the instances involved in the discrepancy.

21. Choose **Menu: Object > Find Text**.

    This opens the Find Text dialog box.

22. Enter RESET in the text box.

23. Select Exact.

24. Select Keep current View for the View.

25. Select All Cells as the option.

26. Choose **Find**.

> A *very* small yellow box appears at the point of the text in the
> layout. You may need to move the Find Text dialog box so it is not
> **Note** obstructing any of the layout.

Do not close the Find Text dialog box yet.

27. Using RVE, highlight X17 and net RESET in the source netlist.

The layout should appear similar to below.
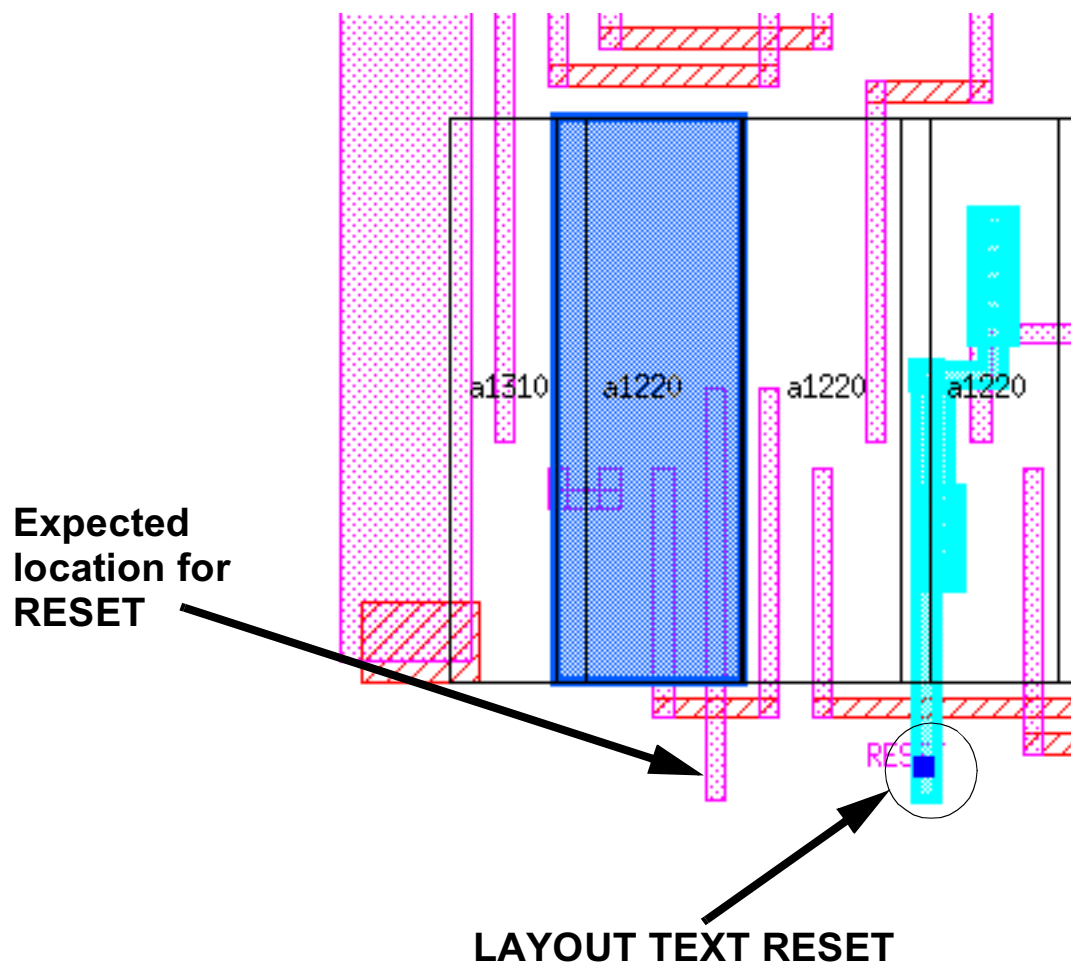
Note that the layout net labeled RESET does not connect to layout cell instance X23. It looks like someone placed the layout text RESET object on the wrong net!

Now we will spend some time examining how the X23 is connected in the layout versus how X17 is connected in the source netlist.

28. Click the LMB once over each of the I/O pins of X23 in the layout netlist. (Nets 55, 54, and 14)

    Note than when you select layout net 55 source net 53 highlights. Since source net 53 does not connect to source instance X17, this appears to be the problem. The layout net 55 should be identified (texted) as RESET.

    You need to move the layout text to the correct net.

29. Make sure Select is selected in the Toolbar.

30. Unselect everything except Text from the object selection list in the upper right of the DESIGNrev window.
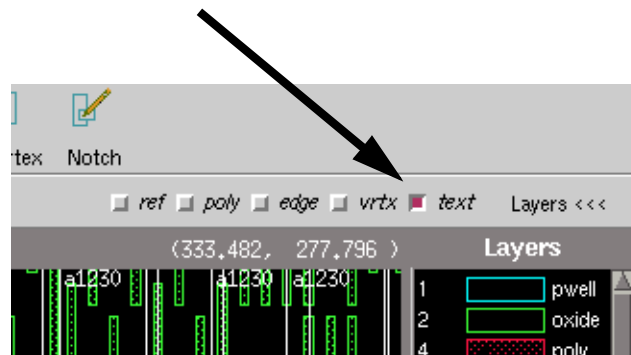
31. Click on the yellow highlight resulting from the Find Text operation.

32. Select **Move** from the Toolbar.

33. Move the text so it is centered in its expected net.

34. Unselect everything. (Type "u".)

35. Choose **Find** in the Find Text dialog box again.

    This checks that the text moved as expected.

36. Close all RVE windows, including the netlist windows and RVE itself.

37. Return to the Calibre Interactive window.

38. Choose the **Inputs** menu button.

39. Change the Layout File from: "lab5b.gds" to "lab5b_fixed.gds".

40. Select the **Import layout database from layout viewer** option.

    By making these two changes you are loading your changes directly from DESIGNrev without saving the layout first. You are also creating a new GDSII, so you are not overwriting your existing file.

41. Run LVS again.

42. If you are asked to save the file, choose **Yes**.

    Did that fix the problem?

    _____

    If that did not fix the problem, try moving the text again until you are sure it is connected to the net.

43. Close RVE and all related window.

44. Return to DESIGNrev.

45. Delete the text.

46. Make the Calibre Interactive LVS window active.

47. Edit the rule file by un-commenting out the RESET text statement.

48. Save the rule file.

49. Run LVS.

    Is the problem still fixed?

    _____

    You have proven that you can enter text either directly in the layout or through a rule file statement and the behavior/results will be the same.

50. Close all Calibre windows except DESIGNrev.

Exercise 5-3: Find Non-functional Text Annotations

Often layout designers will add text to a layout as an aid to help them keep track of their progress. Text similar to "done", "incomplete", "check", or "future" would not be out of the realm of possibilities. These labels certainly do not add functionality to the cell and may cause problems when you get to the LVS checking stage (as you will soon find out).

In this exercise, you will track down and remove non-functional text from the layout.

1. Make DESIGNrev active.

2. Load lab5d.gds.

3. Load the layer properties. (layer_props.txt)

4. Launch Calibre Interactive LVS.

5. Load lab5d_runset as the runset.

6. Choose **Run LVS**.

    What kind of results did you get?

    _____

7. Click on Extraction Report from the Output Tree in the RVE window.

    Again, you haven't really learned exactly what an Extraction Report is just yet, but you can get a hint of its use.

    What do you think after reading the Extraction Report?

    _____

    Which non-functional text is Calibre warning about?

    _____

Which cells contain this text?

_____

8. Find and remove all the non-functional text from the layout.
    (Be careful not to remove the functional text, like VDD and VSS.)

> **Note** Even though there are about 55 total errors reported, you will not need to fix 55 text instances. Fixing one instance of a cell will fix all instances of that cell—the power of hierarchy.

9. When you are ready to test your work, close all RVE windows.

10. Return to the Calibre Interactive window.

11. Choose the **Inputs** menu button.

12. Change the Layout File from: "lab5d.gds" to "lab5d_fixed.gds".

13. Select the **Import layout database from layout viewer** option.

    By making these two changes you are loading your changes directly from the layout viewer without requiring that you save the file as GDSII first. You are also creating a new GDSII, so you are not overwriting your existing file.

14. Run LVS again.

    Any texting problems?
    (Hint: Look at the Extraction Report.)

    _____

When you are finished with this lab, close all Calibre related windows. (Including DESIGNrev, Calibre Interactive DRC/LVS, RVE, and Summary Report.)

Module 6
Connectivity

Objectives

At the completion of this lecture and lab you should be able to:

- Explain how Calibre establishes connectivity

- Explain the difference between:

    o Soft connections

    o Virtual connections

    o Hard connections

- Explain the difference between:

    o CONNECT

    o STAMP

    o SCONNECT

- Explain Colon connections

How does Calibre Establish Connectivity?

How does Calibre Establish Connectivity?

♦ **Like to like always assumes connectivity**
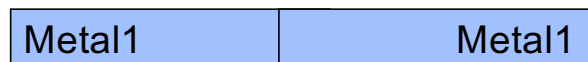
Metal1	Metal1

♦ **Single point connections do NOT give connectivity**
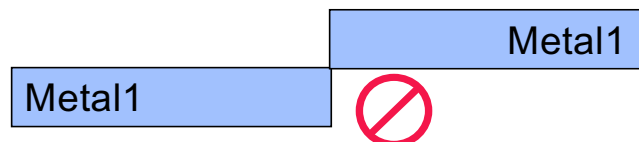
	Metal1

Metal1	

♦ **Use CONNECT statement in the rules file for different layers**

CONNECT METAL1 POLY

Metal1	Poly

Notes:

Review of the CONNECT Statement—Hard Connections

Review of the CONNECT Statement—Hard Connections

- ♦ **Rule syntax:**

  CONNECT LAYER1 LAYER2

  CONNECT LAYER1 LAYER2 BY LAYER3

- ♦ **Example Connects:**
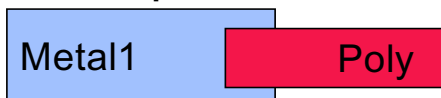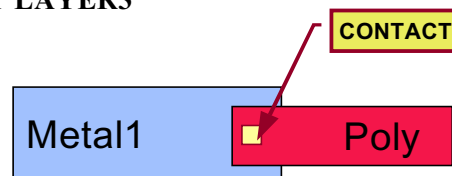
CONNECT METAL1 POLY   **CONNECT METAL1 POLY BY CONTACT**

- ♦ **Example No-Connects:**
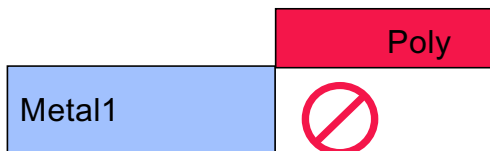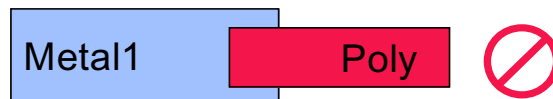
CONNECT METAL1 POLY   **CONNECT METAL1 POLY BY CONTACT**

Notes:

What is Virtual Connect?

What is Virtual Connect?

Virtual-connect paradigm:

♦ **Layout connectivity extractor forms a single net from two or more disjoint nets by virtue of the fact that the net segments share the same name**

♦ **Virtual-connect is triggered by the rule file VIRTUAL CONNECT COLON and VIRTUAL CONNECT NAME specification statements**

Notes:

Using Calibre with DESIGNrev
                                                                                       June 2004

What is VIRTUAL CONNECT NAME?

What is VIRTUAL CONNECT NAME?

- ♦ **Specification statement in the rule file**

- ♦ **Specifies virtual connections between nets having the specified net names**

- ♦ **Syntax: VIRTUAL CONNECT NAME *name1 name2 ...***

  - ● *name***: name of a net—may include wildcard character "?"**

- ♦ **Virtually connects disjoint nets with the same name**

- ♦ **Applies only to nets in the top-level cell**

- ♦ **Names are case-insensitive by default**

- ♦ **You may use this statement more than once**

- ♦ **Names in the list are NOT connected to each other**

Notes:

VIRTUAL CONNECT NAME Example

VIRTUAL CONNECT NAME Example

♦ **You know all the power and ground busses are not connected yet and do not want all the error messages**

♦ **Rule File:**
VIRTUAL CONNECT NAME VDD VSS

VSS

VDD
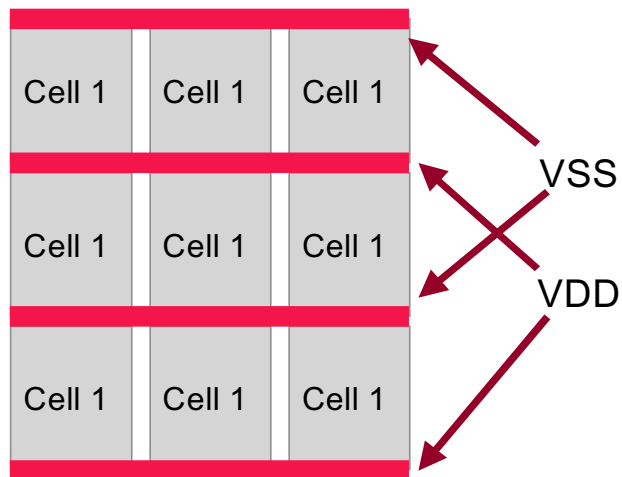
No power or
ground errors
in this run

Notes:

Using Calibre with DESIGNrev
June 2004

More VIRTUAL CONNECT NAME Examples

More VIRTUAL CONNECT NAME Examples

◆ **Virtually connect all disjoint nets whose name begins with "ADDR"**

   ● **For example:**
   Connect ADDR00 to ADDR00 and
   connect ADDR01 to ADDR01

   ● **This does NOT connect ADDR00 to ADDR01!!**

   ● **Rule statement:**
   VIRTUAL CONNECT NAME "ADDR?"

◆ **Virtually connect any disjoint nets with the same name**

   ● **Rule statement:**
   VIRTUAL CONNECT NAME "?"

Notes:

What is VIRTUAL CONNECT COLON?

What is VIRTUAL CONNECT COLON?

♦ **Specification statement in the rule file**

♦ **Specifies whether virtual connections are made between nets having names containing the colon character**

♦ **Syntax: VIRTUAL CONNECT COLON YES|NO**

- **YES: virtually connects disjoint nets having names containing the colon character if their names are identical up to the first colon character**

- **NO: preserves the existing connectivity**

- **Default: NO**

♦ **Applies only to nets in the top-level cell**

♦ **Calibre discards the colon suffix in the resulting net name**

♦ **You may only use this statement once**

Notes:

VIRTUAL CONNECT COLON Example 1

VIRTUAL CONNECT COLON Example 1

Virtually connect three disjoint nets named DATA:0, DATA:123, and DATA:2

- **Rule file:**
  VIRTUAL CONNECT COLON YES
- **This will NOT virtually connect to an existing net "DATA"**
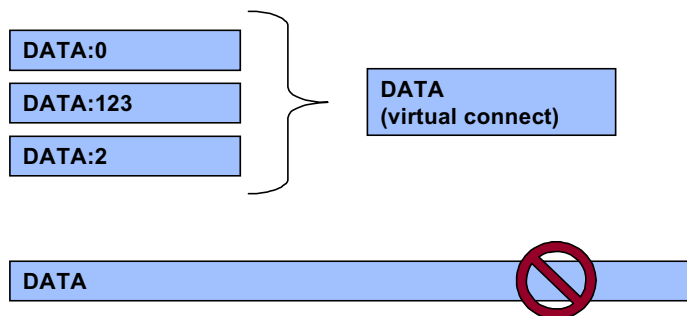
Notes:

VIRTUAL CONNECT COLON Example 2

VIRTUAL CONNECT COLON Example 2

Virtually connect all disjoint nets beginning with "VDD"

- **Connect VDD:pll to VDD:clk to VDD:addr under the net name VDD**
- **Then connect to original VDD**
- **Rule file:**

VIRTUAL CONNECT COLON YES
VIRTUAL CONNECT NAME "VDD"

CONNECT COLON   CONNECT NAME

VDD:pll

VDD:clk   VDD
                          (virtual connect)   VDD
                                                              (virtual connect)
VDD:addr

VDD

Notes:

Using Calibre with DESIGNrev
                                                              June 2004
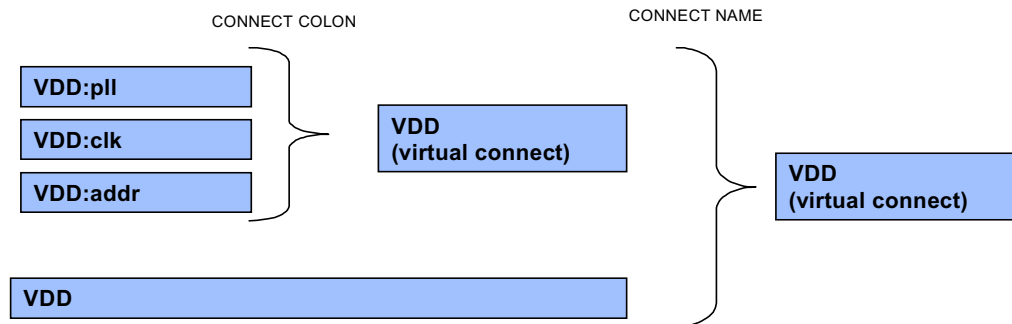
How to Create Virtual Connections from Calibre Interactive

How to Create Virtual Connections from Calibre Interactive

♦ **Menu Button: LVS Options > Connect**

♦ **VIRTUAL COLON CONNECT**

♦ **VIRTUAL CONNECT NAME**
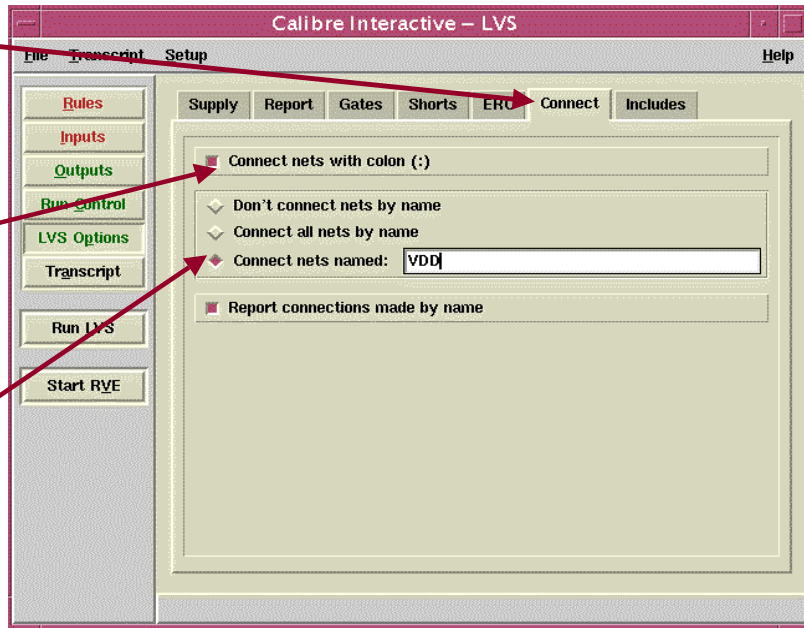
Notes:

What are Soft Connections?

What are Soft Connections?

♦ **The use of a high-resistivity layer to connect two conductors creates a soft connection**

♦ **Soft connections are usually undesirable for electrical performance reasons**

♦ **Soft connections satisfy LVS requirements for network connectivity but can lead to unsatisfactory circuit performance**

Notes:

Using Calibre with DESIGNrev
June 2004

Soft Connections Example

Soft Connections Example

♦ **If the rule file contains these lines:**

> **CONNECT METAL1 WELLTIE BY CONTACT**
>
> **CONNECT WELL WELLTIE**

WELL

METAL1

VSS

METAL1

CONTACT and WELLTIE

The CONNECT statements assign VSS to the WELL layer and the second metal path
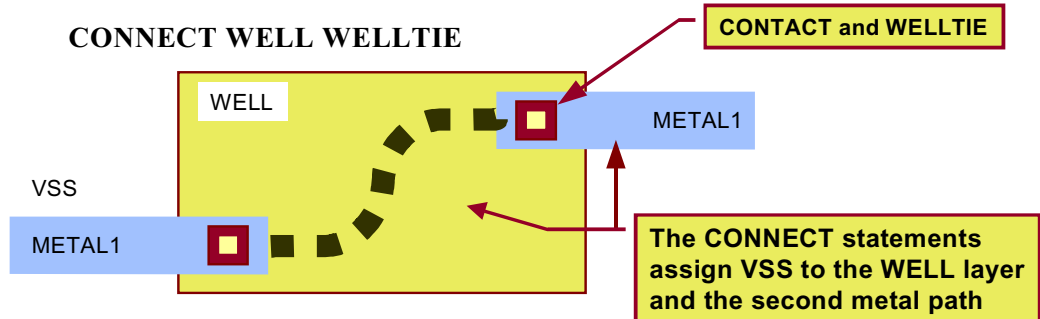
♦ **Then Calibre sees a connection between the two metal paths through the high resistance WELL**

♦ **The missing hardwire connection between the two metal paths is not detected – circuit fails**

Notes:

What is STAMP?

What is STAMP?

- **Derives new layer by selecting all *layer1* polygons overlapped by *layer2* polygons-a copy of the *layer1* shape is put into stamped layer**
- **Syntax:**

   stamp_layer = STAMP *layer1* BY *layer2* [ABUT ALSO]

- **STAMP operations are executed after CONNECT operations**

- **Passes established connectivity from the *layer2* polygons onto the generated *stamp_layer* polygons (one-directional)**

- **Warns of multiple overlapping polygons from different nets**
  - **STAMP violations generally result in a large number of errors**
  - **Does not create a copy of the *layer1* polygon in stamp layer**
  - **Look in the *lvs_report.ext* file for details**
- **Warns of no overlapping polygons (floating *layer1* polygons)**

- **Error locations not reported in LVS - locate with DRC rules**

Notes:

How to Identify Soft Connections with the STAMP Operator

How to Identify Soft Connections with the STAMP Operator

- ◆ **If the rule file contains these lines:**

  CONNECT METAL1 WELLTIE BY CONTACT

  S_WELL = STAMP WELL BY WELLTIE

  CONTACT and WELLTIE

  WELL

  METAL1

  NET 4

  UNASSIGNED
  OR VOID NET

  WELL layer has no net name assigned. Second metal path is assigned an arbitrary net name.

  METAL1

  VSS
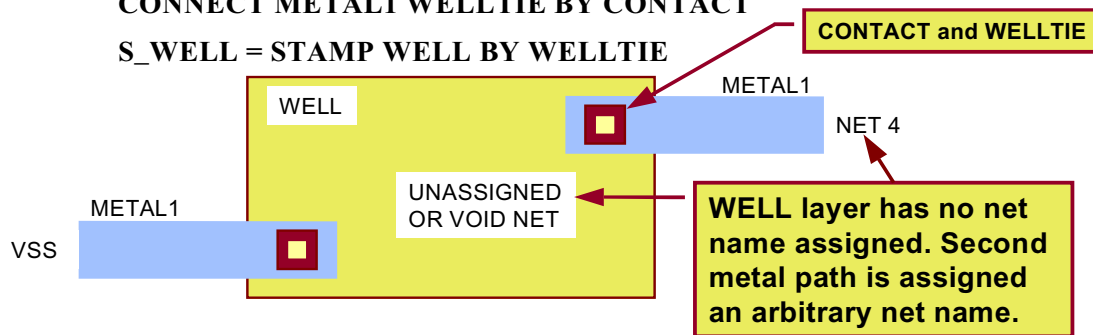
- ◆ **Then the STAMP operation generates a warning that it is trying to stamp the WELL with two different net IDs**
- ◆ **This generally results in a huge number of errors in the LVS report file, since all devices within WELL are undefined**

6-16 • Using Calibre: Connectivity   Copyright © 2004 Mentor Graphics Corporation

Notes:

How to Locate Soft Connections with DRC

How to Locate Soft Connections with DRC

CONTACT PTIE

METAL1

PWELL

4

METAL1

VSS

UNASSIGNED OR VOID NET

PWELL layer has no net name assigned. Second metal path is assigned an arbitrary net name

```
CONNECT METAL1 PTIE BY CONTACT
STAMPED_PWELL = STAMP PWELL BY PTIE

SHOW_BAD_PWELL {PWELL NOT STAMPED_PWELL}

SHOW_BAD_PTIE {
  BADWELL = PWELL NOT STAMPED_PWELL
  PTIE INTERACT BADWELL }
```

Notes:

Using Calibre with DESIGNrev
June 2004
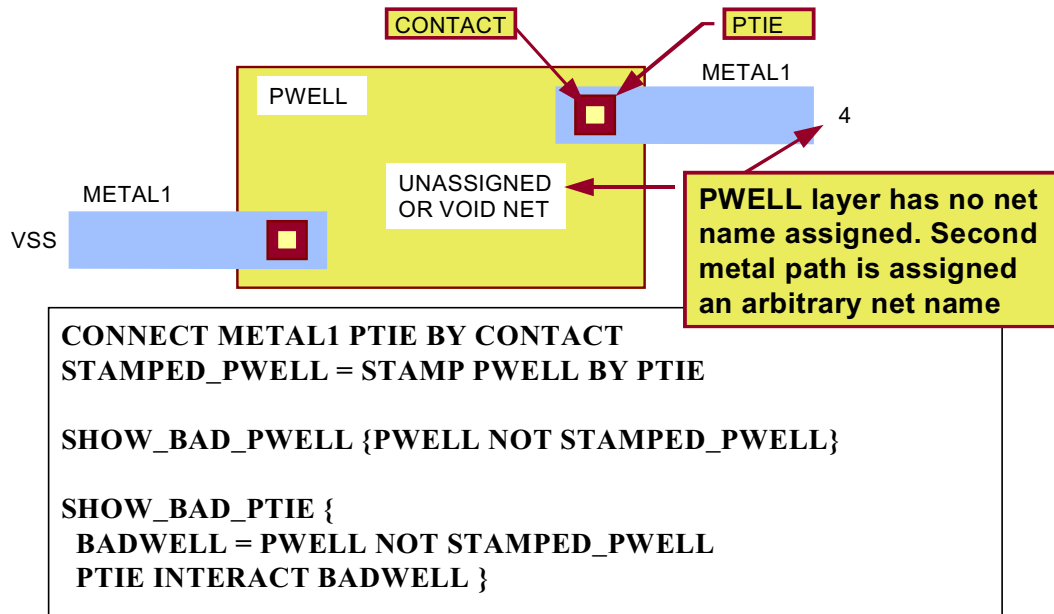
What is the SCONNECT Operator?

- ◆ **Specifies soft connections between upper and lower layer polygons that overlap**
  - ● **Upper layer must appear in a connectivity statement**
  - ● **Lower layers may not appear in any connectivity-based statement**
  - ● **Up to 32 lower layers may be specified**

- ◆ **Passes established connectivity from the upper layer polygons onto the first-encountered overlapping lower layer polygons (one-directional)**

- ◆ **By itself, this statement generates no warnings even if there are soft connections**

Notes:

The SCONNECT Operator Syntax

The SCONNECT Operator Syntax

Syntax:

SCONNECT *upper_layer lower_layer1 lower_layer2* ... [BY *layerN*]

[LINK *link_name*][ABUT ALSO]

♦ BY *layerC* —**specifies an intermediate contact layer**

♦ LINK *link_name* — **specifies a node name for floating polygons on any lower layer**

♦ ABUT ALSO — **specifies that polygon abutment is a valid connection**

♦ **Used with:**
  ● **LVS SOFTCHK**
  ● **LVS REPORT OPTION S**

Notes:

How to Generate Reports from SCONNECT Data

- ♦ **LVS SOFTCHK selects polygons involved in conflicting connections from an SCONNECT statement and generates a results database**
  - ● **If you do not specify this, no conflicting connections will be output to a *.softchk database (DRC format)**
- ♦ **Syntax:**

  LVS SOFTCHK *lower_layer report_layer* **[ALL]**

  - ● *lower_layer* **is a layer through which connectivity is passed**
  - ● *report_layer* **may be one of three keywords: UPPER, LOWER or CONTACT and specifies on which layer the error gets reported**
  - ● **ALL specifies that all nodes involved in conflicting connections to an error polygon are reported (by default, the connection chosen by the SCONNECT operation as "true" is not reported)**
- ♦ **The results database generated is** *layout_primary.softchk* **or lvs.softchk and is stored under the directory specified in your Mask SVDB DIRECTORY statement**

Notes:

How to Generate Reports from SCONNECT Data (Cont.)

How to Generate Reports from Sconnect Data (Cont.)

♦ **LVS REPORT OPTION S reports detailed SCONNECT conflicts in the LVS Report File**

♦ **Syntax:**

   LVS REPORT OPTION S

Notes:

Locating Soft Connections with the SCONNECT Operator

Locating Soft Connections with the SCONNECT Operator

♦ **If the rule file contains these lines:**

> **CONNECT METAL1 WELLTIE BY CONTACT**
> **SCONNECT WELLTIE WELL**
> **LVS SOFTCHK WELL UPPER**
> **LVS REPORT OPTION S**

CONTACT and WELLTIE

METAL1

WELL

NET 4

METAL1

INTERNALLY ASSIGNED NET

VSS

WELL layer has net name assigned based upon Sconnect heuristics. Second metal path is assigned an arbitrary net name by connectivity extractor.
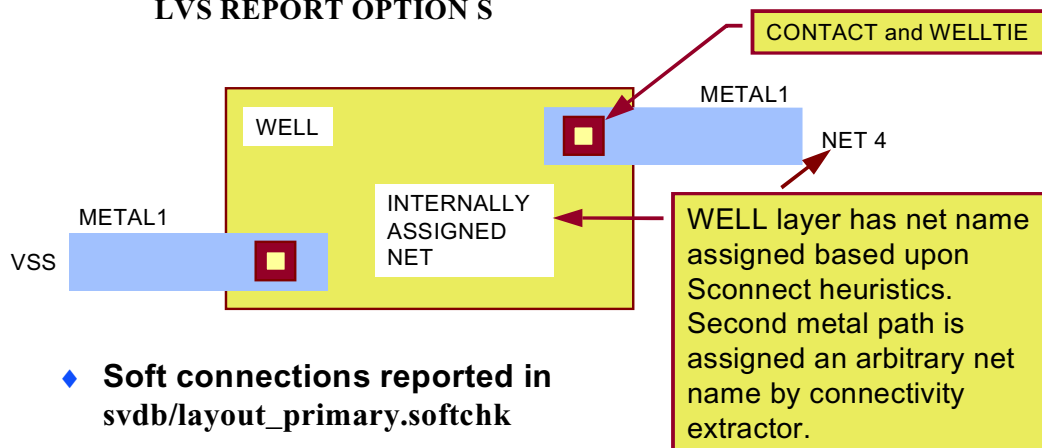
♦ **Soft connections reported in svdb/layout_primary.softchk**

Notes:

Lab Information

Lab Information

In this lab session you will:

♦ **Set up and invoke Calibre LVS to detect a soft connection error using STAMP**

♦ **Use Calibre DRC to find soft connection polygons**

♦ **Use Calibre LVS to detect a soft connection error using SCONNECT**

♦ **Examine the *.softchk database**

Notes:

Using Calibre with DESIGNrev
                                                                              June 2004

Lab: Connectivity

In this lab, you will explore hard and soft connections using Calibre LVS. Again you will be using LVS without a formal introduction, so you will enter most of the data using runsets.

List of Exercises

Exercise 6-1: Finding a Hard Connection Error (Not Shorts or Opens)

Exercise 6-2: Use STAMP to Find Soft Connection Errors

Exercise 6-3: Use DRC and STAMP to Find Soft Connection Errors

Exercise 6-4: Use SCONNECT to Find Soft Connection Errors

Exercise 6-5: Connectivity and CONNECT NAME

Exercise 6-1: Finding a Hard Connection Error (Not Shorts or Opens)

In this lab, you will see what happens when the layers are not properly connected in the rule file.

1. Change to the lab6 directory.
   ```
   cd $HOME/using_calbr/lab6
   ```

2. List the files in the directory.

   There should be the following 24 files in the directory:

golden_rules	lab6_hard_source.spi	lab6_source.spi
golden_rules_hard	lab6_name.gds	lab6_stamp
golden_rules_name	lab6_name_rules	lab6_stamp_drc_runset
golden_sconnect	lab6_name_runset	lab6_stamp_runset
golden_stamp	lab6_name_source.spi	lab6a.gds
lab6_hard.gds	lab6_rules	lab6a_runset
lab6_hard_rules	lab6_sconnect	lab6b.gds
lab6_hard_runset	lab6_sconnect_runset	layer_props.txt

   If any of these files are missing, please double check that you are in the correct directory, and then notify your instructor.

3. Launch DESIGNrev.

4. Open Layout, lab6_hard.gds.

5. Load the layer properties file, layer_props.txt.
   (**Menu: Layer > Load Layer Properties**)

6. Launch Calibre Interactive LVS on cell, lab6.

7. Load lab6_hard_runset as the runset file.

8. Run LVS.

   What happens?

   _____

9. Read the error message carefully.

   What do you think is the problem?

   _____

   Layer psd should be connected to layers: metal1, ipoly, and nsd by contact layer.

10. Open the rule file.

11. Find the CONNECT statements.

    Is psd included in the correct CONNECT statement?

    _____

12. Make the lab6_hard_rules file editable.

13. Add the psd layer to the CONNECT statement.
    Place psd as the last layer in the list of layers connected to metal1 by contact.

14. Save the file.

15. Run LVS again.

    Any problems?

    _____

    This type of problem is not normally encountered. The CONNECT statements are normally part of the "golden" rule file and not often edited.

You may see these problems when you are defining new devices or trying to write rules to flag soft connections.

16. Close the rule file.

17. Close all Calibre windows except DESIGNrev.

Exercise 6-2: Use STAMP to Find Soft Connection Errors

In this exercise you will learn how to find soft connections using STAMP.

1. Make DESIGNrev active.

2. Open lab6b.gds.

3. Launch Calibre Interactive LVS on cell lab6.

4. Use lab6_stamp_runset as the runset.

5. Run LVS.

    What are the results?

    _____

6. Open the Layout and Source netlists.

7. Display the Extraction Report.

    What is the problem according to the Extraction Report?

    _____

    What is the location?

    _____

    What nets?

    _____

    You have all the information you need to fix the problem, right?

    Not this time. The location is just the lower left corner of the nsub layer which is very large.

LVS just isn't very helpful for finding the exact location of the problem this time. In the next exercise, you will learn how to use DRC to find soft connection problems.

8. Close RVE, netlist, and report windows.

Exercise 6-3: Use DRC and STAMP to Find Soft Connection Errors

In this exercise you will learn how to use DRC to find the location of a soft connection error.

1. Make the Calibre Interactive LVS window active.

2. Open the rule file.

3. Find the bad_ntie rule.

    What is the purpose of the bad_ntie rule?

    _____

    This illustration shows all nties in the layout. (This layer is the "link" between VDD and the substrate.)
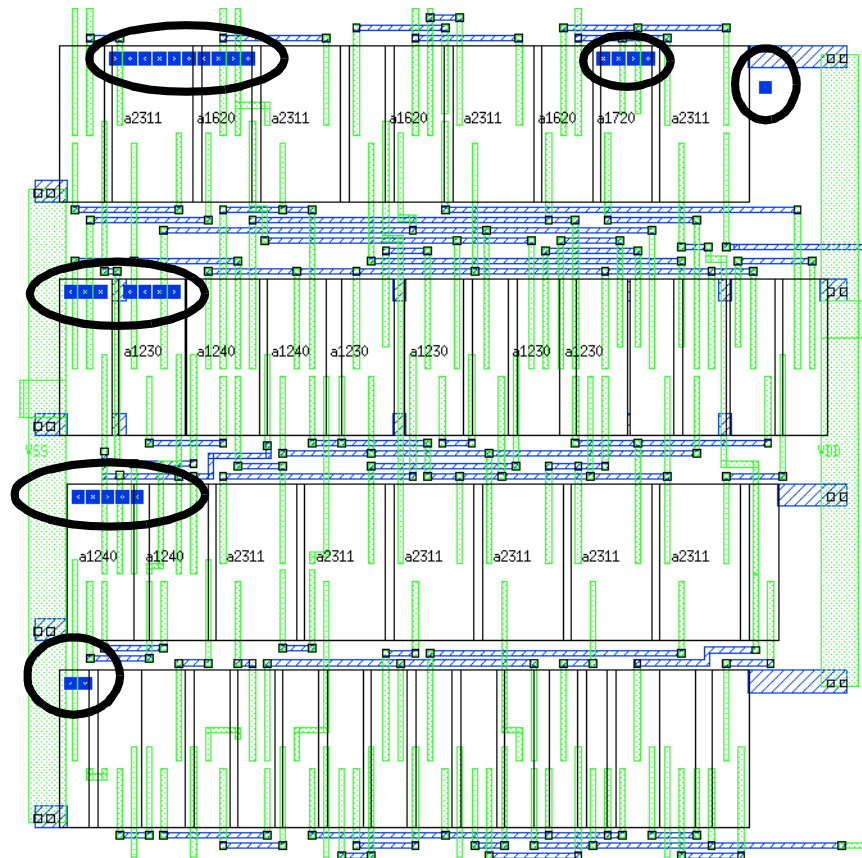
Think about this for a minute... in this design all "good" ntie polygons are connected to VDD. We need to know about ntie polygons that are not part of VDD, these could cause STAMPing violations. This is a DRC rule, not an LVS-type rule!

4. Look at the bad_ptie rule.

    How does the bad_ptie rule work?

    _____

    This rule finds pties that are in pwells with soft connections.

5. Close the rule file.

6. Launch a Calibre Interactive DRC window.
    (Leave the Calibre Interactive LVS window open.)

7. Create a new runset.

8. Enter the following **Inputs** data:

Hierarchical, Flat or Calibre CB	Hierarchical
Layout Files:	lab6b.gds
Import layout database from layout viewer:	unselected
Primary Cell:	lab6
Check Area	unselected

9. Enter the following **Rules** data:

Calibre - DRC Rules File:	lab6_stamp
Calibre - DRC Run Directory:	.

10. Enter the following **Outputs** data:

DRC Results Database File:	drc_stamp_results
Format:	ASCII

     Start RVE after DRC finishes: selected

     Write DRC Summary Report: selected

     File: drc_stamp_summary

     Replace File: selected

     View summary report after DRC finishes: selected

11. View the Transcript.

12. Run DRC.

     What are your results?

     _____

     This is the source of your soft connection problem.

13. In DESIGNrev, Zoom to display the entire layout. (Toolbar: **Z all**)

14. In RVE, set the highlight Zoom to "Don't change the cell view".

15. Highlight the error.

     Where is the problem in the layout?

     _____
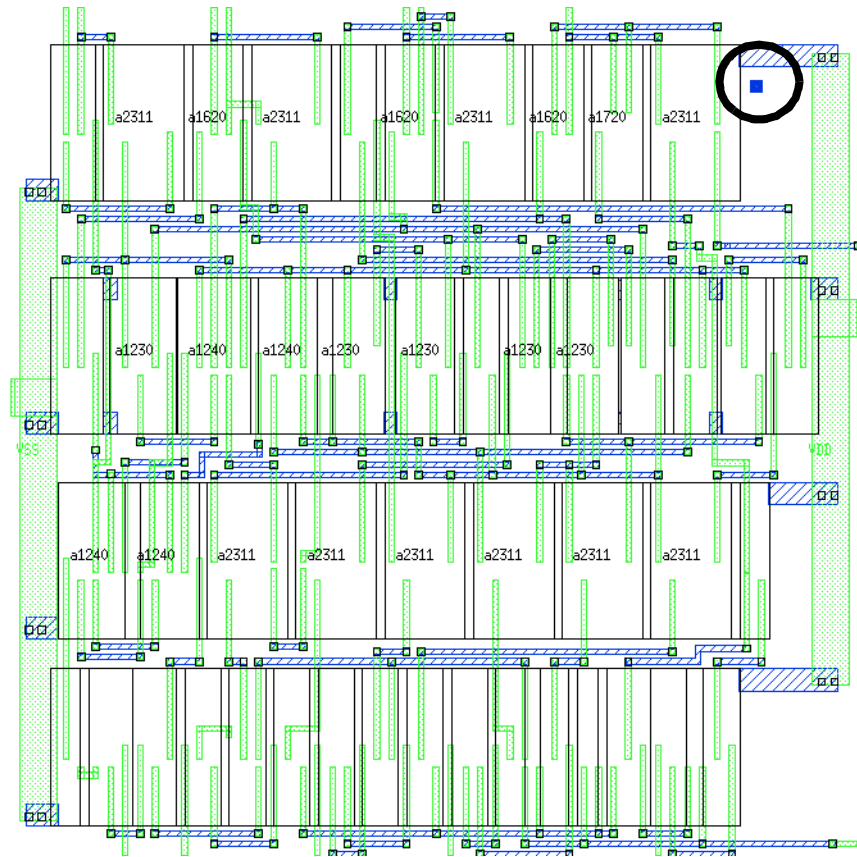
Do NOT fix the error! We will use this same layout to find the error using another method in the next exercise.

16. Erase all highlights in the layout.

17. Return the layout to the full display.

18. Go directly to the next exercise without closing any windows.

Exercise 6-4: Use SCONNECT to Find Soft Connection Errors

In the exercise you will re-run LVS on the layout with a soft connection error again using a method that will allow you to find the exact soft connection from within LVS.

1. Make the Calibre Interactive LVS window active.

2. Load runset lab6_sconnect_runset.
    (**Menu: File > Load Runset**)

3. Load the rule file.

4. View the rule file.

5. Find the two SCONNECT statements.

    What are the SCONNECT statements doing?

    _____

    _____

6. Leave the rule file open.

7. Run LVS.

    What are your results?

    _____

    In order to get any information about soft connections using this statement you need to have LVS perform a soft check and then report on the soft check results.

8. Write a rule statement that highlights upper layer geometries involved in soft connections to nsub.
    (Use the *SVRF Manual* and/or look back through the lecture.)

Answer:

_____

9. Write a rule statement that highlights upper layer geometries involved in soft connections to pwell.

   Answer:

   _____

10. Add these two statements to the rule file.

11. Save the rule file.

    Now that you have written the rules, you need to set Calibre to report Softchecks to return any results.

12. Display the LVS Options.
    (May need to make the LVS Options available using **Menu: Setup > LVS Options**.)

13. Select the **Report** tab.

14. Select **LVS Report Option "S"**.
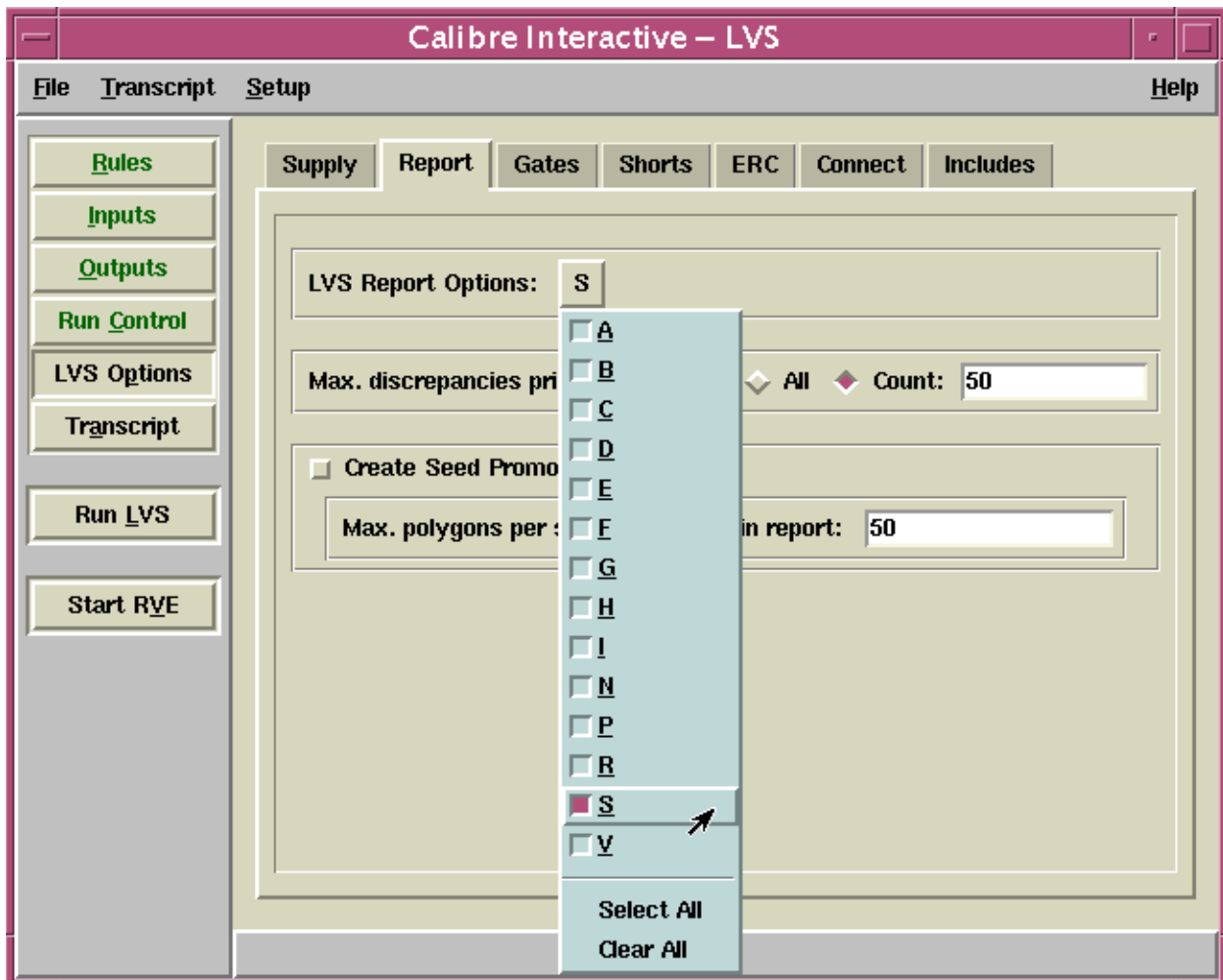
15. Run LVS again.

What are the results?

_____

Yes, everything still appears to check out correct. But you have one additional resource, the Softchk Database.

16. Click on the Softchk Database.
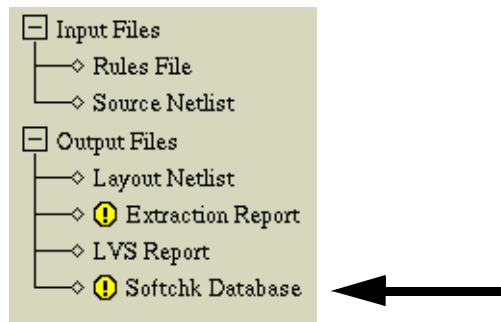
This opens another RVE window, this time for DRC.

What results are displayed in the DRC RVE window?

_____

What is the error?

_____

17. Highlight the error in the layout.

Is it the same error?

_____

Now you know two methods to find soft connections.

This completes this exercise.

18. Close the rule file.

19. Close all Calibre windows except DESIGNrev.

Exercise 6-5: Connectivity and CONNECT NAME

In this exercise, you will fix connectivity errors by virtually connecting nets if they have the same name.

1. In DESIGNrev, open layout lab6_name.gds.

2. Launch Calibre Interactive LVS on cell lab5c.

   Note The cell name for this exercise is "lab5c".

3. Load lab6_name_runset as the runset in Calibre LVS.

   This loads all the data required for your first LVS run on this layout.

   Note If you closed Calibre LVS and needed to launch it again for this exercise, load the runset again to make sure the correct data is in all the fields.

4. Run LVS.

   What are your results?

   _____

   How many errors do you have?

   _____

   These are a lot of errors, where would you start? The Extraction Report has provided good clues in previous exercises, so it is a good starting point for this exercise.

5. Open the Extraction Report.

   What does the Extraction Report tell you?

Next you will go to the layout and find the text, VSS, to see why it is broken into four different nets.

6. Close the Extraction Report.

7. Make the DESIGNrev window active.

8. Choose **Menu: Object > Find Text**.

    This opens the Find Text dialog box.

9. Enter VSS in the Text to Find text box.

10. Choose **Find**.

11. Repeat **Find** until you know the location of all four nets.
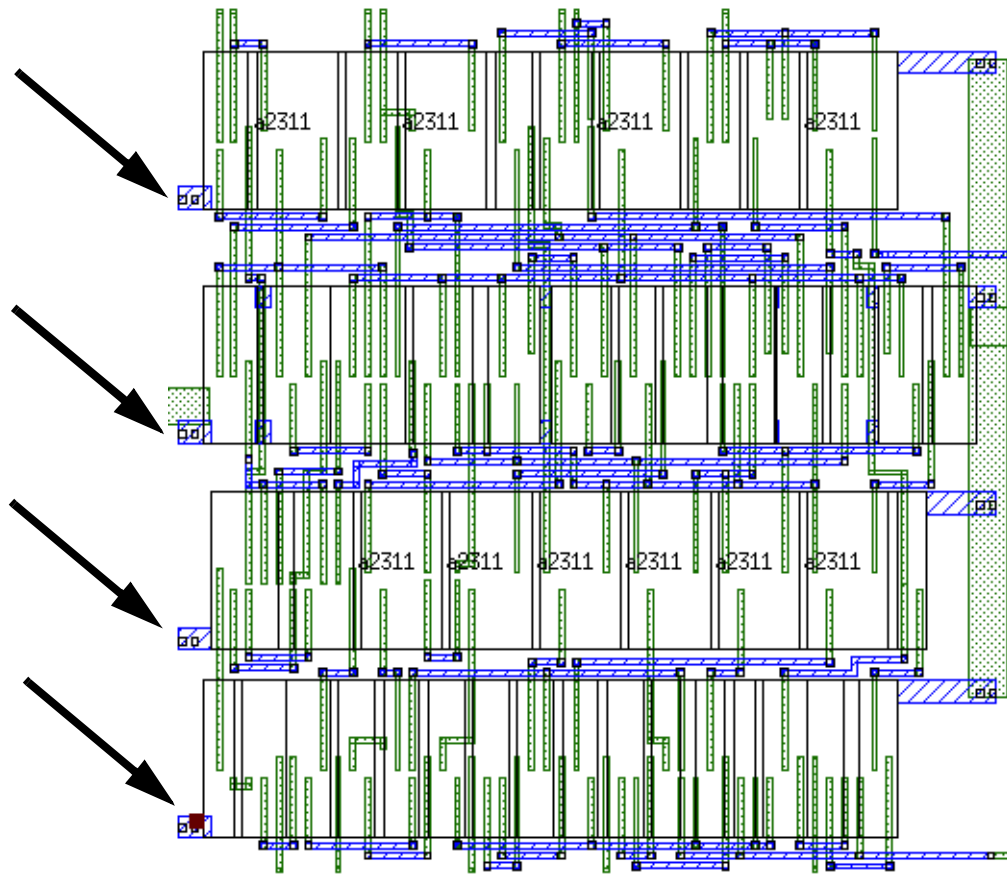
It appears that the layout designer forgot to draw the main VSS bus. The designer may have specific reasons for not connecting the VSS bus, so it might be inappropriate for you to modify the layout at this time.

Is there anything you can do to finish verifying the design without modifying the layout?
(Hint: Look back in the lecture, or the title of this exercise.)

_____

12. Close the LVS Report and RVE windows.

13. Make the Calibre Interactive LVS window active.

14. Choose **Menu: Setup > LVS Options**.

This adds the **LVS Options** button to the list of Menu buttons.

15. Choose the **LVS Options** Menu button.

16. Choose the **Connect** tab.

17. Select the **Connect nets named** option button.

18. Enter VSS in the text box.

19. Select the Report connections made by name check box.

20. Choose **Run LVS**.

What are your results this time?

_____

21. View the Extraction Report.

What information is in the Extraction Report?

_____

Now that you have quickly verified the "correctness" of the layout, you have time to track down the layout designer and find out what is going on with the VSS bus!

When you are finished with this lab, close all Calibre related windows. (Including DESIGNrev, Calibre Interactive DRC/LVS, RVE, and Summary Report.)

Module 7
Basic LVS Concepts

Objectives

At the completion of this lecture and lab you should be able to:

- Describe how LVS fits in a verification flow

- List what input files are required to run an LVS

- Run a Calibre LVS using the Calibre Interactive

- Create an Hcell correspondence file

- Read the various LVS reports

- Instruct Calibre to ignore specified cells during LVS

What is Layout vs. Schematic?

What is Layout vs. Schematic?

RESET

Design View
- Design Architect
- Composer

Layout View
- DESIGNrev
- Virtuoso
- StreamView

RESET

Connectivity   Device
Extraction   Extraction

Schematic   HDL
Compilation   Compilation

COMPARISON
PHASE

LAYOUT NETLIST

SOURCE NETLIST

EXTRACTION PHASE

VERIFICATION
RESULTS

Notes:

Using Calibre with DESIGNrev
                                                                        June 2004
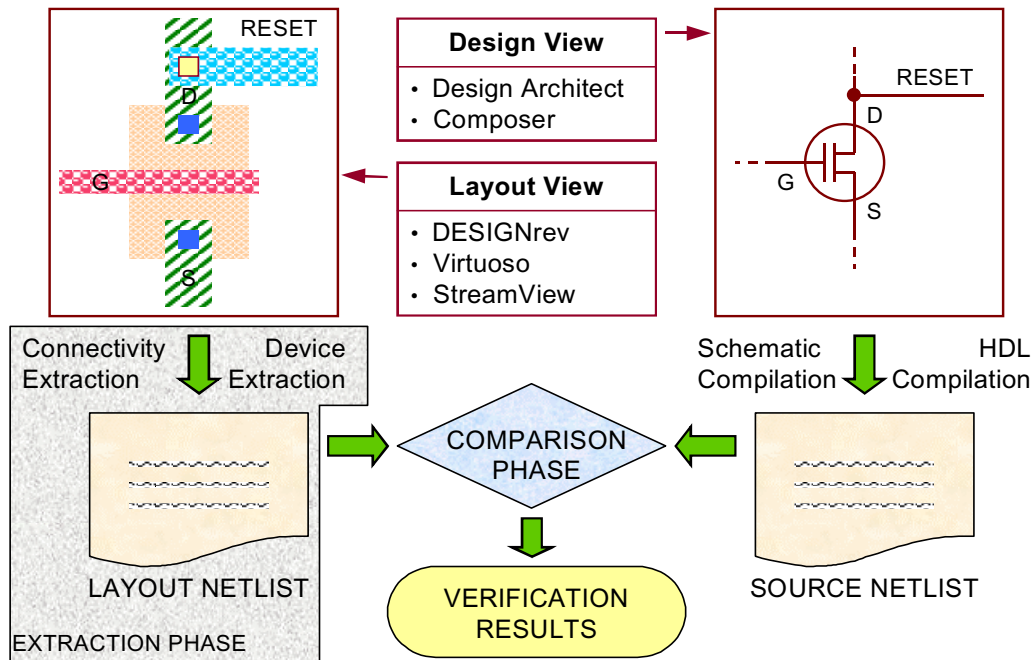
What Files Does Calibre Need to Perform LVS?
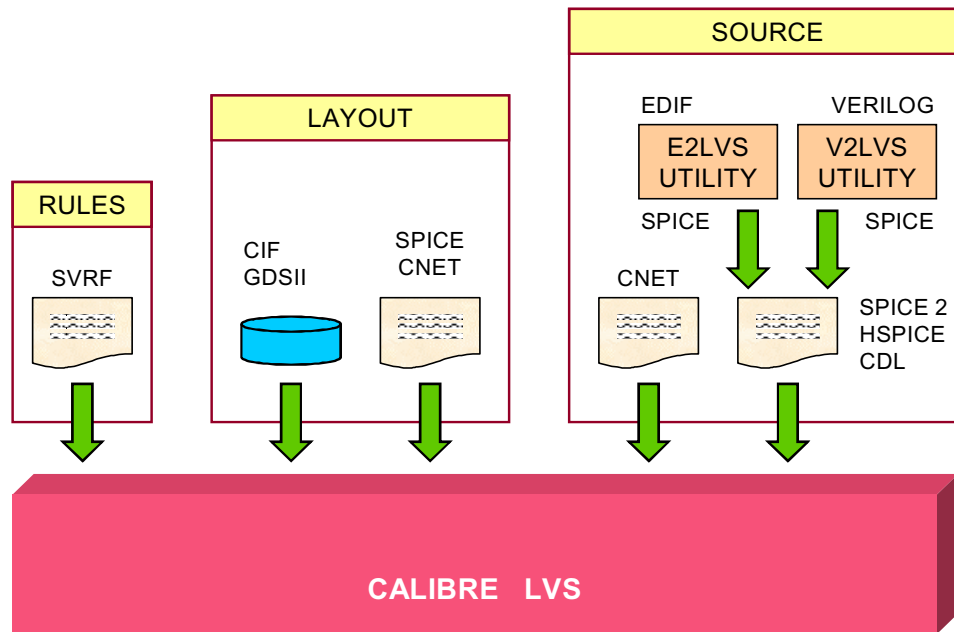
Notes:

How to Use Calibre LVS—Invoking Calibre Interactive

How to Use Calibre LVS—Invoking Calibre Interactive

♦ **Start by launching DESIGNrev**

    $MGC_HOME/bin/calibredrv

♦ **Load GDSII design**

    Menu: File > Open GDS

♦ **Launch Calibre Interactive for LVS**

    Menu: Tools > Calibre Interactive

♦ **Select Calibre LVS**

Notes:

How to Use Calibre LVS—Invoking Calibre Interactive

♦ **Start by launching Virtuoso on the design**

♦ **Launch Calibre Interactive for LVS**

   Menu: Calibre > Run LVS

Calibre
Run DRC
Run LVS
Run PEX
Start RVE
Clear Highlights
Setup
About…

Notes:

How to Use Calibre LVS—Load Runset and Rules

How to Use Calibre LVS—Load Runset and Rules

♦ **Load the Runset or create a new one**

Choose Runset File

Runset File Path

ser/student/calibre/using_calbr/lab5/run ⬇ [...]

[OK]   [New Runset]
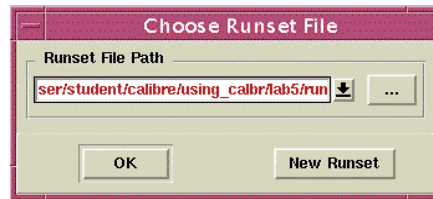
♦ **Load the rules**

♦ **Set run directory**

Calibre Interactive — LVS

File   Transcript   Setup   Help

Rules	Calibre-LVS Rules File
Inputs	/user/sallyw/calibre/using_calbr/lab5/lab5_rules [...] [View] [Load]
Outputs	
Run Control	Calibre-LVS Run Directory
Transcript	. [...]

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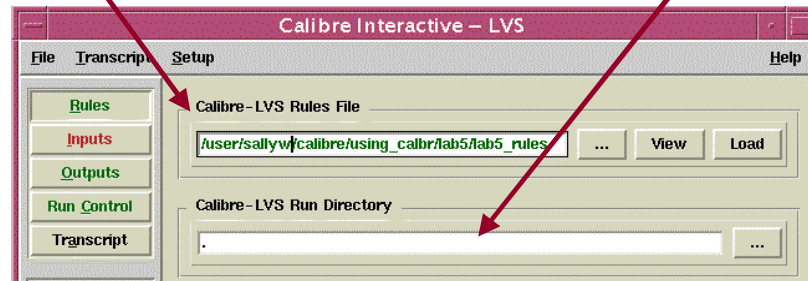
Notes:

How to Use Calibre LVS—Load the Layout

How to Use Calibre LVS—Load the Layout

♦ **Choose the Input Button**

♦ **Select Hierarchical or Flat**

♦ **Select comparison type**

♦ **Load the layout file**

♦ **Define the cell name**

♦ **Define the filename for the layout's netlist**

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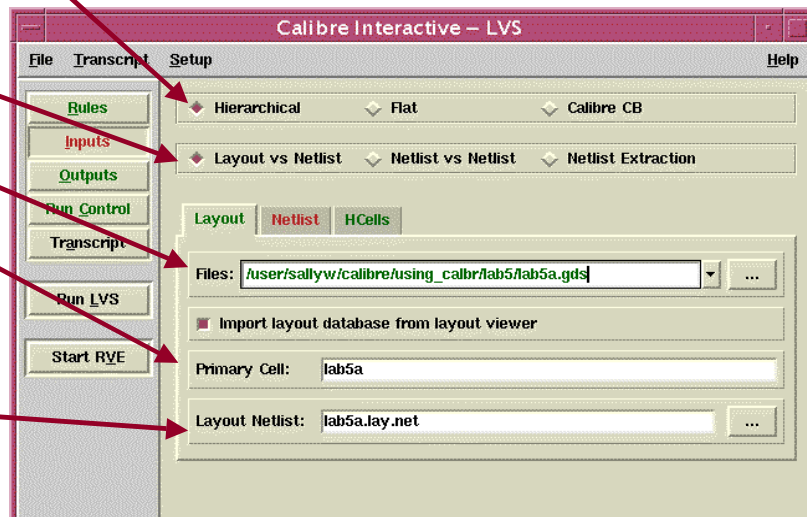
Notes:

How to Use Calibre LVS—Load the Netlist

How to Use Calibre LVS—Load the Netlist

♦ **Choose the Netlist tab**

♦ **Enter the source netlist file**

♦ **Select netlist format**

♦ **Enter the primary cell**

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4
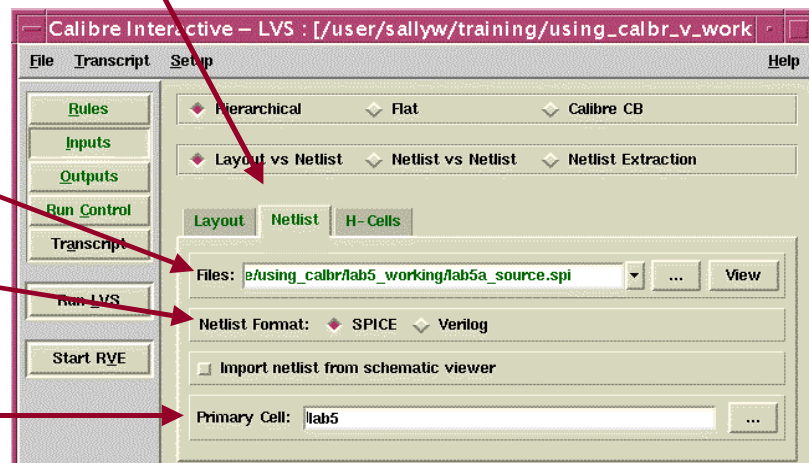
Notes:

How to Use Calibre LVS—Define the Output Files

How to Use Calibre LVS—Define the Output Files

♦ **Choose Output button**

♦ **Enter a name for the LVS Report File**

♦ **Select view the report after the run**

♦ **Select results database creation**

♦ **Select launching RVE**

♦ **Enter a name for the SVDB directory**

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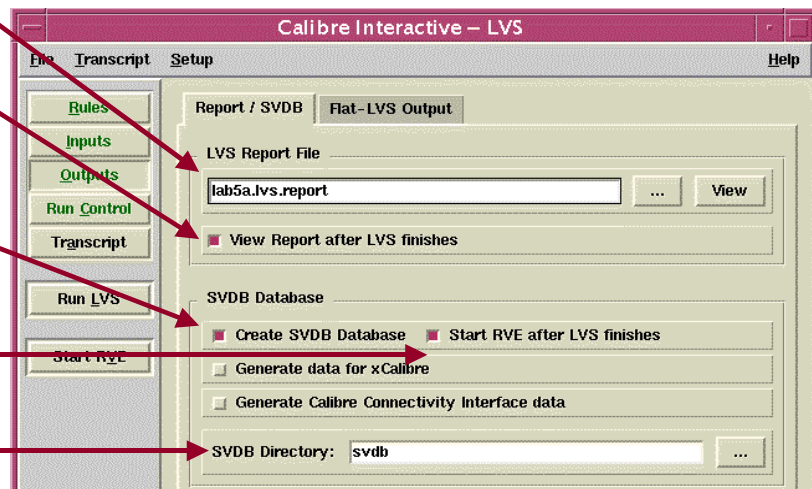
Notes:

How to Use Calibre LVS—LVS Options

Choose Menu: Setup > LVS Options

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Notes:

Using Calibre with DESIGNrev
June 2004
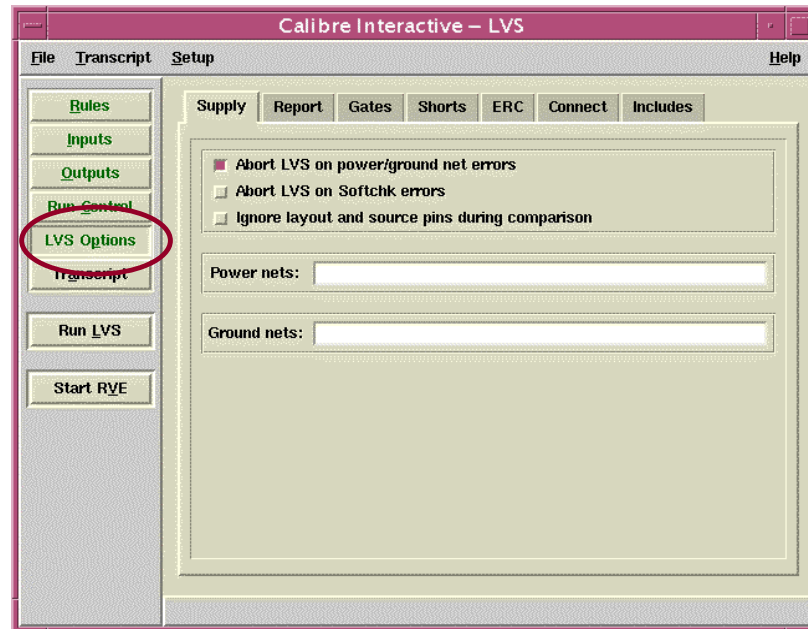
How to Use Calibre LVS—LVS Options: Supply

How to Use Calibre LVS—LVS Options: Supply

LVS Options:

♦ **Supply**

♦ **Report**

♦ **Gates**

♦ **Shorts**

♦ **ERC**

♦ **Connect**

♦ **Includes**
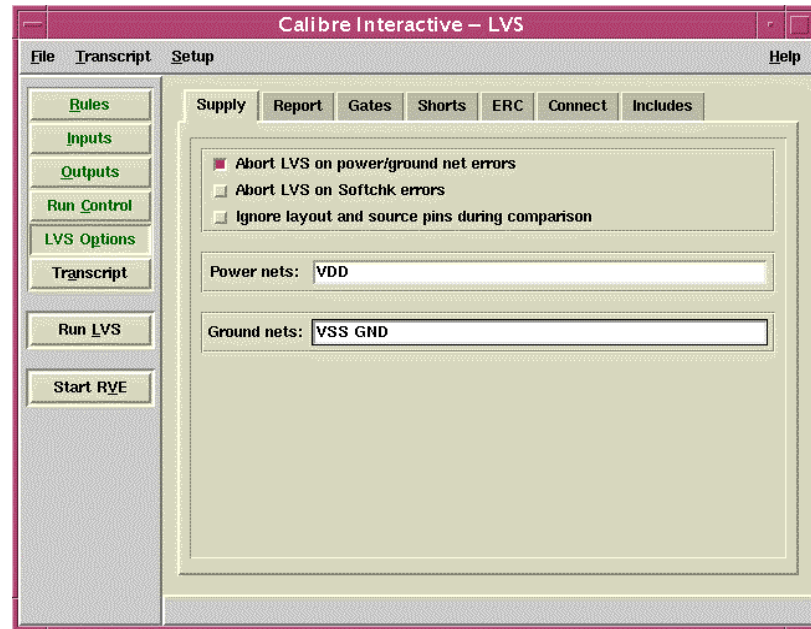
Notes:

Using "Abort LVS on power/ground net errors" will save a large amount of wasted computation time. Generally a good idea to have this option selected.

How to Use Calibre LVS—LVS Options: Report

LVS Options:

♦ **Supply**

♦ **Report**

♦ **Gates**

♦ **Shorts**

♦ **ERC**
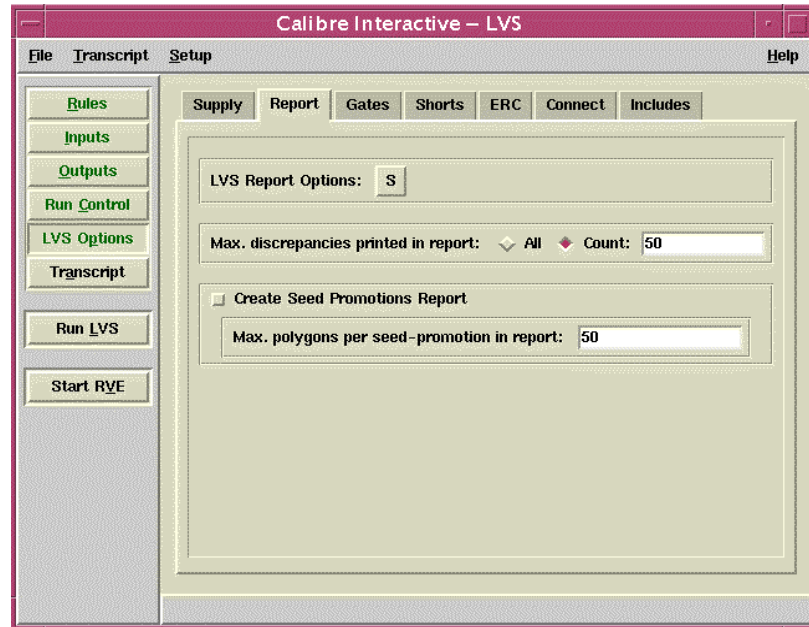
♦ **Connect**

♦ **Includes**

Notes:

How to Use Calibre LVS—LVS Options: Gates

How to Use Calibre LVS—LVS Options: Gates

LVS Options:

♦ **Supply**

♦ **Report**

♦ **Gates**

♦ **Shorts**

♦ **ERC**

♦ **Connect**

♦ **Includes**

Notes:

How to Use Calibre LVS—LVS Options: Shorts

How to Use Calibre LVS—LVS Options: Shorts

LVS Options:

- ◆ **Supply**

- ◆ **Report**

- ◆ **Gates**

- ◆ **Shorts**

- ◆ **ERC**
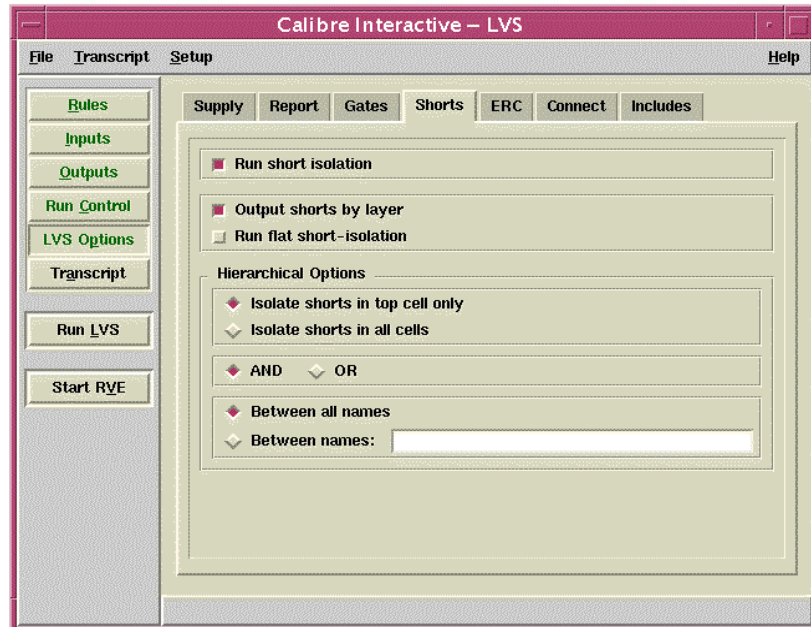
- ◆ **Connect**

- ◆ **Includes**

Notes:

How to Use Calibre LVS—LVS Options: ERC

How to Use Calibre LVS—LVS Options: ERC

LVS Options:

- ◆ **Supply**

- ◆ **Report**

- ◆ **Gates**

- ◆ **Shorts**

- ◆ **ERC**
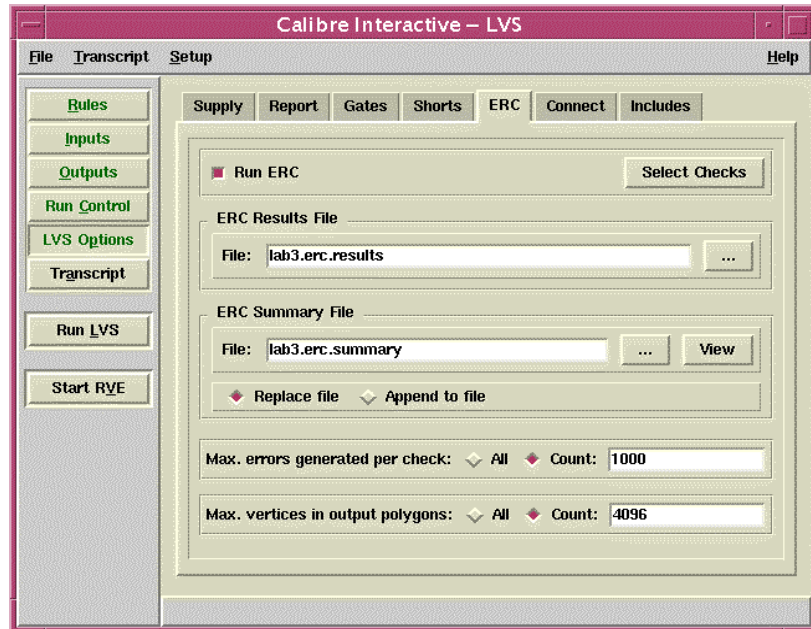
- ◆ **Connect**

- ◆ **Includes**

Notes:

How to Use Calibre LVS—LVS Options: Connect

How to Use Calibre LVS—LVS Options: Connect

LVS Options:

- ♦ **Supply**

- ♦ **Report**

- ♦ **Gates**

- ♦ **Shorts**

- ♦ **ERC**
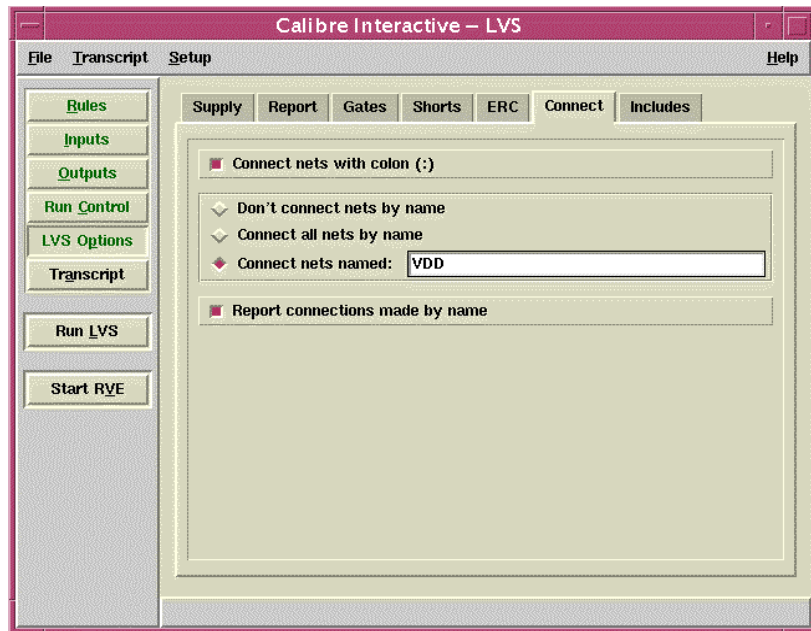
- ♦ **Connect**

- ♦ **Includes**

Notes:

How to Use Calibre LVS—LVS Options: Includes

How to Use Calibre LVS—LVS Options: Includes

LVS Options:

♦ **Supply**

♦ **Report**

♦ **Gates**

♦ **Shorts**

♦ **ERC**

♦ **Connect**

♦ **Includes**

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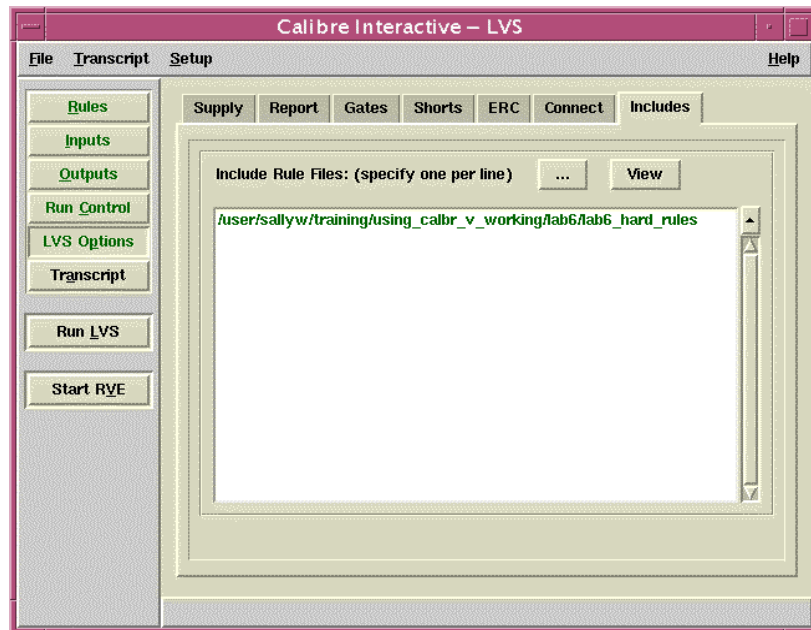
Notes:

How to Use Calibre LVS—Set Run Control and Run LVS

How to Use Calibre LVS— Set Run Control and Run LVS

- ◆ **Choose Run Control button**

- ◆ **Set Run options (as available)**

- ◆ **Choose Run LVS**

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2
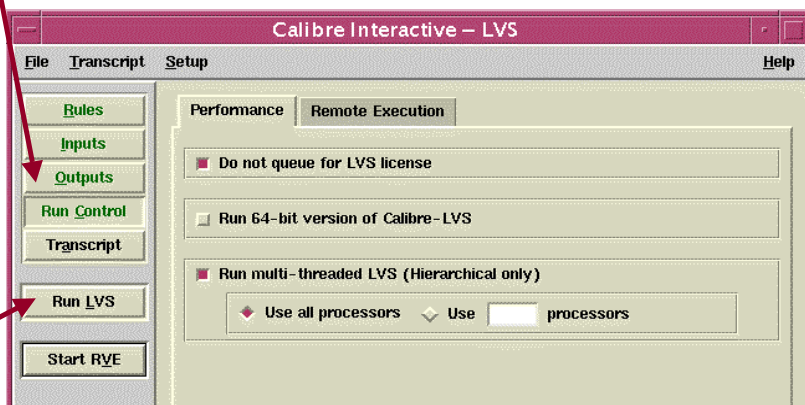
Notes:

What are the Possible Outputs from an LVS Run?

What are the Possible Outputs from an LVS Run?

- ◆ **Calibre LVS Transcript**

- ◆ **Calibre LVS Report File**

- ◆ **Calibre LVS Results Database**

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Notes:

How to Read the LVS Transcript

- ◆ **View using Calibre Interactive**
- ◆ **Identifies:**
  - ● **Individual phases of LVS execution:**
    - – **Compilation of the rule file**
    - – **Translation and transformation of the source and layout cells**
    - – **Generation of the output files**
  - ● **Execution statistics (like Calibre DRC)**
  - ● **Connectivity extraction errors**
  - ● **Warnings**
    - – **Texting problems**
    - – **Stamping errors**
- ◆ **Provides clues if LVS terminates before completion**

Notes:

Transcript in the Calibre Interactive Window

Transcript in the Calibre Interactive Window
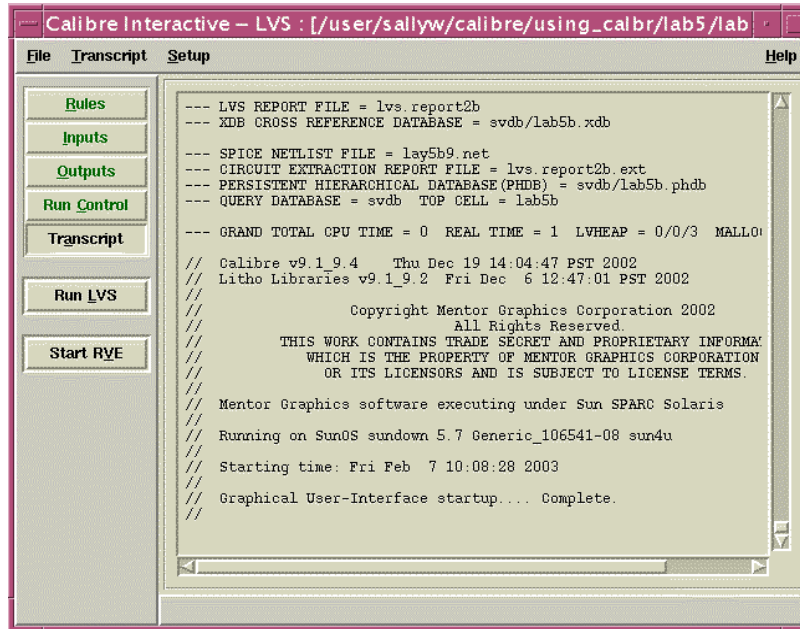
Notes:

How to Read the LVS Report File

How to Read the LVS Report File

- ◆ **LVS generates the report in ASCII format**

- ◆ **Report is readable either with an ASCII editor or with Calibre RVE**

- ◆ **Report lists discrepancies on a cell-by-cell basis**

- ◆ **Report summarizes LVS execution time, memory allocation and other run statistics**

- ◆ **LVS generates the report if Calibre executes to completion**

- ◆ **User specifies report filename from within Calibre Interactive or in a rule file statement**

Notes:

What Information is in the LVS Report File?

What Information is in the LVS Report File?

LVS report has the following sections (see Appendix A):

- ♦ **Header**
- ♦ **Overall Comparison Results**
- ♦ **Incorrect Objects**
- ♦ **Incorrect Nets**
- ♦ **Incorrect Instances**
- ♦ **LVS Parameters**
- ♦ **Information and Warnings**
- ♦ **Detailed Instance Connections**
- ♦ **Unmatched Objects**
- ♦ **Summary**

Notes:

How to Use Calibre LVS RVE

How to Use Calibre LVS RVE

Double-click

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Notes:

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How to Find the Error in the Netlist

How to Find the Error in the Netlist

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Notes:

How to Cross Probe—RVE to Layout Viewer

How to Cross Probe—RVE to Layout Viewer

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Notes:

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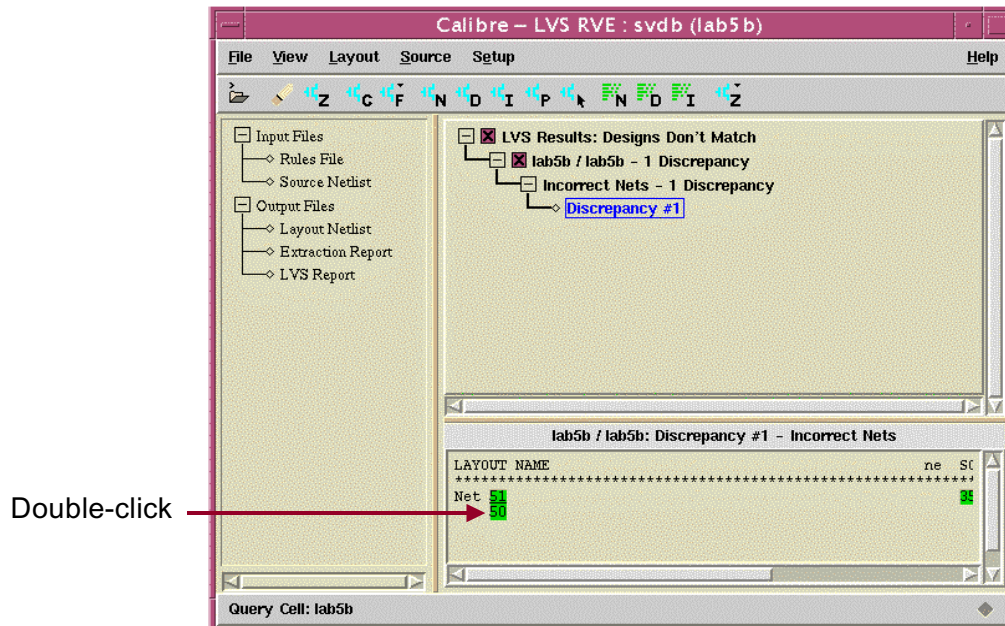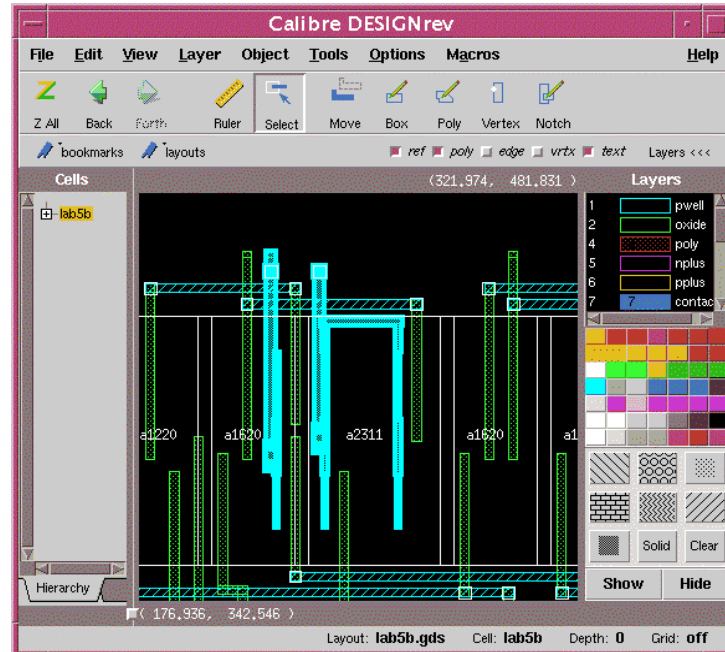
How to Cross Probe—RVE to Layout Viewer

How to Cross Probe—RVE to Layout Viewer
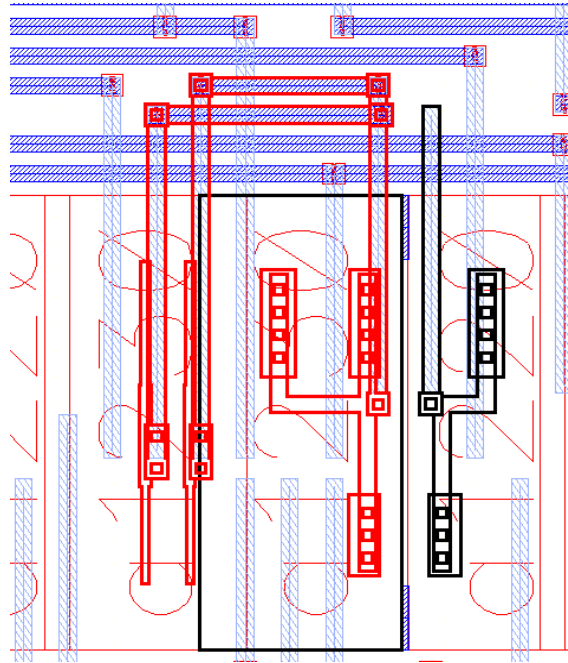
Notes:

What is LVS BOX?

What is LVS BOX?

♦ **Ignores a cell contents during a LVS comparison (Still checks external connections)**

♦ **Allows you to run an LVS when the layout is partially complete**

a1220	a6000	a1220	a5000
a1220	a1220	a7000	a1220

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Notes:

How to use LVS BOX

How to use LVS BOX

♦ **Specification in the Rule File**

LVS BOX **[<u>SOURCE LAYOUT</u> | SOURCE |LAYOUT]** *cellname*
- **SOURCE LAYOUT: Ignore in both the source and the layout (default)**
- **SOURCE: Only ignore these cells in the source**
- **LAYOUT: Only ignore these cells in the layout**
- *cellname*: **Name of the cells you wish to treat as black boxes**

♦ **Example: Ignore cells a1220 in both the layout and source**

LVS BOX a1220

Notes:

What is Automatic Cell Correspondence?

What is Automatic Cell Correspondence?

♦ **Hierarchical analysis requires the identification of corresponding cells between the source and layout**

♦ **LVS-H automatically matches cells in the source and layout with the same name when invoked with the automatch option**

- **Cell names are case insensitive (by default)**
- **Top-level cells always correspond, regardless of names**

♦ **LVS-H expands unmatched cells to the next hierarchical correspondence level nearer the top level**

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Notes:

Using Calibre with DESIGNrev
June 2004

How does Hcell File Specify Cell Correspondence?

How does Hcell File Specify Cell Correspondence?

- ◆ **Enables correspondence when cell names differ between source and layout**

- ◆ **All cells must correspond between source and layout for you to take full advantage of LVS-H**
  - ● **In a large design, a cell used only a few time may actually more efficient to allow Calibre to flatten the design for those rarely used cells.**

- ◆ **LVS-H flattens unmatched cells and promotes them up the hierarchy (toward the top level)**

- ◆ **Requires the name of the cell correspondence file on the command line or in the Calibre Interactive field**

- ◆ **You can use both Hcell and automatch**

Notes:

There are trade-offs to make between having an Hcell file entry for a cell and allowing Calibre to flatten the cell.

Obviously, the more times the cell repeats in the design, the more advantageous it is to have an Hcell file entry for that cell. If a cell is only used once in the design, it may not save you either processing time or "man-hours" to have an Hcell entry for that cell. Calibre requires some additional overhead to process and record hierarchical data above what would be required for the same amount of flat circuitry. (Also, there are the man hours to keep the Hcell file up to date with the names of the cell.)

Due to the Calibre overhead considerations, it also may not be to your advantage to use the automatch option when you have a design with a large number of individual cells. It is more appropriate in the case of a design with a few number of different cells that are used repeatedly.

These are trade-offs you need to weigh as a user.

Creating the Hcell Correspondence File

- ♦ **Create the file with an ASCII editor**

- ♦ **Insert one cell per line in the form:**

    layout_name   *source_name*

- ♦ **Including the top-level cell is not necessary**

- ♦ **Specifying 1-to-n or n-to-1 correspondence is permissible**

- ♦ **Enter comments by starting a line with "//"**

- ♦ **Do not use trailing comments**

- ♦ **LVS-H treats cell names as case insensitive**

- ♦ **LVS-H issues a warning for cell names not found**

Notes:

Example Hcell Correspondence File

Example Hcell Correspondence File

```
                                              CELL FILE
// HCELL FILE
// PROJECT NAME: mydesign
// LAYOUT CELL              SOURCE CELL

a1220                       NAND2_1
a1230                       MUX2
a1240                       NOR2_1
a1310                       A1310
a1620                       A1620
a1720                       A1720
a2311                       A2311
lab5                        top_cell
```

Notes:

How to Select Cell Correspondence

How to Select Cell Correspondence
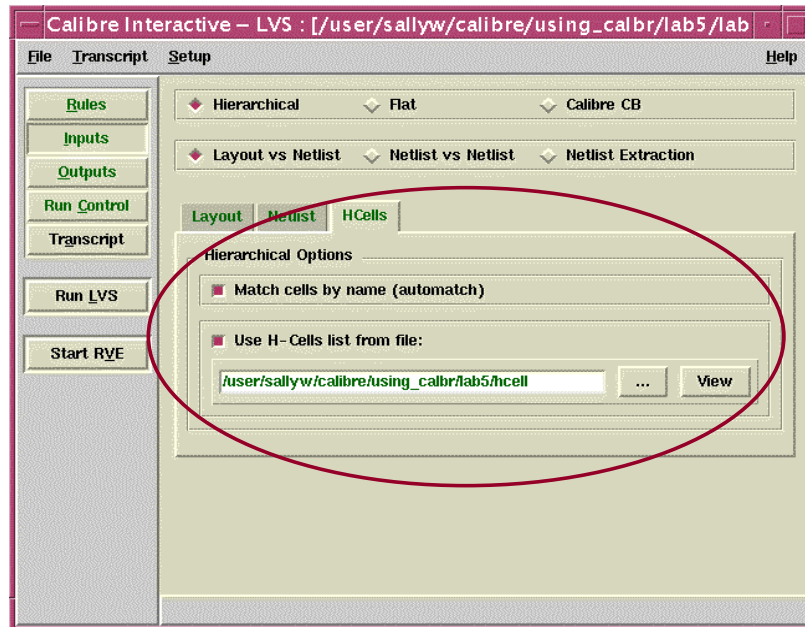
Notes:

Aid for Hcell File Creation: Query Server

Aid for Hcell File Creation: Query Server

- ◆ **What is the Query Server?**
  - **Command line driven**
  - **Access results database information**
  - **Response to queries**
  - **Examples:**
    - list of cells in layout design
    - list of devices attached to a net
    - list of nets connected to a device
  - **Launch from the command line:**
    `calibre -query [results_database top_cell]`

- ◆ **What can the Query Server do to help with Hcell file creation or maintenance?**
  - **Automatically generate complete Hcell file**
  - **Assist with intelligent or selective creation of Hcell file**
  - **Automatically create Hcell file meeting a savings threshold**

Notes:

Useful Query Server commands:

quit
Exits the Query Server and returns to the prompt.

help commands
quick listing of all commands available from the Query Server

response file <filename>
Writes the results to a file (filename) rather than to the standard output. The Query Server will continue to output to the file until you give it the "response direct" command.

response direct
Outputs the results to the screen (STDOUT)

Automatically Generating an Hcells List Using the Query Server

Automatically Generating an Hcell List Using the Query Server

1. **Launch the Query Server:** `calibre -query`

2. **Automatch Hcells by name:** `netlist  automatch on`

3. **Match Hcells by placement count:** `netlist placementmatch on`

4. **Read the rule file:** `netlist read rule_file`

5. **Create Hcell report:** `netlist select hcells`

6. **Specify Hcell file name:** `response file all_hcells`

7. **Create Hcell file:** `netlist report hcells`   `See a transcript`

Notes:

The example above automatically generates an Hcell list by matching the cell names, pin counts, and number of placements. It then limits the Hcell file to the default memory savings threshold (30%). This may not give you the "best" results, but it will quickly give you a place to start.

A complete transcript of the Query Server generating a basic Hcell list is given in Appendix C: Query Server Transcripts, "Transcript of Generating a Basic Hcells List Using the Query Server" on page C-1.

Selective Hcell Creation Using the Query Server

Selective Hcell Creation Using the Query Server

1. **Launch the Query Server:**

   `calibre -query`

2. **Read in netlists specified in rule file:**

   `netlist  read rule_file`

3. **Generate hierarchy report for layout:**

   `netlist report hierarchy layout`

4. **Scan the report file:**

```
<--------------- Flat ---------------->   <-------        Preserving cell a2311 will give          (9)        (10)
   (1)        (2)        (3)       (4)      (5        29% memory savings                                       Cell Name
Instances   Devices     Total    % Total  Instances  Instances     Total    % Total                 %     * (leaf cell)
 of this    in this     Device    Device   of this    in this     Instance  Instance               Memory + (hcell)
  Cell       Cell      Contrib.  Contrib.    Cell      Cell       Contrib.  Contrib.               Savings = (same name)
            (FDC)      (1)x(2)   (3)/TFDC             (HIC)       (5)x(6)   (7)/THIC
=========  =========  ========  ========  =========  =========   ========  ========   ========   ========  =============
     10        10        100        36        10        10          100        36         29       *    a2311
     22         4         88        31        22         4           88        31         22       *    a1220
      4         8         32        11         4         8           32        11        7.1       *    a1240
      5         6         30        11         5         6           30        11        6.8       *    a1230
      3         6         18       6.4         3         6           18       6.4        3.2       *    a1620
      3         2          6       2.1         3         2            6       2.1        0.4       *    a1310
      1       280        280     100.0         1       280          280     100.0        0.0       +=   lab8
      1         6          6       2.1         1         6            6       2.1        0.0       *    a1720
    140                                      140                                                             MP
    140                                      140                                                             MN
```

Notes:

Selective Hcell Creation Using the Query Server (Cont.)

Selective Hcell Creation Using the Query Server (Cont.)

5. Add a2311 to Hcell list: `netlist hcell a2311 s2311`

6. Generate new hierarchy report: `netlist  report hierarchy layout`

7. Scan the new report file:

> Consider adding a1220 to Hcell list saving 31%

> Cell a2311 is an Hcell and will not be flattened

```
<------                                 ----------- With Hcells ------------->
        (                               (5)       (6)       (7)       (8)       (9)           (10)
Instanc                              nstances  Instances    otal    % Total       %        Cell Name
of this      in this   Device   Device  of this  in this  Instance  Instance   Memory   *  (leaf cell)
  Cell         Cell   Contrib.  Contrib.   Cell    Cell   Contrib.  Contrib.  Savings  +  (hcell)
              (FDC)   (1)x(2)  (3)/TFDC                   (HIC)    (5)x(6)  (7)/THIC            = (same name)
=========  =========  ========  ========  =========  =========  ========  ========  =======  ==  ================
    22          4        88       31        22        4        88       44        31    *   a1220
     4          8        32       11         4        8        32       16        10    *   a1240
     5          6        30       11         5        6        30       15       9.5    *   a1230
     3          6        18      6.4         3        6        18        9       4.5    *   a1620
     3          2         6      2.1         3        2         6        3       0.5    *   a1310
     1        280       280    100.0         1      190       190       95       0.0   +=   lab8
    10         10       100       36         1       10        10        5       0.0   *+   a2311
     1          6         6      2.1         1        6         6        3       0.0        a1720
   140                                      95                                               MN
   140                                      95                                               MP
```

Notes:

Selective Hcell Creation Using the Query Server (Cont.)

Selective Hcell Creation Using the Query Server (Cont.)

8. **Add a1220 to Hcell list:**   `netlist hcell a1220 s1220`

9. **Generate new hierarchy report:**   `netlist  report hierarchy layout`

10. **Scan the new report file.**

11. **Repeat until satisfied with Hcell list.**

12. **Define filename:**   `response file test_hcells`

13. **Write custom hcell file:**   `netlist report hcells`

> See a transcript

Notes:

A complete transcript of the Query Server generating a basic Hcell list is given in Appendix C: Query Server Transcripts, "Transcript of Interactively Creating Hcell File" on page C-4.

Automatically Create Hcell File Meeting a Threshold

1. **Launch the Query Server:**   `calibre -query`

2. **Automatch Hcells by name:**   `netlist  automatch on`

3. **Match Hcells by placement count:**   `netlist placementmatch on`

4. **Read the rule file:**   `netlist read rule_file`

5. **Name the current Hcell file:**   `netlist hcells thold_hcells`

6. **Set the evaluation threshold to 10%:**   `netlist evaluation threshold 10`

Notes:

Automatically Create Hcell File Meeting a Threshold (Cont.)

Automatically Create Hcell File Meeting a Threshold (Cont.)

**7.Ignore Hcells in the
 current Hcell file:**   `netlist evaluate current hcells no`

OR

**7.Clear the hcells in the
current list:**   `netlist clear hcells`

8.Generate Hcell report: `netlist select hcells`

9.Specify Hcell file: `response file thold_hcells`

**10. Generate the new
 Hcell file:**   `netlist report hcells`

See a
transcript

Notes:

A complete transcript of the Query Server generating a basic Hcell list is given in Appendix C: Query Server Transcripts, "Transcript of Updating an Existing Hcell File Using a New Threshold" on page C-11.

Other Uses for the Query Server

Other Uses for the Query Server

- ♦ **Find what devices are connected to a given net**
- ♦ **Find what nets are connected to a given device**
- ♦ **Find bad devices**
- ♦ **Find deviceless cells**
- ♦ **Find pseudo cells**

- ♦ **Look in the *Calibre Verification User's Manual* for more functions**

Notes:

Lab Information

<div align="center">

Lab Information

</div>

In this lab session you will:

- ◆ **Run Calibre LVS**
- ◆ **View the Transcript**
- ◆ **View the LVS Report**
- ◆ **Run Calibre LVS in hierarchical mode using automatic cell correspondence**
- ◆ **Use Calibre RVE to view the LVS-H Results Database**
- ◆ **Create an Hcell Correspondence File and use it with Calibre LVS-H**
- ◆ **Use the Calibre RVE SPICE Netlist Browser to cross-probe between netlists**
- ◆ **Experiment with the Query Server**

Notes:

Lab: Basic LVS Concepts

In the past two labs you have been working with LVS without a formal introduction to the interface or reports. In this lab, you will learn how to use the Calibre Interactive LVS interface and a formal introduction on how to read the reports. You will also experiment with the Query Server to automatically generate Hcell files.

List of Exercises

Exercise 7-1: Basic LVS Run

In this exercise you will manually load all of the information required for a Calibre LVS run. You will then run LVS and scan through all the various reports and generated files.

1. Change you directory to lab7.
   ```
   cd $HOME/using_calbr/lab7
   ```

2. List the files in the directory.

   You should see the seven files:

   - golden_rules

   - lab7_rules

   - lab7a.gds

   - lab7a_source.spi

   - lab7b.gds

   - lab7b_source.spi

   - layer_props.txt

   - lay.net

   - query_rules

   If any of these files are missing, please double check that you are in the correct directory, and then notify your instructor.

3. Launch DESIGNrev.
   ```
   $MGC_HOME/bin/calibredrv
   ```

4. Open the GDSII file, lab7a.gds.

5. Load the layer properties file, layer_props.txt.
    (**Menu: Layer > Load Layer Properties**)

6. Launch Calibre Interactive LVS on cell lab7a.

7. Choose **New Runset**.

    You should now have the Calibre Interactive - LVS window open to Inputs
    with the default information loaded.

8. Select Hierarchical.

9. Select Layout vs. Netlist.

10. Enter lab7a.gds as the Layout file.

11. Make sure **Import layout database from layout viewer** is <u>unselected</u>.

12. Enter lab7a as the primary cell.

13. Enter lab7a_layout.net as the layout netlist.

The window should look similar to below.
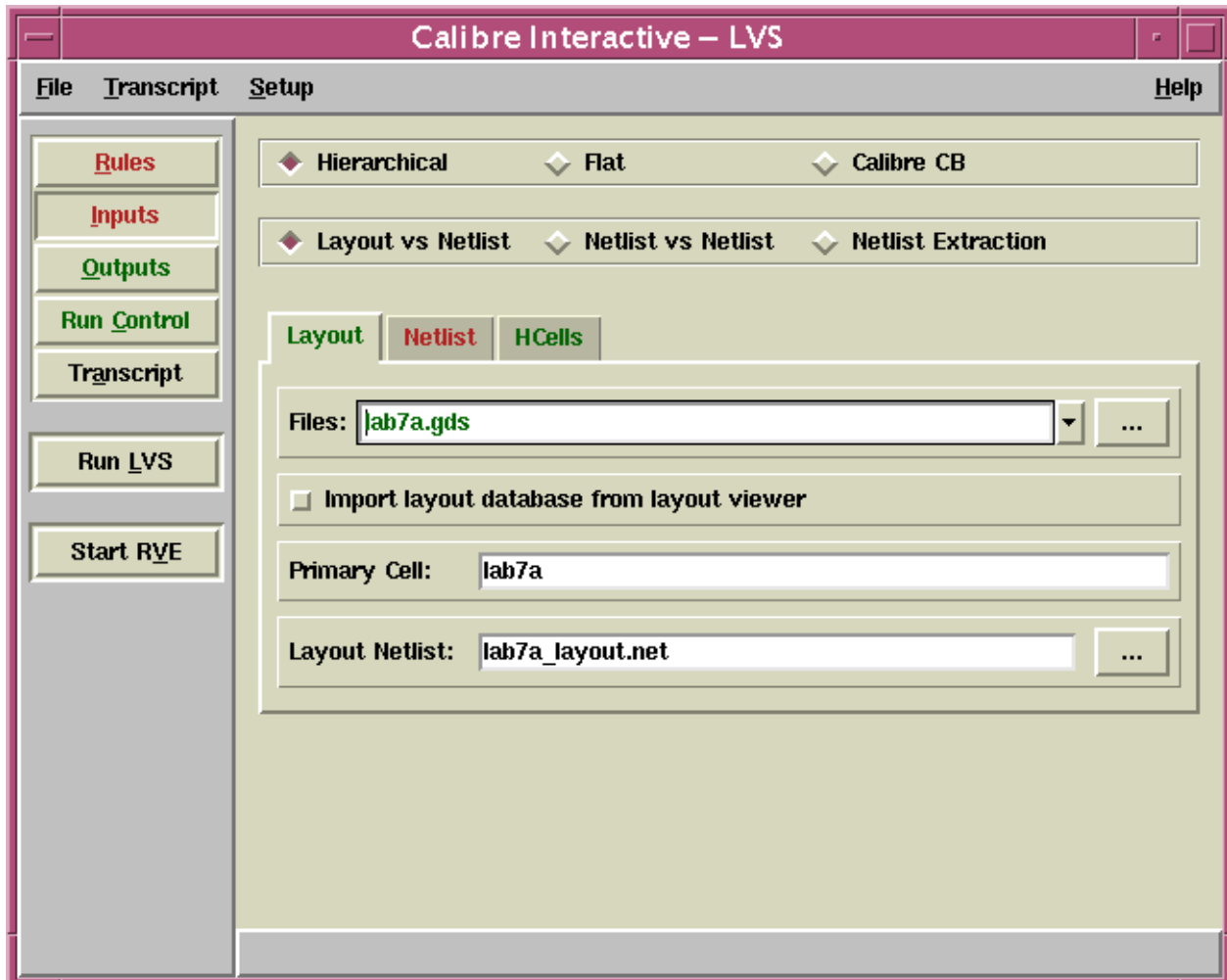
Before you enter information for the next tab, answer the following questions about your selections.

You selected Layout vs. Netlist. What information did you need to provide for the layout?

_____

_____

_____

Do all these files have to "exist" before the Calibre LVS run? Explain.

_____

_____

What do you expect Calibre LVS to do before the actual LVS comparison?

_____

What if you select Netlist vs. Netlist, what layout information would Calibre LVS need?

_____

_____

Do all these files have to "exist" before the Calibre LVS run? Explain.

_____

_____

Where would the layout netlist come from in this case?

_____

_____

What benefits exist for using this two-step process?

_____

_____

Now that you have thought about the various options for the layout, you are ready to enter more data.

14. Choose the **Netlist** tab.

15. Enter lab7a_source.spi as the Netlist File.

16. Select **SPICE** as the Netlist Format.

17. Make sure **Import netlist from schematic viewer** is unselected.

18. Enter lab7a as the Primary Cell.

The dialog box should look similar to below.
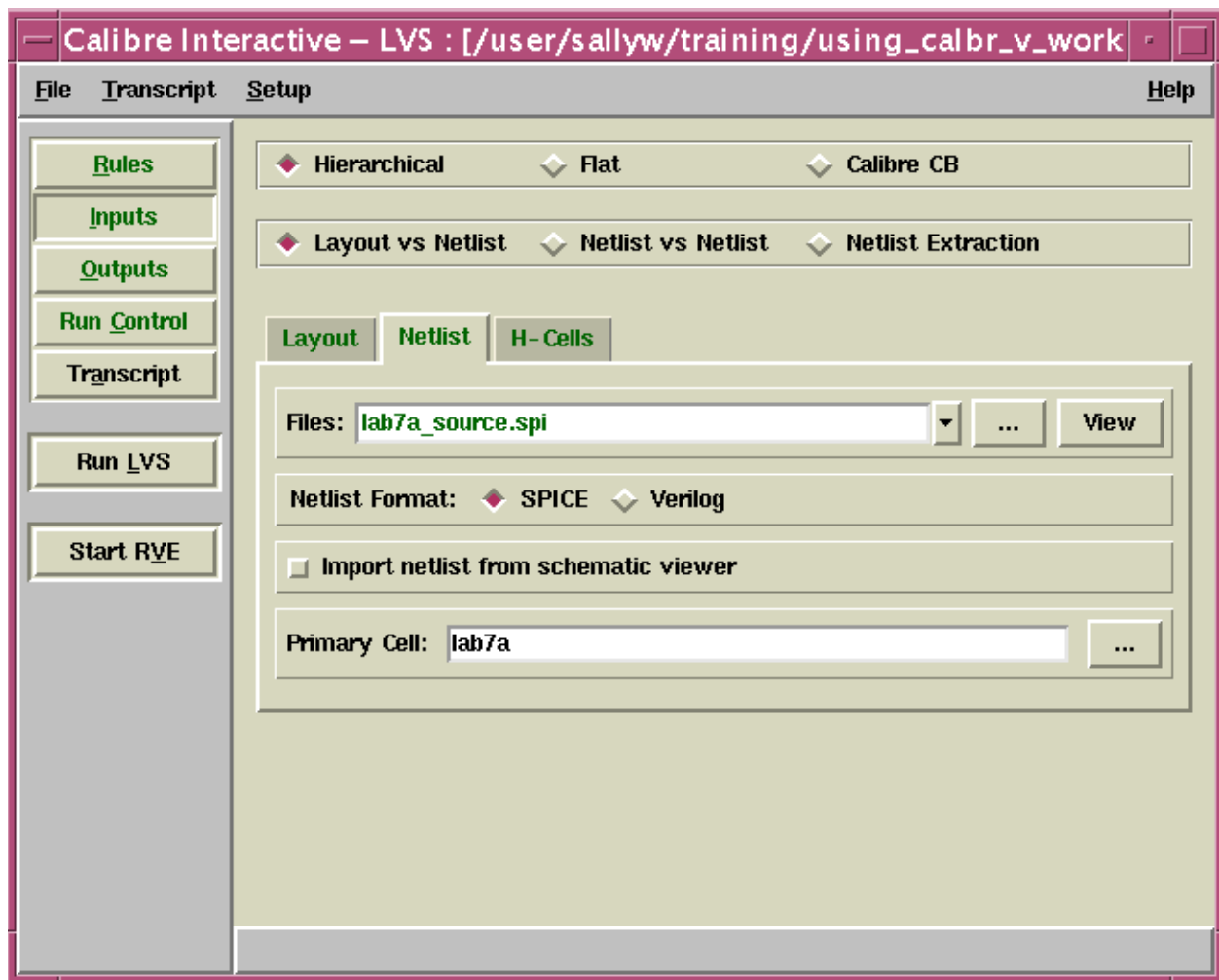
19. Choose the **HCells** tab.

20. Select Match cells by name (automatch).

21. Unselect Use H-Cells list from file.

The Calibre Interactive — LVS window should look similar to below.
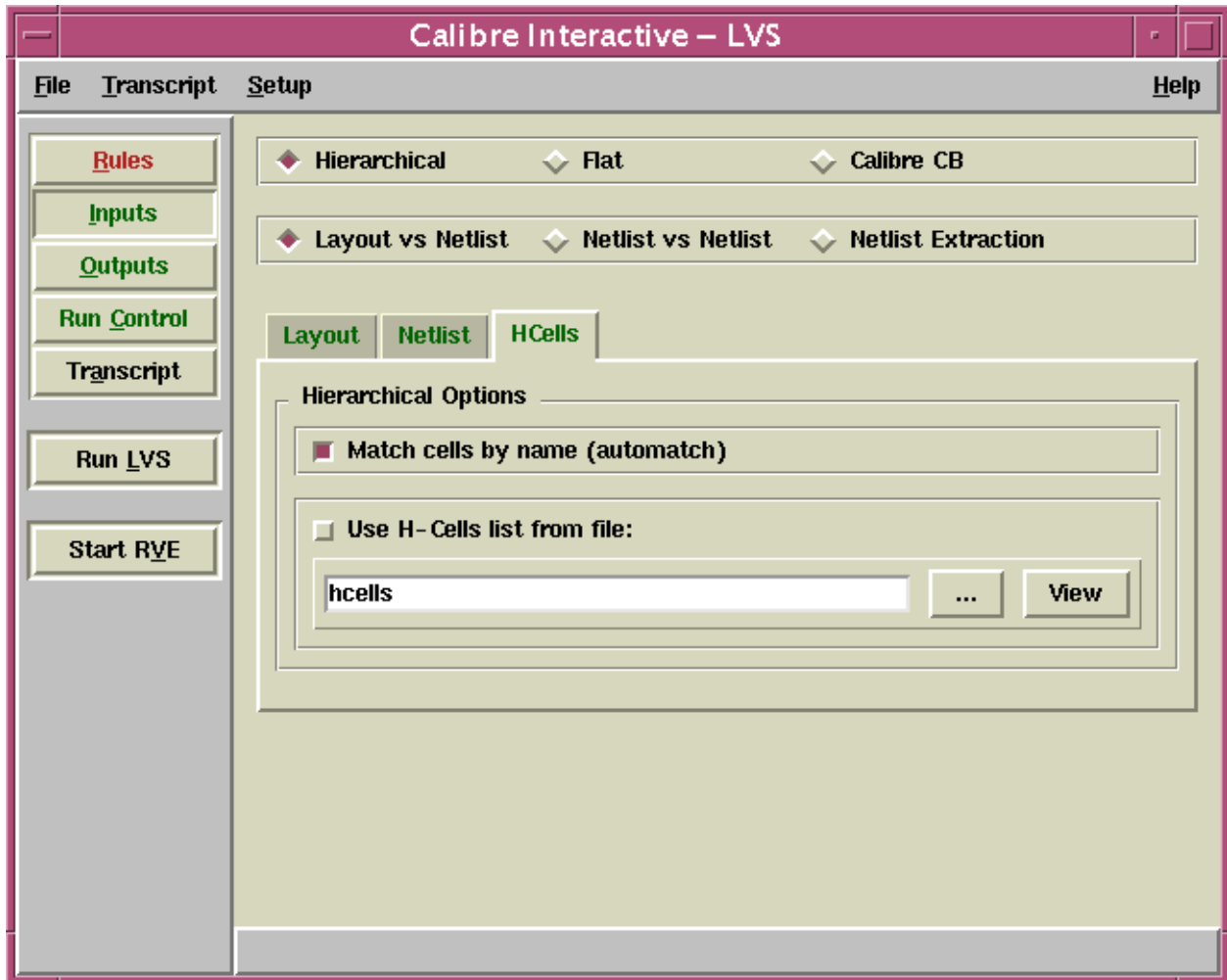
What is automatching? (Think Hierarchy.)

_____

_____

22. Choose the **Rules** Menu button.

23. Enter lab7_rules as the Calibre- LVS Rules File.

24. Choose **Load** to load the rule file.

25. View the rule file.

What does this rule file do?

_____

26. Close the rule file.

27. Enter "." (no quote marks) as the Calibre - LVS Run Directory.

The Calibre Interactive — LVS window should look similar to below.
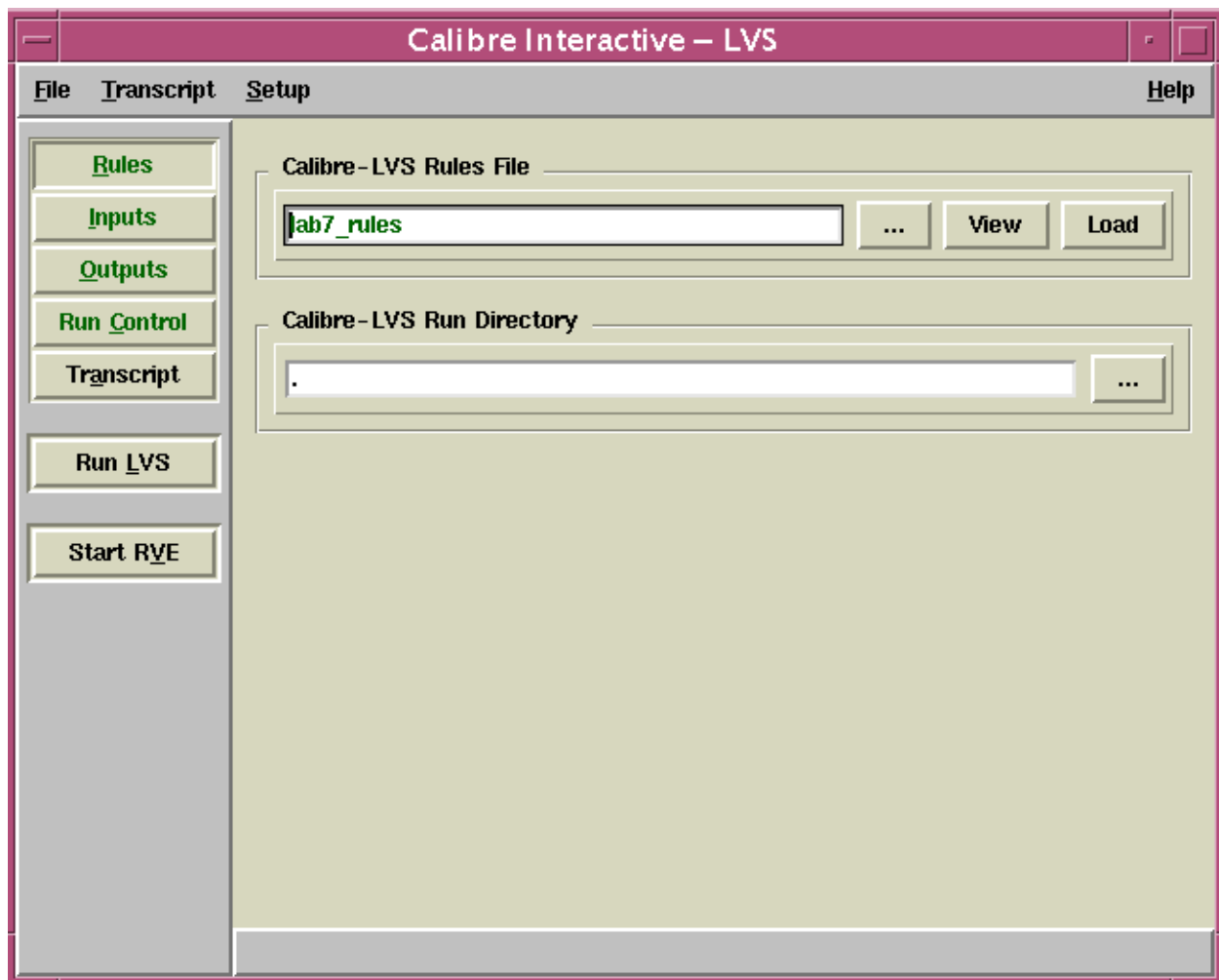
28. Choose the **Outputs** Menu button.

29. Enter lab7a_lvs.report as the LVS Report File.

30. Select **View Report after LVS finishes**.

31. Select **Create SVDB Database**.

32. Select **Start RVE after LVS finishes**.

33. Unselect **Generate data for Calibre - xRC**.

34. Unselect **Generate Calibre Connectivity Interface data**.

35. Enter svdb as the SVDB Directory.

The Calibre Interactive - LVS window should look similar to below.
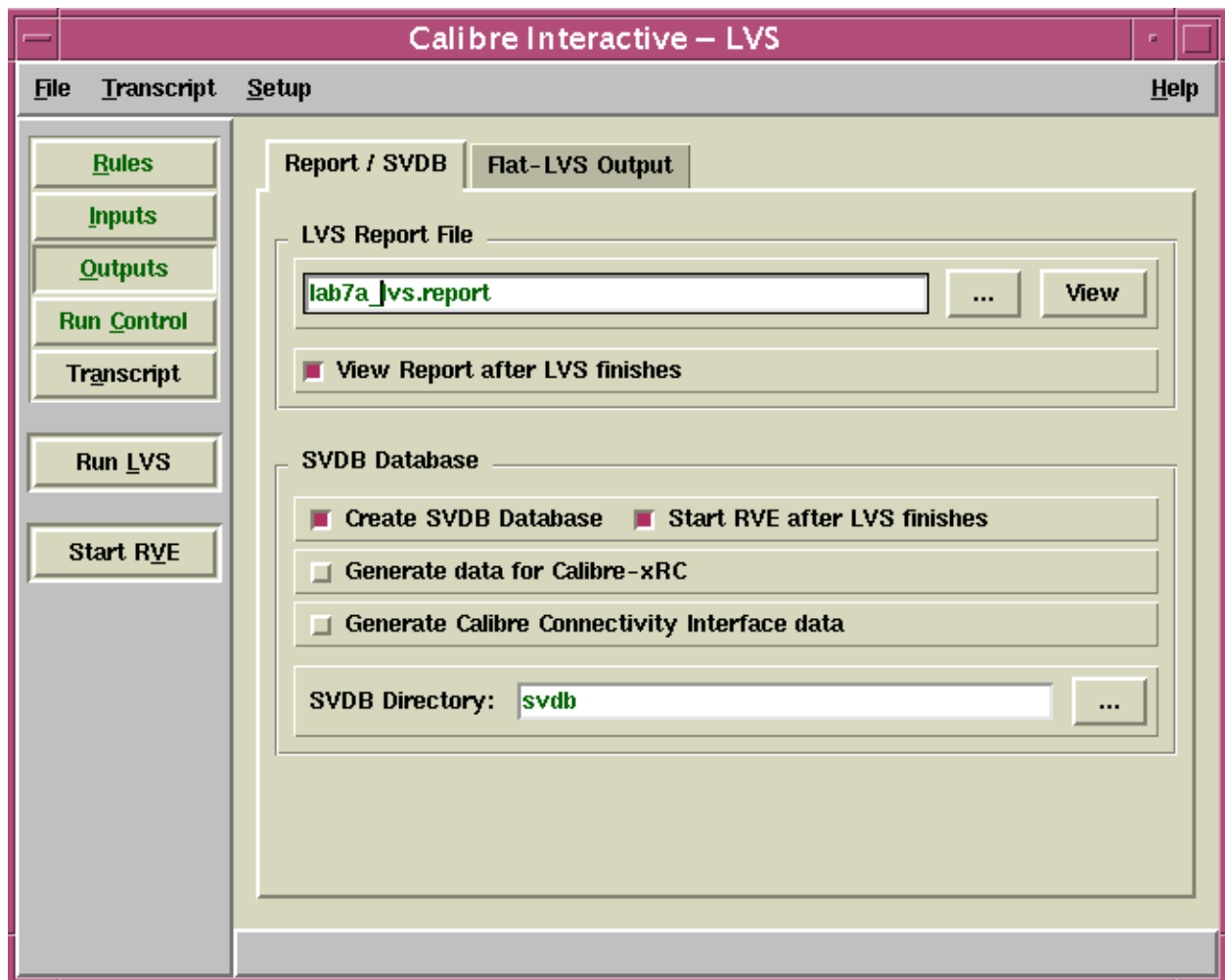
We do not need to enter any data on the Flat-LVS Output tab.

Do you know why?

_____

Now that you have all the data entered you are ready to perform an LVS run.

36. Choose **Run LVS** from the Menu button.

> **Note** If you get a message box asking to overwrite layout file, lab7a.gds, cancel the message box and return to the **Input** Menu button/**Layout** tab. Make sure **Import layout database from layout viewer** is <u>unselected</u>, then try running LVS again.

When LVS completes, Calibre Interactive -LVS should display the Transcript, the LVS report should be open in a new window, and a LVS RVE window should be open with the results loaded.

First you will quickly review the transcript.

37. Starting at the top, skim through the transcript.

Which part of the LVS operation seemed to take the longest? (Based on the amount of information in the transcript.)

_____

Is the comparison correct?

_____

38. Look at the LVS report.

You have seen this report several times in previous labs, lets test to see how much information you can find from this report.

What are the initial correspondence points?

_____

What are the total number of instances in both the source and layout inside cell lab7a?

_____

What are the total number of nets inside lab7a?

_____

Since this is a correct report it is not terribly interesting.

39. Close the LVS Report window.

40. Make the LVS RVE window active.
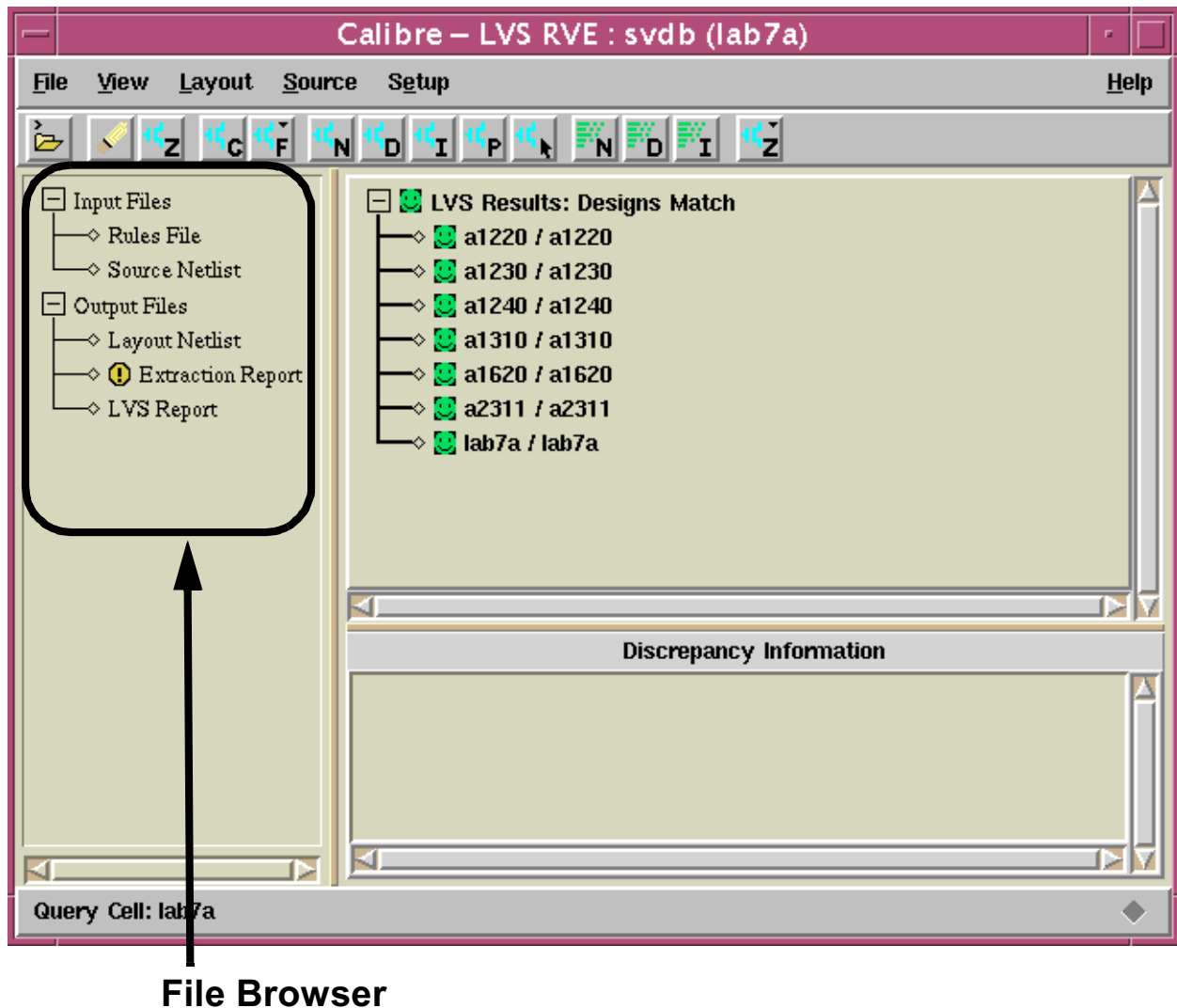
File Browser

Notice all the cells are displayed and they all have "happy faces".

The LVS RVE window has one additional frame that the DRC version does not have, the File Browser.

The File Browser allows you to view the netlists and reports quickly. You have already seen some of this functionality in other labs, we will now spend time on the netlists so you can get a deeper understanding.

41. Click on the **Source Netlist** in the File Browser.

    This opens the source netlist in a new window.

42. Click on the **Layout Netlist** in the LVS RVE File browser.

    This opens the layout netlist in a new window.

43. Arrange the two netlist windows so you can see both at the same time.

44. In both windows, expand the Network and subcircuits to display lab7a, by clicking on the "+" in front of **Top Network** and again for **Subckts**.

    The windows should look similar to below.
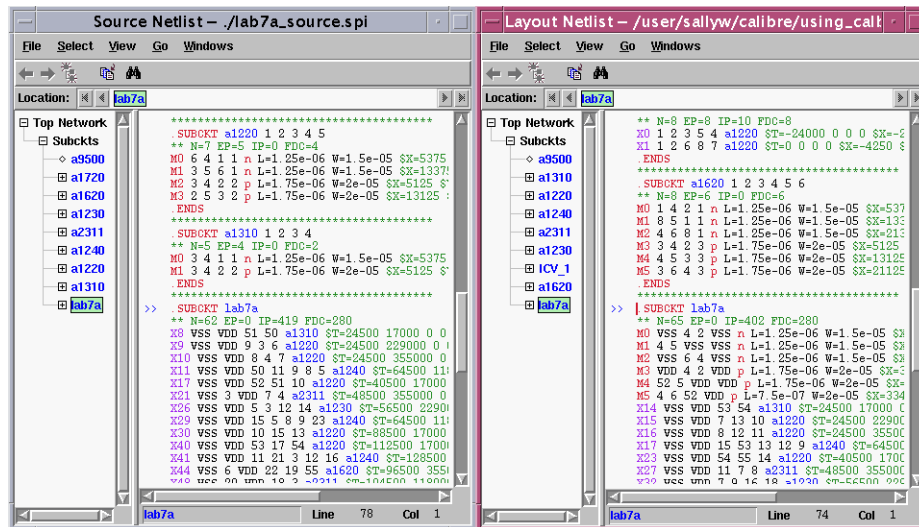
45. Click on instance X9 in the Source netlist.
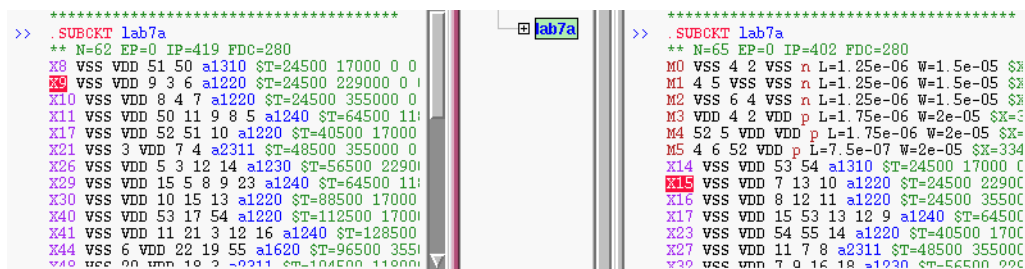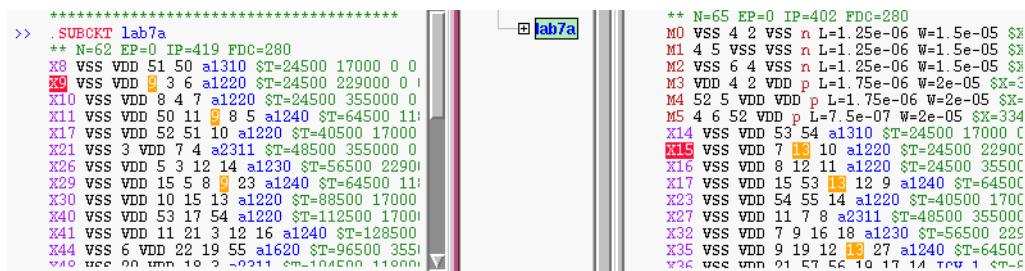
What happened?

_____

How can these instances with different names match?

_____

46. Click on Net 9 (on instance X9) in the source netlist.

You may need to scroll the netlists to view all the highlights.

What happened?

_____

_____

What did you learn about net and instance names?

_____

How easy do you think it would be to match these "by hand"?

_____

47. (Optional) Try matching one of the instances by hand.

48. Make the layout viewer window active.

What do you see?

_____

You can highlight instances and nets in the layout by selecting them in the schematics.

49. Experiment with cross referencing between the netlists and layout until you are comfortable with the mechanics of the operation.

50. Using the LVS RVE window, clear (erase) all highlights.

   Make sure to leave all netlist windows and RVE open for use in the next exercise.

Exercise 7-2: Additional LVS RVE Functionality

You already know how to display netlists and cross probe between the netlist and the layout. In this exercise you will experiment with additional functionary provided by LVS RVE.

First you will review the functional available from the toolbar.

1. Find the function(s) available from each unique Toolbar icon:
   (**Hint**: Use the Query Help or the *Calibre Verification User's Manual*.)

_____

_____

_____

_____

_____

_____

_____

In this exercise you will experiment with using the N (nets), D (devices), and I (instances) tools. Before you start actively experimenting with the buttons notice that they are two different colors (blue and green).

What does the "blue" color indicate?

_____

What does the "green" color indicate?

_____

These colors are used consistently to flag layout and source to help you keep track of what information you are seeing.

Now you are ready to experiment with the toolbar.

2. Erase any of the current highlights.

3. Choose **Query Layout Nets** from the toolbar.

This opens the Query Layout Nets in lab7a dialog box.

4. Choose **Browse**.

This opens the Browse Nets dialog box. We are going to start at the top of the hierarchy and work our way down.

5. Click on lab7a in the Hierarchy in lab7a area.

   Lab7a should now be surrounded by a blue selection box and all the nets in the cell are listed in the Nets in selected cell box.

6. Select net 27.

   The Browse Nets dialog box should look similar to below.
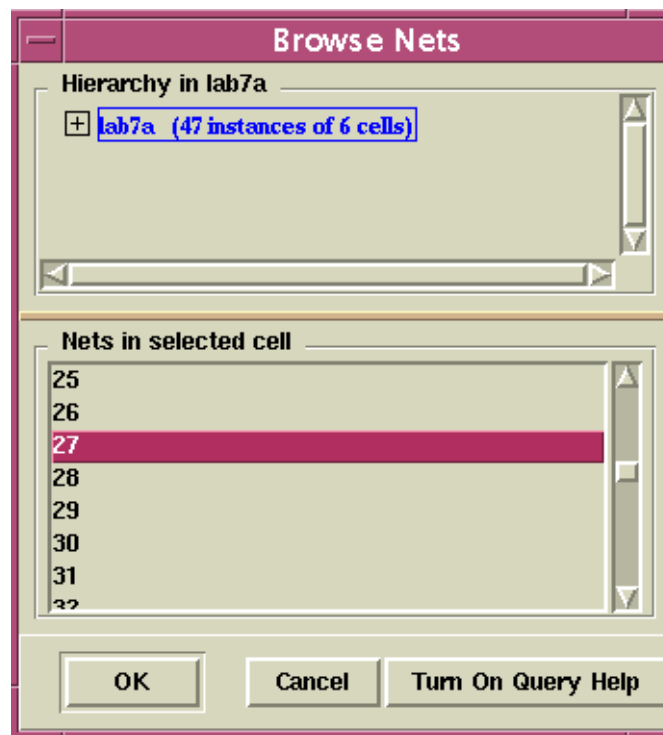
7. Choose **OK** to execute the dialog box.

   This returns you to the Query Layout Nets in lab7a dialog box with net 27 loaded as the layout net.

8. Choose **Net Info**.

This opens the Net 27 in lab7a dialog box. From this dialog box you can find all kinds of information about the net.

```
┌─────────────────────────────────────┐
│ ─    │   Net 27 in lab7a            │
├──────────────────────────────────────┤
│ ⊟ Ⓝ Net 27 in layout cell lab7a    ▲ │
│     ⊞ Net Layers                     │
│     ⊞ Instances on net               │
│     ⊞ Devices on net                 │
│     ⊞ Ports on net                   │
│     ⊞ Corresponding Source Net(s)    │
│     ⊞ Hierarchical Name(s)           │
│                                      │
│                                      │
│                                      │
│                                      │
│                                      │
│  ◁▭▭▭▭▭▭▭▭▭▭▭▭▭▭▭▭▭▭▭▭▭▭▭▭▭▭▷ ▽ │
└──────────────────────────────────────┘
```
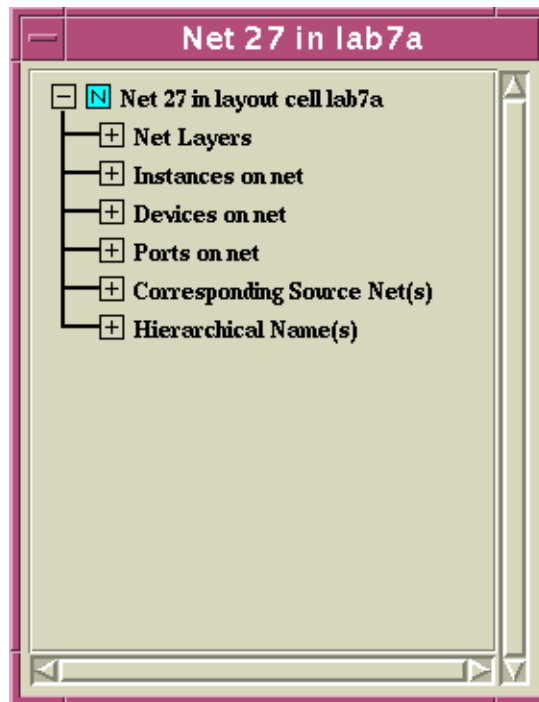
9. Using the Net 27 in lab7a dialog box, answer the following questions.

What layers are a part of net 27?

_____

What instances connect to net 27?

_____
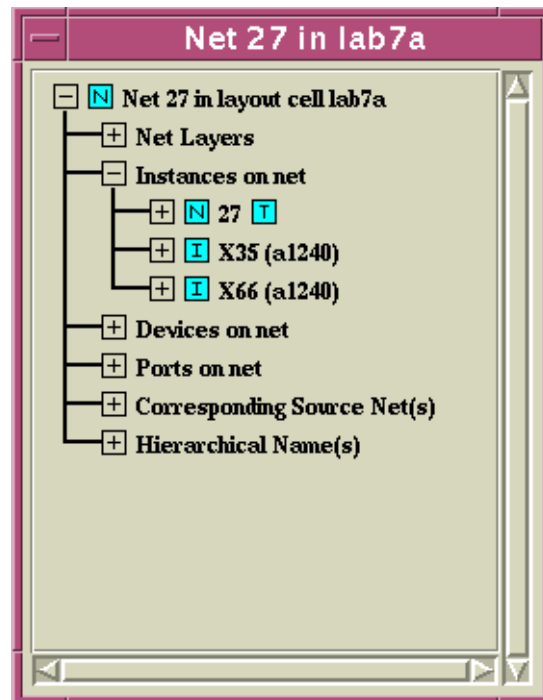
Can you highlight the instances directly from the Net 27 in lab7a dialog box?

_____

You may notice that you have two options for highlighting from the **Net 27 in lab7a** dialog box. If you click on the "**N**" in front of the net, you will highlight the net. If you click on the "**T**" after the net, you will trace the net.

highlight net **trace net**
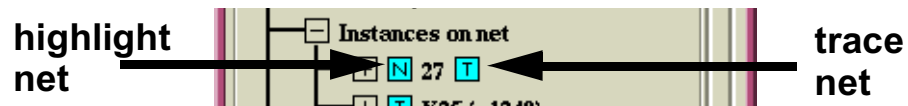
10. Try Highlighting the instances and nets from this dialog box.
    (Make sure to experiment with highlighting a net versus tracing a net.

Highlighting the net　　　　**Tracing the net**
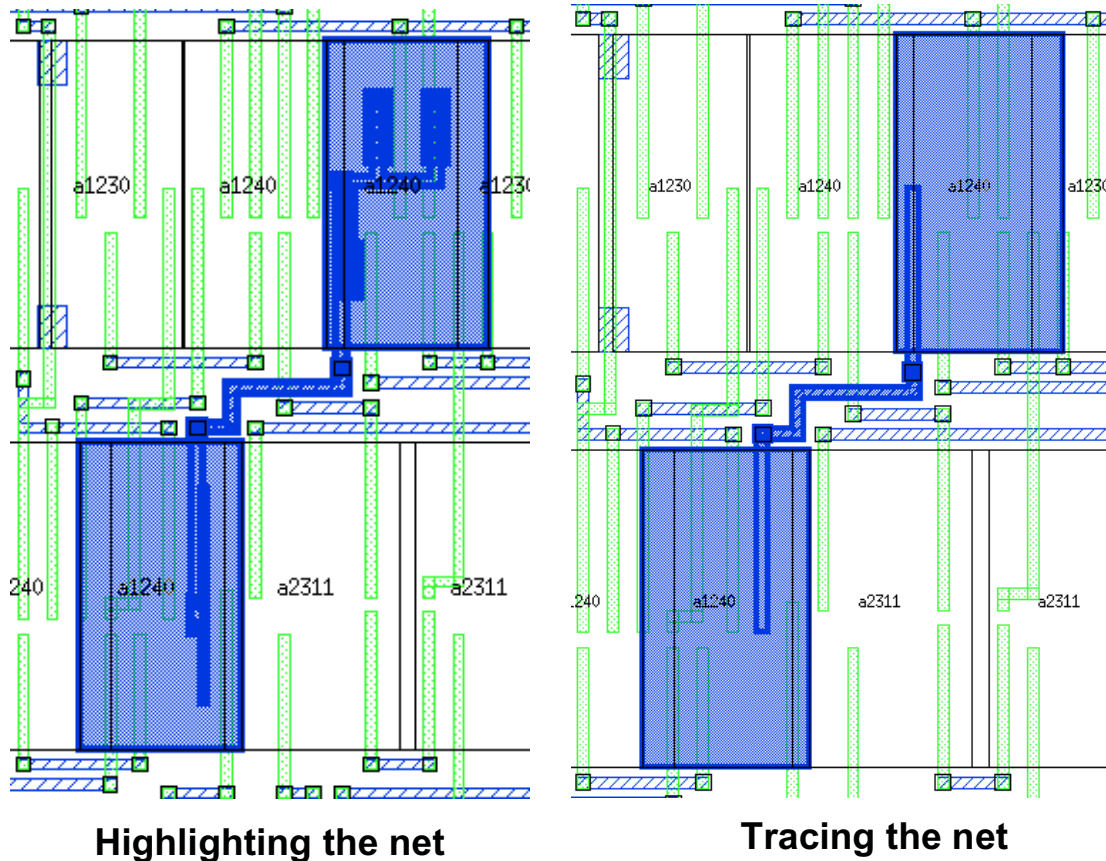
> **Note**　Notice the difference between highlighting a net and using trace. Trace does not take you below the current hierarchy, while highlighting will show the net where ever it travels in the hierarchy.

11. When you are finished erase all highlights.
    Notice that you need to go back to the RVE window to erase highlights.

How many devices connect to net 27?

_____


```
┌─ Net 27 in lab7a
└─ Devices on net
   └─ Show devices hierarchically (2 instances)
      └─ [I] (2 devices) X35 (a1240)
         ├─ + Instance info
         ├─ + [D] X35/M3 (g) (mn)
         └─ + [D] X35/M7 (g) (mp)
      └─ [I] (5 devices) X66 (a1240)
         ├─ + Instance info
         ├─ + [D] X66/M3 (d) (mn)
         ├─ + [D] X66/M4 (d) (mp)
         ├─ + [D] X66/M5 (s) (mp)
         ├─ + [D] X66/M6 (d) (mp)
         └─ + [D] X66/M7 (s) (mp)
   └─ Show all devices (7 devices)
      ├─ + [D] X35/M3 (g) (mn)
      ├─ + [D] X35/M7 (g) (mp)
      ├─ + [D] X66/M3 (d) (mn)
      ├─ + [D] X66/M4 (d) (mp)
      ├─ + [D] X66/M5 (s) (mp)
      ├─ + [D] X66/M6 (d) (mp)
      └─ + [D] X66/M7 (s) (mp)
└─ + Ports on net
└─ + Corresponding Source Net(s)
```
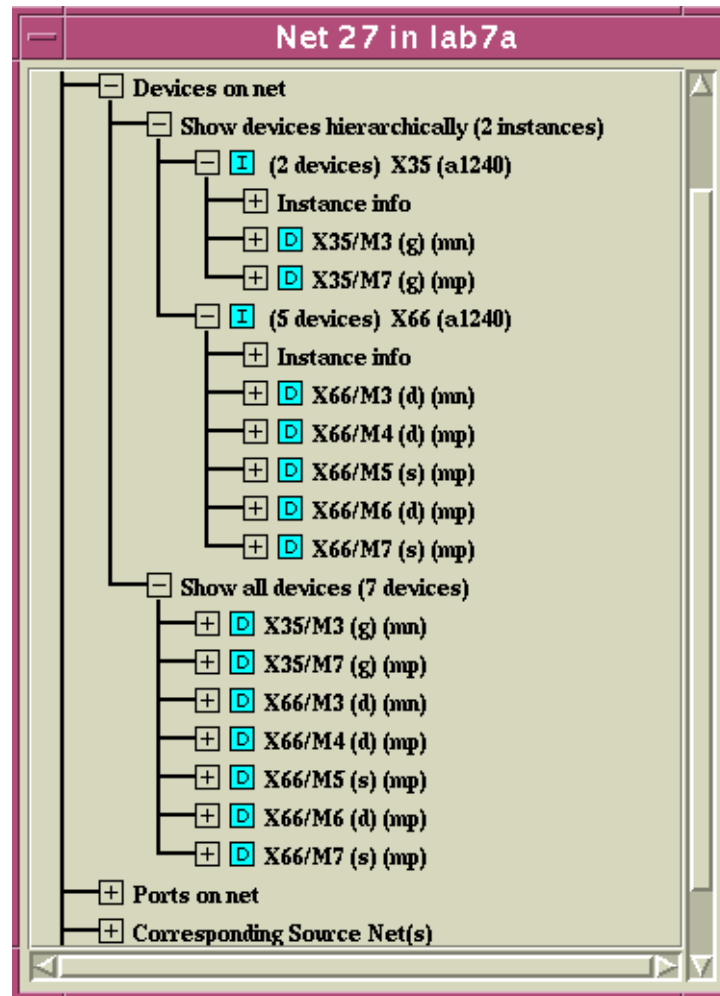
Note You can adjust the size of the Net 27 in lab7a dialog box to display the information you want to see by "stretching" the corners or edges.

12. Experiment highlighting the devices.

What highlights?

_____

Notice that the devices also highlight in the netlists during these experiments.

13. When you are finished experimenting with the devices, erase all highlights.

    What Source Net corresponds to Layout Net 27?

    _____
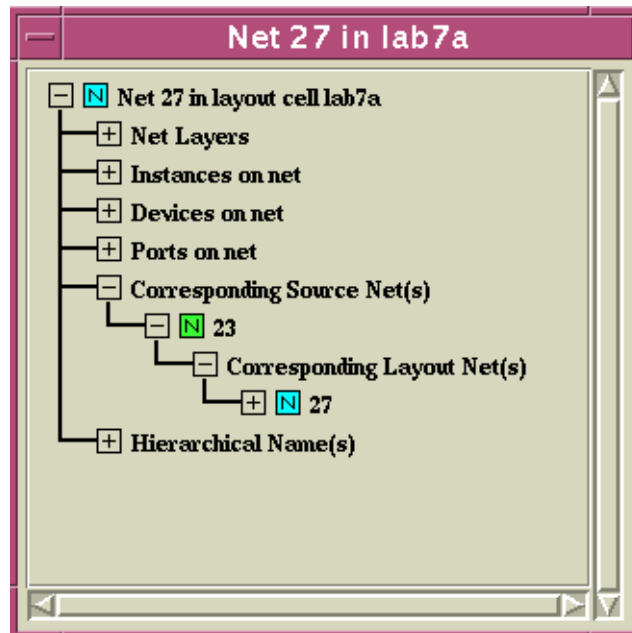
14. Close the Net 27 in lab7a by using the pull down menu from the upper left corner.

    This returns you to the Query Layout Nets in lab7a dialog box.

    Notice that many of the highlighting options available from the previous dialog box are also available from this one.

15. Experiment highlighting net 27 using the various options from the Query Layout Nets in lab7a dialog box.

16. When you are finished erase all highlights.

    This dialog box has one more feature that you may find useful for trouble shooting.

17. Choose **Net by Location**.

    The follow info box appears.

    Get Layout Location

    i Please click at a location in cell

    lab7a

    in the layout-viewer.

    Cancel

18. Click over any net of interest in the layout viewer.

    Notice that the net number automatically appears in the Layout Net text box.

19. If you want you may experiment by finding information on this net.

20. When you are finished, choose **Close** to exit the Query Layout Nets in lab7a dialog box.

21. Erase any highlights.

    Next you are going to query a layout device. First you need to understand what Calibre defines as a device.

Is a NAND gate a device?

_____

Is an NMOS transistor a device?

_____

How can you tell what Calibre defines as a device?
(Hint: rule file)

_____

22. Use the SVRF Manual to list all the available built-in devices.

Calibre's built-in devices are:

_____

_____

_____

_____

_____

_____

_____

_____

_____

Now that you understand what a device is, you can query a device.

23. From the RVE toolbar choose **Query Layout Device**.

This opens the Query Layout Devices in lab7a dialog box.

24. Choose **Browse**.

 This opens the Browse Devices dialog box.

25. Click on the "+" (plus) in front of lab7a to expand down the hierarchy.

26. Select X27: a2311.
 (It will have a blue box surrounding it when selected.)

 This fills all the information about the devices in the cell (a2311).

27. Select M3.
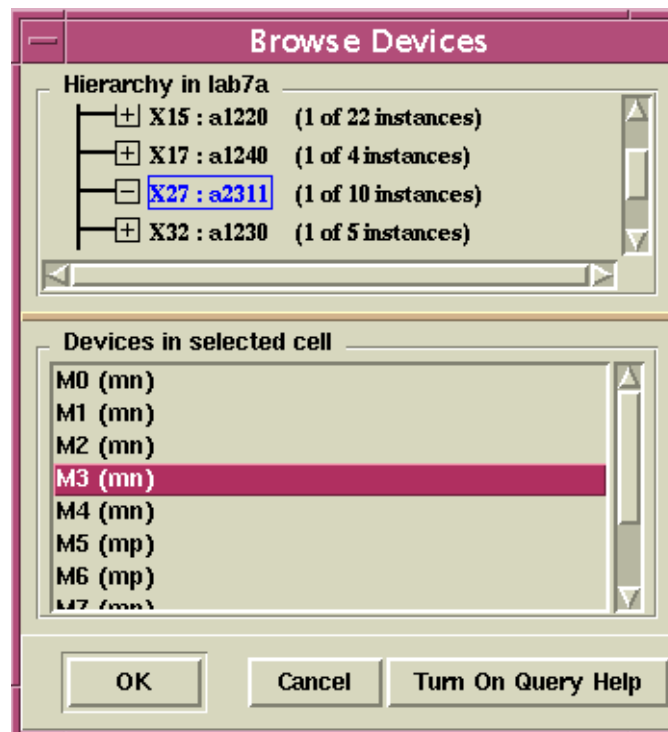
28. Choose **OK** to execute the Browse Devices dialog box.

This returns you to the Query Layout Devices in lab7a dialog box with "X27/M3" entered in the Layout Device text box.

Query Layout Devices in lab7a

Layout Device

X27/M3   Browse...

Device Info...   Device by Location...

◆ Highlight device
◇ Highlight nets connected to pins of device
◇ Highlight bad devices in query cell

Highlight   Close   Turn On Query Help
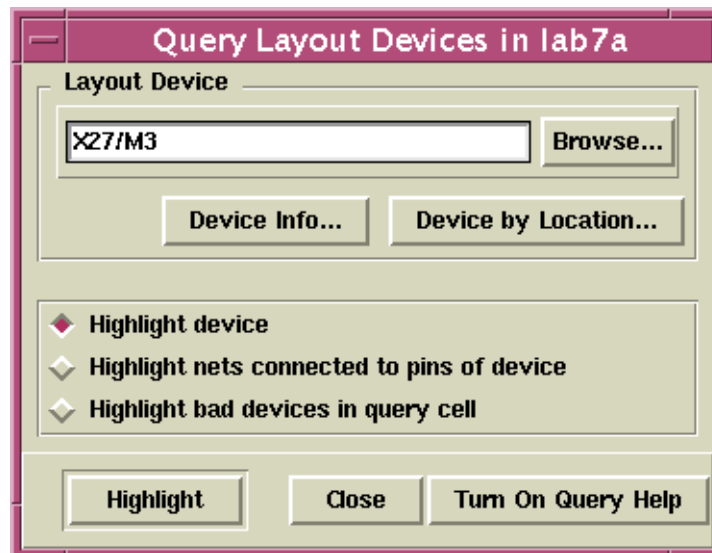
29. Choose **Device Info**.

30. Answer the following questions about X27/M3.

What is the seed layer?

_____

What pins does the device have and what are the connections?

_____

_____

_____

_____

Why does the net connected to the drain (d) include instance information when the other pins/connections do not?

_____

What properties does the device have?

_____

What is corresponding source device?

_____

```
┌─────────────────────────────────────────┐
│ ╳ Device X27/M3 in lab7a            [✕] │
├─────────────────────────────────────────┤
│  ⊟ [D] Device X27/M3 in layout cell lab7a│
│      ◇ Seed Layer: pgate                 │
│      ⊟ Pins                              │
│            ⊞ [N] (g) 11                   │
│            ⊞ [N] (s) VDD                  │
│            ⊞ [N] (d) X27/9                │
│            ⊞ [N] (b) VDD                  │
│      ⊟ Properties                        │
│           ◇ w = 2e-05                    │
│           ◇ l = 1.75e-06                 │
│      ⊞ Device Shape                      │
│      ⊟ Corresponding Source Device(s)    │
│            ⊞ [D] X21/M8                   │
└─────────────────────────────────────────┘
```
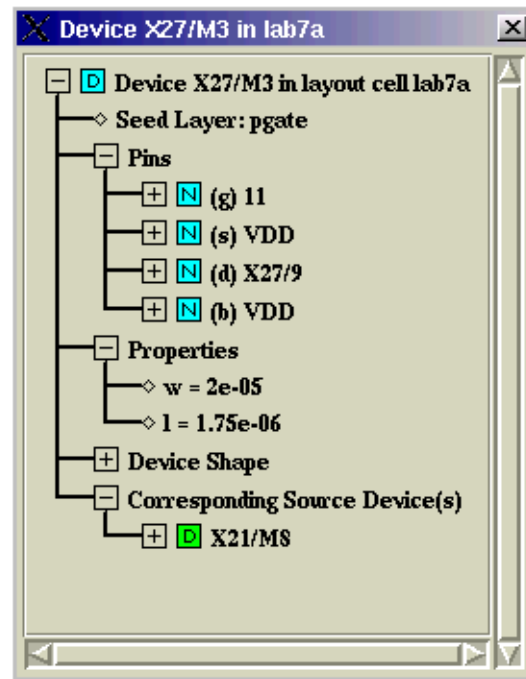
31. Experiment highlighting nets and instances from this dialog box.

32. When you are finished, experimenting with the Device X27/M3 in lab7a dialog box close it.

    This returns you to the Query Layout devices in lab7a.

33. Erase all highlights.

34. Experiment highlighting from the Query Layout devices in lab7a dialog box.

    Are there any bad devices in the query cell? (There should not be.)

35. When you are finished experimenting, erase all highlights.

    Notice that you can also select a device by clicking on it in the layout (just like you did previously for nets) by using the **Device by Location** command button.

36. Experiment selecting devices by using **Device by Location**.

37. When you are finished erase any highlights.

38. Close the Query Layout devices in lab7a dialog box

    Before finishing experimenting with RVE, take a look at the query source commands available.

39. Choose **Query Source Instances**.

    This opens the Query Source Instances in lab7a dialog box. Notice that the **Probe inst. in schematic** is grayed out. That is because you do not have a schematic. If you were using either ICStation or Composer and had a schematic available you could crossprobe all the way back to the schematic. (The data for this class does not have a schematic at its source.)

40. Enter X48 as the Source Instance.

41. Choose **Instance Info**.

    What is corresponding layout instance?

    _____

42. Close the Instance X48 in lab7a dialog box.

43. Highlight the instance in the netlist and the layout.

44. Close the Query Source Instances in lab7a dialog box.

45. Erase any highlights.

    You now have an introduction to the types of information available from the RVE toolbar.

46. Before going to the next exercise, spend a little time exploring features that were not directly covered in this exercise.

47. When you are finished experimenting erase all highlights.

48. Close the LVS RVE window and all netlist windows.
    (The Calibre Interactive—LVS window should still be open.)

Exercise 7-3: Hierarchical LVS and Hcells

In this lab you will run another LVS, this time with an error.

1. Make the DESIGNrev window active.

2. Open the GDSII file, lab7b.gds.

3. Make the Calibre Interactive - LVS window active.

    You should now have the Calibre Interactive - LVS window open to Inputs.

4. Enter the following **Inputs [Layout]** data:

Hierarchical, Flat, or Calibre CB	Hierarchical
Layout vs. Netlist, Netlist vs. Netlist, or Netlist Extraction	Layout vs. Netlist
Layout Files:	lab7b.gds
Import layout database from layout viewer	Unselected
Primary Cell	lab7b
Layout Netlist:	lab7b_layout.net

5. Enter the following **Input [Netlist]** data:

Netlist Files:	lab7b_source.spi
Import netlist from schematic viewer	Unselected
Primary Cell:	lab7b

6. Enter the following **Input [HCells]** data:

Match cells by name (automatch):	Selected
Use H-Cells list from file:	Unselected
[filename]	*does not matter*

7. Enter the following **Rules** data:

> Calibre-LVS Rules File: lab7_rules

> Calibre-LVS Run Directory: .

8. Enter the following **Outputs [Report/SVDB]** data:

LVS Report File:	lab7b_lvs.report
View Report after LVS finishes:	Selected
Create SVDB Database:	Selected
Start RVE after LVS finishes:	Selected
Generate data for xCalibre:	Unselected
Generate Calibre Connectivity Interface data:	Unselected
SVDB Directory:	svdb

9. Run LVS.

> What are your results?
> (Check the LVS Report.)

> _____

> What types of errors and warnings do you have?

> _____

> _____

> _____

10. Look at LVS RVE.

Without opening any file or even expanding the errors in the Results Viewing area, is there a difference between this run and previous LVS runs?

_____

Before you do anything else, you need to explore what happened to the cells in the file.

11. Open the Source and Layout Netlists.

12. Look at the first subcircuit in both netlists.

    What is the name of the first subcircuit?

    Layout: _____

    Source: _____

13. Look at the rest of the subcircuits in the Source and Layout.

    All the Source subcircuits begin with an "s" while the layout subcircuits begin with an "a". Calibre cannot build the hierarchy without perfect matches. You can create a matching list for Calibre.

    What is this list called?

    _____

    What format does this file use?

    _____

    _____

Write the list of subcircuits that need to be added to an Hcell file:

_____

_____

_____

_____

_____

_____

_____

14. Using any text file editor, create a file called lab7b_hcell.

15. Enter the Hcell data in the file.
    (Hint: You need at least seven lines.)

16. Save and close the file.

17. Close all RVE, netlist, and report windows you may have open.

18. Make the Calibre Interactive - LVS window active.

19. Display **Inputs [HCells]**.

20. Select Use H-Cells list from file.

21. Enter lab7b_hcell.

22. Run LVS.

Now what kind of errors and warnings do you have?

_____

What does RVE look like?

_____

_____

Do you think it will be easier to track down the errors now that the hierarchy is back?

_____

23. Open the Source and Layout netlists.

24. Expand the error in the results viewer.

25. Display the information on the discrepancy in the Discrepancy Viewer in RVE.

26. Click on one of the Discrepancies.

27. Double-click on one of the instance names in the Discrepancy Information window.

What happens?

_____

What about the layout viewer?

_____

As you can see, you can cross probe between the netlists, discrepancy lists, and layout.

In future labs we will track down and fix LVS errors, in this lab we were just exploring the tool and learning about the hierarchy.

28. Experiment with cross probing as desired.

29. Erase all highlights.

30. Close all Calibre related windows. (Including DESIGNrev, Calibre Interactive DRC/LVS, RVE, Netlist windows, and Summary Report.)

Exercise 7-4: Using the Query Server

In the previous exercise you entered a complete Hcell file "by hand". This is neither desirable or is it easy to maintain for a very large design. In this exercise you are going to create Hcell files using the Query Server. First you will create the file interactively, then you will create a file that automatically meets a given threshold.

Remember that the Query Server is a command line tool, so most of your work in this exercise will be directly from the command line.

1. Make sure you are in the lab7 directory.

2. Launch the Query server. Type:
   ```
   calibre -query
   ```

   This launches the Query Server. If it started correctly the last line should read: "OK: Ready to serve."

   Since this is a command line tool, you may want to maximize the window to make reading the results returned from the Query Server easier.

3. Read in the netlists (specified in the rule file). Type:
   ```
   netlist read query_rules
   ```

   If the Query Server read the rules properly and found the netlists there should be several lines about Reading the layout and Reading the source and ending with Deleting trivial pins. The last line should be "OK."

4. Generate the hierarchy report for the layout. Type:
   ```
   netlist report hierarchy layout
   ```

This generates the hierarchy report. The information you are looking for is above the Hierarchy Tree, so you may need to scroll up in the results.

```
<--------------- Flat -----------------> <----------- With Hcells ------------->
   (1)        (2)        (3)      (4)       (5)        (6)        (7)      (8)      (9)       (10)
Instances   Devices     Total   % Total  Instances  Instances   Total  % Total     %      Cell Name
of this     in this    Device   Device   of this    in this   Instance Instance  Memory  * (leaf cell)
  Cell       Cell      Contrib. Contrib.   Cell       Cell     Contrib. Contrib.  Savings + (hcell)
            (FDC)      (1)x(2)  (3)/TFDC             (HIC)      (5)x(6)  (7)/THIC          = (same name)
                                                                                          # (same #placements/pins)
========  ========  =======  =======  ========  ========  =======  =======  =======  ================
   10        10         100      36        10        10         100      36        29   *  # a2311
   22         4          88      31        22         4          88      31        22   *  # a1220
    4         8          32      11         4         8          32      11        7.1  *  # a1240
    5         6          30      11         5         6          30      11        6.8  *  # a1230
    3         6          18      6.4        3         6          18      6.4       3.2  *  # a1620
    3         2           6      2.1        3         2           6      2.1       0.4  *  # a1310
    1       280         280    100.0        1       280         280    100.0       0.0  +=    lab7b
    1         6           6      2.1        1         6           6      2.1       0.0  *  # a1720
  140                                     140                                             MN
  140                                     140                                             MP
```

Adding what cell to the hcell file will give the most savings?

_____

5. Add cell a2311 to the hcell list. Type:
    ```
    netlist hcell a2311 s2311
    ```

    (Remember that the source cells for this design all begin with "s".)

6. Generate a new hierarchy report. Type:
    ```
    netlist report hierarchy layout
    ```

```
<--------------- Flat -----------------> <----------- With Hcells ------------->
   (1)        (2)        (3)      (4)       (5)        (6)        (7)      (8)      (9)       (10)
Instances   Devices     Total   % Total  Instances  Instances   Total  % Total     %      Cell Name
of this     in this    Device   Device   of this    in this   Instance Instance  Memory  * (leaf cell)
  Cell       Cell      Contrib. Contrib.   Cell       Cell     Contrib. Contrib.  Savings + (hcell)
            (FDC)      (1)x(2)  (3)/TFDC             (HIC)      (5)x(6)  (7)/THIC          = (same name)
                                                                                          # (same #placements/pins)
========  ========  =======  =======  ========  ========  =======  =======  =======  ================
   22         4          88      31        22         4          88      44        31   *  # a1220
    4         8          32      11         4         8          32      16        10   *  # a1240
    5         6          30      11         5         6          30      15        9.5  *  # a1230
    3         6          18      6.4        3         6          18       9        4.5  *  # a1620
    3         2           6      2.1        3         2           6       3        0.5  *  # a1310
    1       280         280    100.0        1       190         190      95        0.0  +=    lab7b
   10        10         100      36         1        10          10       5        0.0  *+    a2311
    1         6           6      2.1        1         6           6       3        0.0  *  # a1720
  140                                      95                                             MP
  140                                      95                                             MN
```

Now what cell will give the most savings?

_____

Can you tell that a2311 is an hcell?

_____

7. Add cell a1220 to the hcell list. Type:
    ```
    netlist hcell a1220 s1220
    ```

8. Check what is in the current Hcell list. Type:
    ```
    netlist report hcells
    ```

    The Query Server should respond with:
    ```
    a2311 s2311
    a1220 s1220
    ```

9. Use the same process (steps 6 and 7 above) to find the next cell to add to the Hcell list.

10. Add that cell to the Hcell list.

11. Check what is in the current Hcell list. Type:
    ```
    netlist report hcells
    ```

    The Query Server should respond with:
    ```
    a2311 s2311
    a1220 s1220
    a1240 s1240
    ```

12. Write the Hcell list to the file, my_hcells. Type:
    ```
    response file my_hcells
    netlist report hcells
    response direct
    ```

13. Using another terminal window, open my_hcells using any text editor to check the results.

    Next you are going to automatically generate a hcell file where each of the hcells in the file will give you a 5% or greater memory savings.

14. First clear the current Hcell list so you can start fresh. Type:
```
netlist clear hcells
```

15. Automatch Hcells by name. Type:
```
netlist automatch on
```

16. Also set cell matching by placement count. Type:
```
netlist placementmatch on
```

> **Note** By turning on automatch and placementmatch you are creating a starting point for the automatic Hcell file generation. These options match the layout and netlist cell names.

17. Set the evaluation threshold to 5%. Type:
```
netlist evaluation threshold 5
```

18. Generate the Hcell file. Type:
```
netlist select hcells
```

19. Send the results to the Hcell file. Type:
```
response file thold_5_hcells
netlist report hcells
response direct
```

20. Check what is in the query Server's Hcell file. Type:
```
netlist report hcells
```

21. The Query Server should respond with:
```
a2311 s2311
a1220 s1220
a1240 s1240
a1230 s1230
a1620 s1620
```

22. Using another terminal window, open thold_5_hcells using any text editor to check the results.

    If you have time you may want to continue experimenting with the Query Server.

23. When you are finished, exit the Query Server. Type:
    ```
    quit
    ```

Module 8
Troubleshooting
Shorts and Opens

Objectives

At the completion of this lecture and lab you should be able to:

- Identify simple shorts and opens in a report

- Find simple shorts and opens in a layout

- Correct short and open discrepancies in a layout

- Recognize Power and Ground discrepancies in a report

- Find the Power and Ground discrepancies in the layout

- Correct simple Power and Ground discrepancies in the layout

- Use LVS Isolate Shorts to trace a texted net

What are Shorts and Opens?

What are Shorts and Opens?

- ◆ **Short circuits:**
  - ● **Occur when nets that should be isolated are connected**
  - ● **Can lead to a difference between the number of nets:**
    # layout nets < # source nets
- ◆ **Open circuits:**
  - ● **Occur when connectivity is not maintained over the entire length of a layout net**
  - ● **Can lead to a difference between the number of nets:**
    # layout nets > # source nets

Nets 1 and 2 are shorted

NET 1

NET 2

Intended layout

NET 1

NET 2

Net 2 is open

NET 1

NET 2
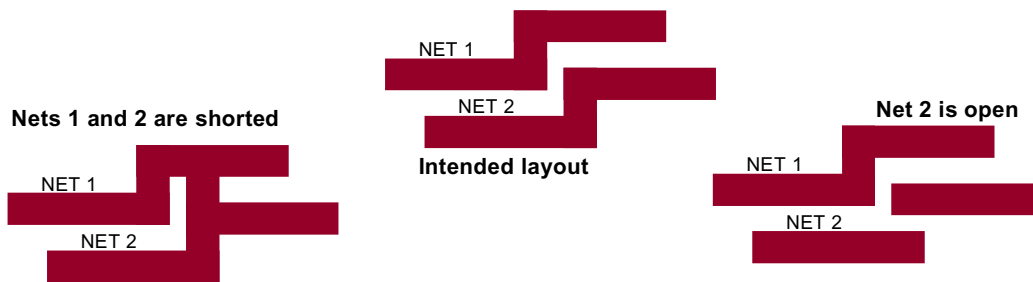
8-3 • Using Calibre: Troubleshooting Shorts and Opens
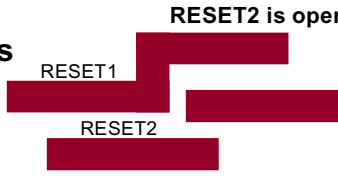
Copyright © 2004 Mentor Graphics Corporation
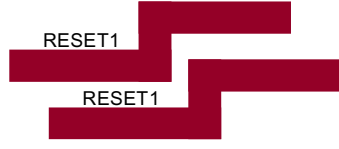
Notes:

What Causes Shorts and Opens?

RESET2 is open

♦ **Misplaced polygons**

RESET1

RESET2

♦ **Incorrect texting**

RESET1

RESET1

♦ **Improper use of VIRTUAL CONNECT NAME or VIRTUAL CONNECT COLON**

   VIRTUAL CONNECT NAME RESET?

   RESET1 and RESET2 are logically connected

RESET1

RESET2

♦ **Careless routing in a hierarchical environment**
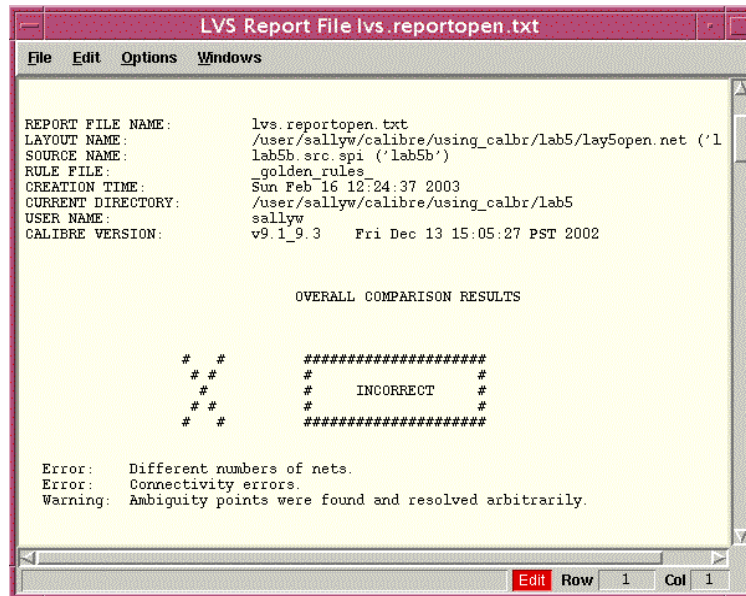
Cell 232

RESET1

Notes:

How to Identify Opens Using the LVS Report

Initial Error message warns about different number of nets

```
LVS Report File lvs.reportopen.txt

File   Edit   Options   Windows


REPORT FILE NAME:        lvs.reportopen.txt
LAYOUT NAME:             /user/sallyw/calibre/using_calbr/lab5/lay5open.net ('l
SOURCE NAME:             lab5b.src.spi ('lab5b')
RULE FILE:               _golden_rules_
CREATION TIME:           Sun Feb 16 12:24:37 2003
CURRENT DIRECTORY:       /user/sallyw/calibre/using_calbr/lab5
USER NAME:               sallyw
CALIBRE VERSION:         v9.1_9.3    Fri Dec 13 15:05:27 PST 2002


                         OVERALL COMPARISON RESULTS


         #   #           ####################
          # #            #                  #
           #             #      INCORRECT    #
          # #            #                  #
         #   #           ####################


    Error:    Different numbers of nets.
    Error:    Connectivity errors.
    Warning:  Ambiguity points were found and resolved arbitrarily.

                                                    Edit  Row   1   Col   1
```

8-5 • Using Calibre: Troubleshooting Shorts and Opens   Copyright © 2004 Mentor Graphics Corporation

Notes:
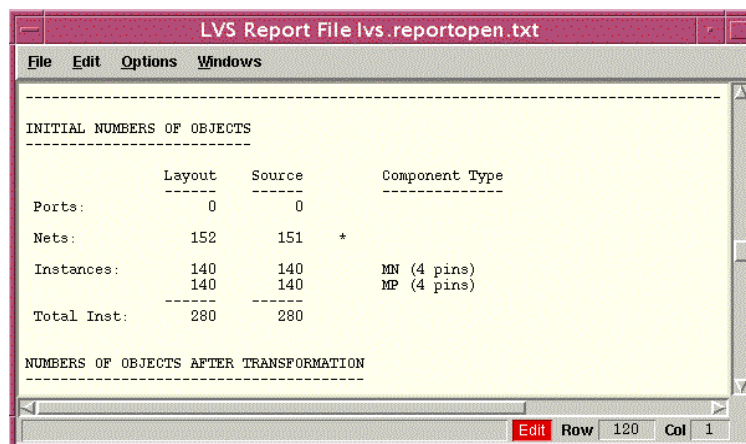
How to Identify Opens Using the LVS Report (Cont.)

How to Identify Opens Using the LVS Report (Cont.)

How do I tell if I should start looking for a short or an open?

- **Does the Source or Layout have more nets?**
- **Check the Initial number of Objects report**
- **# source nets < # layout nets, therefore most likely an open**
- **Calibre may have matched one source net to two layout nets**

```
LVS Report File lvs.reportopen.txt

File   Edit   Options   Windows

---------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
-------------------------

                 Layout    Source          Component Type
                 ------    ------          --------------
Ports:                0         0

Nets:               152       151    *

Instances:          140       140          MN (4 pins)
                    140       140          MP (4 pins)
                 ------    ------
Total Inst:         280       280


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                                                    Edit  Row  120  Col  1
```

Notes:

Tracking Opens Using RVE

Tracking Opens Using RVE

◆ **Display the discrepancy**

◆ **Nets 16 and 42 should be connected in the layout**

Notes:

Using Calibre with DESIGNrev
June 2004
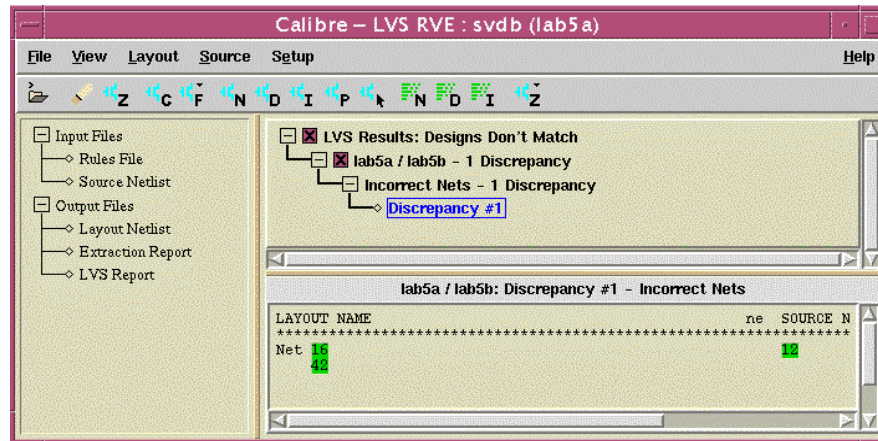
Tracking Opens Using RVE—Display Net in Layout

Tracking Opens Using RVE — Display Nets in Layout

- ♦ **Display Net 16 and Net 42 by clicking on them in RVE**
- ♦ **Nets 16 and 42 should be connected in the layout**

Net 16

Net 42

Break in the connectivity
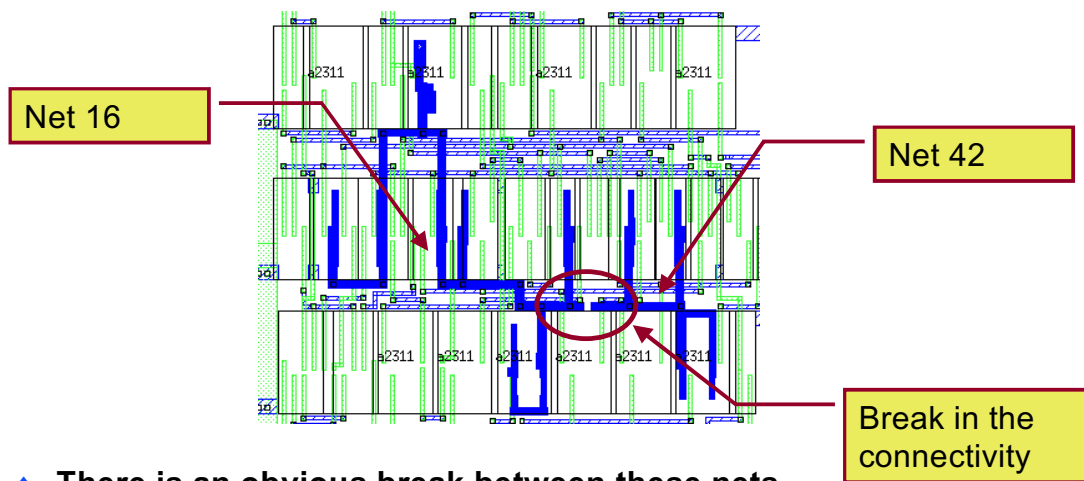
- ♦ **There is an obvious break between these nets**

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Notes:

Tracking Opens—Correct the Problem and Re-run LVS

Tracking Opens — Correct the Problem and Re-run LVS

- ◆ **Correct the layout**
- ◆ **Save the layout**
- ◆ **Re-run LVS**

File Viewer — /user/sallyw/calibre/using_calbr/lab5/lvs.report

File Edit Options Windows

```
                    ##                                          ##
                    ##            L V S   R E P O R T           ##
                    ##                                          ##
                    ################################################

REPORT FILE NAME:           lvs.report
LAYOUT NAME:                lay.net ('lab5a')
SOURCE NAME:                /user/sallyw/calibre/using_calbr/lab5/lab5a.src.spi ('
RULE FILE:                  _lab5_rules
CREATION TIME:              Fri Feb  7 09:16:33 2003
CURRENT DIRECTORY:          /user/sallyw/calibre/using_calbr/lab5
USER NAME:                  sallyw
CALIBRE VERSION:            v9.1_9.4    Thu Dec 19 14:04:47 PST 2002


                            OVERALL COMPARISON RESULTS


                #           ##################
               #   #        #                #           T   T
              #     #       #     CORRECT     #          |   |
             #  #   #       #                #           \   /
                #           ##################            \_/
```

Edit Row 1   Col 1

Notes:

Tracking Opens Summary

Tracking Opens Summary

- ◆ **Look at LVS Report first**
  - ● **Net number discrepancy**
  - ● **# nets in Source < # nets in Layout**
  - ● **One Source net matched to two Layout nets**
- ◆ **Use RVE**
  - ● **Display first discrepancy**
  - ● **Display source netlist**
  - ● **Display layout netlist**
  - ● **Highlight net information from discrepancies (one at a time)**
  - ● **Check highlighted nets in layout for obvious problems**
- ◆ **Correct the problem**
- ◆ **Re-run LVS to check the correction**

Notes:

Identifying Shorts Using the LVS Report

Identifying Shorts Using the LVS Report

♦ **Initial Error message warns about different number of nets**

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Notes:

Using Calibre with DESIGNrev
June 2004
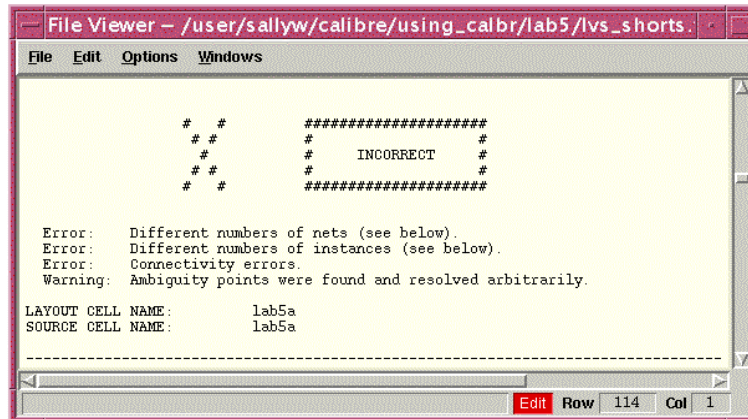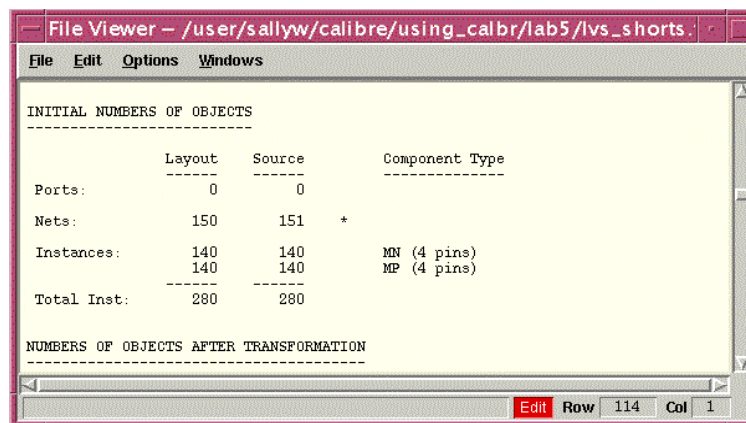
Identifying Shorts Using the LVS Report (Cont.)

Identifying Shorts Using the LVS Report (Cont.)

- ◆ **How do I tell if I should start looking for a short or an open?**
  - ● **Does the Source or Layout have more nets?**
  - ● **Check the Initial number of Objects report**
  - ● **# source nets > # layout nets therefore most likely a short**
  - ● **Calibre matches two Source nets to one Layout net**

```
File Viewer — /user/sallyw/calibre/using_calbr/lab5/lvs_shorts.

File  Edit  Options  Windows

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source        Component Type
                ------    ------        --------------
Ports:              0         0

Nets:             150       151    *

Instances:        140       140        MN (4 pins)
                  140       140        MP (4 pins)
                ------    ------
Total Inst:       280       280


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                                            Edit  Row  114   Col  1
```

Notes:

Tracking Shorts Using RVE

Tracking Shorts Using RVE

♦ **Display the first discrepancy**
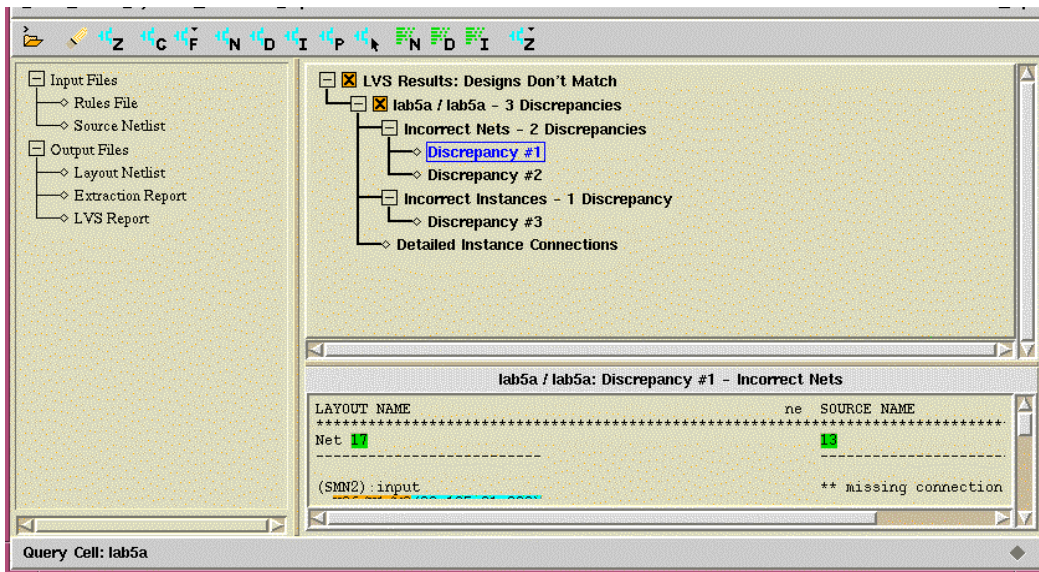
Copyright © 2004 Mentor Graphics Corporation
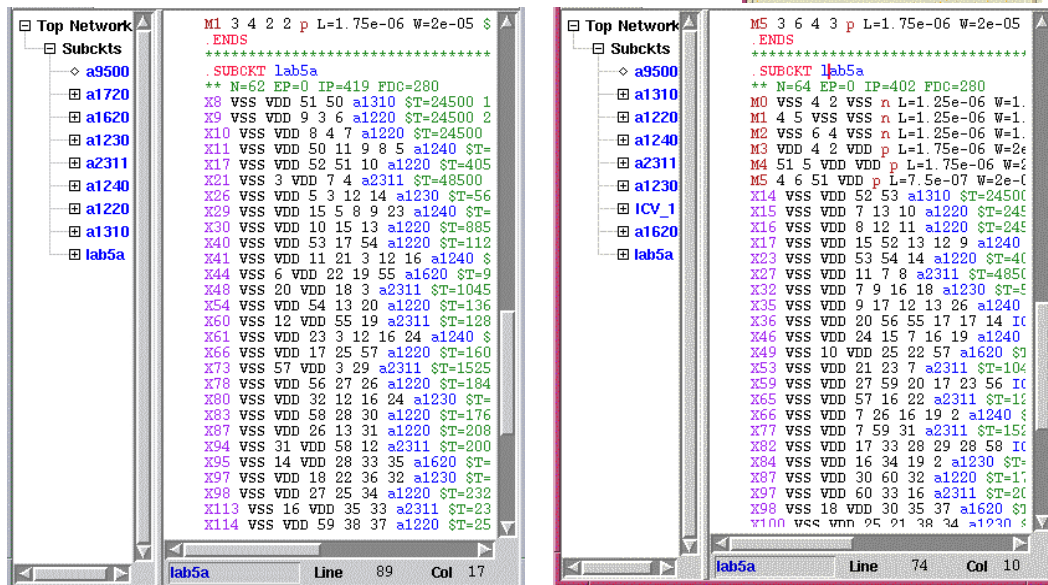
Notes:

Tracking Shorts Using RVE (Cont.)

Notes:

Tracking Shorts Using RVE (Cont.)

- ♦ **Highlight nets from Discrepancy report as a starting point**
- ♦ **Net 13 in source and Net 17 in layout**

Layout net 17 corresponds to source net 13 but connects to more pins

8-15 • Using Calibre: Troubleshooting Shorts and Opens   Copyright © 2004 Mentor Graphics Corporation

Notes:

Using Calibre with DESIGNrev
                                                                                     June 2004

Tracking Shorts to the Layout Viewer

Tracking Shorts to the Layout Viewer

- ◆ **Net 17 in layout highlights**
- ◆ **This is a large net**
- ◆ **Will need more information to narrow down the short location**

Copyright © 2004 Mentor Graphics Corporation
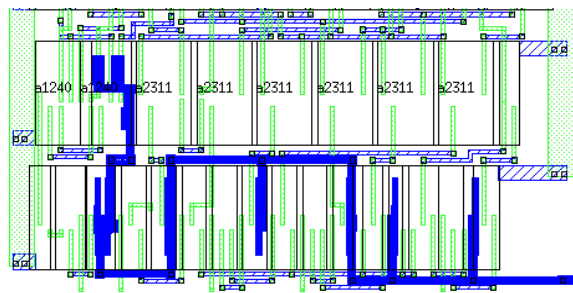
Notes:

Tracking Shorts—Display Next Discrepancy

Tracking Shorts — Display Next Discrepancy

From RVE display next discrepancy

Notes:

Using Calibre with DESIGNrev
June 2004
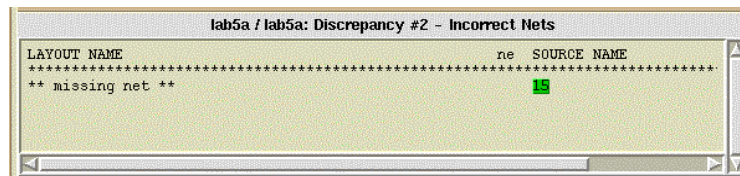
Tracking Shorts—Highlight Next Discrepancy in Netlist

Tracking Shorts — Highlight Next Discrepancy in Netlist

♦ **Highlight Net 15 in the source netlist**
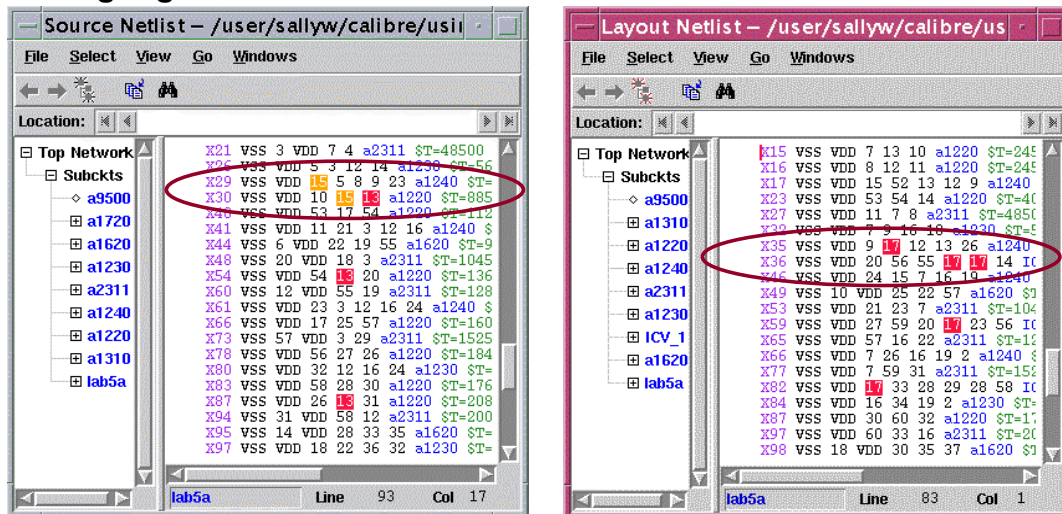
♦ **Looks like short happened in X36 in Layout (x30 in Source)**

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Notes:

Tracking Shorts—Highlight the Instance

Tracking Shorts — Highlight the Instance

- **Click on x36 in the layout netlist to highlight the instance with the short**
- **One of the highlighted paths into x36 is shorted**

x36

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Notes:

Using Calibre with DESIGNrev
June 2004
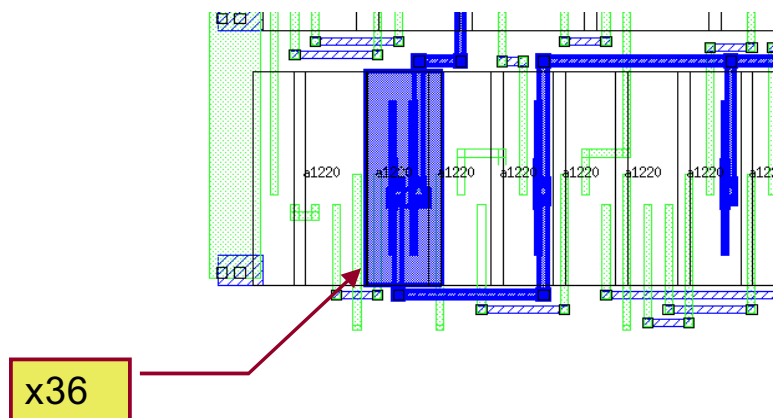
Tracking Shorts—Which Path

Tracking Shorts — Which Path

- ◆ **Look at source netlist**
  - ● **Net 15 is the shorted net**
  - ● **Net 15 goes from x29 to x30**
  - ● **x29 is an a1240**
- ◆ **Look at layout netlist**
  - ● **Net 17 in x36 goes to x35**
  - ● **x35 matches source x29**
  - ● **This connection is the short**
- ◆ **Highlight x35 to isolate the shorted path**

8-20 • Using Calibre: Troubleshooting Shorts and Opens
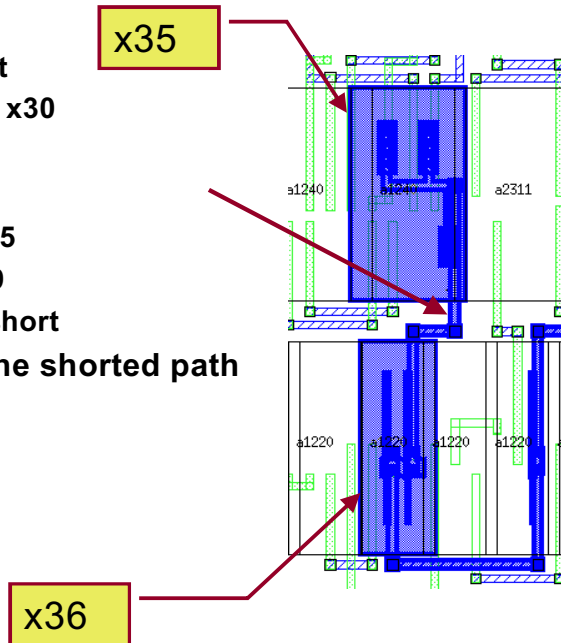
Notes:

Tracking Shorts—Closer View of the Layout

Tracking Shorts—Closer View of the Layout

♦ **Remove the Highlights**

♦ **Zoom in on the cell to find the problem**

From x35

x36

a1220   a1220

Main Net 17

Most likely cause
of the short

Notes:

Using Calibre with DESIGNrev
June 2004
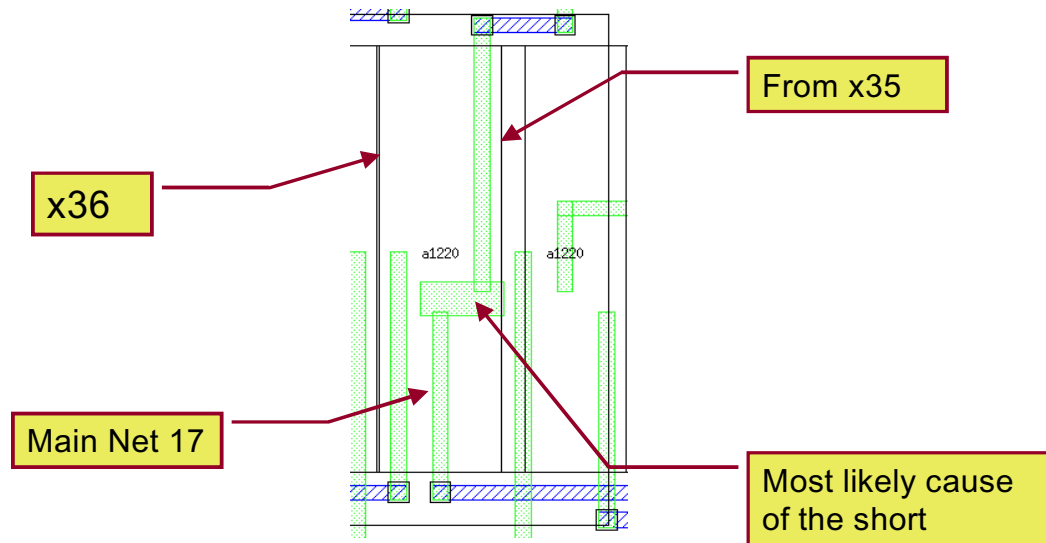
Tracking Shorts—Double-Check Layout

Tracking Shorts — Double-Check Layout

♦ **Display the lower context**

♦ **Does your "suspected" polygon still look like the problem?**

From x35

Main Net 17

Most likely cause of the short

Notes:

Tracking Shorts—Correct the Problem and Re-Run LVS

Tracking Shorts — Correct the Problem and Re-Run LVS
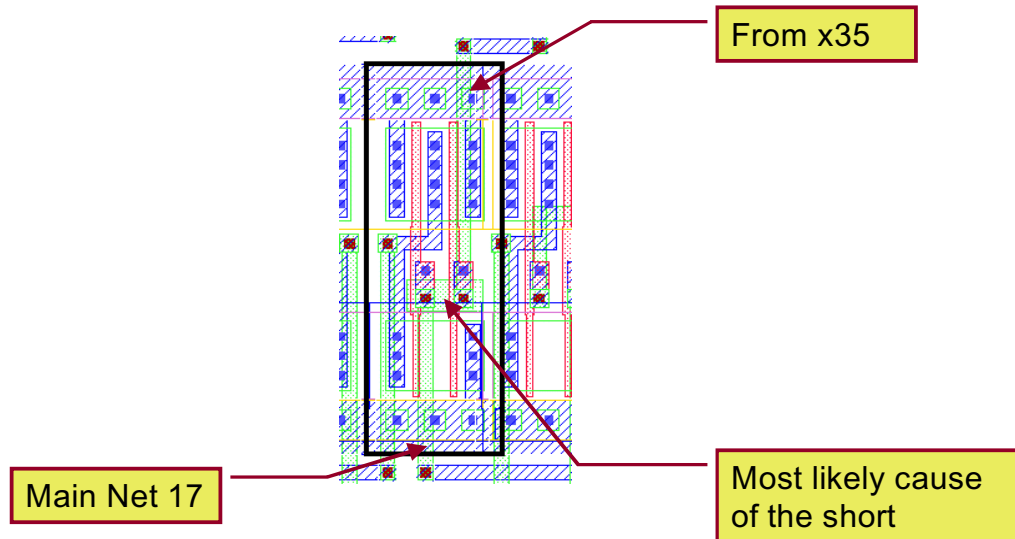
- ♦ **Correct the problem**
- ♦ **Save the GDSII**
- ♦ **Re-run LVS**

```
File Viewer — /user/sallyw/calibre/using_calbr/lab5/lvs.report

File  Edit  Options  Windows

                    ##                                      ##
                    ##           L V S   R E P O R T        ##
                    ##                                      ##
                    #################################################


REPORT FILE NAME:       lvs.report
LAYOUT NAME:            lay.net ('lab5a')
SOURCE NAME:            /user/sallyw/calibre/using_calbr/lab5/lab5a.src.spi ('
RULE FILE:              _lab5_rules_
CREATION TIME:          Fri Feb  7 09:16:33 2003
CURRENT DIRECTORY:      /user/sallyw/calibre/using_calbr/lab5
USER NAME:              sallyw
CALIBRE VERSION:        v9.1_9.4    Thu Dec 19 14:04:47 PST 2002


                        OVERALL COMPARISON RESULTS


              #         ##################          ‾   ‾
            #   #       #                #          *   *
          #   #         #     CORRECT    #           |
          # #           #                #          \_/
            #           ##################
```

Edit Row 1   Col 1

Notes:

Using Calibre with DESIGNrev
June 2004

Tracking Shorts Summary

Tracking Shorts Summary

- ♦ **Look at LVS Report first**
  - ● **Net number discrepancy**
  - ● **# nets in Source > # nets in Layout**
  - ● **Two Source nets matched to one Layout net**
- ♦ **Use RVE**
  - ● **Display first discrepancy**
  - ● **Display source netlist**
  - ● **Display layout netlist**
  - ● **Highlight net information from discrepancies (one at a time)**
  - ● **Check highlighted nets in layout for obvious problems**
  - ● **Look for patterns in the netlist to narrow down the short location**
- ♦ **Correct the problem**
- ♦ **Re-run LVS to check the correction**

Notes:

What Happens if there are Both Shorts and Opens?

What Happens if there are Both Shorts and Opens?

- ◆ **Problem not as obvious**
- ◆ **Reported as Connectivity errors**

```
┌─────────────────────────────────────────────────────────────────────┐
│ ─                    LVS Report File lvs.report2                    □ │
├─────────────────────────────────────────────────────────────────────┤
│ File   Edit   Options   Windows                                       │
├─────────────────────────────────────────────────────────────────────┤
│ RULE FILE:              _golden_rules_                              ▲ │
│ CREATION TIME:          Sun Feb 16 13:00:24 2003                    ▒ │
│ CURRENT DIRECTORY:      /user/sallyw/calibre/using_calbr/lab5       ▒ │
│ USER NAME:              sallyw                                         │
│ CALIBRE VERSION:        v9.1_9.3    Fri Dec 13 15:05:27 PST 2002       │
│                                                                       │
│                                                                       │
│                    OVERALL COMPARISON RESULTS                         │
│                                                                       │
│                                                                       │
│            #   #       ####################                           │
│             # #        #                  #                           │
│              #         #     INCORRECT    #                           │
│             # #        #                  #                           │
│            #   #       ####################                           │
│                                                                       │
│   Error:    Different numbers of instances.                           │
│   Error:    Connectivity errors.                                      │
│   Warning:  Ambiguity points were found and resolved arbitrarily.     │
│                                                                       │
│                                                                       │
│ *******************************************************************    │
│                       CELL   SUMMARY                               ▼ │
│ ◄                                                              ►       │
│                                          ┌────┬─────┬───┬─────┬────┐  │
│                                          │Edit│ Row │ 1 │ Col │ 1  │  │
└─────────────────────────────────────────────────────────────────────┘
```

Notes:

RVE with Both Shorts and Opens

RVE with Both Shorts and Opens

♦ **Need to work through each discrepancy**
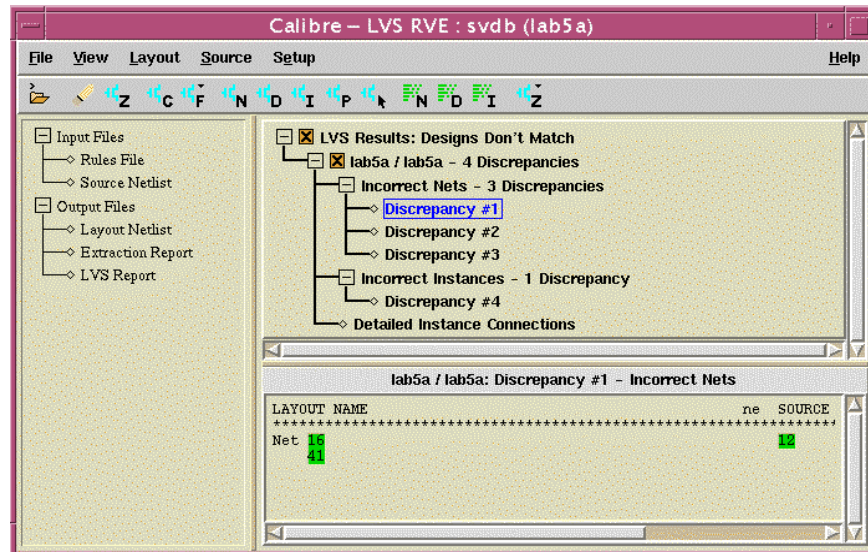
Notes:

The Special Case of Power and Ground Shorts and Opens

The Special Case of Power and Ground Shorts and Opens

- ◆ **Use slightly different techniques**

- ◆ **Power and Ground connections help to define devices, so many instances may be missing**

- ◆ **Often many, many errors for a single problem**

Notes:

Using Calibre with DESIGNrev
June 2004

What is Special about Power and Ground Nets?

What is Special about Power and Ground Nets?

♦ **Usually the largest nets in the design**

♦ **Connect to all levels of the hierarchy**

♦ **May intentionally have several names on the same net**

♦ **Can short between cells at different levels in the hierarchy**

Low-level cell **B** has already been verified OK.

Later, when top-level metal is routed, a short occurs between VDD in top-level cell **A** and VSS in low-level cell **B**.
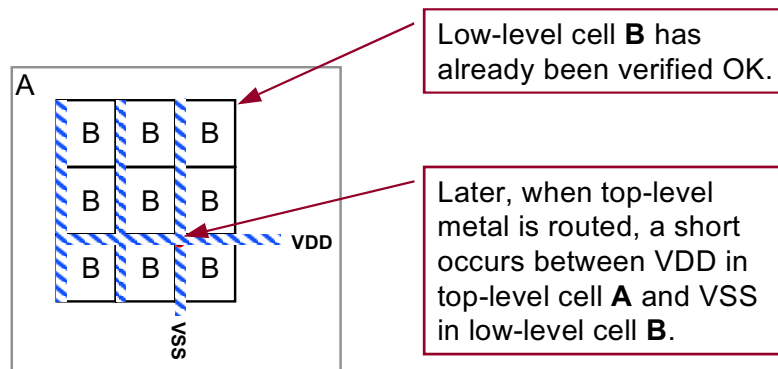
Notes:

How to Identify Power and Ground Net Problems in the LVS Report

How to Identify Power and Ground Net Problems in the LVS Report

♦ **Clues from the LVS report for a short:**

- **Overall Comparison Results states: "Power or ground net missing in hcell"**

- **All Hcells reporting "not compared" or "incorrect"**

♦ **Clues for an open:**

- **Huge number of discrepancies**

- **One power or ground net in the source matches to two or more nets in the layout**

Notes:

Resolving Power and Ground Net Discrepancies

Resolving Power and Ground Net Discrepancies

- ♦ **Give this task high priority**
  - ● **Problems with major nets may generate false discrepancies on the smaller nets**
  - ● **May be able to fix many problems by fixing a simple power/ground problem**
- ♦ **Verify large designs hierarchically from the bottom up**
  - ● **Verify each individual cell first**
  - ● **Then verify cells higher in the hierarchy**
- ♦ **Use power and ground net Rule file specifications**
- ♦ **Use LVS ISOLATE SHORTS method to highlight shorts as DRC violations (covered later in this lecture) or debug like a regular short**

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Notes:

Using Special Tools Targeting Power and Ground Nets

Using Special Tools Targeting Power and Ground Nets

LVS ABORT ON SUPPLY ERROR

- **Stops all LVS comparisons if a problem is encountered with either the power or ground**

- **Quick check for a supply problem**

Notes:

Using Calibre with DESIGNrev
June 2004
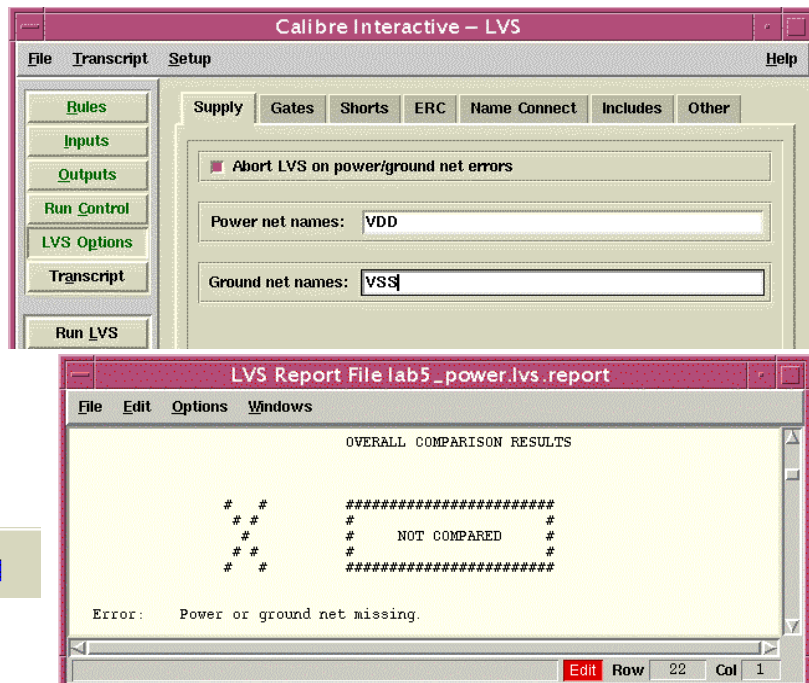
Identifying Power/Ground Texting Problems

Identifying Power/Ground Texting Problems

- ◆ **Incorrectly named power/ground nets may cause one of these results:**

    - ● **LVS reports "Badly formed power/ground net name" error if the name violates the syntax rules**

    - ● **LVS reports "Contradictory power/ground net name" error if the same name is used for both a power and a ground net**

    - ● **LVS aborts with the OVER ALL COMPARISION RESULTS listed as " NOT COMPARED"**
      Overridden by LVS ABORT ON SUPPLY ERROR no

Notes:

June 2004

8-31

Example: Simple VDD to VSS Short

Example: Simple VDD to VSS Short

♦ **The next set of slides will walk you through finding a VDD to VSS short**

♦ **Run LVS with LVS ABORT ON SUPPLY ERROR selected**

```
┌─────────────────────────────────────────────────────────────┐
│ ▬         LVS Report File lab5_power.lvs.report        ⌐  □  │
├─────────────────────────────────────────────────────────────┤
│ File  Edit  Options  Windows                                 │
├─────────────────────────────────────────────────────────────┤
│                   OVERALL COMPARISON RESULTS            ▲     │
│                                                        ▒     │
│                                                        ▒     │
│         #   #        #######################                 │
│          # #         #                     #                 │
│           #          #      NOT COMPARED    #                │
│          # #         #                     #                 │
│         #   #        #######################                 │
│                                                              │
│   Error:    Power or ground net missing.                     │
│                                                        ▼     │
│  ◄                                                  ►        │
├─────────────────────────────────────────────────────────────┤
│                                    [Edit] Row  22  Col  1    │
└─────────────────────────────────────────────────────────────┘
```
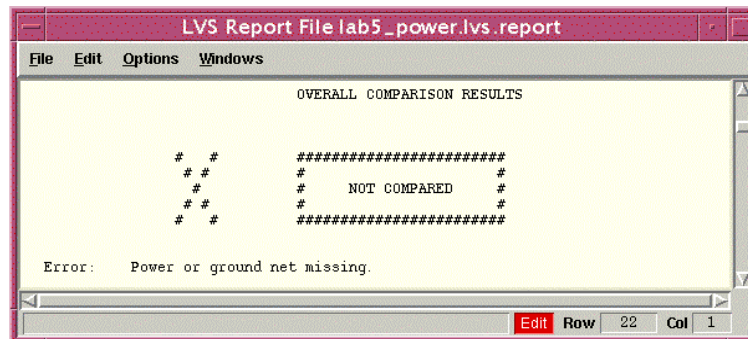
♦ **You know you have a supply problem**

Notes:

Using Calibre with DESIGNrev
June 2004

Run LVS Without ABORT

Run LVS Without ABORT

- ◆ **Run LVS again**
  - ● **With LVS ABORT ON SUPPLY ERROR unselected**
- ◆ **Obvious short in the layout**
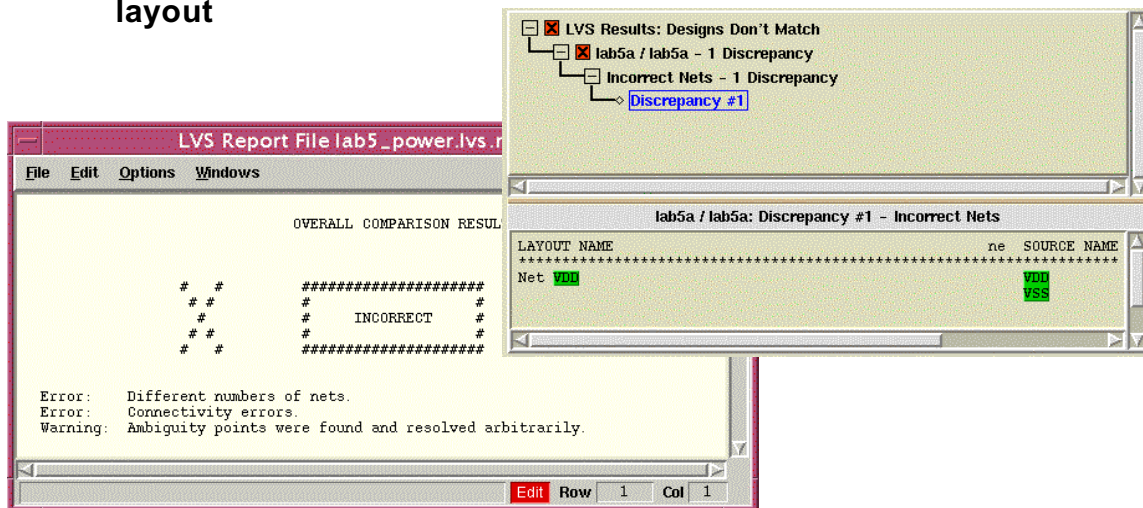
Notes:

Highlight the VDD Net in the Layout Editor

Highlight the VDD Net in the Layout Editor

- ◆ **Too many highlights to find the problem**
- ◆ **Need a way to narrow down the short location**

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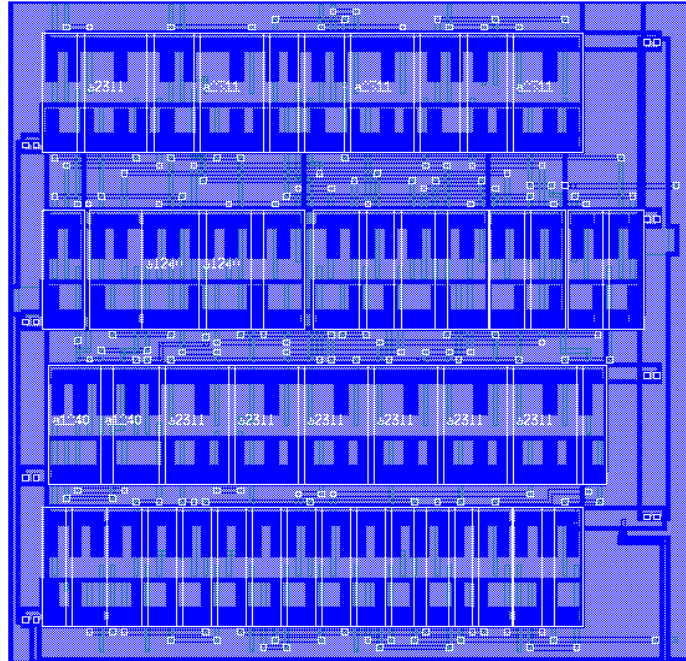
Notes:

What is LVS ISOLATE SHORTS?

What is LVS ISOLATE SHORTS?

♦ **Finds the shortest path between two texted nets**

♦ **Outputs a DRC-like database of the polygons making up the shortest path**

♦ **Although you access this feature from LVS, it is really a DRC-type feature/function.**

♦ **Use this feature with any texted net
(Not limited to power/ground problems)**

Notes:

Set Up LVS Isolate Shorts

Set Up LVS ISOLATE SHORTS

Shorts Tab

LVS Options

Run short isolation

Just look at VDD and VSS

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Notes:

Using Calibre with DESIGNrev
June 2004
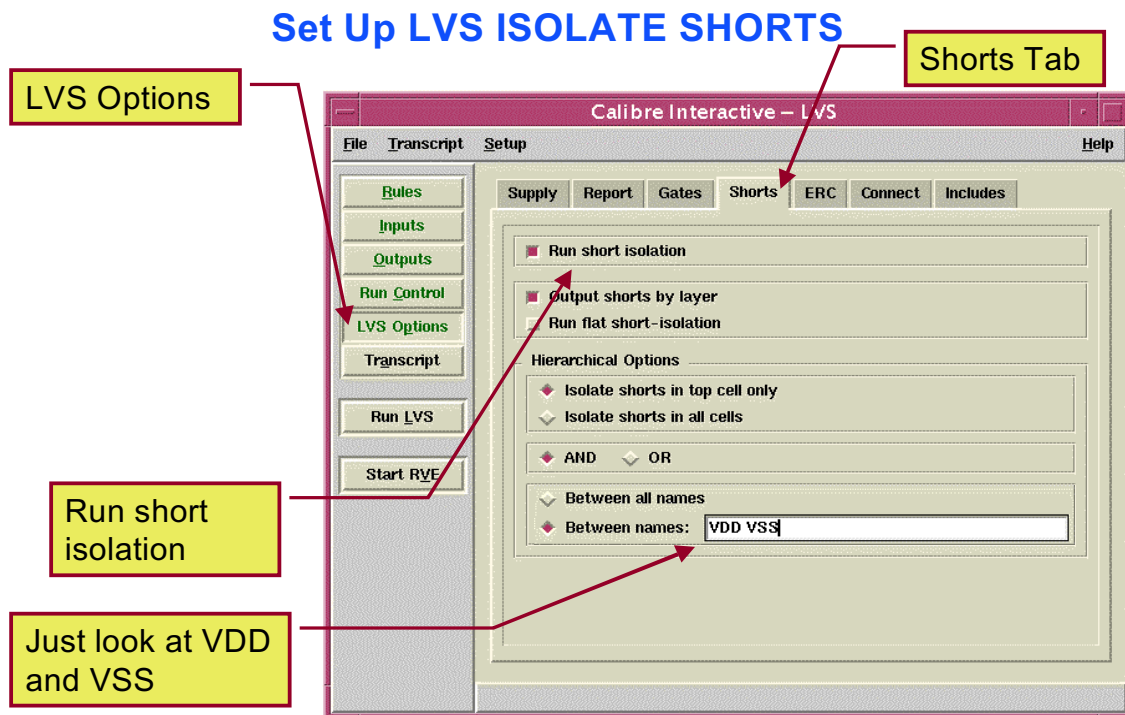
Run LVS with Short Isolation

Run LVS with Short Isolation

- ♦ **Run LVS again**
- ♦ **New Output File in RVE: Shorts Database**
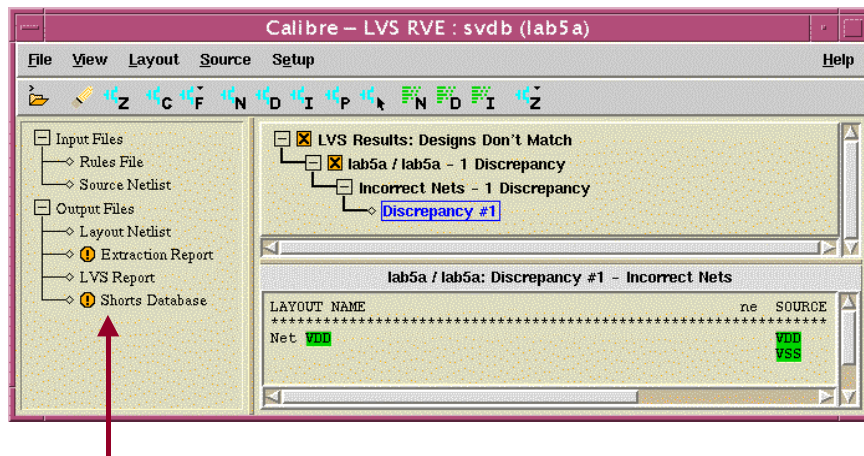
- ♦ **Click on the Shorts Database to launch DRC RVE**

Notes:

Isolate Shorts Using DRC RVE

Isolate Shorts Using DRC RVE

♦ **Each error is a polygon**

♦ **Set "Z" for no view change**

♦ **Highlighting the error steps through the short**

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Notes:

Using Calibre with DESIGNrev
June 2004
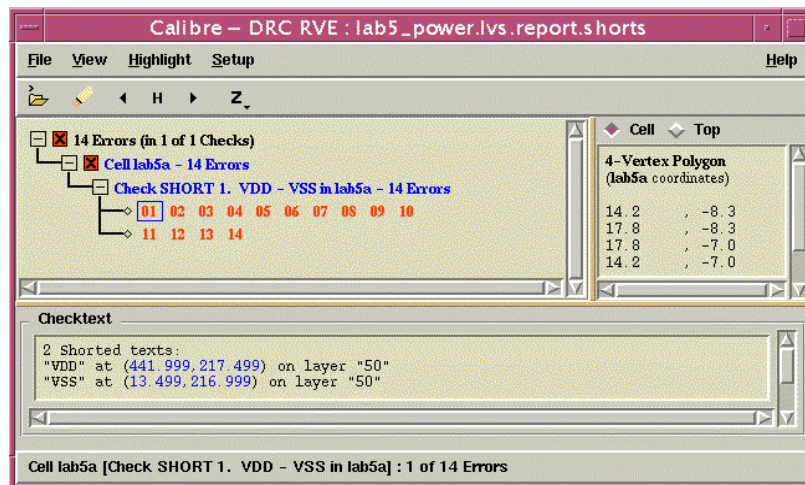
Isolating the Short in the Layout—All Segments Highlighted

Isolating the Short in the Layout—All Segments Highlighted
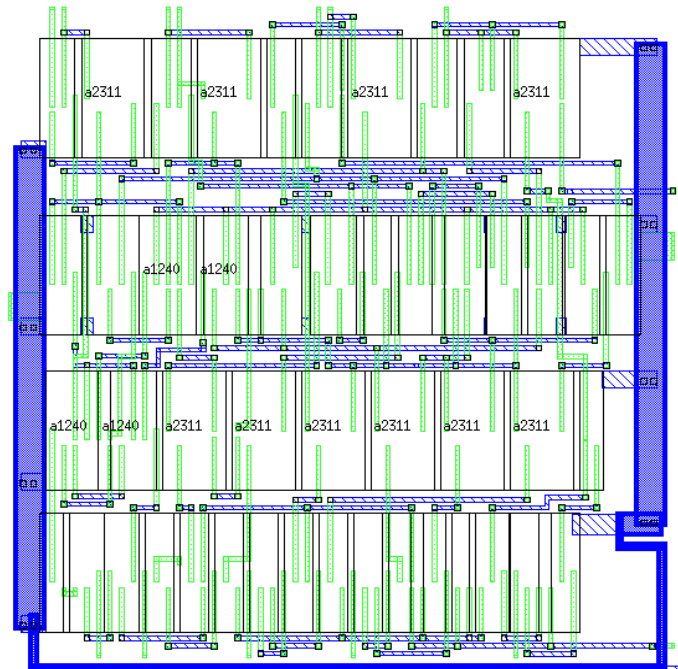
Notes:

Segment Causing the Short

Segment Causing the Short
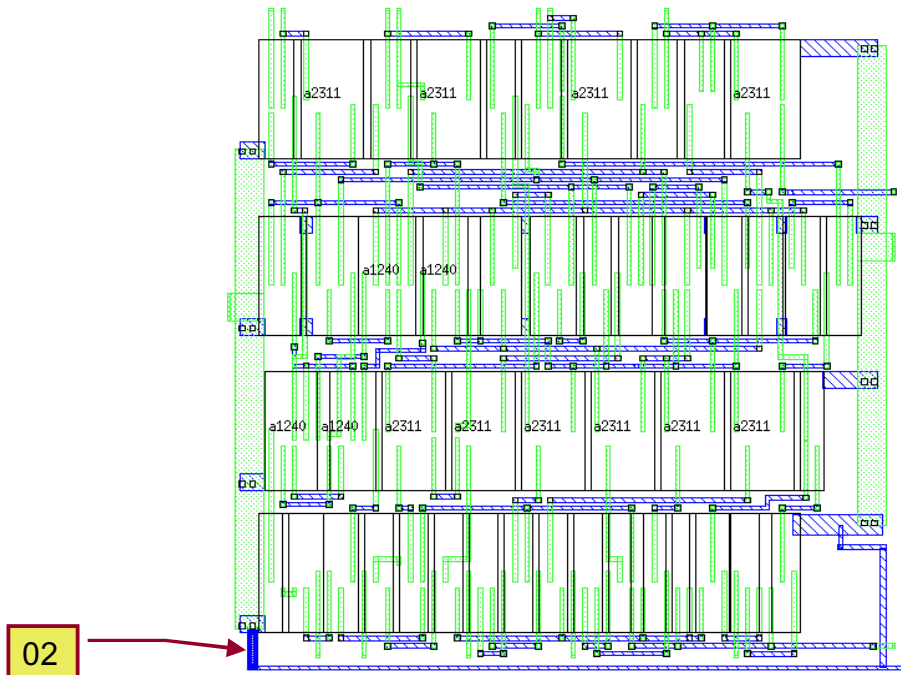
Notes:

Troubleshooting Supply Problems Summary

Troubleshooting Supply Problems Summary

♦ **Start with** LVS ABORT ON SUPPLY ERROR yes **to flag supply problems**

♦ **Run LVS again with** LVS ABORT ON SUPPLY ERROR no **to read LVS report**

♦ **Launch RVE and look for obvious shorts or opens**

♦ **In case of shorts, run LVS again and generate the isolate shorts database**

♦ **Use DRC RVE to step through shorted net to find the problem**

Notes:

Lab Information

Lab Information

In this lab you will:

♦ **Find a simple short**

♦ **Find a simple open**

♦ **Isolate problems in a layout with both shorts and opens**

♦ **Find a supply net problem**

Notes:

Lab: Troubleshooting Shorts and Opens

In this lab you will learn how to troubleshoot shorts and opens. This will include the simple case of "regular" nets and the more complex case of supply shorts.

List of Exercises

Exercise 8-1: Troubleshooting an Open

Exercise 8-2: Troubleshooting a Short

Exercise 8-3: Troubleshooting a Circuit with both Shorts and Opens

Exercise 8-4: Troubleshooting a Power to Ground Short

Exercise 8-1: Troubleshooting an Open

In this lab, you will learn how to find and fix the simplest case of an open circuit on a non-power supply net.

1. Change to the lab8 directory.

2. List the files in the directory.

   You should see at a minimum the following 12 files:

cell_file	lab8_source.spi	lab8c.gds
golden_rules	lab8_supply_rules	lab8d.gds
golden_rules_supply	lab8a.gds	layer_props.txt
lab8_rules	lab8b.gds	

   If any of these files are missing, please double check that you are in the correct directory, and then notify your instructor.

3. Launch DESIGNrev.

4. Open the GDSII file lab8a.gds.

5. Load the layer properties file, layer_props.txt.
   (**Menu: Layer > Load Layer Properties**)

6. Launch Calibre Interactive LVS on cell lab8.

7. Choose to create a new runset.

8. Enter the following **Inputs [Layout]** data:

Hierarchical, Flat, or Calibre CB	Hierarchical
Layout vs. Netlist, Netlist vs. Netlist, or Netlist Extraction	Layout vs. Netlist
Layout Files:	lab8a.gds
Import layout database from layout viewer	Unselected
Primary Cell	lab8
Layout Netlist:	lab8a_layout.net

9. Enter the following **Input [Netlist]** data:

Netlist Files:	lab8_source.spi
Import netlist from schematic viewer	Unselected
Primary Cell:	lab8

10. Enter the following **Input [HCells]** data:

Match cells by name (automatch):	Selected
Use H-Cells list from file:	Selected
[filename]	cell_file

11. Enter the following **Rules** data:

Calibre-LVS Rules File:	lab8_rules
Calibre-LVS Run Directory:	.

12. Enter the following **Outputs [Report/SVDB]** data:

LVS Report File:	lab8_lvs.report
View Report after LVS finishes:	Selected
Create SVDB Database:	Selected
Start RVE after LVS finishes:	Selected
Generate data for xCalibre:	Unselected
Generate Calibre Connectivity Interface data:	Unselected
SVDB Directory:	svdb

13. Run LVS.

What are your results?

_____

Looking at the LVS Report, what kind of errors do you have?

_____

_____

14. Close the LVS Report.

From RVE, what cell has the problem?

_____

What is the discrepancy?

_____

Which has more nets the source or the layout?

_____

Therefore you suspect you have a (open or short)?

_____

15. Display the source and layout netlists.

16. Rearrange your windows so you can see RVE, the two netlists, and DESIGNrev.

17. In the DESIGNrev window, display the cell with the discrepancy (a1220).

18. In RVE, select **Z** (Set Highlight View Options) **> No View Change** from the Toolbar.

19. Highlight the two layout nets.

The layout should look similar to below.
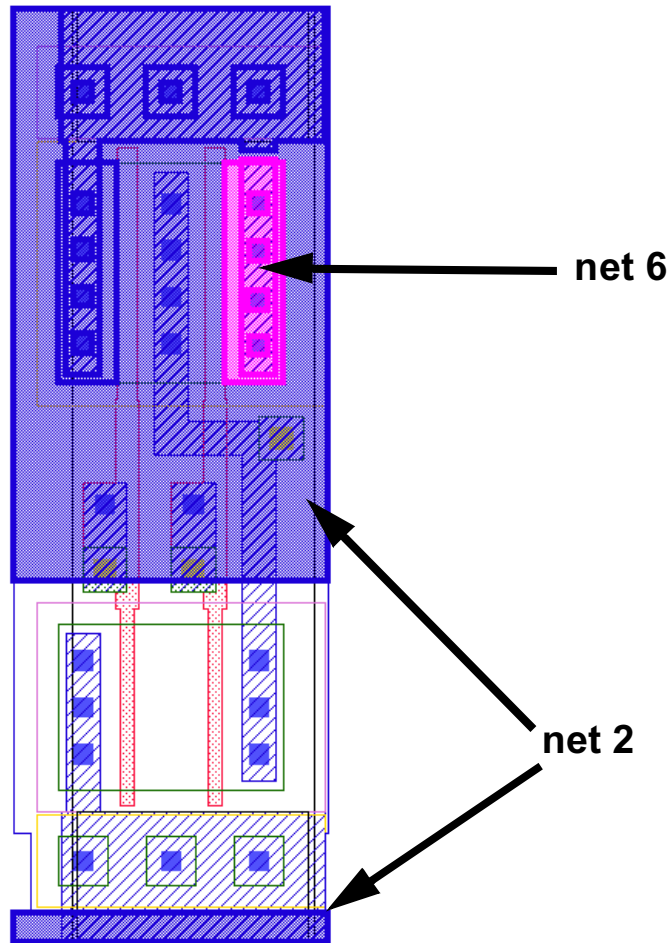
The Source Netlist

The Layout Netlist

```
****************************************
.SUBCKT a1220 1 2 3 4 5
** N=8 EP=5 IP=0 FDC=4
M0 8 3 1 1 n L=1.25e-06 W=1.5e-05 $X=5375 $Y=14000
M1 4 5 8 1 n L=1.25e-06 W=1.5e-05 $X=13375 $Y=14000
M2 4 3 2 2 p L=1.75e-06 W=2e-05 $X=5125 $Y=51000
M3 5 5 4 2 p L=1.75e-06 W=2e-05 $X=13125 $Y=51000
.ENDS
****************************************
```

The nets involved include the power, so much of the layout is highlighted.

20. Look at the netlists to narrow down the solution.

    Which of the two layout nets have the fewest occurrences?

    _____

21. Erase all the highlights.

22. Highlight just net 6.
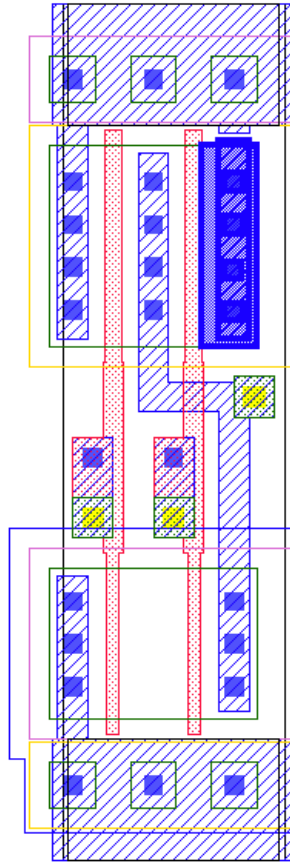
This narrows down the problem.

Can you see the problem?
(Hint: This piece of metal1 would flunk a DRC check.)

_____

23. **OPTIONAL**: Correct the problem in the layout and run LVS again to check your corrections. (Make sure you load the corrected design!)

24. When you are ready to go to the next exercise, close all Calibre windows *except* the Calibre Interactive LVS and DESIGNrev windows.

Exercise 8-2: Troubleshooting a Short

In this lab you will learn how to identify a simple short and find the problem in the layout.

1. In DESIGNrev, open GDSII file, lab8b.gds.

2. Load the layer properties file, layer_props.txt.
    (**Menu: Layer > Load Layer Properties**)

3. In Calibre Interactive LVS, change the following **Inputs [Layout]** data:

    Layout Files: lab8b.gds

    Layout Netlist: lab8b_layout.net

4. Run LVS.

    What are your overall results?

    _____

    Looking at the LVS Report, what kind of errors do you have?

    _____

    _____

    _____

5. Scroll down in the LVS Report until you find the first cell that is incorrect.

    What cell is it?

    _____

How many Ports in the Layout / Source?

Layout: _____

Source: _____

How many Nets in the Layout / Source?

Layout: _____

Source: _____

Which has more nets the source or the layout?

_____

Therefore you suspect you have a (open or short)?

_____

6. Find the next cell that is incorrect.

What cell is it?

_____

What is the problem?

_____

Does it appear to have shorts or opens?

_____

7. Close the LVS Report window.

It is usually easier to try to correct errors in the lower level cells before tackling the errors in the upper level cells. Often correcting the errors at the lower level will automatically fix the upper level errors. Therefore you will start with the lower level cell.

8. Use RVE to display the source and layout netlists.

9. Display cell a1220 in DESIGNrev.

10. Using RVE, highlight the discrepancy.

The discrepancy in the layout:
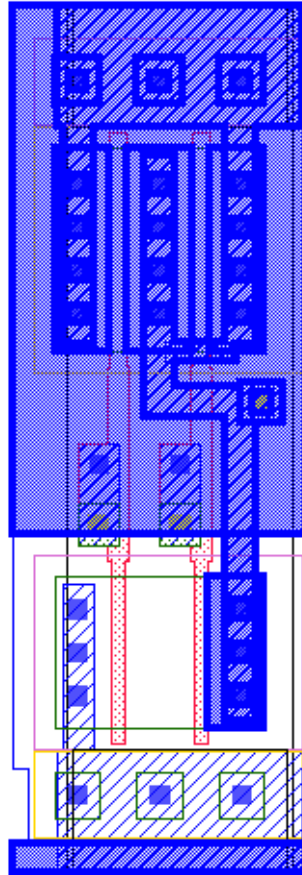
Source Netlist

Layout Netlist

```
.SUBCKT a1220 1 2 3 4
** N=6 EP=4 IP=0 FDC=4
M0 6 3 1 1 n L=1.25e-06 W=1.5e-05 $X=5375 $Y=14000
M1 2 4 6 1 n L=1.25e-06 W=1.5e-05 $X=13375 $Y=14000
M2 2 3 2 2 p L=1.75e-06 W=2e-05 $X=5125 $Y=51000
M3 2 4 2 2 p L=1.75e-06 W=2e-05 $X=13125 $Y=51000
.ENDS
```

Again there is a fairly large area involved, so you will need to do a little detective work.

11. Look carefully at the netlists.

There is a major different between the two netlists, see if you can find it.

How many ports are in each subcircuit?

a1220: _____

s1220: _____

Somewhere in the layout you lost a port. There should be the two power ports and three "regular" ports.

Useful Information: Correct pin layout for S1220 and A1220.

S1220   A1220
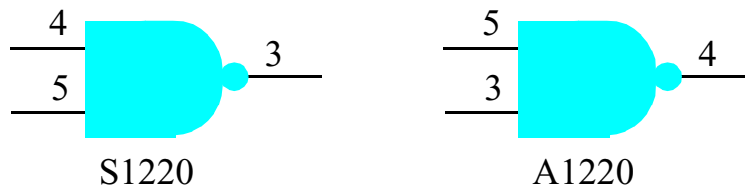
Additional Useful Information:
Source NMOS/PMOS pin order is: D G S B. (Drains and sources are "swappable!)

One more help: S1220 NAND Source Schematic.
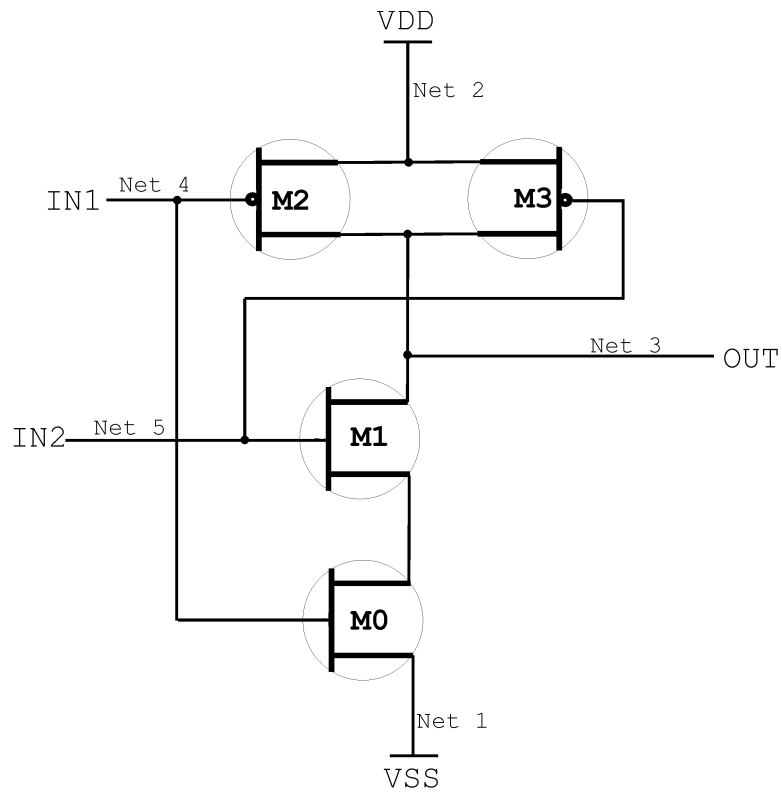
You may want to draw the connections from the A1220 layout netlist below:
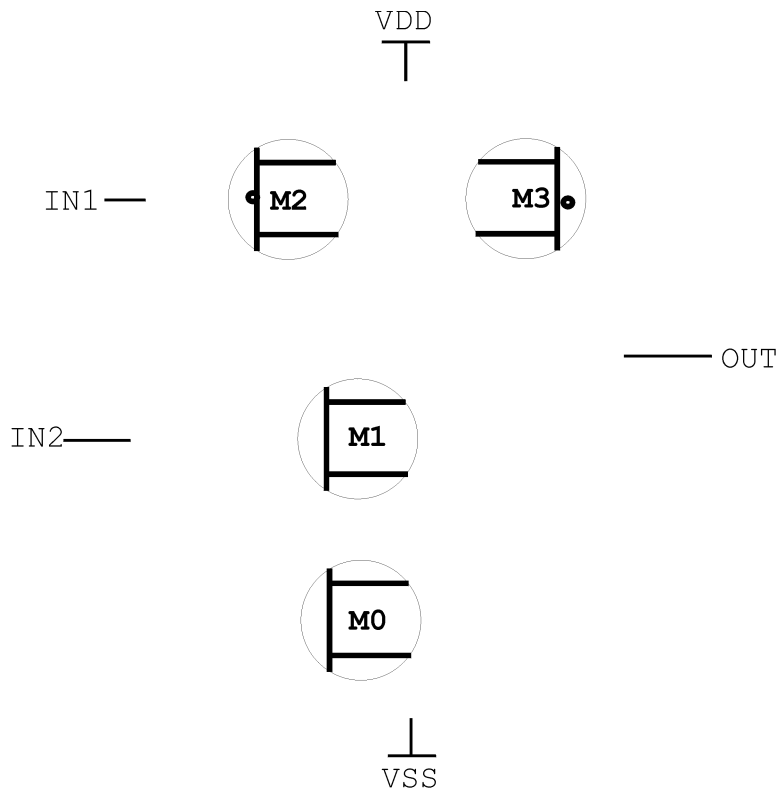
12. Look at the highlights again.

A power bus is running over a port.
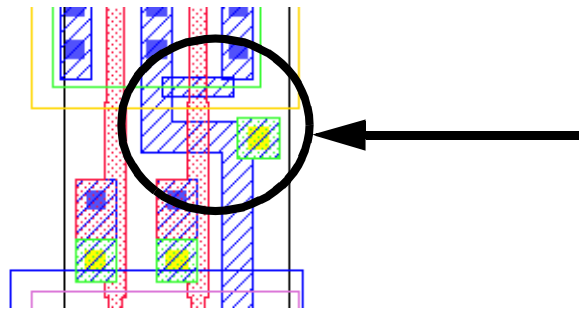
Where is that port supposed to connect?
(Use the Source netlist to find the answer.)

_____

A callout of the cell is illustrated below.
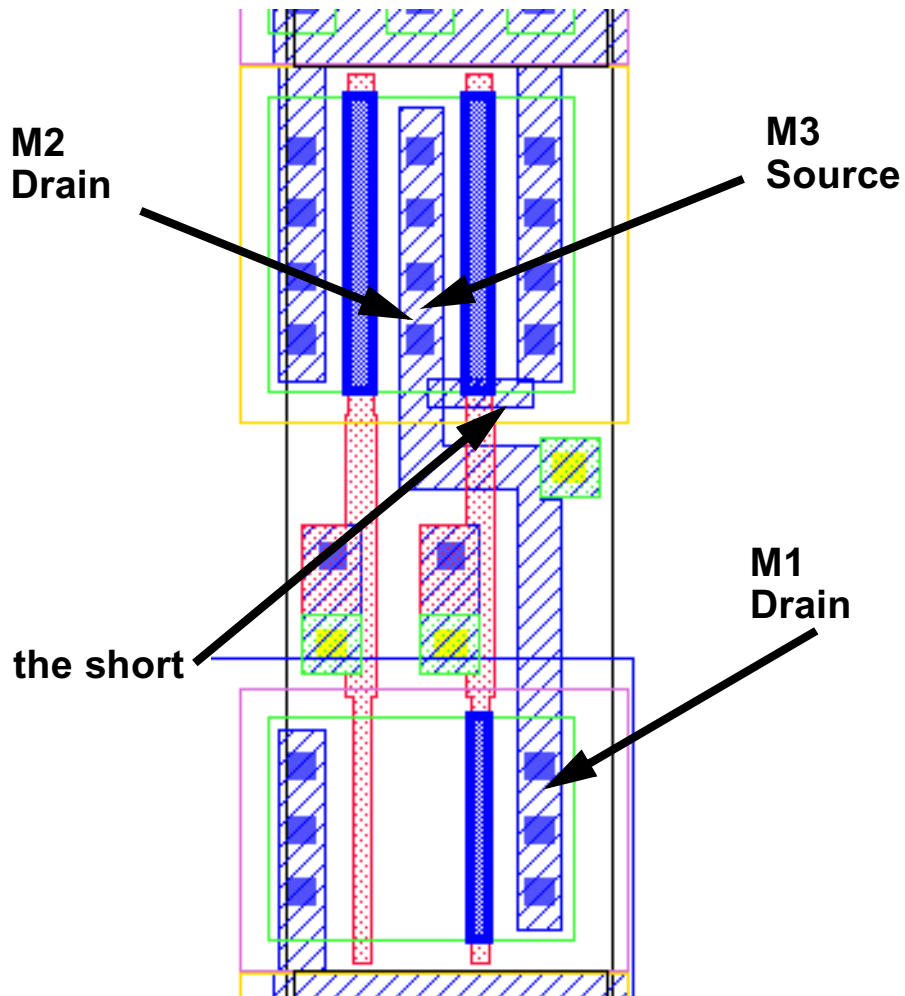
(M1, M2, and M3 are highlighted in the illustration.)

If you look carefully, you will notice there is a small piece of metal1 below M3 that is shorting the M3 drain to its source. That must be your short.

Shorts are never as easy to find as opens and do require more detective work and some educated guessing.

13. Correct the error in the layout by removing the shorting piece of metal1.

14. Return to the Calibre Interactive LVS window.

15. Change the name of the layout input file to: "lab8b_fixed".

The text will turn red, as well as the **Layout** tab and **Input** menu button.

16. Select the **Import layout database from layout viewer** option.

    This will turn the **Layout** tab and **Input** menu button green again.

17. Run LVS.

    What happened to all the errors in the lab8 cell?

    _____

18. When you are ready to go to the next exercise, close all Calibre windows *except* the Calibre Interactive LVS and DESIGNrev windows.

Exercise 8-3: Troubleshooting a Circuit with both Shorts and Opens

Troubleshooting a layout that has both kinds of errors adds an additional level of complexity to the task.

1. Open layout, lab8c.gds in DESIGNrev.

2. Load the layer properties file, layer_props.txt.
    (**Menu: Layer > Load Layer Properties**)

3. Change the following **Inputs [Layout]** data:

Layout Files:	lab8c.gds
Import layout database from layout viewer	Unselected
Layout Netlist:	lab8c_layout.net

4. Run LVS.

5. Using the LVS Summary Report, answer the following questions.

    What kind(s) of error(s)?

    _____

    In what cell(s)?

    _____

    Any differences in the number of Source / Layout nets?

    _____

6. Review the rest of the LVS Summary Report to get an overview of the problems.

7. Close the LVS Summary Report.

8. In RVE, display the Source and Layout netlists.

9. Arrange the windows so you can see RVE, the two netlists, and the layout viewer.

10. Highlight the nets involved in the two discrepancies.

   The layout should look similar to below. (Zoomed in as necessary.)

   The Source netlist:

The Layout netlist:

```
X122 VSS VDD 13 37 59 a1220 $T=280500 17000 1 180 $
X125 VSS VDD 39 29 39 22 a1230 $T=295000 229000 1 1
X131 VSS VDD 25 38 40 a1220 $T=280500 17000 0 0 $X=
X132 VSS 21 VDD 62 41 42 a1620 $T=280500 355000 0 C
X140 VSS VDD 21 39 12 16 a1230 $T=295000 229000 0 C
X141 VSS VDD 16 40 21 a2311 $T=296500 118000 0 0 $X
X147 VSS VDD 13 25 a1310 $T=304500 17000 0 0 $X=30C
X151 VSS 24 VDD 42 41 a1720 $T=312500 355000 0 0 $X
X156 VSS VDD 25 43 45 a1220 $T=320500 17000 0 0 $X=
X161 VSS VDD 16 24 30 12 14 60 ICV_1 $T=352500 229C
X167 VSS VDD 12 34 47 a2311 $T=344500 118000 0 0 $X
```

11. Identify each of the instances.
    (Write the name next to the arrow in the illustration below.)
    Give both the layout and source names.
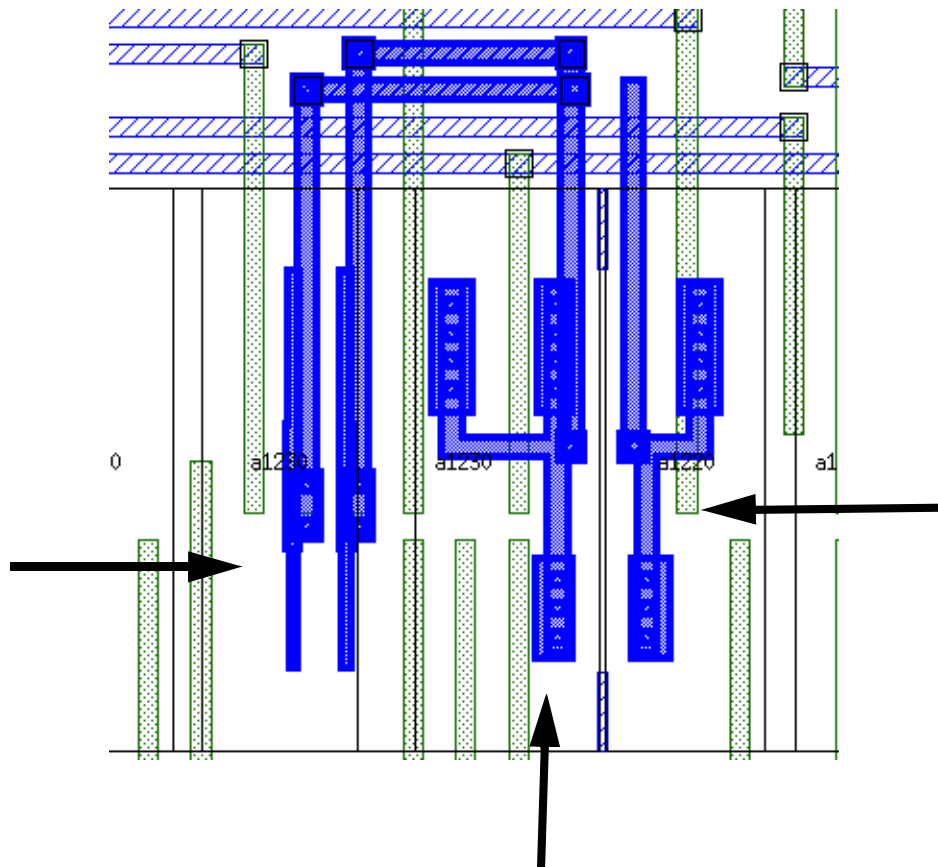
Did anything "interesting" happen while you were looking for instance names?

_____

12. Look at the subcircuits for Layout X161 and Source X164.

    Are they the same type?

    _____

    This could be a big clue to what is happening in the layout. X161 is part of discrepancy 1. You can use this piece of information.

13. Erase all highlights.

14. Highlight Net 60 from discrepancy 1.

    Where does it connect in the source?

    _____

    Where does it connect in the layout?

    _____

    You have a (short or open)?

    _____

    The next task will be to identify where this net should connect.

    It may be helpful to sketch out a portion of the schematic to help visualize the connectivity. You may have noticed from the two netlists that cell pin order does not have to agree between Source and Layout as long as the

overall connectivity is consistent. For example, look at the pin numbering used for the s1230 Source cell.
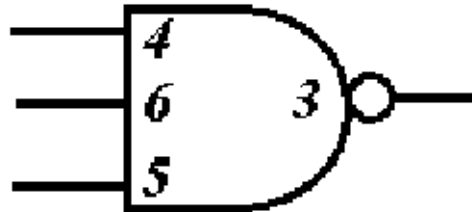
S1230

The pin numbers used for Layout cell, a1230, are different.
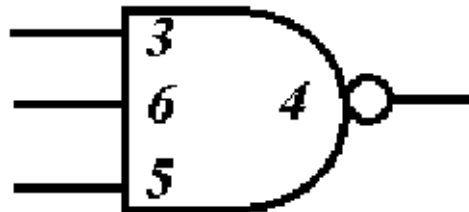
A1230

Using the schematic symbols above and the source and layout netlists as a guide sketch the circuit connectivity for source instances X129 and X144 and for layout instances X125 and X140.

Now can you identify the connectivity error?

15. Try to identify the port where the open should connect.

_____

Locate where the un-matched net should connect in the layout.
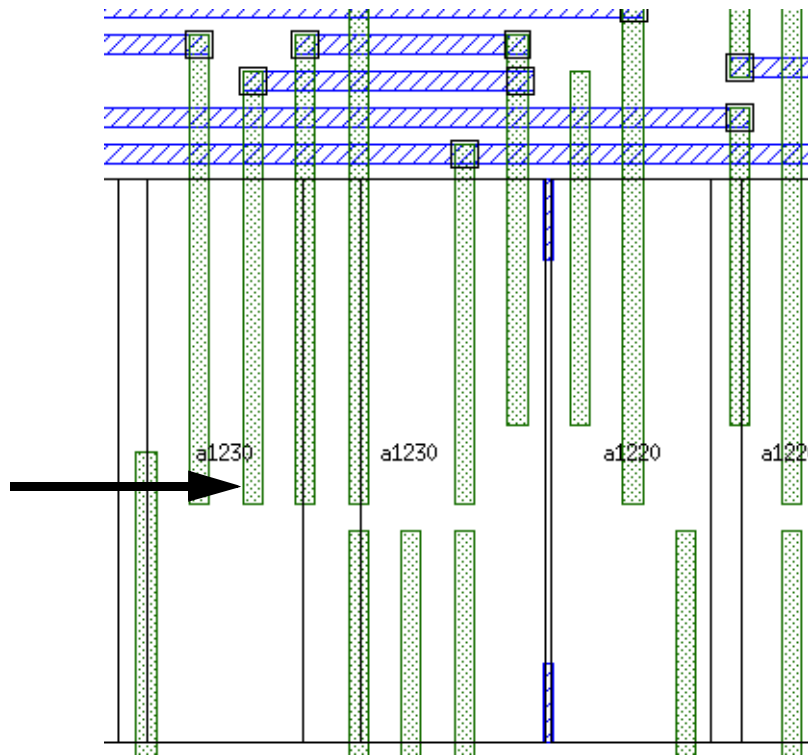
Do not fix anything yet. Look at the second discrepancy first to see if the two are related (since they are so physically close in the layout).

16. Erase all highlights.

17. Highlight Net 39 in the second discrepancy.

Was anything in this error involved in the first one?

_____

Looking at the layout and the netlists, can you find the one correction that will fix both errors?

_____

_____

This fix is illustrated below.

Extend this metal2 run   **Move this via from here to there**
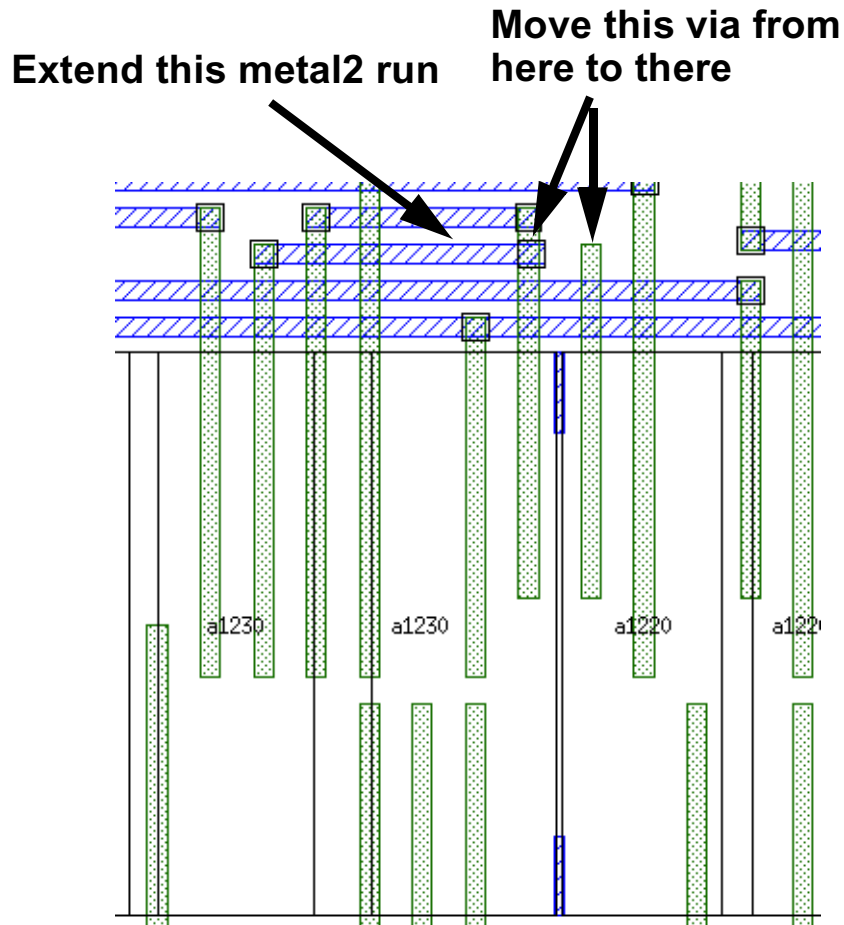
18. **OPTIONAL**: Fix the layout and run LVS again.
(Make sure to import the changes from the layout!)

19. When you are ready to go to the next exercise, close all Calibre windows *except* the Calibre Interactive LVS and DESIGNrev windows.

Exercise 8-4: Troubleshooting a Power to Ground Short

Now that you have mastered simple shorts and opens, you are ready to tackle the difficult problem of tracking down a Power to Ground short. Since Calibre uses the VDD and VSS connects to identify devices, the number of discrepancies are often extremely large for just a "small" layout error.

1. Open layout lab8d.gds in DESIGNrev.

2. Load the layer properties file, layer_props.txt.
   (**Menu: Layer > Load Layer Properties**)

3. In Calibre Interactive LVS, change the following **Inputs [Layout]** data:

Layout Files:	lab8d.gds
Import layout database from layout viewer	Unselected
Layout Netlist:	lab8d_layout.net

4. Change the following **Rules** data:

Calibre-LVS Rules File:	lab8_supply_rules

5. In Calibre Interactive LVS, choose **Menu: Setup > LVS Options**.

   This adds an additional Menu button, LVS Options, and displays the LVS Options.

6. Choose the **Supply** tab.

7. Change the following data:

Abort LVS on power/ground net errors:	Selected
Power net names:	VDD
Ground net names:	VSS

You selected to have LVS abort a run when it encountered a power/ground problem. This is a good option to have as a default setting. It not only alerts you immediately that there is a supply problem, it also prevents you from wasting time on a long LVS run that has such a basic problem.

8. Run LVS.

9. Look at the LVS Report.

   What are the results?

   _____

   Notice this is different from just "Incorrect". The comparison was not even done.

10. Close the RVE and LVS Report windows.

11. In Calibre Interactive, change the following **LVS Options [Supply]** data:

    Abort LVS on power/ground net errors: Unselected

    Power net names: <blank>
    Ground net names: <blank>

12. Run LVS again.

    Now what kind of results do you have?

    _____

13. Highlight the discrepancy in lab8.

    Did you find it?

    _____

14. Erase the highlights.

15. Try highlighting the discrepancy from one of the subcircuits.

Any luck narrowing down the problem?

_____

A straight LVS run is just not adequate for finding a short in a power/ground (or any very large net for that matter).

16. Erase all highlights.

17. Close the LVS Report Window and the RVE window.

18. In Calibre Interactive, change the following **LVS Options [Shorts]** data:

Run short isolation	Selected
Output shorts by layer	Unselected
Run flat short-isolation	Selected
Isolate shorts in top cell only	\<grayed out\>
AND	\<grayed out\>
Between all names	\<grayed out\>

19. Run LVS again.

You have the same results as the previous run in the LVS Report.

20. Close the LVS Report.

In RVE, you will notice that you have a new file available, Shorts Database.

21. Open the Shorts Database.

What happens?

_____

22. Expand the errors in the DRC- RVE window.
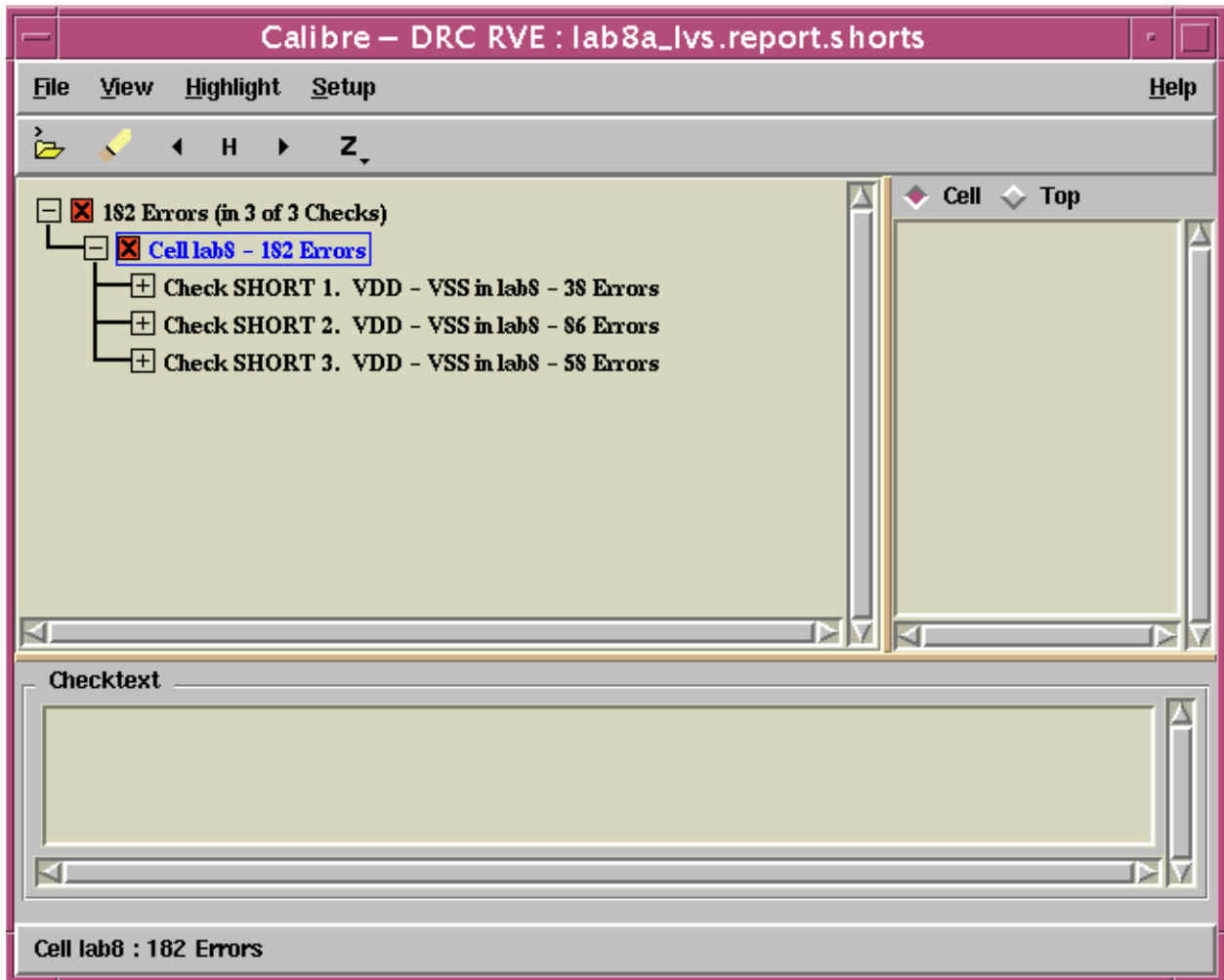
How many shorts do you have?

_____

Next you will highlight all the components on the first short.

23. Click the LMB over the Check SHORT1 statement to highlight it.

24. Click the RMB, to display the popup menu.

25. Choose **Highlight Cluster**.

The layout now looks similar to below.
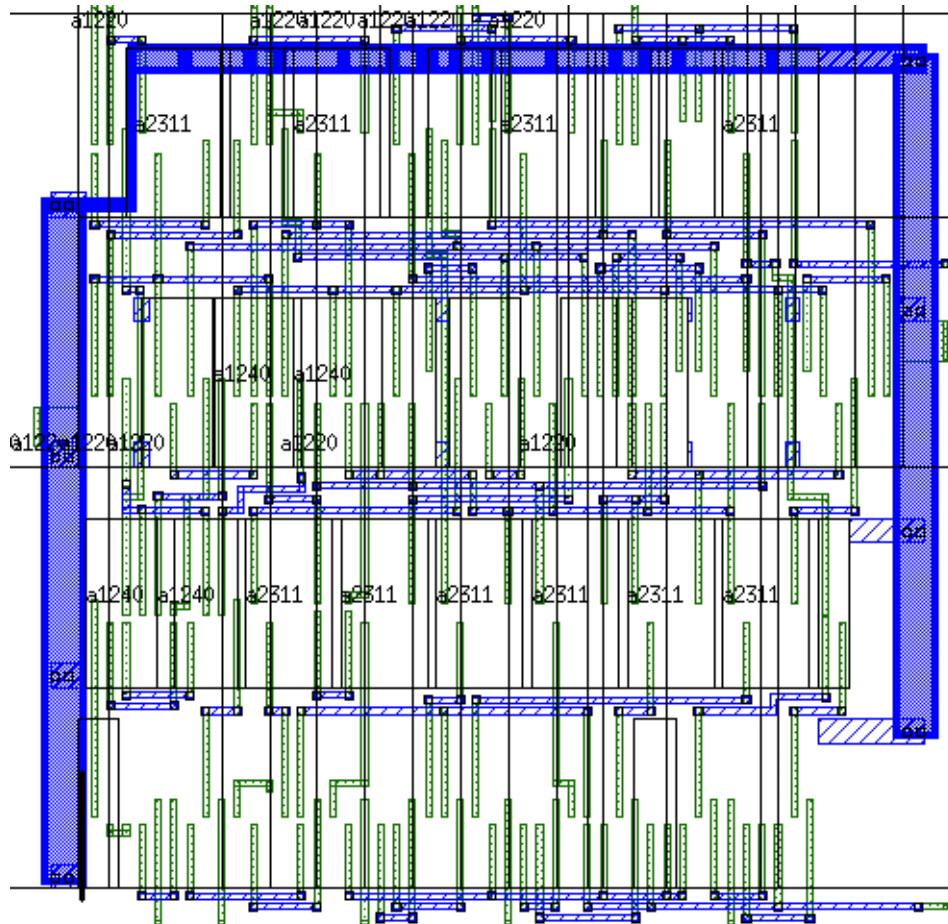
If we are going to find this error, we first need to know a little about the layout.

VDD is the vertical bus on the right.

VSS is the vertical bus on the left.

VDD connections generally run on the top of cells-VSS on the bottom.

26. Erase the highlights.

27. Display the other two short clusters.

28. Look carefully at the layout, while erasing the highlight.
    (You may have to highlight and erase a few times to see it.)

    How often did the "short" run between the VDD and VSS horizontal busses? (More than once?)

    _____

    Does in appear to happen near a consistent cell?

    _____

    Do you think the short is in the lab8 cell or one of the lower ones?

    _____

    Another hint that the short might be in a lower level cell, is that you have three shorts. It is possible to create a short, but not too likely a layout designer would do it three times.

29. Close both RVE windows and the LVS Report.

    We are going to run LVS again, this time looking for shorts in the lower level cells.

30. In Calibre Interactive, change the following **LVS Options [Shorts]** data:

Run short isolation	Selected
Output shorts by layer	Unselected
Run flat short-isolation	Unselected
Isolate shorts in all cells	Selected
AND	Selected
Between all names	Selected

31. Run LVS.

32. Display the Shorts Database.

What is different?

_____

33. Highlight the Cluster in Short 1.

    Notice that now only geometries within the cell containing the short (a1220) highlight.

34. In DESIGNrev, choose **Menu: View > Change Hierarchy Depth > Increment To Depth**.

    This displays the underlying polygons.

35. Zoom in as necessary to see the structures clearly.

The results should look similar to below.
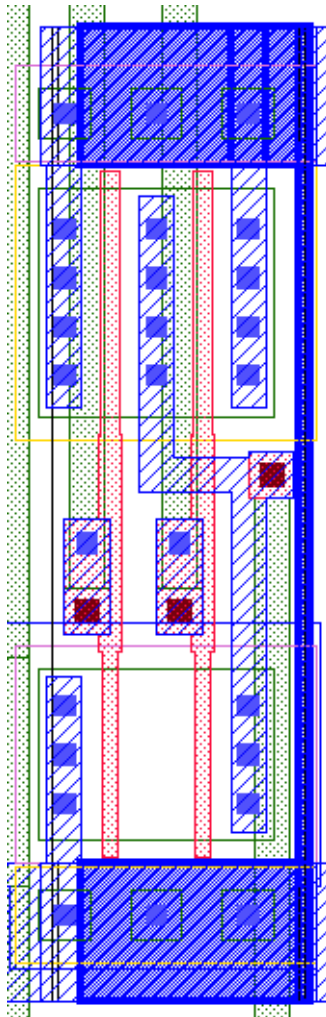
VDD and VSS are directly shorted in this cell by the long thin polygon down the right side of the cell.

36. Erase the highlights.

37. Open Cell a1220 in DESIGNrev.

38. Fix the short.

39. In Calibre Interactive LVS, change the following **Inputs [Layout]** data:

                           Layout Files: lab8d_fixed.gds

Import layout database from layout viewer **SELECTED**

Layout Netlist: lab8d_layout.net

Make sure to change the Layout file name to and select to import the layout database from the viewer!

40. Run LVS again to verify your fix.
    (Make sure to Import the Layout Database from the Layout Viewer!)

41. Close all Calibre related windows. (Including DESIGNrev, Calibre Interactive DRC/LVS, RVE, Netlist windows, and Summary Report.)

Module 9
Device Recognition

Objectives

At the completion of this lecture and lab you should be able to:

- Troubleshoot malformed devices using Calibre LVS

- Troubleshoot mis-connected devices using Calibre LVS

- Troubleshoot properties in the Source and Layout

Prerequisites for Calibre Device Extraction

Prerequisites for Calibre Device Extraction

- ◆ **Prerequisites:**

  - ● **Add shapes to original (drawn) layers**

  - ● **Add layer constructor and layer selector operations to the rule file to generate derived layers**
    NOTE: some layer operations preserve connectivity

  - ● **Add device statements to the rule file to specify which derived layers can form devices**

- ◆ **Connectivity is important**

  - ● **Power supply connections are part of gate recognition**

  - ● **No power supply connections = no gate recognition**

- ◆ **Calibre LVS extracts devices in the layout recognized by the device statements**

Notes:

Example: Device Layer Derivation

LAYER PWELL	1
LAYER OXIDE	2
LAYER POLY	4
LAYER NPLUS	5

ORIGINAL LAYERS

PAREA = OXIDE AND PWELL
NGATE = POLY AND PAREA
NOX   = OXIDE AND NPLUS
NSD   = NOX NOT NGATE

LAYER CONSTRUCTORS

PWELL
OXIDE
POLY
NPLUS

NSD   NSD

OUT
IN
VSS
VSS
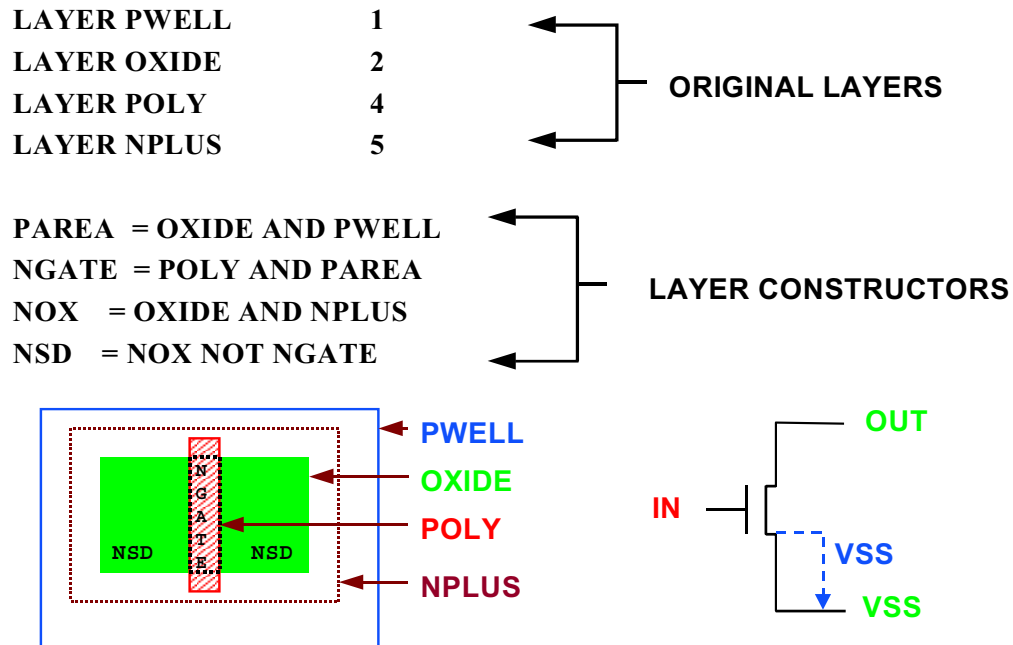
Notes:

Connectivity in derived layers is only passed through the FIRST layer in the derived layer statement. For example, NGATE = POLY AND PAREA, connectivity for NGATE only comes from the POLY layer.

Review of the Device Statement

Review of the Device Statement

- ♦ **Defines a device template for recognizing instances from a union of geometric shapes**

- ♦ **Names and classifies a device**

- ♦ **Specifies device layer, pin layers, and pin swap groups**
  - ● **Shapes on the device layer seed the recognition process**
  - ● **Devices are recognized if a shape on each pin layer touches (overlaps or abuts) the shape on the device layer**
  - ● **Pin layer order determines pin name assignment**

- ♦ **Specifies parameters for device property calculations**

Notes:

Example: Device Statement

Example: Device Statement

Element Name

Device (Seed or Body) Layer

DEVICE MN NGATE POLY NSD NSD PWELL (S D) [0]

Gate Pin Layer

Source Pin Layer

Drain Pin Layer

Bulk Pin Layer

Property Specification

Pin Swap List
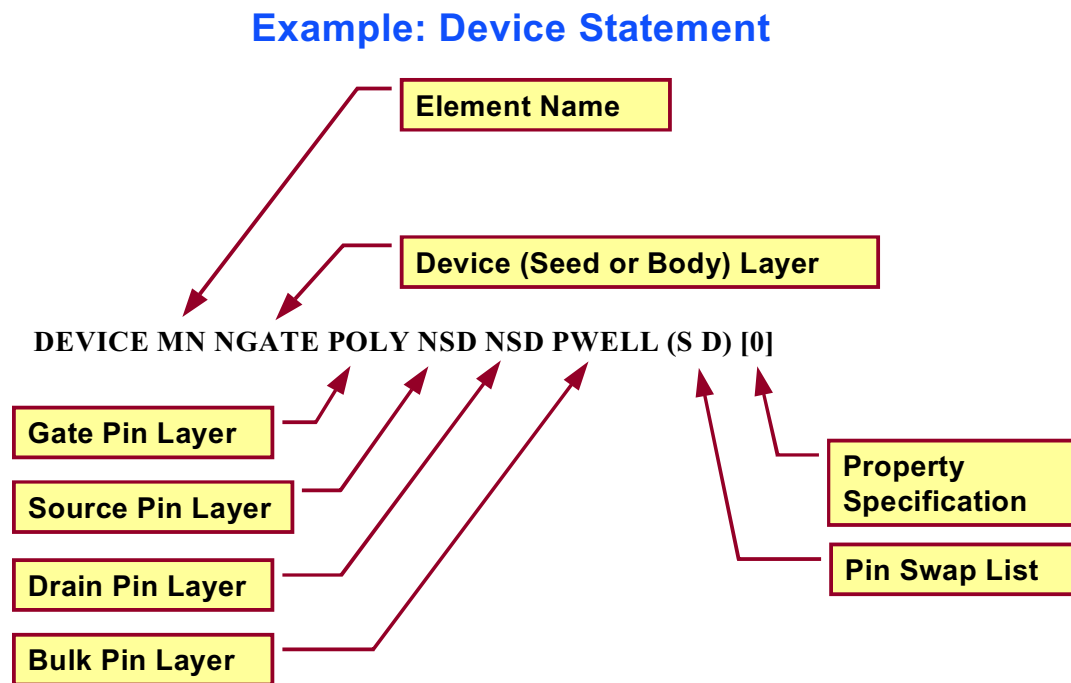
Notes:

Associating Layout Devices to Source Components

Associating Layout Devices to Source Components

// Device Statement
DEVICE MN NGATE POLY NSD NSD PWELL [0]
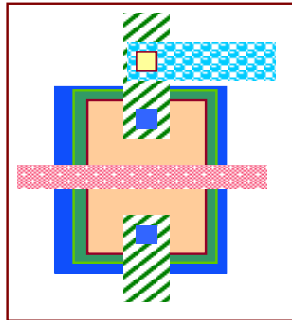
1. LVS defines the MN element template based upon the Device statement.
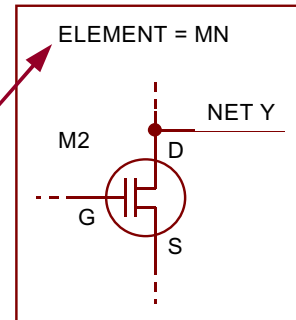
ELEMENT = MN

NET Y

M2

G D S

LAYER PWELL   1
LAYER OXIDE   2
LAYER POLY   4
LAYER NPLUS   5

PAREA   = OXIDE AND PWELL
NGATE   = POLY AND PAREA
NOX   = OXIDE AND NPLUS
NSD   = NOX NOT NGATE

Notes:

Using Calibre with DESIGNrev
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Associating Layout Devices to Source Components (Cont.)

Associating Layout Devices to Source Components (Cont.)

// Device Statement
DEVICE MN NGATE POLY NSD NSD PWELL [0]
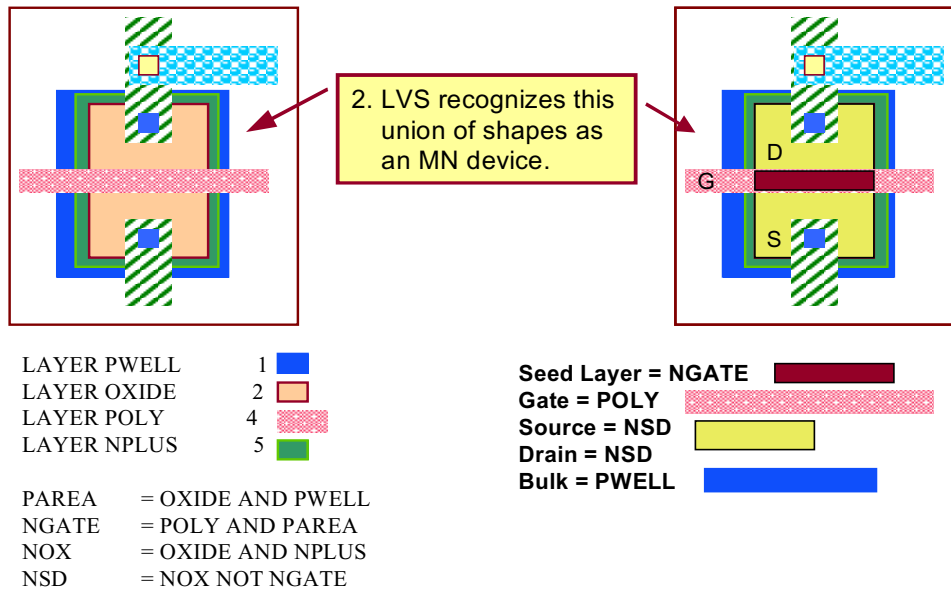
2. LVS recognizes this union of shapes as an MN device.

LAYER PWELL	1	
LAYER OXIDE	2	
LAYER POLY	4	
LAYER NPLUS	5	

PAREA	= OXIDE AND PWELL
NGATE	= POLY AND PAREA
NOX	= OXIDE AND NPLUS
NSD	= NOX NOT NGATE

Seed Layer = NGATE
Gate = POLY
Source = NSD
Drain = NSD
Bulk = PWELL

9-8 • Using Calibre: Device Recognition   Copyright © 2004 Mentor Graphics Corporation

Notes:

Associating Layout Devices to Source Components (Cont.)

Associating Layout Devices to Source Components (Cont.)

NET 42

3. LVS extracts layout connectivity and assigns net IDs.

ELEMENT = MN

NET Y

M2

D

G

S
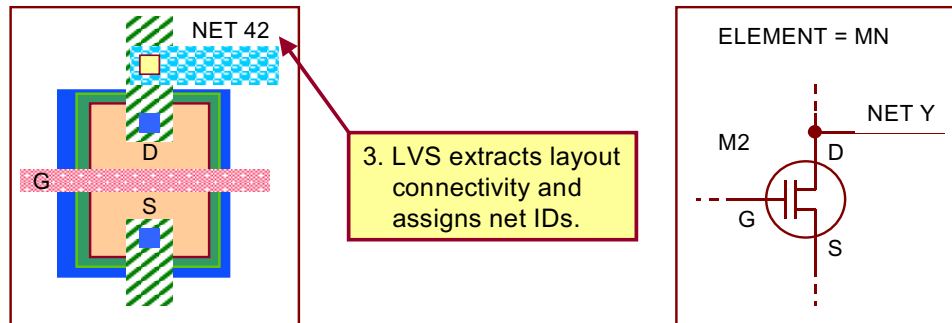
METAL1   VIA

METAL2   CONTACT

//Connection statements
CONNECT METAL1 METAL2 by VIA
CONNECT METAL1 NOX by CONTACT

Notes:

Associating Layout Devices to Source Components (Cont.)

Associating Layout Devices to Source Components (Cont.)

NET 42

ELEMENT = MN

NET Y

M2

D

NET 1 G

4. LVS associates device pins with net IDs to form the layout netlist.

G

S

D

S

NET 2

Bulk= NET 3

//Layout Netlist
M0 42 1 2 3 n L=1.25e-6 W=1.5e-5
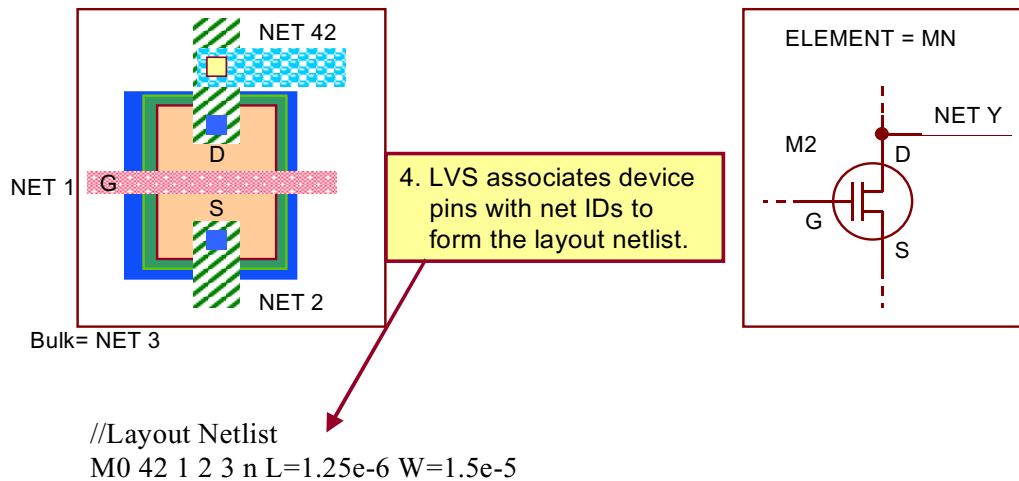
NOTE: Nets 1 2 42 and 3 are arbitrary numbers

Notes:

Associating Layout Devices to Source Components (Cont.)

Associating Layout Devices to Source Components (Cont.)

5. LVS compares the layout netlist to the source netlist.

//Layout Netlist
M0 42 1 2 3 n L=1.25e-6 W=1.5e-5

//Source Netlist
M2 Y 55 4 7 n L=1.25e-6 W=1.5e-5

Device matches at this point, additional connectivity information is required for complete match (what other devices/instances share these nets)
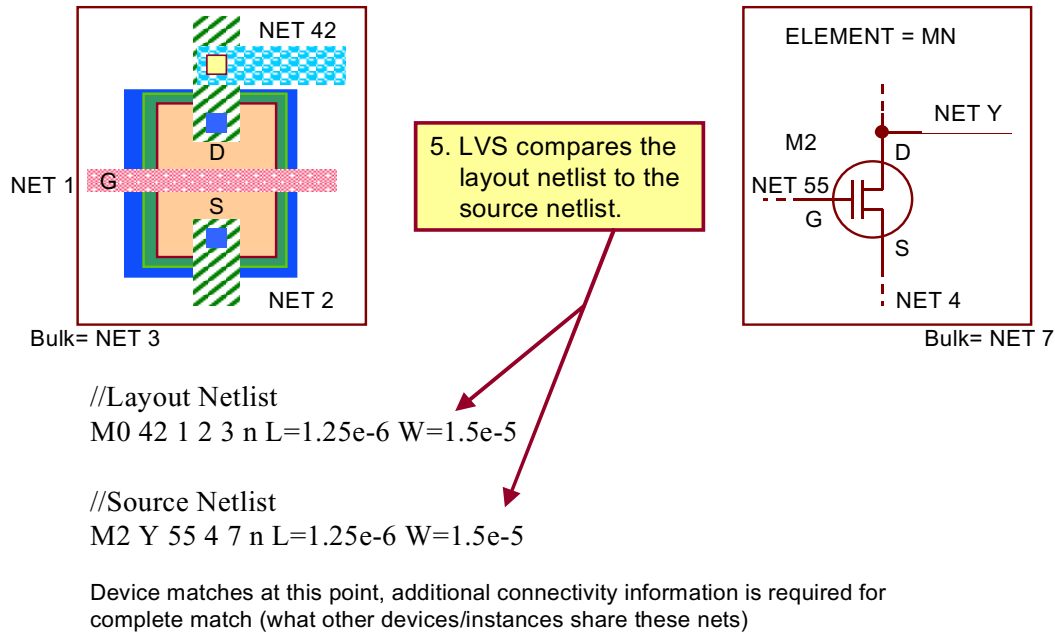
Notes:

How Calibre Recognizes Logic Gates in the Layout

- **LVS RECOGNIZE GATES ALL | SIMPLE |NONE**
  - **ALL (default): allows complex gate recognition (AOI, OAI, high level series-parallel structures)**
  - **SIMPLE: all recognition of (N)AND, (N)OR, INVERTER gates**
  - **NONE: prevents recognition**

- **Gate recognition allows swapping of equivalent pins**

- **Restrictions**
  - **Power and ground nets must be named in the layout**
  - **Transistors must have at least three pins with pin names consistent throughout the gate**
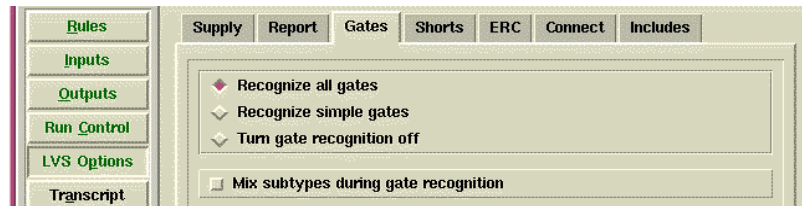
Notes:

Examples of Recognizable Simple CMOS Gates
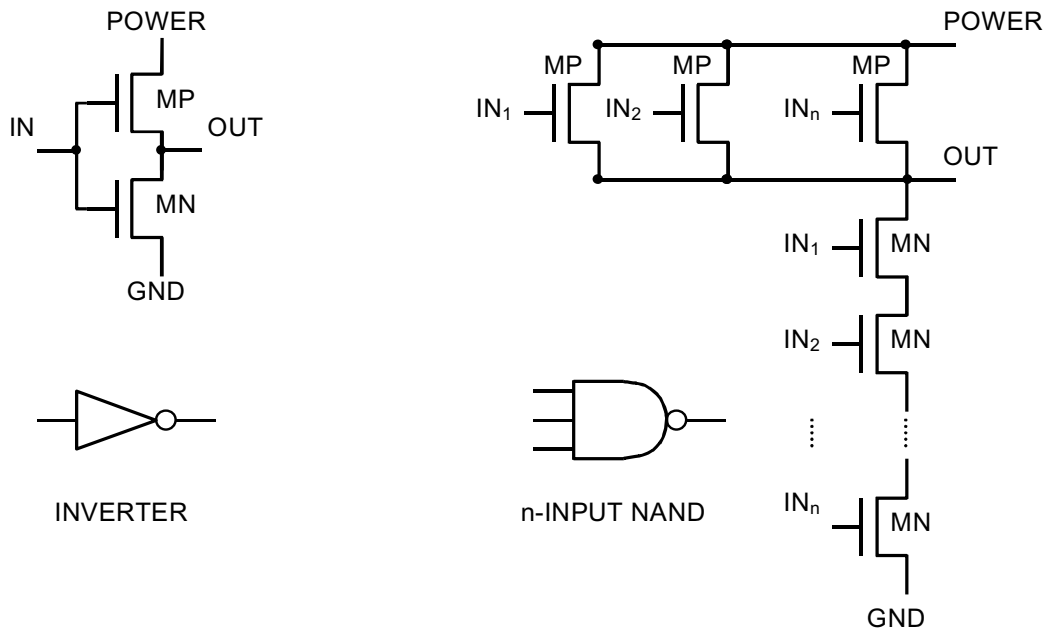
Notes:

Property Tracing Overview

Property Tracing Overview

♦ **After device recognition, Calibre makes default and user-defined properties available for LVS comparison**

♦ **TRACE PROPERTY statement must be used for each property to make the property available for LVS comparison**

♦ **Internal properties available:**
  - **MOSFET (MN, MP, MD, ME): W and L**
  - **Diode (D): A and P**
  - **Capacitor (C): C**
  - **Resistor (R): R**

Notes:

TRACE PROPERTY Statement

TRACE PROPERTY Statement

TRACE PROPERTY *component_type* **[(***component_subtype***)]**
     {*source_property* **[(***spice_value***)]** }
     {*layout_property* **[(***spice_value***)]** }
     {[*tolerance1* **[(***tolerance1_prop)***]]**
     [*tolerance2* **[(***tolerance2_prop)***]]**
     [ABSOLUTE] | STRING}

Examples:
 TRACE PROPERTY MP W W 2 **// Compare width property**
            // on PMOS devices with a
            // 2% tolerance

 TRACE PROPERTY MP W W 2e-6 ABSOLUTE
            // Compare width property
            // on PMOS devices with a
            // tolerance of +/- 2microns

Notes:

Key TRACE PROPERTY Statement Parameters

Key TRACE PROPERTY Statement Parameters

- ♦ *component_type*
  Type of device
- ♦ **[(*component_subtype*)]**
  Component subtype. If unspecified, all devices of the same type will be included.
- ♦ *source_property* **[(*spice_value*)]**
  The Source property to be traced. The optional parameter allows you to parse strings to find the desired value.
- ♦ *layout_property* **[(*spice_value*)]**
  The Layout property to be traced. The optional parameter allows you to parse strings to find the desired value.
- ♦ **ABSOLUTE**
  Tolerance parameters are treated as absolute values rather than percentages.

Notes:

There are additional parameters available for the TRACE PROPERTY statement, but they are beyond the scope of the class. If you would like more information, see the *SVRF Manual*.

TRACE PROPERTY Examples

TRACE PROPERTY Examples

- **Example 1:**

  TRACE PROPERTY MP W W

  TRACE PROPERTY MP L L

  - **These statements enable LVS to compare width and length in all PMOS devices not specifically covered by any other sub-type**
  - **The tolerance is 0%.**

- **Example 2:**

  TRACE PROPERTY C C C 2

  TRACE PROPERTY C A A 2

  TRACE PROPERTY C P P 2

  - **These statements enable LVS to compare capacitance, area, and perimeter in capacitors**
  - **Tolerance is 2% tolerance.**
  - **Note: A and P must be user-defined**

References:

To find more information about matching "reduced" transistors when there are fewer transistor in the layout than in the source (should be rare in most cases), please search for the phrase "multiplier" in the *Calibre User's Manual* or look up LVS REDUCE in the *SVRF Manual*.

Notes:

Reducing Parallel MOS Transistors

Reducing Parallel MOS Transistors
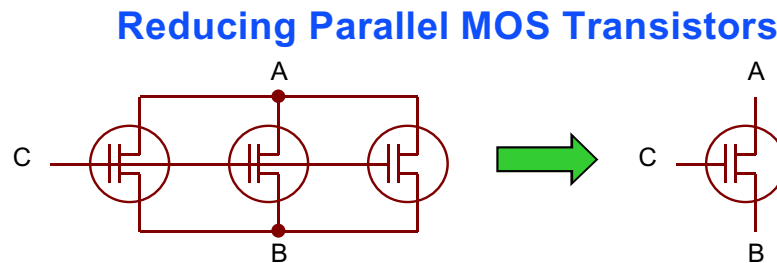
♦ **To specify whether to perform device reduction:**

LVS REDUCE PARALLEL MOS <u>YES</u> | NO

♦ **Reduces the number of transistors in the Layout to match the number of transistors in the Source**
(to go in the other direction:
see the LVS REDUCE statement in the *SVRF Manual*)

♦ **Restrictions: Transistor component type, subtype, pin number and pin names must be consistent throughout the group**

Notes:

Reducing Series MOS Transistors

Reducing Series MOS Transistors
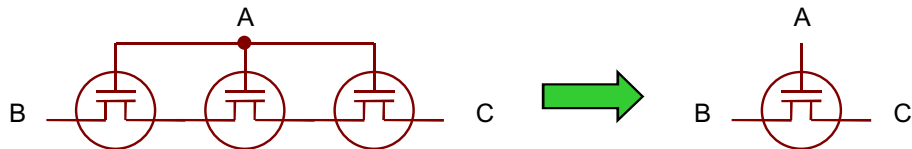
♦ **To specify whether to perform device reduction:**

LVS REDUCE SERIES MOS <u>NO</u> | YES

♦ **Restrictions:**

● **Transistors must be of same device type, have same number of pins and matching pin names**

Notes:

What Other Devices are Reducible

♦ **Split gate (series-parallel) MOS transistors**

♦ **Parallel bipolar transistors**

♦ **Parallel capacitors**

♦ **Series capacitors**

♦ **Parallel resistors**

♦ **Series resistors**

♦ **Parallel diodes**

Notes:

How to Handle Unused Devices

♦ **Filtering**

♦ **In the rule file:**

LVS FILTER UNUSED MOS | BIPOLAR

♦ **What configurations are filtered out:**

● **Floating source or drain**

● **Shorted gate, source, and drain**

● **Floating gate with source tied to VDD or VSS**

● **Shorted source and Drain with gate tied to VDD or VSS**

● **Shorted base and emitter**

♦ **Can specify other filtering options using LVS FILTER OPTION**

Notes:

Pin Swapping

Pin Swapping

- ♦ **Occurs when the pin connection order of a primitive is different between source and layout netlists**

- ♦ **Is allowable when pins of a device or gate primitive are designated as logically equivalent**
  - • **Resistor pins = swappable**
  - • **Diode pins = not swappable**

- ♦ **Facilitates routing**

- ♦ **Pin Swapping example:**
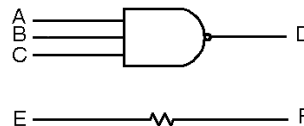
Pins A, B and C are swappable gate pins

Pins E and F are swappable device pins

Notes:

Avoiding False Pin Swap Discrepancies in LVS

- ◆ **Use the rule file to designate swappable pins:**
  - ● **Add pin names to Pin Swap list in the** `DEVICE` **statement**
  - ● **List pins on a single layer in the** `DEVICE` **statement**
  - ● **Add the** `LVS RECOGNIZE GATES` **specification**

- ◆ **Pins swappable by default include:**
  - ● **Device pins with identical names**
  - ● **Source and Drain pins of MOS regular transistors**
  - ● **Capacitor pins, unless rule file contains the specification:**
    `LVS ALL CAPACITOR PINS SWAPPABLE NO`
  - ● **Resistor pins**

Notes:

Identifying a Pin Swap Discrepancy with LVS-RVE

Identifying a Pin Swap Discrepancy with LVS-RVE

♦ **Cross-probe from the Discrepancy Viewer into the netlists:**

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Notes:

Identifying a Pin Swap Discrepancy with LVS-RVE (Cont.)

Identifying a Pin Swap Discrepancy with LVS-RVE (Cont.)

♦ **View the two superimposed discrepancies in the layout netlist and source netlist:**

The layout pins are swapped. If you interchange them, you can match the pin connections in the source netlist.

Notes:

Using Calibre with DESIGNrev
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Resolving a Pin Swap Discrepancy

- ◆ **Correct the discrepancy in the layout editor**
  - ● **Use LVS-RVE to cross-probe into source netlist and layout netlist**
  - ● **Use LVS-RVE to highlight the problem nets**
  - ● **Change the connections in the Layout**

OR

- ◆ **Add**

  `LVS RECOGNIZE GATES ALL │ SIMPLE`

  specification to the rule file

Notes:

What Types of Errors Occur if a Contact is Misplaced?

What Types of Errors Occur if a Contact is Misplaced?

- ◆ **Connectivity errors - Incorrect Nets**

- ◆ **Instance errors - Incorrect Instances**

- ◆ **Similar discrepancies as a short or open**


```
☐ ☒ LVS Results: Designs Don't Match
    ☐ ☒ lab5a / lab5a – 80 Discrepancies
        ☐ Incorrect Nets – 50 Discrepancies
        ☐ Incorrect Instances – 30 Discrepancies
        ◇ Detailed Instance Connections
```
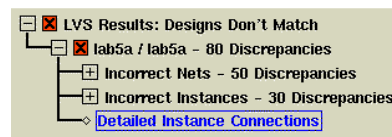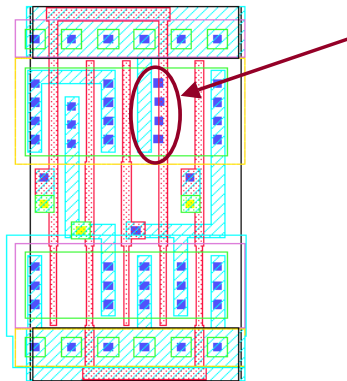
Notes:

Identifying Mismatched Instances

Identifying Mismatched Instances

- ♦ **Could look like any other discrepancy**
  - ● **Incorrect Nets**
  - ● **Incorrect Instances**
- ♦ **Clue is in the netlists**
- ♦ **Mismatched device instances**
  - ● **Source = a1230**
  - ● **Layout = a1620**

Notes:

Lab Information

Lab Information

In this lab you will:

- ♦ **Find swapped pins**
- ♦ **Trace properties**

Notes:

Using Calibre with DESIGNrev
June 2004

Lab: Device Recognition

Introduction

In the lab with the power/ground short you already experienced that Calibre cannot recognize gates without proper Power and Ground connections. In this lab, you will experiment with two other aspects of device recognition: pin swapping and property tracing.

List of Exercises

Exercise 9-1: Find a Pin Swap Discrepancy

Exercise 9-2: Property Tracing

Exercise 9-1: Find a Pin Swap Discrepancy

In this lab you will find a swapped pin.

1. Change to the lab9 directory.

2. List the files in the directory.

   You should see the files:

cell_file	lab9_rules	lab9_trace_rules
golden_rules	lab9_source.spi	lab9_trace_source.spi
golden_rules_trace	lab9_trace.gds	lab9a.gds
		layer_props.txt

   If any of these files are missing, please double check that you are in the correct directory, and then notify your instructor.

3. Launch DESIGNrev.

4. Open lab9a.gds.

5. Load the layer properties file, layer_props.txt.
   (**Menu: Layer > Load Layer Properties**)

6. Launch Calibre Interactive LVS on cell lab9.

7. Choose **New Runset**.

8. Enter the following **Inputs [Layout]** data:

Hierarchical, Flat, or Calibre CB	Hierarchical
Layout vs. Netlist, Netlist vs. Netlist, or Netlist Extraction	Layout vs. Netlist
Layout Files:	lab9a.gds
Import layout database from layout viewer	Unselected
Primary Cell	lab9

Layout Netlist: lab9a_layout.spi

9. Enter the following **Input [Netlist]** data:

Netlist Files: lab9_source.spi

Import netlist from schematic viewer   Unselected

Primary Cell: lab9

10. Enter the following **Input [HCells]** data:

Match cells by name (automatch):   Selected

Use H-Cells list from file: Selected

[filename]   cell_file

11. Enter the following **Rules** data:

Calibre-LVS Rules File: lab9_rules

Calibre-LVS Run Directory: .

12. Enter the following **Outputs [Report/SVDB]** data:

LVS Report File: lab9_lvs.report

View Report after LVS finishes: Selected

Create SVDB Database: Selected

Start RVE after LVS finishes: Selected

Generate data for xCalibre: Unselected

Generate Calibre Connectivity Interface data: Unselected

SVDB Directory: svdb

13. Run LVS.

   📄 **Note** If you get a message box asking to overwrite layout file, lab9a.gds, cancel the message box and return to the **Input** Menu button/**Layout** tab. Make sure **Import layout database from layout viewer** is <u>unselected</u>, then try running LVS again.

   What are your results?

   _____

   What cell contains the connectivity error(s)?

   _____

   How many discrepancies?

   _____

   What Instance(s) have the discrepancies?

   Source: _____

   Layout: _____

14. Display the Layout netlist.

   ```
   X156 VSS VDD 25 44 45 a1220 $T=320500 17000 0 0 $X=
   X160 VSS VDD 16 24 30 12 14 39 ICV_1 $T=352500 2290
   X167 VSS VDD 12 34 48 a2311 $T=344500 118000 0 0 $X
   X168 VSS VDD 43 45 42 a2311 $T=344500 355000 0 0 $X
   X169 VSS VDD 46 61 44 a1220 $T=368500 17000 1 180 $
   X179 VSS VDD 13 46 47 a1220 $T=368500 17000 0 0 $X=
   X187 VSS VDD 49 28 48 21 16 49 ICV_1 $T=407000 2290
   X190 VSS VDD 45 47 a1310 $T=392500 118000 0 0 $X=38
   ```

15. Display the Source netlist.

   ```
   X160 VSS VDD 44 25 46 s1220 $T=320500 17000 0 0 $X=
   X164 VSS VDD 39 12 14 s1220 $T=352500 229000 1 180
   X171 VSS 34 VDD 12 48 s2311 $T=344500 118000 0 0 $X
   X172 VSS 46 VDD 43 42 s2311 $T=344500 355000 0 0 $X
   X173 VSS VDD 61 44 45 s1220 $T=368500 17000 1 180 $
   X176 VSS VDD 30 16 24 s1220 $T=376500 229000 1 180
   X184 VSS VDD 45 13 47 s1220 $T=368500 17000 0 0 $X=
   X192 VSS VDD 49 21 16 s1220 $T=407000 229000 1 180
   ```

16. Highlight the discrepancies in the layout.

Net 44

Net 45/46

**Layout:
X156
Source:
X161**

**Layout:X179
Source: X184**

**Layout:X169
Source: X173**
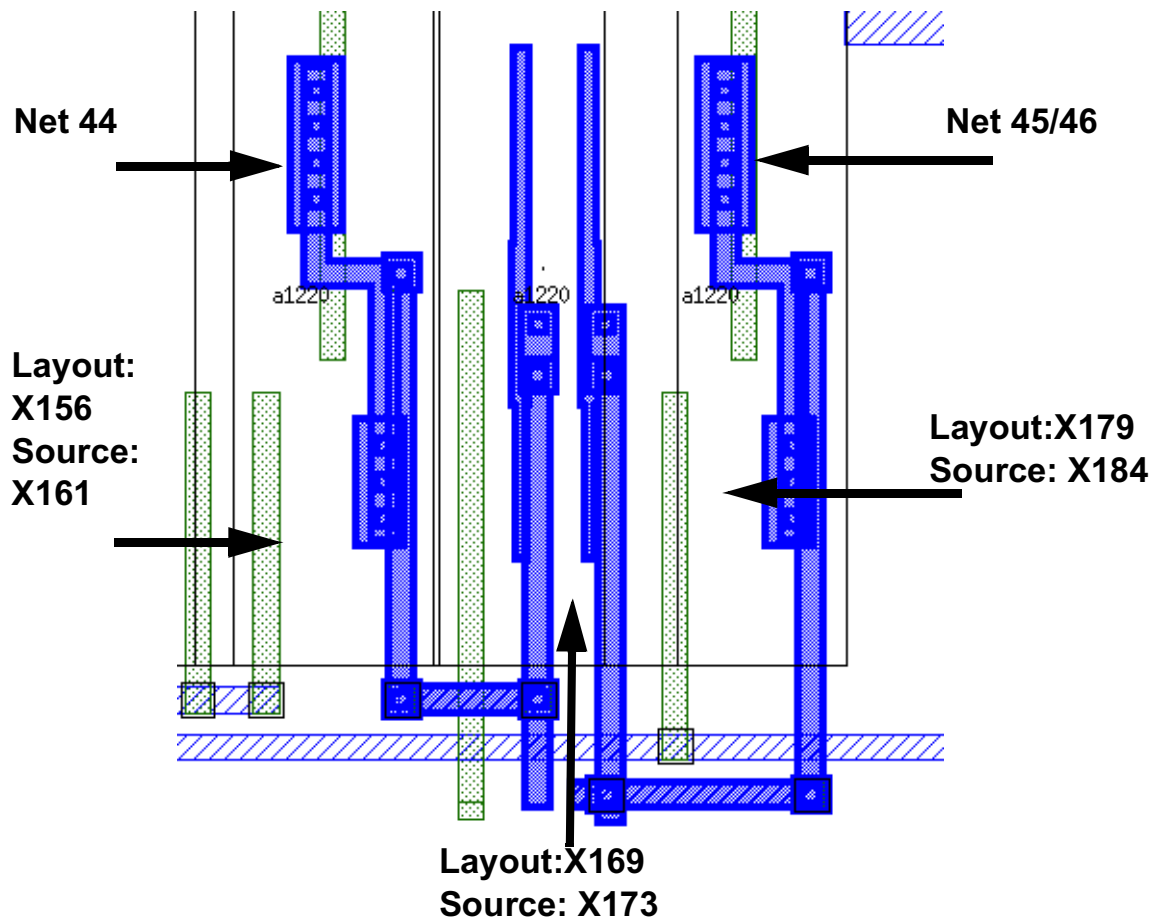
Useful Information: Pin layout for S1220 and A1220.

4
5
3
S1220

5
3
4
A1220
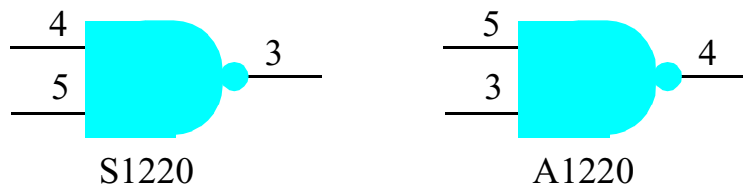
It looks like the connections to the 4 and 5 pins in x169 are swapped.

Is it functionally acceptable to swap these pins?
(You may need to view both the netlist and the layout for a1220.)

_____

17. Close all RVE windows and the netlists.

18. In the Calibre Interactive LVS window, choose **Menu: Setup > LVS Options**.

    This adds the **LVS Options** Menu button.

19. Choose **LVS Options** Menu button.

20. Choose the **Supply** tab.

    You need to define the Power and Ground net names to aid LVS in recognizing gates.

21. Enter VDD in the Power net names text box.

22. Enter VSS in the Ground net names text box.

23. Choose the **Gates** tab.

24. Select **Recognize all gates**.

25. Run LVS again.

    What are the results?

    _____

    Pin swapping is not always permitted, but when it is allowed, this is the method to resolve the discrepancies.

26. Close the LVS RVE window and all netlist windows.

27. Close the Calibre Interactive—LVS window.
    (The DESIGNrev window should still be open.)

Exercise 9-2: Property Tracing

In this lab, you will write rule statements to enable property tracing and view the results.

1. In DESIGNrev, open lab9_trace.gds.

2. Load the layer properties file, layer_props.txt.
   (**Menu: Layer > Load Layer Properties**)

3. Launch Calibre Interactive LVS on cell lab9_trace.

4. Choose to create a new runset.

5. Enter the following **Inputs [Layout]** data:

Hierarchical, Flat, or Calibre CB	Hierarchical
Layout vs. Netlist, Netlist vs. Netlist, or Netlist Extraction	Layout vs. Netlist
Layout Files:	lab9_trace.gds
Import layout database from layout viewer	Unselected
Primary Cell	lab9_trace
Layout Netlist:	lab9_trace_layout.spi

6. Enter the following **Input [Netlist]** data:

Netlist Files:	lab9_trace_source.spi
Import netlist from schematic viewer	Unselected
Primary Cell:	lab9_trace

7. Enter the following **Rules** data:

Calibre-LVS Rules File:	lab9_trace_rules
Calibre-LVS Run Directory:	.

8. Enter the following **Outputs [Report/SVDB]** data:

<div align="right">

LVS Report File: lab9_trace_lvs.report

View Report after LVS finishes: Selected

Create SVDB Database: Selected

Start RVE after LVS finishes: Selected

Generate data for xCalibre: Unselected

Generate Calibre Connectivity Interface data: Unselected

SVDB Directory: svdb

</div>

9. Run LVS.

> **Note**   If you get a message box asking to overwrite layout file, lab9_trace.gds, cancel the message box and return to the **Input** Menu button/**Layout** tab. Make sure **Import layout database from layout viewer** is <u>unselected</u>, then try running LVS again.

What are your results?

_____

10. Close all RVE and LVS Report windows.

Now you want to check the design a little more closely. In simulation runs, several properties were found to be critical for correct operation. You are going to write rules to allow you to check (trace) these properties. Before you start, you will need to review the source netlist to find the correct parameters.

The source netlist is re-created here for easier discussion.

```
* SPICE NETLIST
*************************************

.SUBCKT lab9_trace
** N=10 EP=0 IP=0 FDC=7
M0 2 7 VSS VSS n L=1.1e-05 W=1.3e-05 $X=27000 $Y=142000
M1 VDD 7 2 VDD p L=1.1e-05 W=1.3e-05 $X=67000 $Y=73000
R2 VSS 10 40000 $[pl] $X=215000 $Y=128000
R3 VSS 4 35.4412 $[dp] $X=208000 $Y=185000
R4 VSS 6 13.551 $[dn] $X=208000 $Y=73000
C5 9 VSS 3.00e-13 $[nmos] $X=137000 $Y=143000
C6 8 VSS 1.91e-13 $[pmos] $X=137000 $Y=73000
.ENDS
*************************************
```

What are the three component types in the design?

_____

_____

_____

What are the component subtypes for the Resistors?

_____

What are the component subtypes for the Capacitors?

_____

How many different types of Mosfets are in this subcircuit?

_____

Are these Mosfet subtypes or types?
(You need to know the difference for the PROPERTY TRACE syntax.)
(HINT: Mosfets are treated differently syntactically in the SPICE netlist and rule file DEVICE statements.)

_____

What are the component types for the NMOS and PMOS transistors?
(Hint: Check the lecture notes!)

_____

Now you are ready to write some TRACE PROPERTY statements. Use the lecture notes and the *SVRF Manual* if you need help with the syntax.

11. Write a statement comparing the NMOS widths in the Source and Layout.

    Answer:

    _____

    What is the tolerance in the above rule statement?

    _____

12. Be a little generous and change the rule statement to include a tolerance of 2%.

    Answer:

    _____

13. Write a rule to compare the NMOS lengths and flag any 2% difference between the Source and the Layout.

    Answer:

    _____

14. Write a rule to compare the resistance of the resistors in the source and layout, flagging any difference greater than 5%.

    Answer:

    _____

15. Change the above rule so only the poly (pl) resistors are checked.

    Answer:

    _____

16. Write a rule that flags 5% tolerance of the capacitance for the NMOS (nmos) capacitors.

    Answer:

    _____

17. Open the rule file, lab9_trace_rules, for editing.

18. Add these four additional rule statements to the rule file.

19. Save the rule file.

20. Run LVS again.

    What are your results?

    _____

    What component has the error?

    _____

    It is beyond the scope of this class to fix this error.

21. If you like, you may experiment tracing various properties with different tolerances.

22. You may also experiment with the design from the previous exercise.

23. When you are done, erase all highlights.

24. Close all Calibre related windows. (Including DESIGNrev, Calibre Interactive LVS, RVE, Netlist windows, and Summary Report.)

Module 10
Additional Topics

Objectives

At the completion of this lecture and lab you should be able to:

- Use Calibre to identify antenna problems

- Create custom output from Calibre

- Perform Layout vs. Layout comparisons

What is an Antenna?

What Is an Antenna?

♦ **During the fabrication process, metal and poly interconnect paths can act like antennas and build up electrical charge.**

♦ **Charges of sufficient magnitude may find a path to ground by arcing from poly through the oxide layer to the well in a gate region, thereby damaging or destroying the gate.**
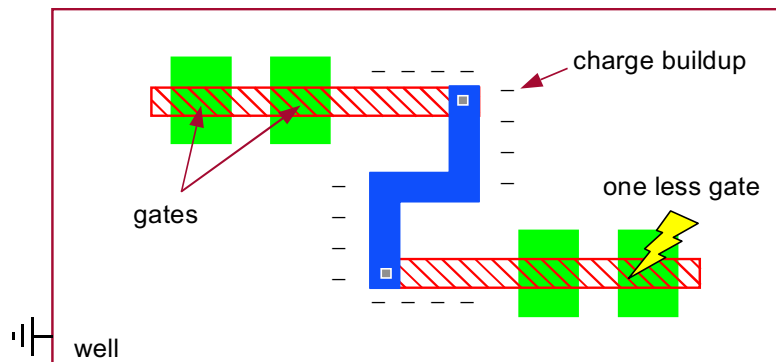
Notes:

Antenna Rule Basics

Antenna Rule Basics

♦ **Antenna rules identify Layout nets with a significant potential to exhibit antenna-related gate damage**

♦ **The ratio of antenna area to gate area (known as the Net Area Ratio, or NAR) serves as a good predictor of damage potential**

♦ **Antenna rules flag nets with NAR's that exceed a specific value:**

$$\frac{area}{area} < \text{antenna ratio}$$

gate area
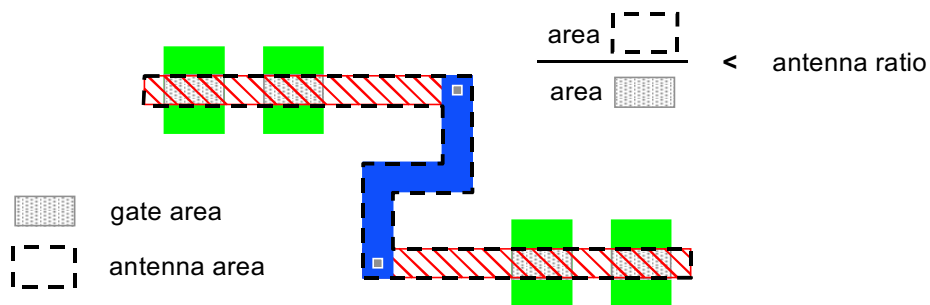
antenna area

Notes:

How to Find Net Area Ratio

How to Find Net Area Ratio

- **Use the NET AREA RATIO statement to find potentially "bad" antennas:**

  NET AREA RATIO *layer1 … layern dlayer > value*

- **NET AREA RATIO performs these steps:**
  - **Sums the area of all *layer1 - layern* shapes on the same net (numerator)**
  - **Sums the area of all *dlayer* shapes connected to that net (denominator)**
  - **Computes the ratio of the numerator divided by the denominator (NAR)**
  - **Outputs copies of all *layer1* shapes belonging to nets with a NAR greater than the specified value**
- **Output can be viewed just like any regular DRC result**
- **Consult the SVRF manual for additional NET AREA RATIO options**

Notes:

Antenna Rule Example

Antenna Rule Example

♦ **This simple antenna rule considers shapes on three layers of interconnect (poly, metal1, & metal2):**

```
antenna_level2 {
@Ratio of area of poly+metal1+metal2 on same net
@to area of gates formed by poly must be =< 50
  gate = poly and oxide
  x = net area ratio metal1 metal2 poly gate > 50
  y = net area ratio poly metal1 metal2 gate > 50
  z = net area ratio metal2 poly metal1 gate > 50
  (x or y) or z
}
```

♦ **NET AREA RATIO statement used three times to produce DRC output on all three interconnect layers (remember that only shapes from the first layer are copied to the output).**

♦ **Use RVE to highlight antenna rule results in the layout ...**

Notes:

In the example x, y, and z are derived layers.

The last line (x or y) or z outputs the derived layer.

Side Note: Gate is most likely defined as a derived layer in some other part of the rule file. This is not a problem, because gate in used within the rule it is only a local variable.

Additional Antenna Considerations (Cont.)

Antenna Rule Example (Cont.)

Notes:

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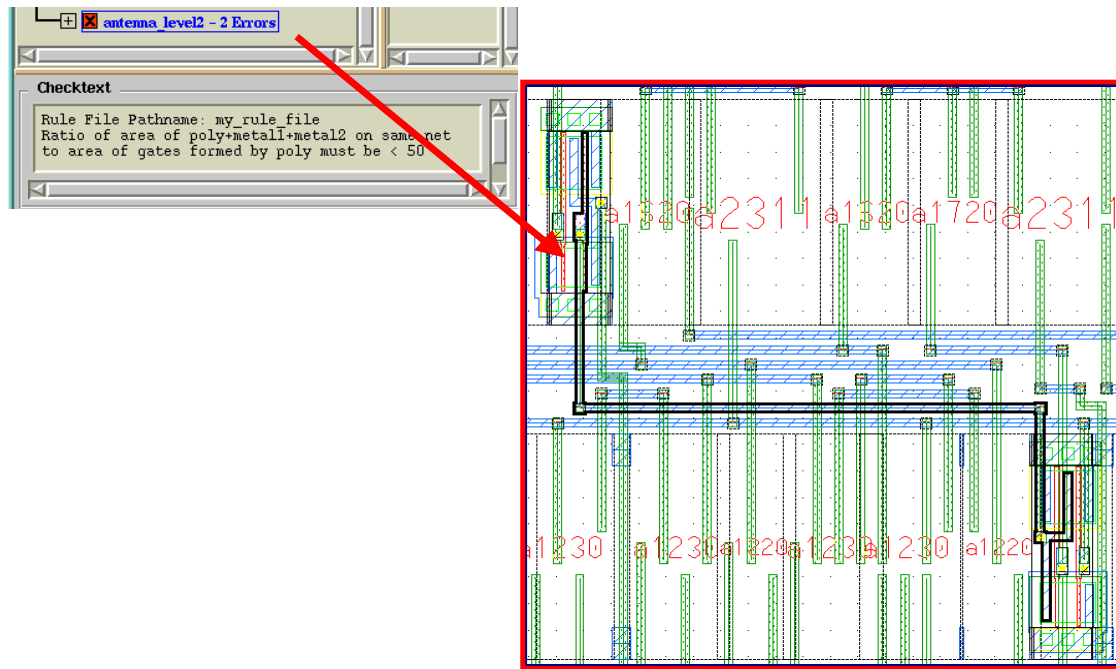
Additional Antenna Considerations

Additional Antenna Considerations

As interconnect layers are added to the chip, antenna nets grow and antenna-specific gate area changes:
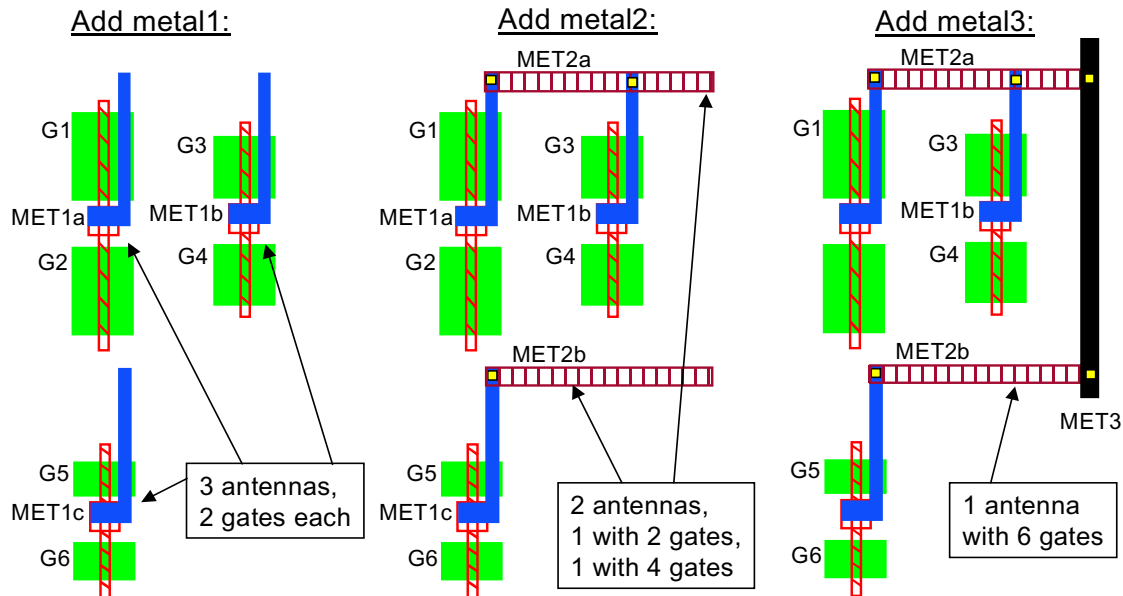
Add metal1:

Add metal2:

Add metal3:

3 antennas, 2 gates each

2 antennas, 1 with 2 gates, 1 with 4 gates

1 antenna with 6 gates

2

Notes:

Additional Antenna Considerations (Cont.)

Additional Antenna Considerations (Cont.)

♦ **A single rule that looks at all interconnect layers at once can be too simplistic**

♦ **Specific SVRF features address the antenna build-up issue**
- **Incremental connectivity specification**
- **Accumulate ratios from multiple NET AREA RATIO statements**

♦ **Consult the *SVRF Manual* and SupportNet Application Notes for additional information**

Notes:

How Can Calibre Produce Custom Output

How Can Calibre Produce Custom Output

The following slides present useful output options:

- ◆ **Creating GDSII output from Calibre**

- ◆ **Writing all shapes from one layer to a GDSII file**

- ◆ **Writing all shapes from one net to a GDSII file**

Notes:

Generating GDSII Output from Calibre

Generating GDSII Output from Calibre

♦ **Normally, Calibre writes DRC results to an ASCII file for subsequent display with RVE**

♦ **Alternately, you can instruct Calibre to write DRC results to a specific file in GDSII format**

♦ **Specify the output on a per-rulecheck basis via the DRC CHECK MAP statement:**

> **DRC CHECK MAP** *rule_check* **GDSII** *layer datatype filename*

♦ **Provide a DRC CHECK MAP statement for every rule if the DRC RESULTS DATABASE statement specifies GDSII as the format for all DRC output**

♦ **Additional DRC CHECK MAP options are available — consult the *SVRF Manual***

Notes:

Examples: Generating GDSII Output from Calibre

Examples: Generating GDSII Output from Calibre

- **Example 1:**

  "Grow all metal1 by 0.1u and save the result as GDS data."

  Grow_Metal1 {@ Grow metal1 by 0.1u

              SIZE metal1 BY 0.1

              }

  DRC CHECK MAP Grow_Metal1 GDSII 21 0 "./mask/grown_m1.gds"

- **Example 2:**

  "Output all metal shapes in net 'RESET' for a GDS plot."

  LAYER metal metal1 metal2 metal3 //Define layer set "metal"

  Plot_RESET {@Output all metal shapes belonging to the RESET net

              NET metal RESET

              }

  DRC CHECK MAP Plot_RESET GDSII 1 0 "./plots/RESET.gds"

Notes:

How to Compare Two Layout Versions

How to Compare Two Layout Versions

The next several slides will discuss Calibre's dual database capabilities:

♦ **Dual database overview**
♦ **Specifying the second layout database**
♦ **Bumping layer numbers from the second database**
♦ **Reconciling cell name changes between layout versions**

Notes:

Dual Database Capabilities

Dual Database Capabilities

- ◆ **Calibre has the capability to compare two separate layout databases**
- ◆ **This is known as "Layout vs. Layout" or "LVL"**

- ◆ **LVL comparison requires the following specification statements to be included in the rule file:**
  - ● **LAYOUT SYSTEM2**
  - ● **LAYOUT PATH2**
  - ● **LAYOUT PRIMARY2**
  - ● **LAYOUT BUMP2**

Notes:

LVL Comparison

LVL Comparison

♦ **Use LAYOUT SYSTEM, LAYOUT PATH, and LAYOUT PRIMARY statements (or use the GUI fields) in the usual way to specify the first layout**

♦ **Use LAYOUT SYSTEM2, LAYOUT PATH2 and LAYOUT PRIMARY2 statements to specify the second layout**

♦ **Use LAYOUT BUMP2 to specify an increment for all layout2 layer numbers (see next slide)**

♦ **Use LAYOUT RENAME CELL to map corresponding cells to the same name (if cell names change between layout versions):**

LAYOUT RENAME CELL *source_cell target_cell*

source cell: the cell name in the layout database
target_cell: the new cell name to be assigned as the layout data is read in

---

Notes:

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Example: LAYOUT BUMP2

Example: LAYOUT BUMP2

//DATABASE 1 LAYERS

LAYER POLY   1
LAYER OXIDE   2
LAYER CONTACT 3
.
.
.
LAYER VIA5   31

//DATABASE 2 LAYERS

LAYER POLY   1
LAYER OXIDE   2
LAYER CONTACT 3
.
.
.
LAYER VIA5   31

♦ **Use LAYOUT BUMP2 to increment all layout2 layer numbers by 100:**

  LAYOUT BUMP2 100

♦ **To compare the POLY layer data use XOR:**

  XOR 1 101

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10-15

Sample LVL Rule File

Sample LVL Rule File

Here is a sample Rule file for doing an LVL comparison:

```
LAYOUT SYSTEM GDSII
LAYOUT PATH "./my_chip_v1.gds"
LAYOUT PRIMARY my_chip

LAYOUT SYSTEM2 GDSII
LAYOUT PATH2 "./my_chip_v2.gds"
LAYOUT PRIMARY2 my_chip
LAYOUT BUMP2 100

DRC RESULTS DATABASE "./my_chip_diff"
DRC SUMMARY REPORT "./my_chip_rpt"

diff_my_chip_m1 {   @Compare metal1 masks for versions 1 & 2
                    @Metal 1 is layer 20
          XOR 20 120
}
// File golden_rules defines all layer mapping
INCLUDE "/data/golden_rules"
```

Notes:

Lab Information

Lab Information

In this lab you will:

♦ **Use Calibre to identify an antenna problem in an existing Layout**

♦ **Modify a rule file to output several GDSII files**

♦ **View the generated GDSII files in the Layout viewer**

♦ **Perform a LVL comparison on two versions of a Layout**

Notes:

Lab: Additional Topics

Introduction

This lab will take you through three unique scenarios, each representing situations often encountered in chip verification. The first exercise will give you the opportunity to enhance an antenna rule to more clearly see the "bad" antennas. The second exercise will guide you through the process of creating a GDS plot file using Calibre SVRF capabilities. Finally, the third exercise will demonstrate how you can use Calibre's Layout vs. Layout feature to display layout differences found when comparing two versions of the layout.

List of Exercises

Exercise 10-1: Improving Antenna Rules

Exercise 10-2: Create A GDSII Plot File

Exercise 10-3: Run A Layout vs. Layout Check

Exercise 10-1: Improving Antenna Rules

You've just been asked to check a design for antenna problems. Since you haven't done this before, your manager has given you a rule file that was left behind by your predecessor. You've been assured that this rule file will find "bad" antennas. Let's take a look.

1. From a UNIX shell, change your directory to "lab10".

   ```
   cd $HOME/using_calbr/lab10
   ```

2. List the contents of the lab10 directory.

   You should see at a minimum the following eight files:

   - lab10.gds

   - lab10_rev1.gds

   - lab10a_rules

   - lab10b_rules

   - lab10c_rules

   - golden_rules

   - lab10_runset.txt

   - layer_props.txt

   If any of these files are missing, please double check that you are in the correct directory, and then notify your instructor.

3. Launch DESIGNrev.

   ```
   $MGC_HOME/bin/calibredrv
   ```

   Now you will load the GSDII file.

4. Choose **Menu: File > Open Layout**.

5. Select file **lab10.gds**.

6. Choose **OPEN**.

   This loads the layout design you will be using for this exercise.

7. Load the layer properties file, layer_props.txt.
   (**Menu: Layer > Load Layer Properties**)

   The DESIGNrev window should look similar to below.
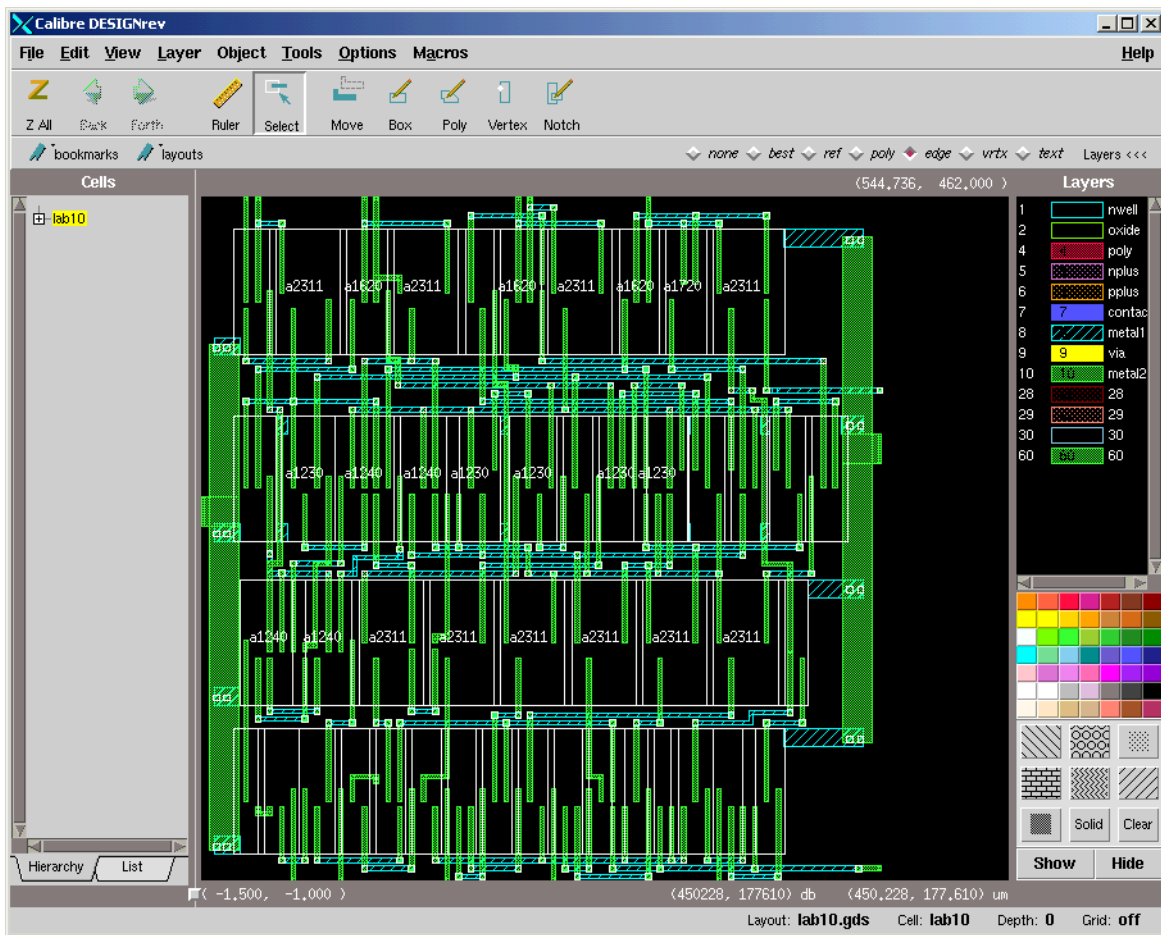
8. From DESIGNrev, choose **Menu: Tools > Calibre Interactive**.

   This opens the Calibre Interactive Server dialog box.

9. In the dialog box, select **Calibre DRC**.

10. Leave the socket as the default number (unless the instructor tells you otherwise).

11. Check that the cell name is "lab10".

12. Choose **Run** to execute the dialog box.

    Both the "Calibre Interactive - DRC" and "Choose Runset File" windows open.

13. Enter lab10_runset.txt as the runset file.
    (You can use the "..." browser to locate the file name).

14. Choose **OK** to execute the dialog box.
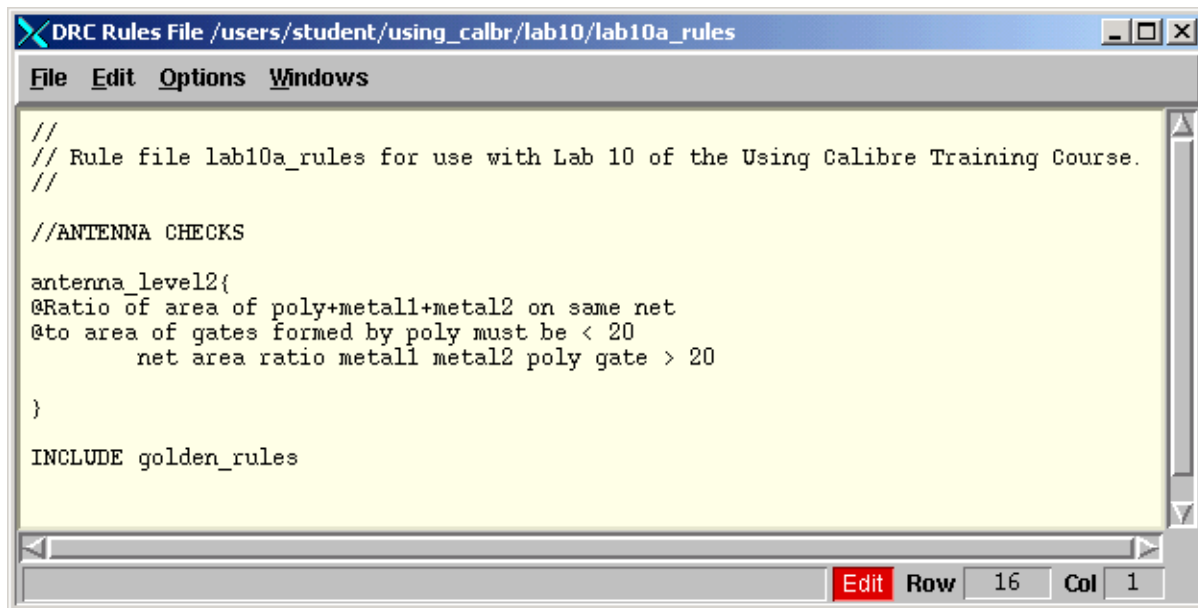
    The Calibre Interactive DRC window opens with the Inputs menu button selected. We will now take a closer look at the rule file.

15. Click on the **Rules** menu button.

    This will display the Rules frame in the Calibre Interactive window. File "lab10a_rules" should already be specified in the "Calibre-DRC Rules File" field (if not, use the browser to select the file).

16. Choose **View**.

This will open a text window displaying the lab10a_rules file:

```
DRC Rules File /users/student/using_calbr/lab10/lab10a_rules          _ □ ×

File  Edit  Options  Windows

//
// Rule file lab10a_rules for use with Lab 10 of the Using Calibre Training Course.
//

//ANTENNA CHECKS

antenna_level2{
@Ratio of area of poly+metal1+metal2 on same net
@to area of gates formed by poly must be < 20
        net area ratio metal1 metal2 poly gate > 20

}

INCLUDE golden_rules

                                                          Edit  Row   16   Col   1
```

Study the rule file carefully to answer the following questions:

Which layers can contribute shapes to antenna nets?

_____

What information would you expect to find in the golden_rules file?

_____

17. Choose **Menu: File > Close** to close the text window.

18. In the Calibre Interactive DRC window, Choose the **Inputs** menu button.

19. If it is selected, unselect the **Import layout database from layout viewer** option button.

The Calibre window should look similar to below:
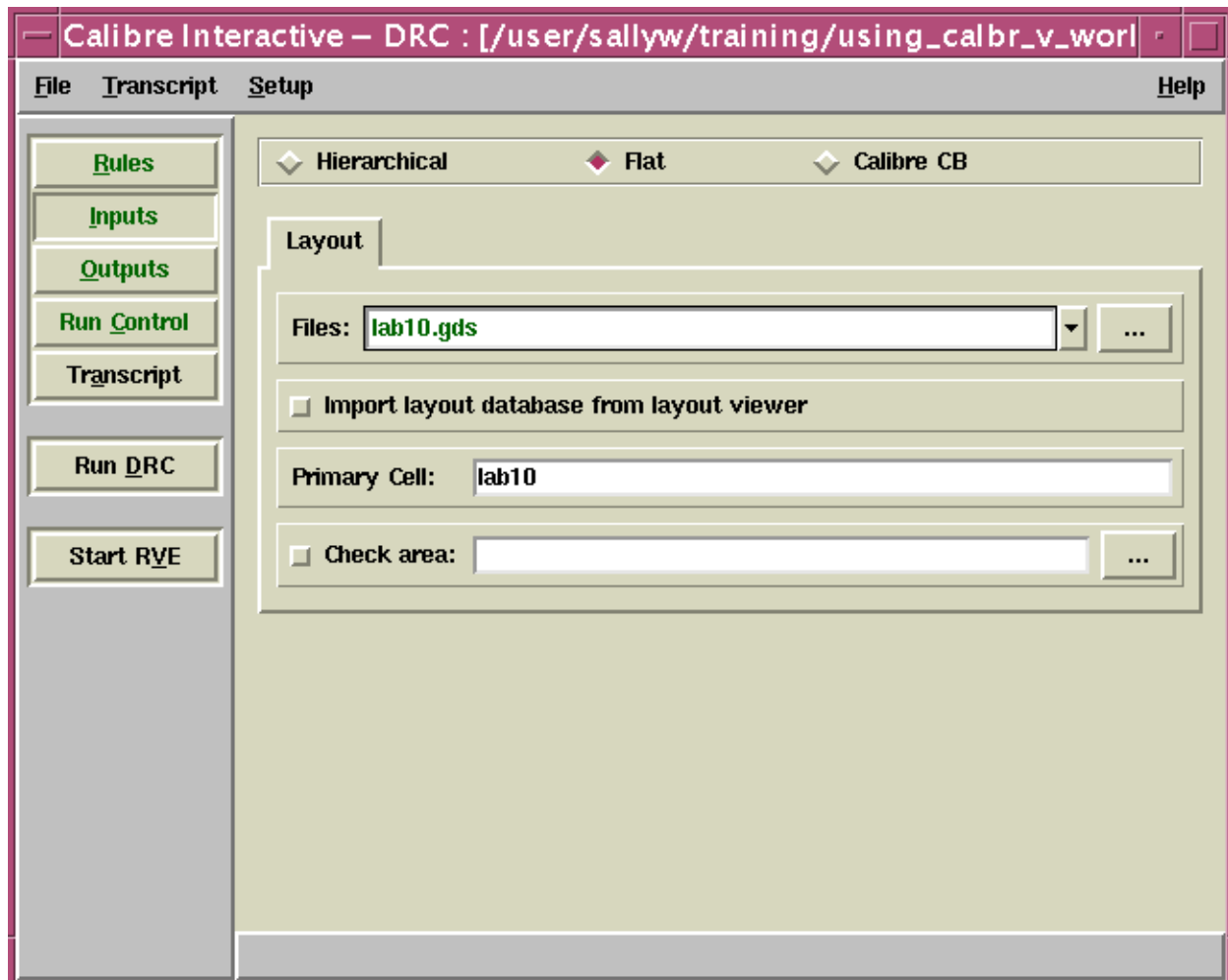
20. Choose the **Run DRC** Menu button.

> **Note**
> If you get a message box asking to overwrite layout file, lab10.gds, cancel the message box and return to the **Input** Menu button/**Layout** tab. Make sure **Import layout database from layout viewer** is <u>unselected</u>, then try running DRC again.

At the completion of the DRC run the Calibre RVE window will appear.

21. Expand the error tree display in the RVE window to show the list of six antenna rule results and select result number 01.

The RVE window should look similar to below:
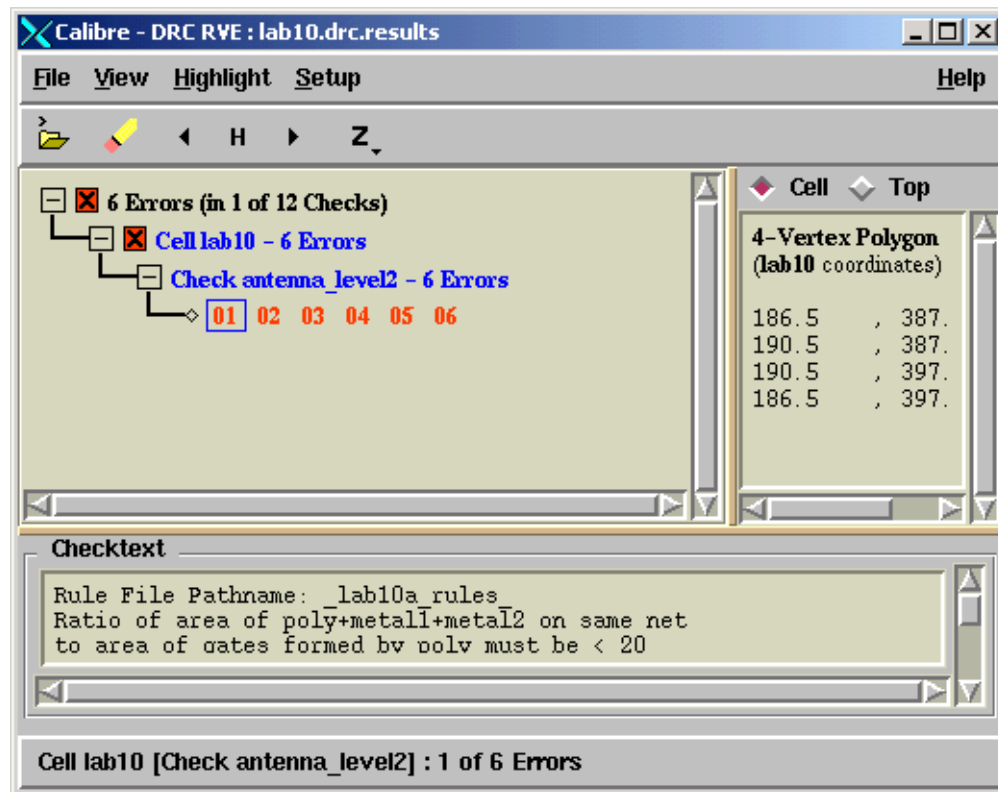
22. In the RVE window, select **Menu: Setup > Options**.

23. In the RVE Options window choose the **Highlight** tab.

24. Select option "**Zoom cell view to highlights by:**".

25. Enter **0.9** as the zoom factor.

26. Choose **OK** to execute the dialog box.

27. Position the RVE and Calibre DRC windows so that you can clearly see the layout (you may want to minimize the DRC window for now).

28. In the RVE window select **Menu: Highlight > Highlight All**.

This will highlight shapes in the layout belonging to "bad" antennas. The DESIGNrev window should look similar to below:

How many bad antennas have been identified?

_____
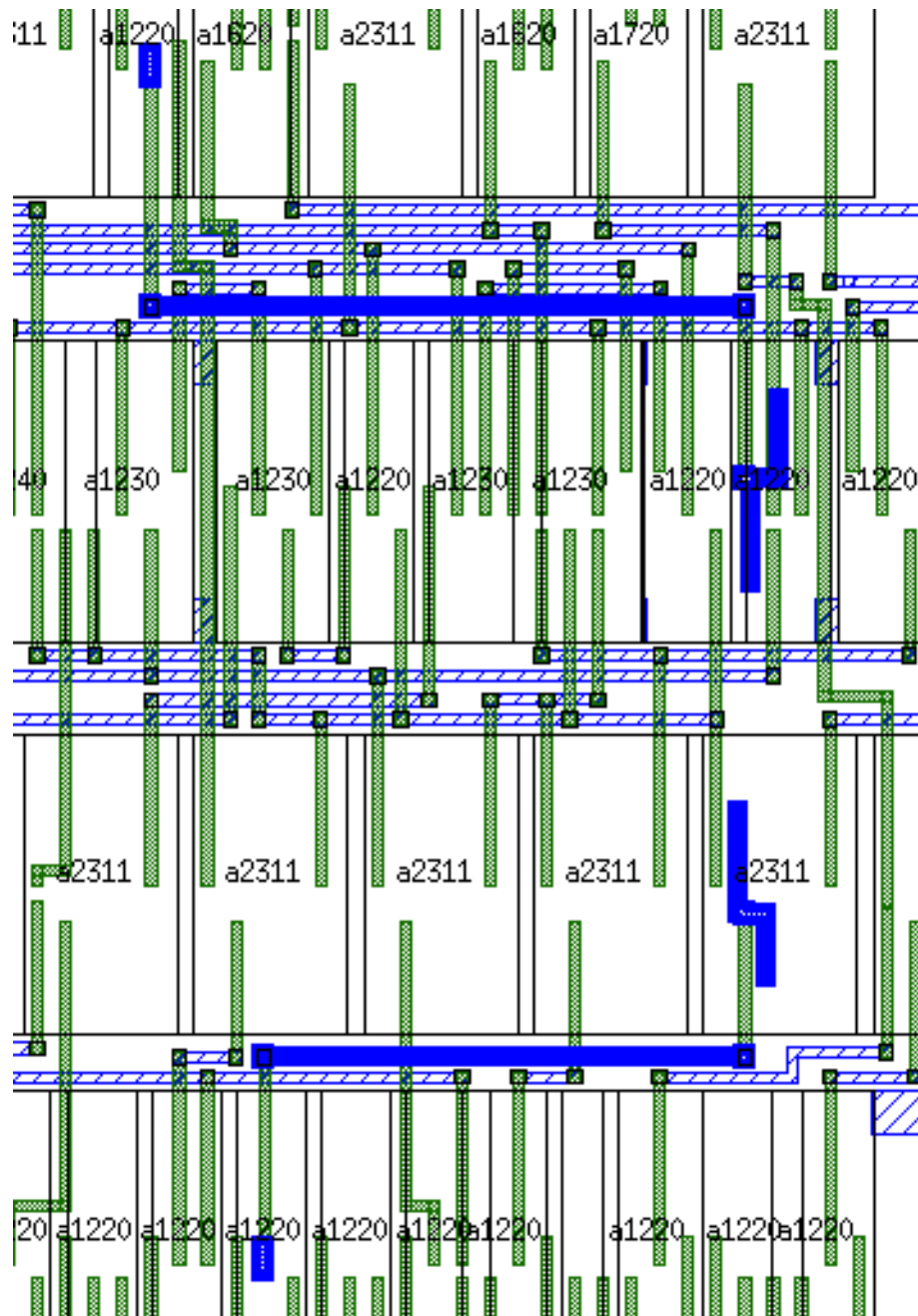
How could you improve the results to better see the antennas?

_____

29. Choose the **Eraser** icon in the RVE window to clear all highlights.

30. Close RVE.

31. In the Calibre window, select the **Rules** Menu button

32. Choose **View** next to the rule file name.

33. Take a good look at the antenna rule.

    Which layer(s) will be highlighted by this rule?

    _____

    Let's improve our antenna rule so that it highlights shapes from all three antenna net layers, poly, metal1 and metal2.

34. Click on the red **Edit** button at the bottom of the text edit window.

    The button will turn green, indicating that the rule file may now be edited.

35. Edit the antenna rule so that antenna shapes on the poly and metal2 layers will be highlighted in addition to metal1 shapes (Hint: refer to the antenna rule example in the lecture notes).

36. In the text edit window, choose **Menu: File > Save** to save your changes.

37. Choose **Menu: File > Close** in the text edit window.

38. In the Calibre DRC window, choose the **Load** button next to the rule file name field.

    If there are any errors in your modified rule file, an error dialog will give you information to help you find the problem. If there are problems, use the View button to again edit the rule file and correct any errors you find; load

the rule file after correcting any errors. If you still get load errors, ask the instructor for help.

39. Re-run DRC.

40. Highlight all of the errors.

   What do you see highlighted now?

   _____

If you modified the antenna rule correctly, you should now see this display:
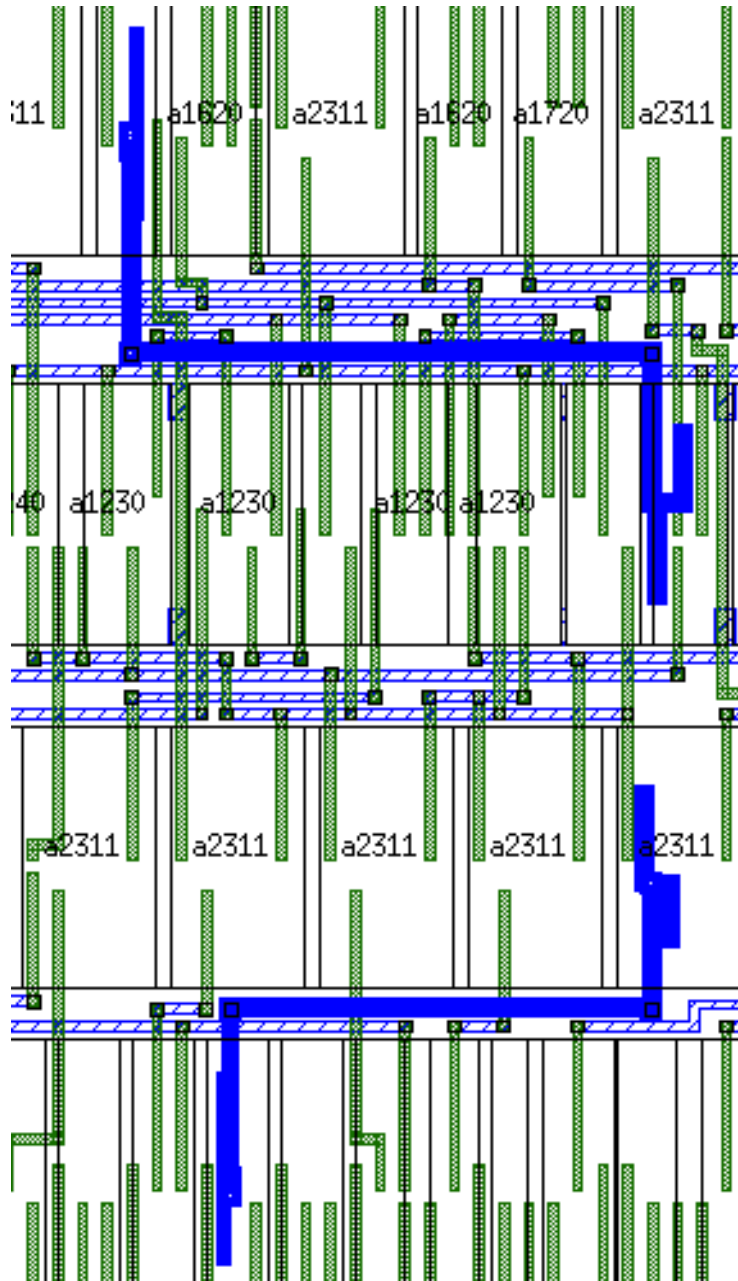
Congratulations! You have made the antenna nets more visible by adding the poly and metal2 shapes to your highlighted display.

41. Choose the **Eraser** icon in the RVE window to clear all highlights.

42. Close the RVE window.

43. Close the rule file.
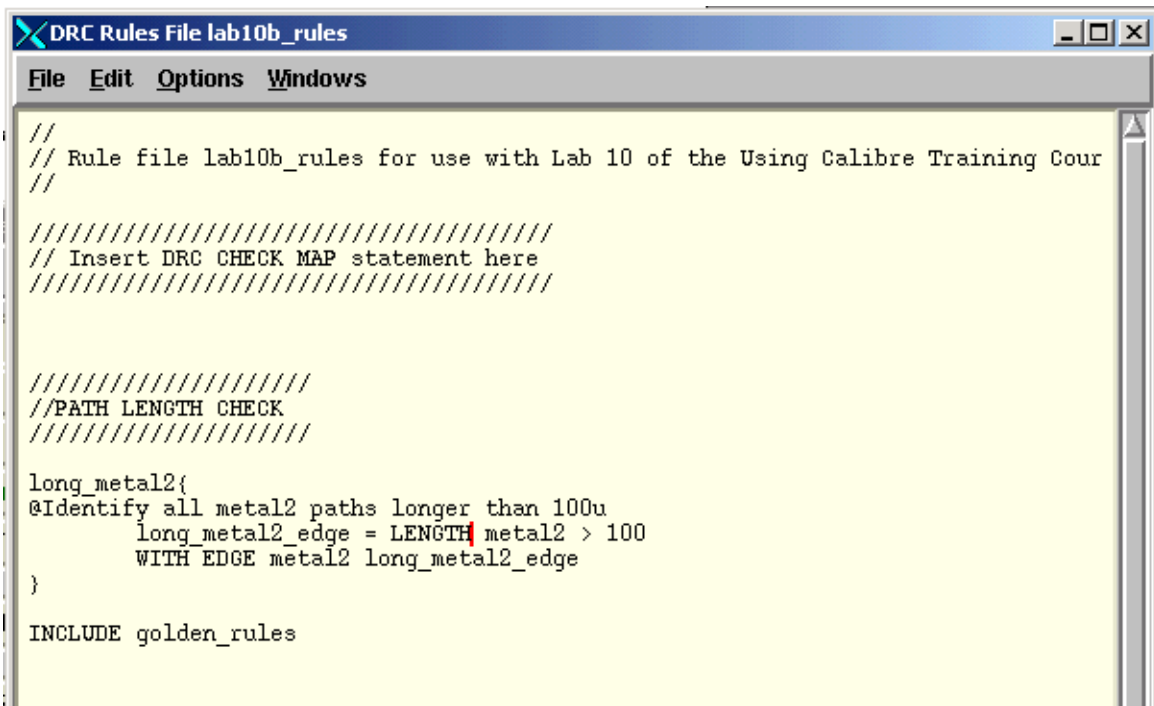
    Leave Calibre Interactive and the layout editor running.

Exercise 10-2: Create A GDSII Plot File

You've just finished the layout for a new chip and the design engineer has come over to take a look. The designer is concerned that some metal2 nets may be longer than current design standards allow. The designer asks you to highlight all metal2 nets that are over 100 microns long. Let's do it.

1. In Calibre Interactive DRC, choose the **Rules** Menu button.

2. Use the browser to select file **lab10b_rules**.

3. Choose **View** to see the rule file.

   A text edit window opens containing the rule file:

```
DRC Rules File lab10b_rules                                    _ □ ×

File  Edit  Options  Windows

//
// Rule file lab10b_rules for use with Lab 10 of the Using Calibre Training Cour
//

/////////////////////////////////////////
// Insert DRC CHECK MAP statement here
/////////////////////////////////////////



//////////////////////
//PATH LENGTH CHECK
//////////////////////

long_metal2{
@Identify all metal2 paths longer than 100u
        long_metal2_edge = LENGTH metal2 > 100
        WITH EDGE metal2 long_metal2_edge
}

INCLUDE golden_rules
```

   Study the "long_metal2" rule. The LENGTH statement creates a derived edge layer containing all metal2 edges longer than 100u. The WITH EDGE statement highlights all metal2 shapes which contain edges found in the derived edge layer generated in the LENGTH statement.

4. Close the text edit window when you are finished studying the rule file.

5. Choose **Load** to load the rule file.

> ⬜
> **Note**
>
> You must load the rule file to guarantee Calibre uses the correct rule file.

6. In the Calibre Interactive DRC window, choose the **Run DRC** Menu button.

7. When the DRC run completes and the RVE window opens, use RVE to highlight all of the long metal2 nets.

    The DESIGNrev display will now look similar to below
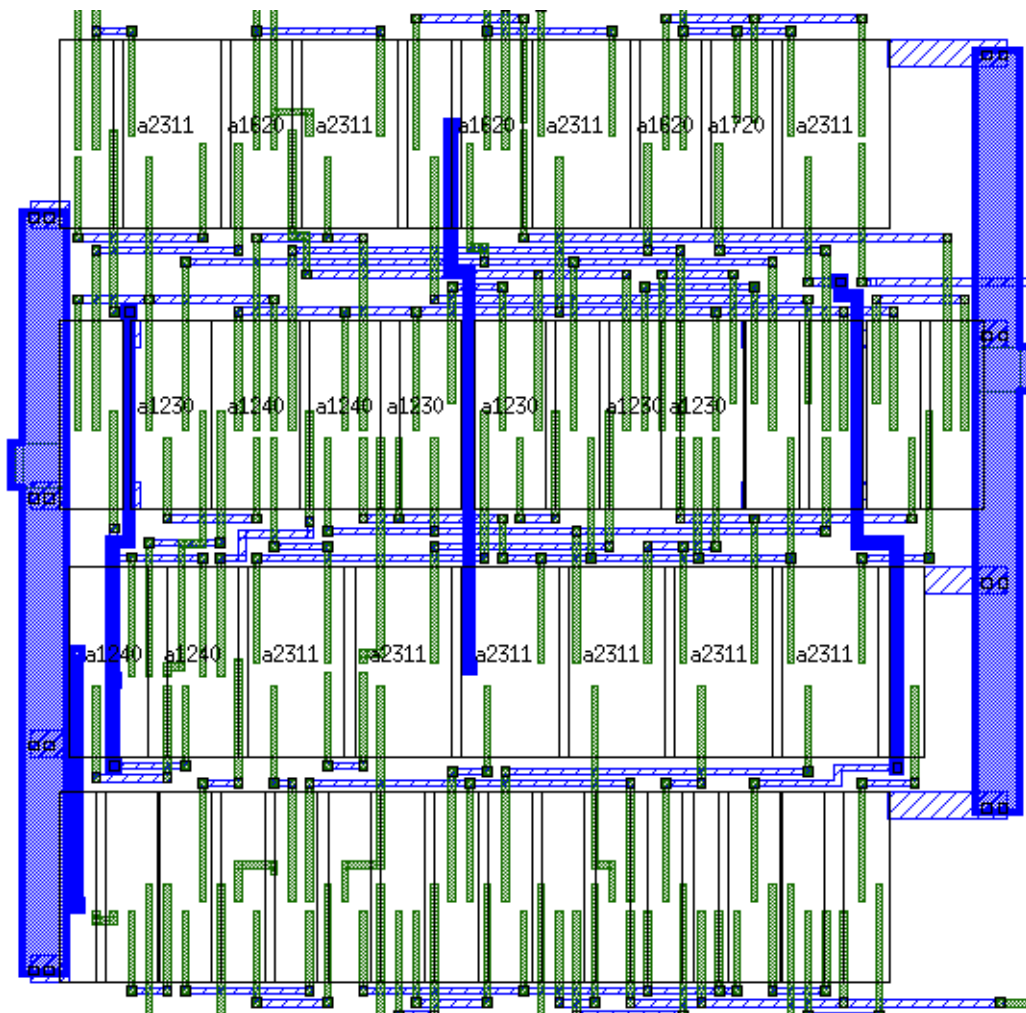
Having seen the highlighted long metal2 nets, the designer now asks you to produce a plot showing just those nets. How will you do this? One approach is to create a new GDS file that contains only the long metal2 shapes. This file can then be loaded into the layout viewer for plotting. It looks like we'll need to modify the rule file to generate the GDSII plot file.

8. Edit the rule file by adding a statement which will:

   o write all results from the long_metal2 rule to a GDSII file named "long_metal2.gds"

   o place the shapes on GDS layer 1

   o datatype 0

      (**Hint**: Refer to the lecture slide examples).

9. Erase all current highlights.

10. Close RVE.

11. Re-run DRC.

    If you correctly modified the rule file, the RVE window should now show no errors because the long metal2 results were written to the GDSII plot file instead of to the DRC results database. You can verify that the GDSII file was created either by listing the contents of the lab10 directory or by scrolling up in the DRC transcript until you see the message "Write to GDS Results Database ./long_metal2.gds COMPLETED." If you don't see evidence of the new GDSII file, review your rule file modifications and, if necessary, ask your instructor for help.

    Let's take a look at your new GDSII plot file.

12. In the DESIGNrev window, choose **Menu: File > Open Layout** to load the long_metal2.gds file.

The DESIGNrev window should look similar to below:
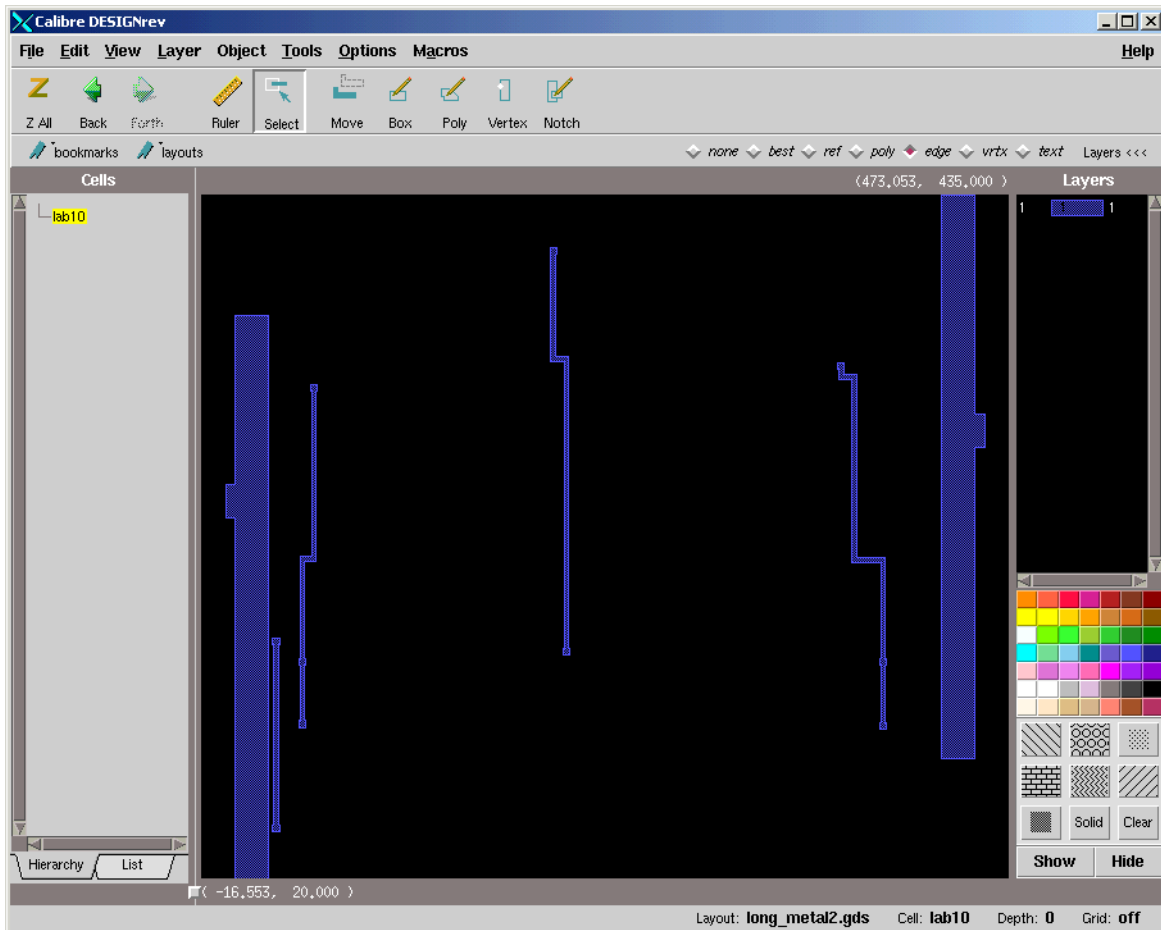
Congratulations! You now have a file which can be used to easily generate the requested plot.

13. Close the rule file (if it is still open).

14. When you are finished reviewing the plot data, close the RVE window but leave the Calibre Interactive DRC and DESIGNrev windows open and proceed to the next exercise.

Exercise 10-3: Run A Layout vs. Layout Check

You've just returned from working on another project to discover that a junior layout engineer was given the task of making several minor metal2 changes to your chip layout. Now you want to check the new version of the layout to insure that only the specified changes were made. This sounds like a perfect application for Calibre's Layout vs. Layout (LVL) capabilities, so let's try that.

1. Re-display the **lab10.gds** file into DESIGNrev by choosing the Back button in DESIGNrev.

2. In the Calibre Interactive DRC window, specify file **lab10c_rules** as the rule file.

3. Open file lab10c_rules for editing.

   Note that there are places in the rule file that have been reserved for inserting the layout2 specification statements and the XOR rule that will compare layout1 with layout2.

   Given that the revised GDS data is in file **lab10_rev1.gds**, the type of that file is **GDS** and the name of the top-level cell in that file is **lab10_rev1**, what three specification statements need to be added to the rule file for layout2?

   _____

   _____

   _____

4. Insert the necessary layout2 specification statements into the rule file.

   One more statement will be required to tell Calibre to add 100 to each layout2 shape layer value (the "bump" value). What does this statement look like?

   _____

5. Insert the "bump" statement into the rule file directly after the three layout2 specification statements.

    Now all you need is an actual statement to compare metal2 on the two versions of the layout.

    What will the statement look like (metal2 is on layer 10)?

    _____

6. Insert the needed layer compare statement into the diff_metal2 rule.

7. Save the rule file.

8. Load the rule file.

9. Run DRC.

10. In RVE, select **Menu: Highlight > Highlight All**.

If you modified the rule file correctly, your display should show seven highlighted areas indicating changes from the original data. The display should look similar to below. (The arrows indicate the highlighted shapes):
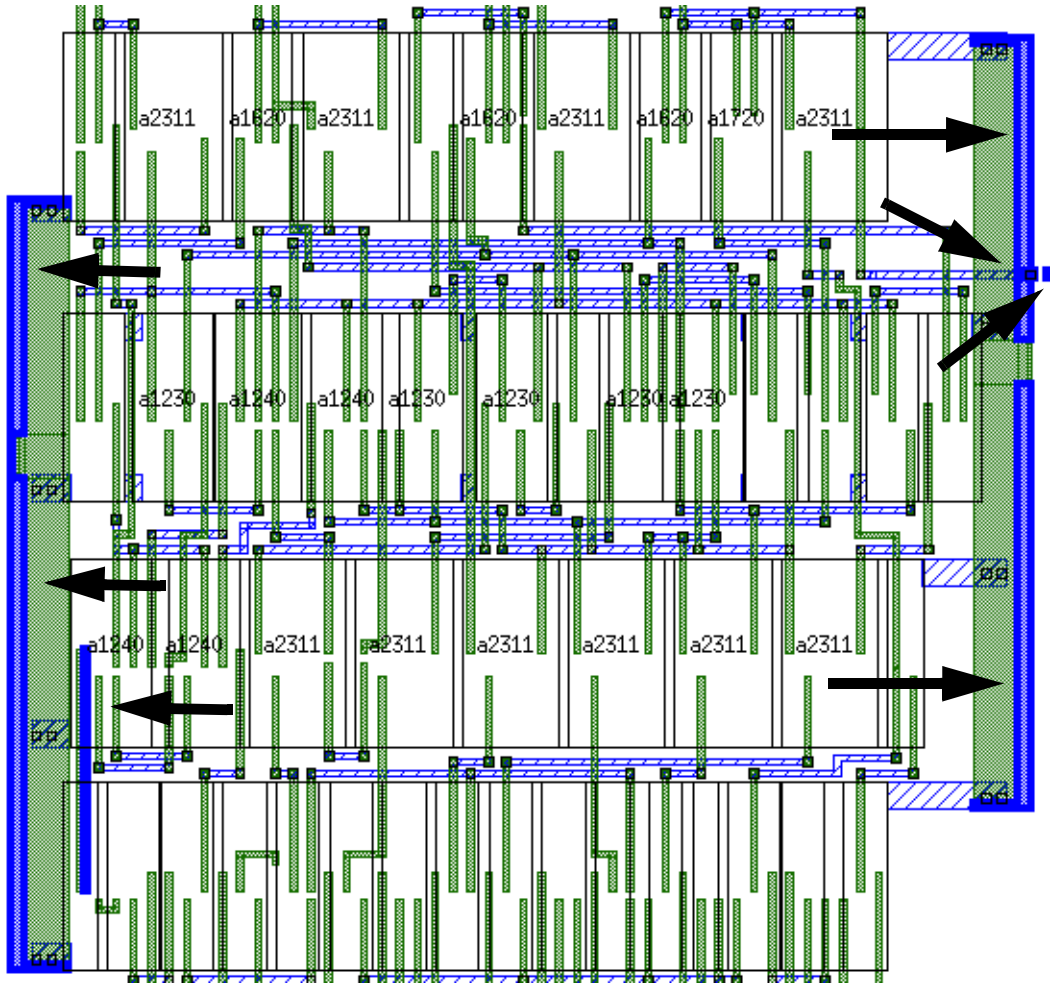
11. Experiment with different RVE viewing options to better study and visualize the metal2 changes which have been made.

When you are finished with this lab, close all Calibre related windows. (Including DESIGNrev, Calibre Interactive DRC, RVE, rule files, and Reports.)

Module 11
Command Line Calibre

Objectives

At the completion of this lecture and lab you should be able to:

- Launch Calibre Interactive from the command line

- Explain the three steps required for command line Calibre operation

- Edit the rule file for command line Calibre operation

- Invoke a Calibre command line DRC run

- Invoke a Calibre command line LVS run

- Read the various reports from the command line

How to Launch Calibre Interactive from the Command Line

How to Launch Calibre Interactive from the Command Line

- ◆ **Launch Calibre Interactive using the following:**

    $MGC_HOME/bin/calibre -gui

- ◆ **Displays the following:**

- ◆ **Choose a button to launch the desired Calibre Interactive**
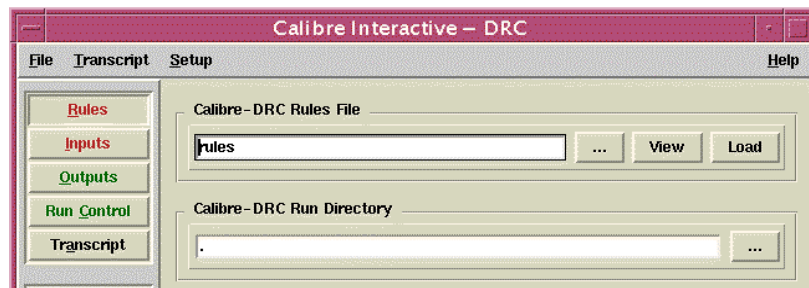
Notes:

How to Run Calibre Exclusively from the Command Line

How to Run Calibre Exclusively from the Command Line

- ♦ **Edit the rule file**

- ♦ **Invoke Calibre using the various option switches**

- ♦ **View the reports using a text editor**
  (or view results using RVE)

Notes:

Why do I Need to Edit the Rule File?

Why do I Need to Edit the Rule File?

♦ **Never want to edit the "golden" rule file!**

♦ **Define all the information that Calibre Interactive would normally supply:**

- **Input and output file names**

- **Layout file format**

- **Name of the top level cell**

- **Summary report name**

- **Results database name**

- **Other options**

♦ **Allows the rule file to be re-used consistently**

11-5 • Using Calibre: Command Line Calibre   Copyright © 2004 Mentor Graphics Corporation

Notes:

What Specifications are Required in the Rule File—All Calibre Runs

**What Specifications are Required in the Rule File—
All Calibre Runs**

- ◆ **LAYOUT SYSTEM**
  - ● **Specifies the layout data format**
- ◆ **LAYOUT PATH**
  - ● **Specifies the layout data location (filename)**
- ◆ **LAYOUT PRIMARY**
  - ● **Specifies the top-level cell within the layout data**
- ◆ **INCLUDE "golden_rules"**
  - ● **Specifies the "golden" rule file**
  - ● **This is "optional" — you can add all the custom information to your "golden" rule file**

Notes:

What Specifications are Required in the Rule File—Calibre DRC

What Specifications are Required in the Rule File—Calibre DRC

- ◆ **DRC RESULTS DATABASE**
  Specifies where to save the results

- ◆ **Other useful DRC specification statements (optional):**

  - ● **DRC SUMMARY REPORT**
    Specifies a filename for the DRC Summary Report

  - ● **DRC MAXIMUM RESULTS**
    Specifies the DRC RuleCheck maximum result count

  - ● **DRC SELECT CHECK**
    Specifies which RuleCheck statements will be initially selected when the rule file load

Notes:

Example: Rule File for DRC

Example: Rule File for DRC

// Use this Rule File for running DRC checks on the 4 bit adder design

LAYOUT SYSTEM gdsii
LAYOUT PATH "$HOME/layout_files/4_bit_adder.gds"
LAYOUT PRIMARY 4_bit_adder
DRC RESULTS DATABASE 4_bit_adder_drc_results
DRC SUMMARY REPORT 4_bit_drc_summary_report

// Include the factory "golden rules"

INCLUDE "$HOME/master_rules/factory/golden_rules"

Notes:

What Specifications are Required in the Rule File—Calibre LVS

What Specifications are Required in the Rule File—Calibre LVS

- ◆ **SOURCE SYSTEM**
  Specifies the source data format

- ◆ **SOURCE PATH**
  Specifies the source data path (filename)

- ◆ **SOURCE PRIMARY**
  Specifies the top-level cell within the source data

- ◆ **LVS REPORT**
  Specifies where to save the LVS Report

Notes:

What Specifications are Optional in the Rule File—LVS Calibre

What Specifications are Optional in the Rule File— LVS Calibre

Other useful LVS specification statements:

- **MASK SVDB DIRECTORY**

- **LVS ABORT ON SOFTCHK**

- **LVS ABORT ON SUPPLY ERROR**

- **LVS BOX**

- **LVS GROUND NAME**

- **LVS POWER NAME**

- **LVS ISOLATE SHORTS**

- **LVS RECOGNIZE GATES**

- **LVS REPORT MAXIMUM**

- **LVS SOFTCHK**

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Notes:

Example: Rule File for LVS

Example: Rule File for LVS

// Use this Rule File for running LVS checks on the 4 bit adder design

LAYOUT SYSTEM gdsii
LAYOUT PATH "$HOME/layout_files/4_bit_adder.gds"
LAYOUT PRIMARY 4_bit_adder
SOURCE SYSTEM spice
SOURCE PATH "$HOME/source_files/4_bit_adder.spi"
SOURCE PRIMARY 4_bit_adder
LVS REPORT 4_bit_adder_lvs_report
MASK SVDB DIRECTORY svdb

// Include the factory "golden rules"

INCLUDE "$HOME/master_rules/factory/golden_rules"

Notes:

How to Launch a Calibre DRC Run

How to Launch a Calibre DRC Run

♦ **Flat Calibre DRC run:**

  calibre -drc rule_file_name

♦ **Hierarchical Calibre DRC run:**

  calibre -drc -hier rule_file_name

Notes:

What Optional Command Line Switches are Available for Calibre DRC?

What Optional Command Line Switches are Available for Calibre DRC?

♦ **[-mergedatabase]**
This switch directs the GDSII reader to merge geometries on a per-cell, per-layer basis as it reads the stream into memory. Generally, you would use this only for databases created by module generator tools that redundantly place geometries on top of each other.

♦ **[-writedatabase]**
This switch translates a GDSII layout database into binary polygon format. Calibre performs no rule checking in this mode. (Flat runs only)

♦ **[-64]**
This switch invokes the 64-bit version of Calibre. When enough physical memory is available, this speeds up runs involving large data bases.

Notes:

What Optional Command Line Switches are Available for Calibre DRC? (Cont.)

♦ **[-nowait]**
This switch instructs the MGLS license queuing features to be
disabled. This results in Calibre exiting, instead of queuing for a
license, if one is not available.

♦ **[-turbo [** *no_of_cpus***]]**
This switch instructs Calibre DRC-H to use multi-threaded parallel
processing for all stages except Litho operations. The *no_of_cpus*
argument is a positive integer that specifies the number of CPUs to
use in the processing. If you do not specify a value, Calibre DRC-H
runs on the maximum number of CPUs available.

Notes:

How to Launch a Calibre LVS Run

How to Launch a Calibre LVS Run

- **Flat Calibre LVS run:**

  calibre -lvs rule_file_name   //comparison only run

- **Hierarchical Calibre LVS run:**

  calibre -lvs -hier rule_file_name   //comparison only run

- **Calibre LVS extraction only run:**

  calibre -spice layout.spice rule_file_name   // extraction only

- **Calibre LVS extraction and comparison run:**

  calibre -spice layout.spice -lvs -hier -auto rule_file_name
                                                     // extract and compare

Notes:

The first two examples assume that there already exists an extracted spice netlist for the layout.

What Optional Command Line Switches are Available for Calibre LVS?

♦ **[-automatch]**
This switch specifies automatic correspondence by name for cells in hierarchical LVS comparison.

♦ **[-spice** *spice_file_name***]**
This switch extracts a hierarchical Spice netlist from the layout system, which must be GDSII or CIF and directs output to *spice_file_name*. When you specify this option with -lvs, Calibre extracts a Spice netlist from the layout system and uses it in place of the original layout system for comparison against the source.

♦ **[-turbo [** *no_of_cpus***]]**
This switch instructs Calibre LVS-H to use multi-threaded parallel processing. The *no_of_cpus* argument is a positive integer that specifies the number of CPUs to use in the processing. If no value is specified, Calibre LVS-H runs on the maximum number of CPUs available.

Notes:

What Optional Command Line Switches are Available for Calibre LVS? (Cont.)

♦ **[-hcell** *cell_correspondence_file_name***]**
This switch specifies a cell correspondence file for hierarchical LVS comparison.

♦ **[-mergedatabase]**
This switch directs the GDSII reader to merge geometries on a per-cell, per-layer basis as it reads the stream into memory. Generally, you would use this only for databases created by module generator tools that redundantly place geometries on top of each other.

♦ **[-64]**
This switch invokes the 64-bit version of Calibre.

♦ **[-nowait]**
This switch instructs the MGLS license queuing features to be disabled. This results in Calibre exiting, instead of queuing for a license, if one is not available.

Notes:

What Optional Command Line Switches are Available for Calibre LVS? (Cont.)

What Command Line Switches are Available for Calibre LVS? (Cont.)

- **[-cs]**
  This switch instructs Calibre LVS to read and verify the Spice netlist specified in the Source Path specification statement. Calibre LVS issues any applicable warnings or errors, and also writes them to the LVS report.

- **[-cl]**
  This switch instructs Calibre LVS to read and verify the Spice netlist specified in the Layout Path specification statement. Calibre LVS issues any applicable warnings or errors, and also writes them to the LVS report.

- **Additional options are available for Flat LVS runs.**
  See the *Calibre User's Manual* for additional information.

Notes:

Saving the Transcript

Saving the Transcript

From the UNIX shell:

◆ **calibre - drc rule_file | tee ic.log**

   Runs in the foreground, spawn a background process to capture the transcript in the file ic.log

◆ **calibre -drc rule_file > ic.log &**

   Run calibre in the background, capture the transcript in the file ic.log

Notes:

How to View the Results

How to View the Results

♦ **Use any text editor to view the reports**

♦ **Use RVE to cross-probe results**

- **Use the results database files**

- **Invoke RVE from command line:**

  calibre -rve *results_database_file*

- **Invoke RVE from Calibre Interactive**

Notes:

Command Line Calibre DRC Example: Edit the Rule File

Command Line Calibre DRC Example: Edit the Rule File

```
Text Editor V3.6.1 build_21 [sundown] — lab4_rules (
File ▽    View ▽    Edit ▽    Find ▽

//
// Rule file for use with Lab 4 of the Using Calibre Training Course.
//

LAYOUT SYSTEM          GDS
LAYOUT PATH            "$MGC_WD/lab4/lab4.gds"
LAYOUT PRIMARY         lab4

DRC RESULTS DATABASE   "lab4_hier.db"
DRC SUMMARY REPORT     lab4_hier_report

INCLUDE "golden_rules"
```

Notes:

Using Calibre with DESIGNrev
June 2004
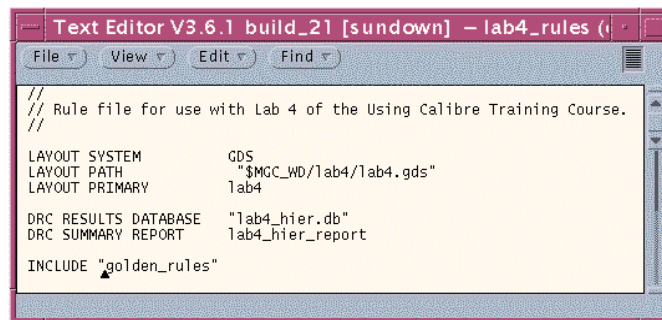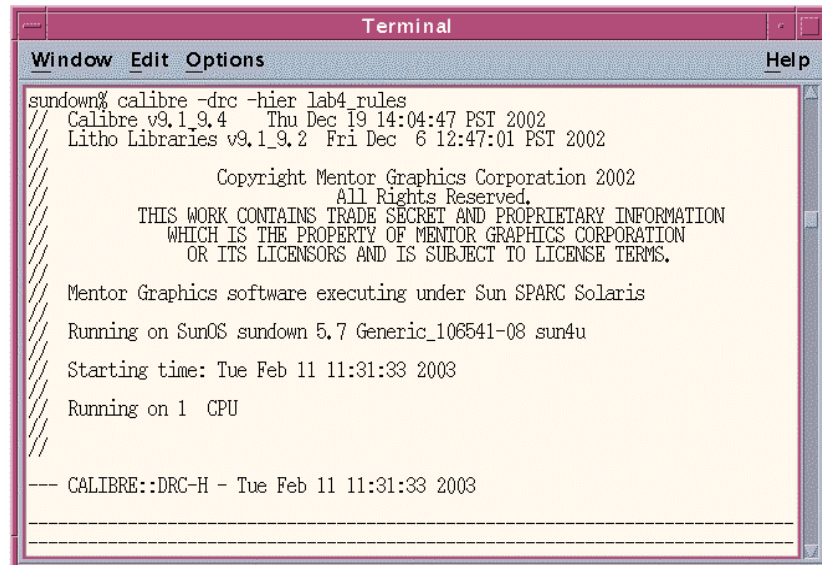
Command Line Calibre DRC Example: Launch Calibre

Command Line Calibre DRC Example: Launch Calibre

```
                            Terminal
Window  Edit  Options                              Help

sundown% calibre -drc -hier lab4_rules
// Calibre v9.1_9.4   Thu Dec 19 14:04:47 PST 2002
// Litho Libraries v9.1_9.2  Fri Dec  6 12:47:01 PST 2002

            Copyright Mentor Graphics Corporation 2002
                    All Rights Reserved.
        THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
            WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
                OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.

// Mentor Graphics software executing under Sun SPARC Solaris

// Running on SunOS sundown 5.7 Generic_106541-08 sun4u

// Starting time: Tue Feb 11 11:31:33 2003

// Running on 1  CPU
//

--- CALIBRE::DRC-H - Tue Feb 11 11:31:33 2003
```
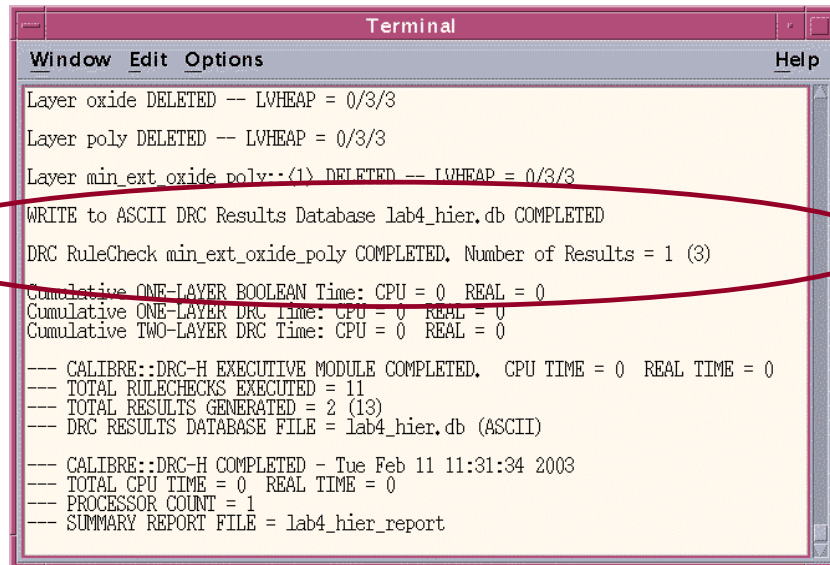
Notes:

Command Line Calibre DRC Example: Scan Transcript

Command Line Calibre DRC Example: Scan Transcript
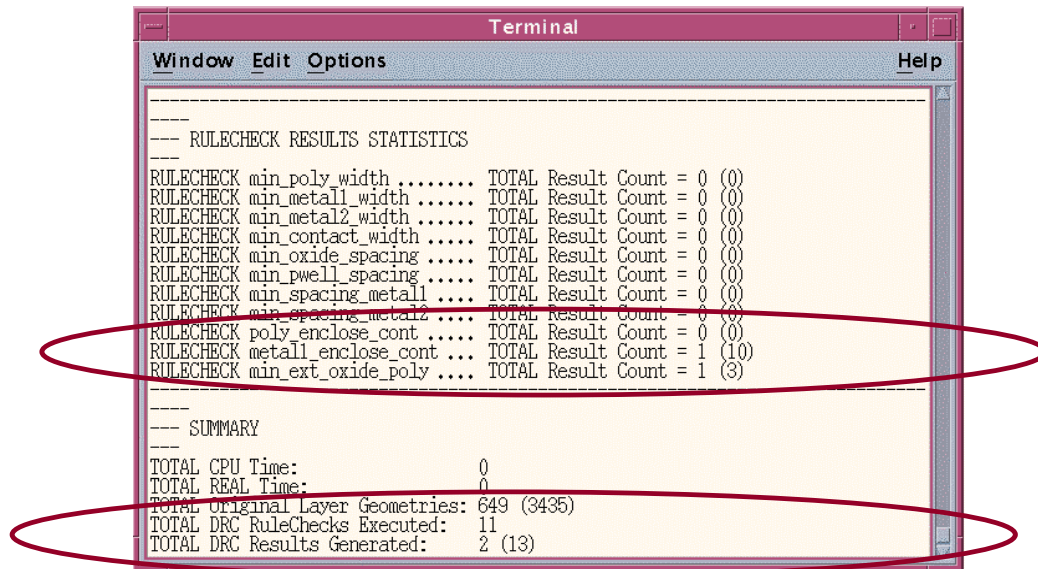

```
Terminal

Window  Edit  Options                                              Help

Layer oxide DELETED -- LVHEAP = 0/3/3

Layer poly DELETED -- LVHEAP = 0/3/3

Layer min_ext_oxide_poly::(1) DELETED -- LVHEAP = 0/3/3

WRITE to ASCII DRC Results Database lab4_hier.db COMPLETED

DRC RuleCheck min_ext_oxide_poly COMPLETED. Number of Results = 1 (3)

Cumulative ONE-LAYER BOOLEAN Time: CPU = 0   REAL = 0
Cumulative ONE-LAYER DRC Time: CPU = 0   REAL = 0
Cumulative TWO-LAYER DRC Time: CPU = 0   REAL = 0

--- CALIBRE::DRC-H EXECUTIVE MODULE COMPLETED.  CPU TIME = 0   REAL TIME = 0
--- TOTAL RULECHECKS EXECUTED = 11
--- TOTAL RESULTS GENERATED = 2 (13)
--- DRC RESULTS DATABASE FILE = lab4_hier.db (ASCII)

--- CALIBRE::DRC-H COMPLETED - Tue Feb 11 11:31:34 2003
--- TOTAL CPU TIME = 0   REAL TIME = 0
--- PROCESSOR COUNT = 1
--- SUMMARY REPORT FILE = lab4_hier_report
```

Notes:

Using Calibre with DESIGNrev
                                                         June 2004

Command Line Calibre DRC Example: View Report

Command Line Calibre DRC Example: View Report

```
-----------------------------------------------------------------------
----
--- RULECHECK RESULTS STATISTICS
---
RULECHECK min_poly_width ........ TOTAL Result Count = 0 (0)
RULECHECK min_metal1_width ...... TOTAL Result Count = 0 (0)
RULECHECK min_metal2_width ...... TOTAL Result Count = 0 (0)
RULECHECK min_contact_width ..... TOTAL Result Count = 0 (0)
RULECHECK min_oxide_spacing ..... TOTAL Result Count = 0 (0)
RULECHECK min_pwell_spacing ..... TOTAL Result Count = 0 (0)
RULECHECK min_spacing_metal1 .... TOTAL Result Count = 0 (0)
RULECHECK min_spacing_metal2 .... TOTAL Result Count = 0 (0)
RULECHECK poly_enclose_cont ..... TOTAL Result Count = 0 (0)
RULECHECK metal1_enclose_cont ... TOTAL Result Count = 1 (10)
RULECHECK min_ext_oxide_poly .... TOTAL Result Count = 1 (3)
-----------------------------------------------------------------------
----
--- SUMMARY
---
TOTAL CPU Time:                 0
TOTAL REAL Time:                0
TOTAL Original Layer Geometries: 649 (3435)
TOTAL DRC RuleChecks Executed:  11
TOTAL DRC Results Generated:    2 (13)
```

Notes:

Using Calibre with DESIGNrev
June 2004

Command Line Calibre DRC Example: Scan Results DB

Command Line Calibre DRC Example: Scan Results DB

Notes:

Command Line Calibre DRC Example: Load DB into RVE

Command Line Calibre DRC Example: Load DB into RVE

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Notes:

Lab Information

Lab Information

In this lab you will:

- ◆ **Edit Rule files**
- ◆ **Run Calibre DRC from the command line**
- ◆ **Run Calibre LVS from the command line**
- ◆ **View reports**
- ◆ **View results databases**
- ◆ **Launch RVE from the command line**

Notes:

Lab: Command Line Calibre

In this lab you will perform some of the same tasks as in previous labs only this time you will be working directly from the command line, without any type of GUI interface.

List of Exercises

Exercise 11-1: Command Line DRC Run

Exercise 11-2: Command Line LVS Run

Exercise 11-3: Command Line to Calibre Interactive

Exercise 11-1: Command Line DRC Run

In this lab, you will run Calibre DRC directly from the command line.

1. Change to the lab11 directory.
    ```
    cd $HOME/using_calbr/lab11
    ```

2. List the files in the directory.

    You should see the five files:

    *   golden_rules

    *   lab11_rule_results

    *   lab11_rules

    *   lab11a.gds

    *   lab11a_source.spi

    If any of these files are missing, please double check that you are in the correct directory, and then notify your instructor.

3. Using your favorite ASCII text editor, open the lab11_rules file for edits.

    What is currently in the file?

    _____

    This is the type of starting rule file that you have used for all the other labs. In this exercise, you need to add manually all the additional information that Calibre Interactive has been adding automatically.

What are the three Specification Statements that Calibre requires for all runs?

_____

_____

_____

4. Write each rule Specification Statement next for the descriptions below.

The layout data format is GDSII:

_____

The layout filename is lab11a.gds

_____

The primary cell in the layout is lab11a.

_____

5. Enter these commands in your rule file.

What is the command to specify the DRC results database filename?

_____

6. Enter this command into the rule file, using lab11_drc_results as the filename.

What is the command to create the DRC Summary Report?

_____

7. Enter this command into the rule file, using lab11_drc_summary as the file name.

8. Save the rule file.

You are almost ready to launch a Calibre DRC run. Before you start you need to know which option switches you will need.

What is the option switch for a DRC run?

_____

What is the option switch for a hierarchical run?

_____

What is the command to launch a hierarchical Calibre DRC run using lab11_rules as the rule file?

_____

9. Use the above command to launch a Calibre DRC run.

The Transcript displays in the window where you launched Calibre.

From the transcript, do you have any results?

_____

10. Use any ASCII text editor to open the Summary Report, lab11_drc_summary.

The Summary Report contains basically the same information as the transcript, just in a slightly more readable form.

What rules have errors?

_____

_____

How many occurrences of each error?

_____

11. Close the DRC Summary Report.

12. Open the DRC Results Database file, lab11_drc_results, using a text editor.

    Can you find the location of each error?

    min_poly width: _____

    min_ext_oxide_poly: _____

13. Close the DRC Results Database.

    If you did not have RVE and DESIGNrev available you would be able to find the problem by finding these coordinates in the layout. Not as easy, but doable.

    Now you are ready to try an LVS run.

Exercise 11-2: Command Line LVS Run

In this exercise you will perform an LVS run and see if you can track down the problem. You will then launch RVE from the command line to assist in verifying your solution.

1. Answer the following questions.

   What are the four additional specification statements that need to be added to the rule file for an LVS run?

   _____

   _____

   _____

   _____

2. Using any text editor open the lab11_rules file.

   Do you need to remove any of the specification statements you added for the DRC run?

   _____

   Write a specification statement specifying the source system to be spice.

   _____

3. Add this statement to the rule file.

   Write a specification statement specifying the source file as lab11a_source.spi.

   _____

4. Add this statement to the rule file.

Write a specification statement specifying the source's top_cell as lab11a.

_____

5. Add this statement to the rule file.

Write a specification statement creating the LVS Report lvs_report_lab11a.

_____

6. Add this statement to the rule file.

You will want to enter one more specification line to the rule file. You will want to launch Calibre RVE after you do as much analysis as you can from the command line. To do this you need to create the SVDB Mask data.

Look in the *SVRF Manual* to find the command for creating directory, svdb, with the query option. Write the answer below.

_____

7. Add this line to the rule file.

8. Save the file.

9. Close the file.

You will want to run this in hierarchical mode and have Calibre automatically match any cell names to aid in hierarchical comparisons. You will also want to create a netlist of the layout and place it in file lab11a_layout.spi.

What are the option switches you will need for command line Calibre?

_____

_____

_____

_____

What will your command line for this run look like?

_____

10. Run LVS using your command.

    (If it does not work, go back to the lecture or documentation to find out what is missing.)

11. Look at the transcript.

    Is the LVS comparison correct?

    _____

12. Open the lvs_report_lab11a file using any text editor/viewer.

    What are the error(s)?

    _____

    _____

    What cell has the problem?

    _____

Is the problem obvious from the report?

_____

_____

What are the net names?

Layout Net: _____

Source Net: _____

13. Close the LVS report.

14. Open the source (lab11a_source.spi) and layout (lab11a_layout.spi) netlists in text editors/viewers.

15. Find these nets in both netlists.
    (Not to easy to find, are they?)

    What instances do they connect to?

    Layout net 22: _____

    Layout net 51: _____

    Source: _____

    Where would you look to fix the problem in the layout?

    _____

16. Close the netlist files.

    Before leaving this exercise, you will launch RVE from the command line using the results from the LVS run.

17. At the command line prompt type:
    ```
    calibre -rve svdb
    ```

What is the svdb and where did it come from?

_____

Your command opened a Calibre LVS RVE window with the results from the last LVS run automatically loaded.

18. Use the RVE interface to verify the LVS problem and how you will fix it.

19. When you are done, close any open RVE or netlist windows.

Exercise 11-3: Command Line to Calibre Interactive

In this exercise you will simply launch Calibre Interactive from the command line.

1. From the command line, type:
   ```
   calibre -gui
   ```

   This opens a small window, which allows you to launch Calibre Interactive DRC, LVS, RVE, and PEX.

2. Choose the DRC button

   This opens the Calibre Interactive DRC application that you have used for all the previous Labs. This is just another method to access these tools.

3. Close all windows and applications.

Module 12
Final Exam

This is your final exam for the Using Calibre course.

The Layout Designer has just been fired. (You will soon find out why.) Your manager is very concerned about the quality on the work from this particular Layout Designer and would like this design thoroughly check out before it goes to tape.

All the files you need are in the lab_final directory.

Hints:

- The top_cell name in both the layout and the source is: lab_final.

- There are four LVS discrepancies.(You may see up to seven if you perform DRC corrections first.)

- There are 12 DRC discrepancies (running flat).

- Use the power of hierarchy. (Hcells!)

- Keep track of the errors, so the instructor can help you if needed.

- Go for the "low hanging fruit" first by checking the Extraction Report

Good Luck!

Appendix A
LVS Report Examples

Report 1

(Step One. Notice that there are no connectivity extraction or netlist compilation errors.)

```
#################################################
##               C A L I B R E            ##
##            L V S   R E P O R T         ##
#################################################
REPORT FILE NAME:         /user3/train3/icv/lvs.rep
LAYOUT NAME:              $LVS_ONLINE/layout/M_foo_1
SOURCE NAME:              $LVS_ONLINE/logic/ictraceM/default
LVS MODE:                 Mask
RULE FILE NAME:           /user3/train3/icv/lvs_online/layout/master_rules
CREATION TIME:            Thu Jul  6 08:22:30 1995
CURRENT DIRECTORY:        /tmp_mnt/net/bentley/user3/train3/icv
USER NAME:                train3
```

(Step Two. Notice that this header refers to all the correct pathnames.)

```
************************************************************    OVERALL COMPARISON RESULTS
************************************************************************
              #   #          ####################
             # #             #                  #
              #              #     INCORRECT     #
             # #             #                  #
              #   #          ####################
  Error:    Different numbers of nets (see below).
```

(Step Three. This LVS comparison result is INCORRECT. The problem is described in general as "Different numbers of nets. This could mean anything from misconnects to shorts or opens.)

```
-------------------------------------------------------------------------
INITIAL NUMBERS OF OBJECTS
--------------------------
             Layout   Source        Component Type
             ------   ------        --------------
 Ports:          16       19    *
 Nets:          356      154    *
 Instances:     140      140        mn (4 pins)
```

```
            140        140        mp (4 pins)
          ------     ------
Total Inst:    280        280
```

(Step Four. The main thing no notice in this INITIAL NUMBERS OF OBJECT report is that layout and source contain the same kinds of objects.)

```
NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------
              Layout   Source      Component Type
              ------   ------      --------------
Ports:           16       16
Nets:            74       73    *
Instances:       25       25       NAND2 (3 pins)
                  7        7       INV (2 pins)
                 10       10       AOI_2_1 (4 pins)
                  5        5       NAND3 (4 pins)
                 11       11       NOR2 (3 pins)
                  4        4       NAND4 (5 pins)
               ------   ------
Total Inst:       62       62
```

(Step Five.   Here it is apparent that Calibre has transformed the xtors into logical gates and is recognizing the same numbers of everything in the layout and source except for Nets. NOtice that Source Ports has gone from 19 to 16. This is likely because a single net had more than one port on it which were logically equivalent. Notice that the layout has one more net than the source.)

```
       * = Number of objects in layout different from number in source.
*************************************************************************INCORRECT OBJECTS
*********************************************************************
LEGEND:
-------
  ne  = Naming Error (same layout name found in source
        circuit, but object was matched otherwise).
 (Aside: Note that this is a _Legend_, not an actual error.  Only if "ne" shows up in the
  INCORRECT NETS or INCORRECT INSTANCES lists below is there an actual naming error.)
*********************************************************************   INCORRECT NETS
DISC#  LAYOUT NAME                                        ne  SOURCE NAME
*********************************************************************
  1   Net 150(217.000,205.000)                              /N$125
      N$125(135.375,406.000)
```

(Step Six. Skim the Discrepancy (or INCORRECT OBJECTS) list. Notice that there is only a single INCORRECT NETS discrepancy. Continue on to Step Seven in the INFORMATION AND WARNINGS section.)

(Step Nine. Finally, look over this list in detail. Since you know from the INFORMATION AND WARNINGS section below that Calibre has found a

**match for all objects in the Layout and Source, this discrepancy should make
sense to you. It is telling you that the two nets labelled "150" and "N$125" in
the layout, when taken together, seem to match Source net "/N$125". Another
way of looking at it is that layout net 150 matches part of source net /N$125
and layout net N$125 matches the rest of source net /N$125. Or _two_ layout
nets match a _single_ source net. This is an open circuit in the layout. Now you
could go back to the interactive debugging environment, knowing that you
were looking for an open circuit.)**

```
**************************************************************************
                            LVS PARAMETERS
**************************************************************************
(Aside: Skip over this information to the INFORMATION AND WARNINGS section.)
o LVS Setup:
    Component Type Properties:            phy_comp element comp
    Subtype Property:                     model
    Pin Name Properties:                  phy_pin
    Power Net Names:                      VDD
    Ground Net Names:                     VSS
    Ignore Ports:                         NO
    All Capacitor Pins Swappable:         NO
    Reduce Parallel Mos Transistors:      YES
    Recognize Gates:                      YES
    Recognize Only Simple Gates:          NO
    Reduce Split Gates:                   YES
    Reduce Parallel Bipolar Transistors:  YES
    Reduce Series Capacitors:             YES
    Reduce Parallel Capacitors:           YES
    Reduce Series Resistors:              YES
    Reduce Parallel Resistors:            YES
    Reduce Parallel Diodes:               YES
    Filter Unused Mos Transistors:        NO
    Filter Unused Bipolar Transistors:    NO
    Report List Limit:                    50

o Numeric Trace Properties:
 Component    Component    Source         Direct       Mask         Tole-  Trace
   Type       Subtype      Prop Name      Prop Name    Prop Name    rance
   mn                      instpar(w)     width         w             0%     NO
   mp                      instpar(w)     width         w             0%     NO
   me                      instpar(w)     width         w             0%     NO
   md                      instpar(w)     width         w             0%     NO
   mn                      instpar(l)     length        l             0%     NO
   mp                      instpar(l)     length        l             0%     NO
   me                      instpar(l)     length        l             0%     NO
   md                      instpar(l)     length        l             0%     NO
   r                       instpar(r)     resistance    r             0%     NO
   c                       instpar(c)     capacitance   c             0%     NO
   d                       instpar(a)     area          a             0%     NO
   d                       instpar(p)     perimeter     p             0%     NO

*********************** INFORMATION AND WARNINGS
**************************************************************************
              Matched     Matched     Unmatched     Unmatched     Component
              Layout      Source      Layout        Source        Type
              -------     -------     ---------     ---------     ---------
```

```
Ports:              16        16         0          0
Nets:               74        73         0          0
Instances:          25        25         0          0     NAND2
                     7         7         0          0     INV
                    10        10         0          0     AOI_2_1
                     5         5         0          0     NAND3
                    11        11         0          0     NOR2
                     4         4         0          0     NAND4
                  -------   -------   ---------  ---------
Total Inst:         62        62         0          0
```

(Step Seven. Notice that there are no Unmatched objects in the layout or the source. This means that in spite of a difference in the numbers of nets, Calibre has found a match for every net and instance in the database. This doesn't mean its correct (obviously since we have an extra net), it just means that Calibre thinks it knows how things are supposed to match up.

```
o Statistics:
  204 isolated layout nets were deleted.
  3 passthrough source nets were deleted.
  2 layout nets were reduced to passthrough nets.
  2 source nets were reduced to passthrough nets.
o Isolated Layout Nets:
      (Layout nets which are not connected to any instances or ports).
  356(455.000,329.000) 355(442.000,431.000) 354(442.000,305.000) 353(442.000,194.000)
  352(442.000,93.000) 351(441.000,5.500) 350(435.000,431.000) 349(435.000,305.000)
  348(435.000,194.000) 347(435.000,93.000) 346(425.000,321.500) 345(417.000,349.000)
  344(409.000,273.000) 343(409.000,205.000) 342(402.500,150.000) 341(402.500,104.000)
  340(401.000,223.000) 339(394.500,111.000) 338(393.000,316.000) 337(386.500,61.000)
  336(386.500,-0.159) 335(385.000,321.500) 334(385.000,273.000) 333(378.500,447.500)
  332(378.500,329.000) 331(378.500,205.000) 330(378.500,104.000) 329(370.500,316.000)
  328(370.500,5.500) 327(369.000,329.000) 326(362.500,343.500) 325(362.500,217.500)
  324(362.500,11.000) 323(354.500,329.000) 322(354.500,321.500) 321(354.500,273.000)
  320(354.500,109.500) 319(354.500,-0.159) 318(346.500,442.000) 317(346.500,205.000)
  316(346.500,61.000) 315(338.500,387.000) 314(338.500,338.000) 313(338.500,61.000)
  312(338.500,11.000) 311(330.500,447.500) 310(330.500,327.000) 309(330.500,273.000)
  308(330.500,223.000) 307(330.375,104.000)
o Initial Correspondence Points:
  Ports:        VDD VSS B(3) A(3) A(2) B(2) A(1) B(1) A(0) B(0) C0 C4 S(3) S(2) S(1) S(0)
```

(Step Eight. Scan the remaining INFORMATION AND WARNINGS section. Sometimes useful information such as bad devices shows up here (there would have been a warning at the top if so). Its also useful to see that the Initial Correspondence Points make sense. Another point to note is the plethora of Isolated Layout Nets. It is the rare rule write who creates a rule deck that doesn't create many, many isolated layout nets. Usually this section doesn't have much value. Occasionally, the user will stumble upon an Isolated Layout Net as being integral to the current LVS problem, however it is difficult identify that problem from this report. Continue to Step Nine in the INCORRECT OBJECTS section back in the middle of the report.)

```
***************************************************************    SUMMARY
***************************************************************
Total CPU Time:          5.2
Total Elapsed Time:      10.4111
```

Report 2

(Step One. Again, notice that there are no compilation or extraction errors.)

```
##################################################
##              C A L I B R E              ##
##            L V S   R E P O R T          ##
##################################################
REPORT FILE NAME:        /user3/train3/icv/lvs.rep
LAYOUT NAME:             $LVS_ONLINE/layout/M_foo_2
SOURCE NAME:             $LVS_ONLINE/logic/ictraceM/default
LVS MODE:                Mask
RULE FILE NAME:          /user3/train3/icv/lvs_online/layout/master_rules
CREATION TIME:           Thu Jul  6 08:24:46 1995
CURRENT DIRECTORY:       /tmp_mnt/net/bentley/user3/train3/icv
USER NAME:               train3
```

(Step Two. The header indicates the correct pathnames.)

```
***********************************************************    OVERALL COMPARISON RESULTS
***********************************************************
              #   #         ####################
             # #            #                  #
              #             #    INCORRECT     #
             # #            #                  #
              #   #         ####################
  Error:   Different numbers of nets (see below).
  Error:   Different numbers of instances (see below).
```

(Step Three. The comparison result is INCORRECT. The errors are generally described as differing numbers   of nets _and_ instances.

```
------------------------------------------------------------------------
INITIAL NUMBERS OF OBJECTS
-------------------------
             Layout   Source         Component Type
             ------   ------         -------------
 Ports:          16       19    *
 Nets:          356      154    *
 Instances:     140      140         mn (4 pins)
                140      140         mp (4 pins)
                ------   ------
 Total Inst:    280      280
```

(Step Four. Note that when the databases were initially read in, Calibre

recognized the same kinds of Instances and the same numbers of instances.)

```
NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------
            Layout   Source      Component Type
            ------   ------      --------------
Ports:          16       16
Nets:           74       73    *
Instances:      19        0    *   mn (4 pins)
                 9        0    *   mp (4 pins)
                25       25        NAND2 (3 pins)
                 6        7    *   INV (2 pins)
                 4       10    *   AOI_2_1 (4 pins)
                 5        5        NAND3 (4 pins)
                 5       11    *   NOR2 (3 pins)
                 2        4    *   NAND4 (5 pins)
                 6        0    *   SPUP_2_1 (4 pins)
                 6        0    *   SUP2 (3 pins)
                 2        0    *   SMN4 (6 pins)
                 6        0    *   SMN2 (4 pins)
            ------   ------
Total Inst:     95       62
```

(Step Five. However, after TRANSFORMATION, Calibre appears to be _very_ confused with many different logic gate counts and many logic gates recognized in the layout that don't appear in the source at all. Also notice that the number of nets after transformation is very close in the layout and source.

```
      * = Number of objects in layout different from number in source.
****************************************************************************INCORRECT OBJECTS
****************************************************************************
LEGEND:
-------
  ne  = Naming Error (same layout name found in source
        circuit, but object was matched otherwise).
(Aside. Again notice that this isn't an error. Its a legend.)
****************************************************************************  INCORRECT NETS
DISC#  LAYOUT NAME                                        ne  SOURCE NAME
****************************************************************************
```

(Step Six. At this point it makes sense to go directly to the INFORMATION AND WARNINGS section before even really looking at the discrepancies.)

```
   1   Net N$10(327.375,68.000)                            /N$9
       -------------------------                           -------------------------

       (NAND2):output                                      ** missing connection **
         114(333.875,31.000):d
         251(325.625,68.000):d
         254(333.625,68.000):s


       ** missing connection **                            (NAND2):output
                                                            /ND$18/MN1:D
                                                            /ND$18/MP2:D
```

```
                                                     /ND$18/MP1:D

--------------------------------------------------------------------------
   2   Net N$9(375.375,68.000)                       /N$10
       -------------------------                      -------------------------

       (NAND2):output                                ** missing connection **
         132(381.875,31.000):d
         269(373.625,68.000):d
         272(381.625,68.000):s


       ** missing connection **                      (NAND2):output
                                                        /ND$19/MN1:D
                                                        /ND$19/MP2:D
                                                        /ND$19/MP1:D

--------------------------------------------------------------------------
   3   Net N$182(35.375,169.000)                     ** no similar net **
--------------------------------------------------------------------------
   4   Net N$262(55.375,406.000)                     ** no similar net **
--------------------------------------------------------------------------
   5   Net N$197(63.375,280.000)                     ** no similar net **
--------------------------------------------------------------------------
   6   Net 3(28.250,123.250)                         ** no similar net **
--------------------------------------------------------------------------
   7   Net N$195(31.375,280.000)                     ** no similar net **
--------------------------------------------------------------------------
   8   Net N$124(31.375,406.000)                     ** no similar net **
--------------------------------------------------------------------------
   9   Net N$176(99.375,280.000)                     ** no similar net **
--------------------------------------------------------------------------
  10   Net N$187(71.375,169.000)                     ** no similar net **
--------------------------------------------------------------------------
  11   Net N$199(139.375,280.000)                    ** no similar net **
--------------------------------------------------------------------------
  12   Net N$263(239.375,406.000)                    ** no similar net **
--------------------------------------------------------------------------
  13   Net N$115(210.750,280.000)                    ** no similar net **
--------------------------------------------------------------------------
  14   Net N$54(111.375,169.000)                     ** no similar net **
--------------------------------------------------------------------------
  15   Net 27(143.375,169.000)                       ** no similar net **
--------------------------------------------------------------------------
  16   Net N$51(159.375,169.000)                     ** no similar net **
--------------------------------------------------------------------------
  17   Net N$118(266.750,280.000)                    ** no similar net **
--------------------------------------------------------------------------
  18   Net 37(191.375,169.000)                       ** no similar net **
--------------------------------------------------------------------------
  19   Net N$84(183.375,406.000)                     ** no similar net **
--------------------------------------------------------------------------
  20   Net N$46(207.375,169.000)                     ** no similar net **
--------------------------------------------------------------------------
  21   Net N$45(351.375,169.000)                     ** no similar net **
--------------------------------------------------------------------------
  22   Net 47(239.375,169.000)                       ** no similar net **
--------------------------------------------------------------------------
  23   Net N$68(255.375,169.000)                     ** no similar net **
--------------------------------------------------------------------------
  24   Net 60(287.375,169.000)                       ** no similar net **
```

```
    ------------------------------------------------------------------------
 25   Net N$69(303.375,169.000)                              ** no similar net **
    ------------------------------------------------------------------------
 26   Net 70(335.375,169.000)                               ** no similar net **
    ------------------------------------------------------------------------
 27   Net N$90(417.875,280.000)                             ** no similar net **
    ------------------------------------------------------------------------
 28   Net 82(383.375,169.000)                               ** no similar net **
    ------------------------------------------------------------------------
 29   Net 85(399.375,169.000)                               ** no similar net **
    ------------------------------------------------------------------------
 30   ** no similar net **                                  /N$263
    ------------------------------------------------------------------------
 31   ** no similar net **                                  /N$262
    ------------------------------------------------------------------------
 32   ** no similar net **                                  /N$46
    ------------------------------------------------------------------------
 33   ** no similar net **                                  /N$221
    ------------------------------------------------------------------------
 34   ** no similar net **                                  /XR$121/INT
    ------------------------------------------------------------------------
 35   ** no similar net **                                  /N$84
    ------------------------------------------------------------------------
 36   ** no similar net **                                  /N$118
    ------------------------------------------------------------------------
 37   ** no similar net **                                  /N$45
    ------------------------------------------------------------------------
 38   ** no similar net **                                  /N$199
    ------------------------------------------------------------------------
 39   ** no similar net **                                  /XR$120/INT
    ------------------------------------------------------------------------
 40   ** no similar net **                                  /N$90
    ------------------------------------------------------------------------
 41   ** no similar net **                                  /N$187
    ------------------------------------------------------------------------
 42   ** no similar net **                                  /N$124
    ------------------------------------------------------------------------
 43   ** no similar net **                                  /XR$133/INT
    ------------------------------------------------------------------------
 44   ** no similar net **                                  /N$54
    ------------------------------------------------------------------------
 45   ** no similar net **                                  /N$115
    ------------------------------------------------------------------------
 46   ** no similar net **                                  /N$197
    ------------------------------------------------------------------------
 47   ** no similar net **                                  /N$68
    ------------------------------------------------------------------------
 48   ** no similar net **                                  /N$69
    ------------------------------------------------------------------------
 49   ** no similar net **                                  /XR$132/INT
    ------------------------------------------------------------------------
 50   ** no similar net **                                  /N$51
***********************************************************************INCORRECT INSTANCES
DISC#  LAYOUT NAME                                     ne  SOURCE NAME
***********************************************************************
 51   154(69.625,169.000)                                  ** missing instance **
    ------------------------------------------------------------------------
 52   158(77.625,169.000)                                  ** missing instance **
    ------------------------------------------------------------------------
 53   162(85.625,169.000)                                  ** missing instance **
    ------------------------------------------------------------------------
```

```
54    164(93.625,169.000)                                        ** missing instance **
-----------------------------------------------------------------------------
55    143(33.625,169.000)                                        ** missing instance **
-----------------------------------------------------------------------------
56    146(41.625,169.000)                                        ** missing instance **
-----------------------------------------------------------------------------
57    148(49.625,169.000)                                        ** missing instance **
-----------------------------------------------------------------------------
58    151(57.625,169.000)                                        ** missing instance **
-----------------------------------------------------------------------------
59    130(373.875,132.000)                                       ** missing instance **
-----------------------------------------------------------------------------
60    133(381.875,132.000)                                       ** missing instance **
-----------------------------------------------------------------------------
61    126(365.875,132.000)                                       ** missing instance **
-----------------------------------------------------------------------------
62    112(325.875,132.000)                                       ** missing instance **
-----------------------------------------------------------------------------
63    115(333.875,132.000)                                       ** missing instance **
-----------------------------------------------------------------------------
64    109(317.875,132.000)                                       ** missing instance **
-----------------------------------------------------------------------------
65    94(277.875,132.000)                                        ** missing instance **
-----------------------------------------------------------------------------
66    97(285.875,132.000)                                        ** missing instance **
-----------------------------------------------------------------------------
67    90(269.875,132.000)                                        ** missing instance **
-----------------------------------------------------------------------------
68    76(229.875,132.000)                                        ** missing instance **
-----------------------------------------------------------------------------
69    78(237.875,132.000)                                        ** missing instance **
-----------------------------------------------------------------------------
70    72(221.875,132.000)                                        ** missing instance **
-----------------------------------------------------------------------------
71    58(181.875,132.000)                                        ** missing instance **
-----------------------------------------------------------------------------
72    61(189.875,132.000)                                        ** missing instance **
-----------------------------------------------------------------------------
73    55(173.875,132.000)                                        ** missing instance **
-----------------------------------------------------------------------------
74    39(133.875,132.000)                                        ** missing instance **
-----------------------------------------------------------------------------
75    42(141.875,132.000)                                        ** missing instance **
-----------------------------------------------------------------------------
76    37(125.875,132.000)                                        ** missing instance **
-----------------------------------------------------------------------------
77    136(397.875,132.000)                                       ** missing instance **
-----------------------------------------------------------------------------
78    276(397.625,169.000)                                       ** missing instance **
-----------------------------------------------------------------------------
79    (SPUP_2_1)                                                 ** missing gate **
      Transistors:
        177(125.625,169.000)
        170(109.625,169.000)
        173(117.625,169.000)
-----------------------------------------------------------------------------
80    (SUP2)                                                     ** missing gate **
      Transistors:
        179(133.625,169.000)
        182(141.625,169.000)
-----------------------------------------------------------------------------
```

```
81   (SPUP_2_1)                                          ** missing gate **
     Transistors:
       195(173.625,169.000)
       189(157.625,169.000)
       192(165.625,169.000)
--------------------------------------------------------------------------
82   (SUP2)                                              ** missing gate **
     Transistors:
       198(181.625,169.000)
       201(189.625,169.000)
--------------------------------------------------------------------------
83   (SPUP_2_1)                                          ** missing gate **
     Transistors:
       212(221.625,169.000)
       206(205.625,169.000)
       208(213.625,169.000)
--------------------------------------------------------------------------
84   (SPUP_2_1)                                          ** missing gate **
     Transistors:
       266(365.625,169.000)
       259(349.625,169.000)
       262(357.625,169.000)
--------------------------------------------------------------------------
85   (SUP2)                                              ** missing gate **
     Transistors:
       216(229.625,169.000)
       218(237.625,169.000)
--------------------------------------------------------------------------
86   (SPUP_2_1)                                          ** missing gate **
     Transistors:
       230(269.625,169.000)
       224(253.625,169.000)
       227(261.625,169.000)
--------------------------------------------------------------------------
87   (SUP2)                                              ** missing gate **
     Transistors:
       234(277.625,169.000)
       237(285.625,169.000)
--------------------------------------------------------------------------
88   (SPUP_2_1)                                          ** missing gate **
     Transistors:
       249(317.625,169.000)
       243(301.625,169.000)
       247(309.625,169.000)
--------------------------------------------------------------------------
89   (SUP2)                                              ** missing gate **
     Transistors:
       252(325.625,169.000)
       255(333.625,169.000)
--------------------------------------------------------------------------
90   (SUP2)                                              ** missing gate **
     Transistors:
       270(373.625,169.000)
       273(381.625,169.000)
--------------------------------------------------------------------------
91   (SMN4)                                              ** missing gate **
     Transistors:
       3(33.875,132.000)
       11(57.875,132.000)
       8(49.875,132.000)
       6(41.875,132.000)
```

```
--------------------------------------------------------------------------
 92   (SMN4)                                            ** missing gate **
      Transistors:
       14(69.875,132.000)
       24(93.875,132.000)
       22(85.875,132.000)
       18(77.875,132.000)
--------------------------------------------------------------------------
 93   (SMN2)                                            ** missing gate **
      Transistors:
       30(109.875,132.000)
       33(117.875,132.000)
--------------------------------------------------------------------------
 94   (SMN2)                                            ** missing gate **
      Transistors:
       49(157.875,132.000)
       52(165.875,132.000)
--------------------------------------------------------------------------
 95   (SMN2)                                            ** missing gate **
      Transistors:
       66(205.875,132.000)
       68(213.875,132.000)
--------------------------------------------------------------------------
 96   (SMN2)                                            ** missing gate **
      Transistors:
       84(253.875,132.000)
       87(261.875,132.000)
--------------------------------------------------------------------------
 97   (SMN2)                                            ** missing gate **
      Transistors:
       103(301.875,132.000)
       107(309.875,132.000)
--------------------------------------------------------------------------
 98   (SMN2)                                            ** missing gate **
      Transistors:
       119(349.875,132.000)
       122(357.875,132.000)
--------------------------------------------------------------------------
 99   ** missing gate **                                (AOI_2_1)
                                                        Transistors:
                                                         /XR$121/MPA
                                                         /XR$121/MPC
                                                         /XR$121/MPB
                                                         /XR$121/MNA
                                                         /XR$121/MNC
                                                         /XR$121/MNB
--------------------------------------------------------------------------
100   ** missing gate **                                (INV)
                                                        Transistors:
                                                         /IV$201/MP1
                                                         /IV$201/MN1
**************************************************************************
                            LVS PARAMETERS
**************************************************************************
o LVS Setup:
   Component Type Properties:        phy_comp element comp
   Subtype Property:                 model
   Pin Name Properties:              phy_pin
   Power Net Names:                  VDD
   Ground Net Names:                 VSS
   Ignore Ports:                     NO
```

```
          All Capacitor Pins Swappable:         NO
          Reduce Parallel Mos Transistors:      YES
          Recognize Gates:                      YES
          Recognize Only Simple Gates:          NO
          Reduce Split Gates:                   YES
          Reduce Parallel Bipolar Transistors:  YES
          Reduce Series Capacitors:             YES
          Reduce Parallel Capacitors:           YES
          Reduce Series Resistors:              YES
          Reduce Parallel Resistors:            YES
          Reduce Parallel Diodes:               YES
          Filter Unused Mos Transistors:        NO
          Filter Unused Bipolar Transistors:    NO
          Report List Limit:                    50

o Numeric Trace Properties:
 Component   Component    Source       Direct      Mask        Tole-   Trace
   Type      Subtype     Prop Name    Prop Name   Prop Name    rance
   mn                    instpar(w)    width          w          0%     NO
   mp                    instpar(w)    width          w          0%     NO
   me                    instpar(w)    width          w          0%     NO
   md                    instpar(w)    width          w          0%     NO
   mn                    instpar(l)    length         l          0%     NO
   mp                    instpar(l)    length         l          0%     NO
   me                    instpar(l)    length         l          0%     NO
   md                    instpar(l)    length         l          0%     NO
   r                     instpar(r)    resistance     r          0%     NO
   c                     instpar(c)    capacitance    c          0%     NO
   d                     instpar(a)    area           a          0%     NO
   d                     instpar(p)    perimeter      p          0%     NO

************************************************************************* INFORMATION AND
WARNINGS
*************************************************************************
             Matched   Matched   Unmatched  Unmatched  Component
             Layout    Source    Layout     Source     Type
             -------   -------   ---------  ---------  ---------
    Ports:       16        16           0          0
    Nets:        41        41          33         32
    Instances:    0         0          19          0    mn
                  0         0           9          0    mp
                 20        20           5          5    NAND2
                  6         6           0          1    INV
                  4         4           0          6    AOI_2_1
                  5         5           0          0    NAND3
                  5         5           0          6    NOR2
                  0         0           2          4    NAND4
                  0         0           6          0    SPUP_2_1
                  0         0           6          0    SUP2
                  0         0           2          0    SMN4
                  0         0           6          0    SMN2
             -------   -------   ---------  ---------
    Total Inst:  40        40          55         22
```

(Step Seven. Apparently only about half of the circuit was able to compare properly. These errors look fairly serious, as if there are numerous big problems. However, before getting too concerned, its important to realize that Calibre couldn't even recognize the same numbers of logic gates in the source

and layout. We still don't have any clue what the real problem is, but a good plan would be to go back and rerun the LVS with the "Recognize Logic Gates" switch turned off. Calibre will then try to match individual transistors without assembling them into logic gates. In this case, you would see that the problem was really quite simple, another open circuit, and that the logic gate recognition feature ended up confusing Calibre rather that assisting it.)

```
o Statistics:
   204 isolated layout nets were deleted.
   3 passthrough source nets were deleted.
   1 layout net was reduced to a passthrough net.
   2 source nets were reduced to passthrough nets.
o Isolated Layout Nets:
      (Layout nets which are not connected to any instances or ports).
   356(455.000,329.000) 355(442.000,431.000) 354(442.000,305.000) 353(442.000,194.000)
   352(442.000,93.000) 351(441.000,5.500) 350(435.000,431.000) 349(435.000,305.000)
   348(435.000,194.000) 347(435.000,93.000) 346(425.000,321.500) 345(417.000,349.000)
   344(409.000,273.000) 343(409.000,205.000) 342(402.500,150.000) 341(402.500,104.000)
   340(401.000,223.000) 339(394.500,111.000) 338(393.000,316.000) 337(386.500,61.000)
   336(386.500,-0.159) 335(385.000,321.500) 334(385.000,273.000) 333(378.500,447.500)
   332(378.500,329.000) 331(378.500,205.000) 330(378.500,104.000) 329(370.500,316.000)
   328(370.500,5.500) 327(369.000,329.000) 326(362.500,343.500) 325(362.500,217.500)
   324(362.500,11.000) 323(354.500,329.000) 322(354.500,321.500) 321(354.500,273.000)
   320(354.500,109.500) 319(354.500,-0.159) 318(346.500,442.000) 317(346.500,205.000)
   316(346.500,61.000) 315(338.500,387.000) 314(338.500,338.000) 313(338.500,61.000)
   312(338.500,11.000) 311(330.500,447.500) 310(330.500,327.000) 309(330.500,273.000)
   308(330.500,223.000) 307(330.375,104.000)
o Initial Correspondence Points:
   Ports:         VDD VSS B(3) A(3) A(2) B(2) A(1) B(1) A(0) B(0) C0 C4 S(3) S(2) S(1) S(0)
************************************************************************  DETAILED INSTANCE
CONNECTIONS
      LAYOUT NAME                                         ne  SOURCE NAME
************************************************************************
         (This section contains detailed information about connections of
          matched instances that are involved in net discrepancies).
-------------------------------------------------------------------------
      (NAND2)                                             (NAND2)
        input: N$63(311.375,68.000)                        input: /N$63
        input: 76(351.375,406.000)                         input: /N$7
        output: N$10(327.375,68.000)                      ** /N$9 **
        ** N$9(375.375,68.000) **                          output: /N$10
      Transistors:
        111(325.875,31.000)                                /ND$19/MN2
        114(333.875,31.000)                                /ND$19/MN1
        251(325.625,68.000)                                /ND$19/MP2
        254(333.625,68.000)                                /ND$19/MP1
************************************************************************
UNMATCHED OBJECTS
      LAYOUT                                              SOURCE
************************************************************************
      N$207(175.375,280.000)                             ** unmatched net **
      N$82(363.375,280.000)                              ** unmatched net **
      N$205(249.875,280.000)                             ** unmatched net **
      N$203(339.375,280.000)                             ** unmatched net **
      N$201(301.875,280.000)                             ** unmatched net **
      N$98(393.875,280.000)                              ** unmatched net **
```

```
--------------------------------------------------------------------------  (NAND4)
** unmatched gate **
        Transistors:
          36(121.875,243.000)
          32(113.875,243.000)
          29(105.875,243.000)
          26(97.875,243.000)
          176(121.625,280.000)
          172(113.625,280.000)
          169(105.625,280.000)
          166(97.625,280.000)
--------------------------------------------------------------------------  (NAND4)
** unmatched gate **
        Transistors:
          51(161.875,243.000)
          48(153.875,243.000)
          45(145.875,243.000)
          41(137.875,243.000)
          191(161.625,280.000)
          188(153.625,280.000)
          185(145.625,280.000)
          181(137.625,280.000)
--------------------------------------------------------------------------  (NAND2)
** unmatched gate **
        Transistors:
          38(129.875,31.000)
          35(121.875,31.000)
          178(129.625,68.000)
          175(121.625,68.000)
--------------------------------------------------------------------------  (NAND2)
** unmatched gate **
        Transistors:
          47(153.875,31.000)
          44(145.875,31.000)
          187(153.625,68.000)
          184(145.625,68.000)
--------------------------------------------------------------------------  (NAND2)
** unmatched gate **
        Transistors:
          93(273.875,31.000)
          89(265.875,31.000)
          233(273.625,68.000)
          229(265.625,68.000)
--------------------------------------------------------------------------  (NAND2)
** unmatched gate **
        Transistors:
          96(285.875,31.000)
          100(293.875,31.000)
          236(285.625,68.000)
          240(293.625,68.000)
--------------------------------------------------------------------------  (NAND2)
** unmatched gate **
        Transistors:
          129(373.875,31.000)
          132(381.875,31.000)
          269(373.625,68.000)
          272(381.625,68.000)
--------------------------------------------------------------------------
        ** unmatched net **                                    /N$201
        ** unmatched net **                                    /N$203
        ** unmatched net **                                    /N$98
```

```
      ** unmatched net **                                          /N$82
      ** unmatched net **                                          /N$207
      ** unmatched net **                                          /N$205
--------------------------------------------------------------------  ** unmatched gate
**                                       (NAND2)
                                                       Transistors:
                                                        /ND$18/MN2
                                                        /ND$18/MN1
                                                        /ND$18/MP2
                                                        /ND$18/MP1
--------------------------------------------------------------------  ** unmatched gate
**                                       (NAND4)
                                                       Transistors:
                                                        /ND$158/MN4
                                                        /ND$158/MN3
                                                        /ND$158/MN2
                                                        /ND$158/MN1
                                                        /ND$158/MP4
                                                        /ND$158/MP3
                                                        /ND$158/MP2
                                                        /ND$158/MP1
--------------------------------------------------------------------  ** unmatched gate
**                                       (NAND4)
                                                       Transistors:
                                                        /ND$151/MN4
                                                        /ND$151/MN3
                                                        /ND$151/MN2
                                                        /ND$151/MN1
                                                        /ND$151/MP4
                                                        /ND$151/MP3
                                                        /ND$151/MP2
                                                        /ND$151/MP1
--------------------------------------------------------------------  ** unmatched gate
**                                       (NAND2)
                                                       Transistors:
                                                        /ND$31/MN2
                                                        /ND$31/MN1
                                                        /ND$31/MP2
                                                        /ND$31/MP1
--------------------------------------------------------------------  ** unmatched gate
**                                       (NAND2)
                                                       Transistors:
                                                        /ND$32/MN2
                                                        /ND$32/MN1
                                                        /ND$32/MP2
                                                        /ND$32/MP1
--------------------------------------------------------------------  ** unmatched gate
**                                       (NAND2)
                                                       Transistors:
                                                        /ND$102/MN2
                                                        /ND$102/MN1
                                                        /ND$102/MP2
                                                        /ND$102/MP1
--------------------------------------------------------------------  ** unmatched gate
**                                       (NAND2)
                                                       Transistors:
                                                        /ND$103/MN2
                                                        /ND$103/MN1
                                                        /ND$103/MP2
                                                        /ND$103/MP1
```

```
-------------------------------------------------------------------------  ** unmatched gate
**                                    (NAND4)
                                                      Transistors:
                                                        /ND$152/MN4
                                                        /ND$152/MN3
                                                        /ND$152/MN2
                                                        /ND$152/MN1
                                                        /ND$152/MP4
                                                        /ND$152/MP3
                                                        /ND$152/MP2
                                                        /ND$152/MP1
-------------------------------------------------------------------------  ** unmatched gate
**                                    (NAND4)
                                                      Transistors:
                                                        /ND$180/MN4
                                                        /ND$180/MN3
                                                        /ND$180/MN2
                                                        /ND$180/MN1
                                                        /ND$180/MP4
                                                        /ND$180/MP3
                                                        /ND$180/MP2
                                                        /ND$180/MP1
*************************************************************************  SUMMARY
*************************************************************************
Total CPU Time:          3.67
Total Elapsed Time:      4.42851
```

Report 3

```
 Extraction Errors and Warnings for cell "$LVS_ONLINE/layout/M_foo_4"
 ---------------------------------------------------------------------
WARNING:  Short circuit - Different names on one net:
         Net Id:  63
         (1)  name "C0"  at location  (441.5,6)  on layer  10 "metal2"
         (2)  name "N$69"  at location  (291,53)  on layer  10 "metal2"
         The name "C0" was assigned to the net.
```

(Step One: Notice this connectivity extraction warning. Right away you know that something is strange about the layout. It could be one of the labels is a mistake and Calibre just happened to pick the right label. The circuit could still come out correct with this problem. However, its always a good idea to look at those labels at the given locations and make certain they are placed correctly, on the correct layers, over the correct polygons, with the correct values. In this case the problem will turn out to be fairly obvious, but in more complex cases, it is always best to investigate these warnings before expending too much effort in debugging the LVS reports.)

```
##################################################
```

```
##                C A L I B R E                   ##
##              L V S   R E P O R T               ##
##################################################
REPORT FILE NAME:          /user3/train3/icv/lvs.rep
LAYOUT NAME:               $LVS_ONLINE/layout/M_foo_4
SOURCE NAME:               $LVS_ONLINE/logic/ictraceM/default
LVS MODE:                  Mask
RULE FILE NAME:            /user3/train3/icv/lvs_online/layout/master_rules
CREATION TIME:             Thu Jul  6 08:25:45 1995
CURRENT DIRECTORY:         /tmp_mnt/net/bentley/user3/train3/icv
USER NAME:                 train3
```

(Step Two. Check the header. Its OK in this case.)

```
**************************************************************************  OVERALL COMPARISON
RESULTS
**************************************************************************
              #   #        ####################
              # #          #                  #
               #           #      INCORRECT   #
              # #          #                  #
              #   #        ####################
  Error:   Different numbers of nets (see below).
```

(Step Three. The overall result is incorrect with a differing number of nets.)

```
----------------------------------------------------------------------
INITIAL NUMBERS OF OBJECTS
------------------------
            Layout    Source         Component Type
            ------    ------         --------------
 Ports:         16        19     *
 Nets:         354       154     *
 Instances:    140       140         mn (4 pins)
               140       140         mp (4 pins)
               ------    ------
 Total Inst:   280       280
NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------
            Layout    Source         Component Type
            ------    ------         --------------
 Ports:         16        16
 Nets:          72        73     *
 Instances:     25        25         NAND2 (3 pins)
                 7         7         INV (2 pins)
                10        10         AOI_2_1 (4 pins)
                 5         5         NAND3 (4 pins)
                11        11         NOR2 (3 pins)
                 4         4         NAND4 (5 pins)
               ------    ------
 Total Inst:    62        62
      * = Number of objects in layout different from number in source.
```

(Step Four. Note that ICtrace is recognizing the same numbers of everything except for nets. Fewer nets in Layout than Source can mean short circuits.)

```
**************************************************************************INCORRECT OBJECTS
**************************************************************************
LEGEND:
-------
```

```
   ne  = Naming Error (same layout name found in source
         circuit, but object was matched otherwise).
*********************************************************************  INCORRECT NETS
DISC#  LAYOUT NAME                                     ne  SOURCE NAME
*********************************************************************
  1    Net C0(303.375,169.000)                             /C0
                                                           /N$69
```

(Step Five. Notice in passing that the sole discrepancy is an INCORRECT NET as you might expect. Proceed to Step Six below.)

(Step Seven. After Checking the INFORMATION AND WARNINGS section below, you know that this   report is telling you that a single net, "C0" in the layout appears to match two nets, "/C0" and "N$69", in the source. If you will recall the extraction warning at the top regarding net labels, you will see that the layout labels that you were warned about match the source net names. It appears that the labels were placed correctly and that this error is a short circuit between two nets in the layout. You may now go to the interactive Calibre debugging environment to find the problem that you now know is a short circuit.)

```
*********************************************************************
                         LVS PARAMETERS
*********************************************************************
o LVS Setup:
   Component Type Properties:         phy_comp element comp
   Subtype Property:                  model
   Pin Name Properties:               phy_pin
   Power Net Names:                   VDD
   Ground Net Names:                  VSS
   Ignore Ports:                      NO
   All Capacitor Pins Swappable:      NO
   Reduce Parallel Mos Transistors:   YES
   Recognize Gates:                   YES
   Recognize Only Simple Gates:       NO
   Reduce Split Gates:                YES
   Reduce Parallel Bipolar Transistors: YES
   Reduce Series Capacitors:          YES
   Reduce Parallel Capacitors:        YES
   Reduce Series Resistors:           YES
   Reduce Parallel Resistors:         YES
   Reduce Parallel Diodes:            YES
   Filter Unused Mos Transistors:     NO
   Filter Unused Bipolar Transistors: NO
   Report List Limit:                 50

o Numeric Trace Properties:
 Component   Component   Source      Direct    Mask      Tole-  Trace
   Type      Subtype     Prop Name   Prop Name Prop Name rance
   mn                    instpar(w)    width           w        0%     NO
   mp                    instpar(w)    width           w        0%     NO
```

```
me                  instpar(w)       width          w        0%      NO
md                  instpar(w)       width          w        0%      NO
mn                  instpar(l)       length         l        0%      NO
mp                  instpar(l)       length         l        0%      NO
me                  instpar(l)       length         l        0%      NO
md                  instpar(l)       length         l        0%      NO
r                   instpar(r)       resistance     r        0%      NO
c                   instpar(c)       capacitance    c        0%      NO
d                   instpar(a)       area           a        0%      NO
d                   instpar(p)       perimeter      p        0%      NO


************************************************************************ INFORMATION AND
WARNINGS
************************************************************************
              Matched    Matched    Unmatched   Unmatched   Component
              Layout     Source     Layout      Source      Type
              -------    -------    ---------   ---------   ---------
    Ports:         16         16           0           0
    Nets:          72         73           0           0
    Instances:     25         25           0           0      NAND2
                    7          7           0           0      INV
                   10         10           0           0      AOI_2_1
                    5          5           0           0      NAND3
                   11         11           0           0      NOR2
                    4          4           0           0      NAND4
                   -------    -------    ---------   ---------
    Total Inst:    62         62           0           0
```

(Step Six: Note that everything has been matched so ICtrace believes it can identify Source/Layout correspondences for everything. Go back to the INCORRECT OBJECTS list above for Step Seven.)

```
o Statistics:
  204 isolated layout nets were deleted.
  3 passthrough source nets were deleted.
  2 layout nets were reduced to passthrough nets.
  2 source nets were reduced to passthrough nets.
o Isolated Layout Nets:
    (Layout nets which are not connected to any instances or ports).
  354(455.000,329.000) 353(442.000,431.000) 352(442.000,305.000) 351(442.000,194.000)
  350(442.000,93.000) 349(441.000,5.500) 348(435.000,431.000) 347(435.000,305.000)
  346(435.000,194.000) 345(435.000,93.000) 344(425.000,321.500) 343(417.000,349.000)
  342(409.000,273.000) 341(409.000,205.000) 340(402.500,150.000) 339(402.500,104.000)
  338(401.000,223.000) 337(394.500,111.000) 336(393.000,316.000) 335(386.500,61.000)
  334(386.500,-0.159) 333(385.000,321.500) 332(385.000,273.000) 331(378.500,447.500)
  330(378.500,329.000) 329(378.500,205.000) 328(378.500,104.000) 327(370.500,316.000)
  326(370.500,5.500) 325(369.000,329.000) 324(362.500,343.500) 323(362.500,217.500)
  322(362.500,11.000) 321(354.500,329.000) 320(354.500,321.500) 319(354.500,273.000)
  318(354.500,109.500) 317(354.500,-0.159) 316(346.500,442.000) 315(346.500,205.000)
  314(346.500,61.000) 313(338.500,387.000) 312(338.500,338.000) 311(338.500,61.000)
  310(338.500,11.000) 309(330.500,447.500) 308(330.500,327.000) 307(330.500,273.000)
  306(330.500,223.000) 305(330.375,104.000)
o Initial Correspondence Points:
  Ports:        VDD VSS B(3) A(3) A(2) B(2) A(1) B(1) A(0) B(0) C0 C4 S(3) S(2) S(1) S(0)
************************************************************************        SUMMARY
************************************************************************
Total CPU Time:        3.51
Total Elapsed Time:    3.18274
```

Appendix B
Web Links of Interest

Mentor Graphics Web Sites

There are a few websites of interest you will want to visit:

www.mentor.com/supportnet - This is the customer support home page. You will have to register and receive a password to access it. Just fill out a registration form online and your login information will be sent to you.

www.mentor.com/calibre/index.html - Download the latest executables. See what's new in Calibre. Monthly releases. Application notes and other documentation. Password registry required.

www.mentor.com/supportnet/appnotes.html - This is a listing of application notes that you can download from the web.

www.mentor.com/supportnet/dsm - This is the deep-submicron home page. Many useful links.

Appendix C
Query Server Transcripts

This appendix contains transcripts from several Query Server Sessions.

Transcript of Generating a Basic Hcells List Using the Query Server

The information below is the transcript of a "basic"[1] and automatic Hcell file generation using the Query Server. All commands enters by the user are

"boxed" to make them easier to find.

```
% calibre -query
```

```
//  Calibre v2004.1_5.29   Wed Apr  7 23:26:06 PDT 2004
//  Litho Libraries v2004.1_5.28  Tue Apr  6 21:24:25 PDT 2004
//
//                Copyright Mentor Graphics Corporation 2004
//                          All Rights Reserved.
//         THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
//            WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
//               OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
//
//  Mentor Graphics software executing under Sun SPARC Solaris
//
//  Running on SunOS ding 5.8 Generic_108528-20 sun4u
//
//  Starting time: Fri Apr 16 07:45:09 2004
//

--- CALIBRE::HDB QUERY SERVER --- Fri Apr 16 07:45:10 2004
```

1. This will not generate a complete Hcell file since there is a pseudo cell in the layout. Also it will bump into the default threshold and will not add cells that to not contribute that minimum amount of memory savings.

```
--------------------------------------------------------------------------------
-    CPU TIME = 0   REAL TIME = 0   LVHEAP = 0/0/0 MALLOC = 0/0/0
--------------------------------------------------------------------------------


--------------------------------------------------------------------------------
--------------------------------------------------------------------------------
-----            CALIBRE::HDB QUERY SERVER - EXECUTIVE MODULE            -----
--------------------------------------------------------------------------------
--------------------------------------------------------------------------------

INITIATING HDB QUERY SERVER:
--------------
   OK: Ready to serve.
```

```
netlist automatch on
```

```
   OK.
```

```
netlist placementmatch on
```

```
   OK.
```

```
netlist read query_rules
```

```
Initializing LVS ...

READING layout ...
Layout READ.  CPU TIME = 0   REAL TIME = 0   LVHEAP = 0/0/0  MALLOC = 1/1/1

READING source ...
Source READ.  CPU TIME = 0   REAL TIME = 0   LVHEAP = 0/0/0  MALLOC = 1/1/1

Identifying CORRESPONDING cells ...
CORRESPONDING Cells Identified.  CPU TIME = 0   REAL TIME = 0

Adding GLOBAL elements ...
GLOBAL elements added.  CPU TIME = 0   REAL TIME = 0

Resolving DEEP SHORTS ...
DEEP SHORTS resolved.  CPU TIME = 0   REAL TIME = 0

Resolving HIGH SHORTS ...
HIGH SHORTS resolved.  CPU TIME = 0   REAL TIME = 0

Deleting TRIVIAL PINS ...
TRIVIAL PINS deleted.  CPU TIME = 0   REAL TIME = 0
   OK.
```

```
netlist select hcells
```

```
                    =======================
                     C A L I B R E   L V S
                    HCELL EVALUATION REPORT
                    =======================


    Total Hier.    Saved    Total Potential Layout  Source
  Instance Count By This  Savings Remaining   Cell    Cell
   Layout Source    Cell   So Far   Savings   Name    Name
================= ======= ======= ========= ====== =======
      280     280    0.0%    0.0%       68%
      200     200     29%     29%       55%  a2311   s2311
      138     138     31%     51%       35%  a1220   s1220
      118     118     14%     58%       24%  a1240   s1240
   OK.
```

```
response file basic_hcells
```

```
   OK.
```

```
netlist report hcells
```

```
   OK.
```

```
response direct
```

```
   OK.
```

Resulting Hcell File

File basic_hcells contains the following lines:

```
   a2311   s2311
   a1220   s1220
   a1240   s1240
```

It is ready to be used as an Hcell file with no additional editing required.

Transcript of Interactively Creating Hcell File

The information below is a transcript of interactively creating the Hcell file, *interactive_hcells*.

```
% calibre -query
```

```
//  Calibre v2004.1_5.29   Wed Apr  7 23:26:06 PDT 2004
//  Litho Libraries v2004.1_5.28  Tue Apr  6 21:24:25 PDT 2004
//
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//         THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
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//               OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
//
//  Mentor Graphics software executing under Sun SPARC Solaris
//
//  Running on SunOS ding 5.8 Generic_108528-20 sun4u
//
//  Starting time: Fri Apr 16 08:52:16 2004
//

--- CALIBRE::HDB QUERY SERVER --- Fri Apr 16 08:52:17 2004
-------------------------------------------------------------------------------
-    CPU TIME = 0  REAL TIME = 0  LVHEAP = 0/0/0 MALLOC = 0/0/0
-------------------------------------------------------------------------------


-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
-----           CALIBRE::HDB QUERY SERVER - EXECUTIVE MODULE          -----
-------------------------------------------------------------------------------
-------------------------------------------------------------------------------

INITIATING HDB QUERY SERVER:
--------------
   OK: Ready to serve.
```

```
netlist read query_rules
```

```
Initializing LVS ...

READING layout ...
Layout READ.  CPU TIME = 0  REAL TIME = 0  LVHEAP = 0/0/0  MALLOC = 1/1/1

READING source ...
Source READ.  CPU TIME = 0  REAL TIME = 0  LVHEAP = 0/0/0  MALLOC = 1/1/1

Identifying CORRESPONDING cells ...
CORRESPONDING Cells Identified.  CPU TIME = 0  REAL TIME = 0

Adding GLOBAL elements ...
GLOBAL elements added.  CPU TIME = 0  REAL TIME = 0

Resolving DEEP SHORTS ...
DEEP SHORTS resolved.  CPU TIME = 0  REAL TIME = 0
```

```
Resolving HIGH SHORTS ...
HIGH SHORTS resolved.  CPU TIME = 0  REAL TIME = 0

Deleting TRIVIAL PINS ...
TRIVIAL PINS deleted.  CPU TIME = 0  REAL TIME = 0
   OK.
```

```
┌─────────────────────────────────────────┐
│ netlist report hierarchy layout         │
└─────────────────────────────────────────┘
```

```
              =======================================
                       C A L I B R E   L V S
                 HCELL ANALYSIS AND HIERARCHY TREE REPORT
              =======================================

Top Level Data
--------------
Netlist file: lay.net
Total Flat Device Count (TFDC)          =           280 (count of all devices represented flat)
Total Hierarchical Instance Count (THIC) =          280 (count of all devices expanded to hcells)

Potential Hcell Analysis
-----------------------
This report presents information useful for selecting LVS hcells for a netlist.
Cells are presented in order of potential memory savings if the cell is used as an hcell.

Column Definitions
------------------
Flat - The following columns present statistics concerning the flattened design.

 (1) Instances of this Cell
     The number of times the cell is instantiated throughout the entire flattened design.

 (2) Devices in this Cell (FDC)
     The number of devices in this cell when its entire contents are flattened (Flat
     Device Count).

 (3) Total Device Contrib. (1)x(2)
     The number of devices this cell contributes to the total flat device count.

 (4) % Total Device Contrib. ((3)/TFDC)*100
     Column (3) represented as a percentage of total flat device count.


With Hcells - the following columns present statistics taking into account the current hcells and
automatch setting.

 (5) Instances of this Cell
     The number of times the cell is instantiated within all existing hcells (always 1 for an hcell).

 (6) Instances in this Cell (HIC)
     The number of instances that would be in this cell if all non-hcells inside it were expanded
     (Hierarchical Instance Count).

 (7) Total Instance Contrib. (5)x(6)
     The number of instances this cell contributes to the total hierarchical instance count.

 (8) % Total Instance Contrib. ((7)/THIC)*100
     Column (7) represented as a percentage of total hierarchical instance count.

 (9) % Memory Savings
     Expected memory savings if this cell is used as an hcell.

(10) Cell Name
     Cell names.
     * designates leaf cells (all contents are devices).
     + designates current hcells.
     = designates cells with the same name in layout and source.
     # designates cells that would match via placementmatch.



<---------------- Flat ----------------> <------------ With Hcells ------------->
     (1)        (2)        (3)        (4)        (5)        (6)        (7)        (8)        (9)        (10)
```

Instances of this Cell	Devices in this Cell (FDC)	Total Device Contrib. (1)x(2)	% Total Device Contrib. (3)/TFDC	Instances of this Cell	Instances in this Cell (HIC)	Total Instance Contrib. (5)x(6)	% Total Instance Contrib. (7)/THIC	% Memory Savings	Cell Name * (leaf cell) + (hcell) = (same name) # (same #placements/pins)
10	10	100	36	10	10	100	36	29	* # a2311
22	4	88	31	22	4	88	31	22	* # a1220
4	8	32	11	4	8	32	11	7.1	* # a1240
5	6	30	11	5	6	30	11	6.8	* # a1230
3	6	18	6.4	3	6	18	6.4	3.2	* # a1620
3	2	6	2.1	3	2	6	2.1	0.4	* # a1310
1	280	280	100.0	1	280	280	100.0	0.0	+= lab7b
1	6	6	2.1	1	6	6	2.1	0.0	* # a1720
140				140					MN
140				140					MP

```
Hierarchy Tree
--------------

   Devices   Cell Name
   in this
      Cell
==========  =========
       280  lab7b (level=0)
         4  . a1220 (x10) (level=1)
         1  . . MN (x2) (level=2)
         1  . . MP (x2) (level=2)
         6  . a1230 (x5) (level=1)
         1  . . MN (x3) (level=2)
         1  . . MP (x3) (level=2)
         8  . a1240 (x4) (level=1)
         1  . . MN (x4) (level=2)
         1  . . MP (x4) (level=2)
         2  . a1310 (x3) (level=1)
         1  . . MN (x1) (level=2)
         1  . . MP (x1) (level=2)
         6  . a1620 (x3) (level=1)
         1  . . MN (x3) (level=2)
         1  . . MP (x3) (level=2)
         6  . a1720 (x1) (level=1)
         1  . . MN (x3) (level=2)
         1  . . MP (x3) (level=2)
        10  . a2311 (x10) (level=1)
         1  . . MN (x5) (level=2)
         1  . . MP (x5) (level=2)
         8  . ICV_1 (x6) (level=1)
         4  . . a1220 (x2) (level=2)
         1  . . . MN (x2) (level=3)
         1  . . . MP (x2) (level=3)

   OK.
```

```
netlist hcell a2311 s2311
```

```
   OK.
```

```
netlist report hierarchy layout
```

```
          =======================================
                     C A L I B R E   L V S
              HCELL ANALYSIS AND HIERARCHY TREE REPORT
          =======================================

Top Level Data
--------------
Netlist file: lay.net
Total Flat Device Count (TFDC)          =        280 (count of all devices represented flat)
Total Hierarchical Instance Count (THIC) =        200 (count of all devices expanded to hcells)
```

```
Potential Hcell Analysis
------------------------
This report presents information useful for selecting LVS hcells for a netlist.
Cells are presented in order of potential memory savings if the cell is used as an hcell.


Column Definitions
------------------
Flat - The following columns present statistics concerning the flattened design.

 (1) Instances of this Cell
     The number of times the cell is instantiated throughout the entire flattened design.

 (2) Devices in this Cell (FDC)
     The number of devices in this cell when its entire contents are flattened (Flat
     Device Count).

 (3) Total Device Contrib. (1)x(2)
     The number of devices this cell contributes to the total flat device count.

 (4) % Total Device Contrib. ((3)/TFDC)*100
     Column (3) represented as a percentage of total flat device count.


With Hcells - the following columns present statistics taking into account the current hcells and
automatch setting.

 (5) Instances of this Cell
     The number of times the cell is instantiated within all existing hcells (always 1 for an hcell).

 (6) Instances in this Cell (HIC)
     The number of instances that would be in this cell if all non-hcells inside it were expanded
     (Hierarchical Instance Count).

 (7) Total Instance Contrib. (5)x(6)
     The number of instances this cell contributes to the total hierarchical instance count.

 (8) % Total Instance Contrib. ((7)/THIC)*100
     Column (7) represented as a percentage of total hierarchical instance count.

 (9) % Memory Savings
     Expected memory savings if this cell is used as an hcell.

(10) Cell Name
     Cell names.
     * designates leaf cells (all contents are devices).
     + designates current hcells.
     = designates cells with the same name in layout and source.
     # designates cells that would match via placementmatch.
```

```
<---------------- Flat ----------------->  <------------ With Hcells ------------->
    (1)        (2)       (3)       (4)          (5)        (6)       (7)       (8)       (9)       (10)
Instances   Devices     Total    % Total   Instances  Instances     Total    % Total       %      Cell Name
 of this    in this    Device    Device     of this    in this   Instance   Instance   Memory  * (leaf cell)
   Cell       Cell     Contrib.  Contrib.     Cell       Cell    Contrib.   Contrib.   Savings  + (hcell)
             (FDC)    (1)x(2)   (3)/TFDC                (HIC)    (5)x(6)   (7)/THIC            = (same name)
                                                                                              # (same #placements/pins)

=========  =========  ========  ========  =========  =========  ========  ========  =======  =================
       22          4        88        31         22          4        88        44       31  *  # a1220
        4          8        32        11          4          8        32        16       10  *  # a1240
        5          6        30        11          5          6        30        15      9.5  *  # a1230
        3          6        18       6.4          3          6        18         9      4.5  *  # a1620
        3          2         6       2.1          3          2         6         3      0.5  *  # a1310
        1        280       280     100.0          1        190       190        95      0.0  +=   lab7b
       10         10       100        36          1         10        10         5      0.0  *+   a2311
        1          6         6       2.1          1          6         6         3      0.0  *  # a1720
      140                                        95                                             MP
      140                                        95                                             MN


Hierarchy Tree
--------------

   Devices   Cell Name
```

```
      in this
        Cell
==========  =========
      280  lab7b (level=0)
        4  . a1220 (x10) (level=1)
        1  . . MN (x2) (level=2)
        1  . . MP (x2) (level=2)
        6  . a1230 (x5) (level=1)
        1  . . MN (x3) (level=2)
        1  . . MP (x3) (level=2)
        8  . a1240 (x4) (level=1)
        1  . . MN (x4) (level=2)
        1  . . MP (x4) (level=2)
        2  . a1310 (x3) (level=1)
        1  . . MN (x1) (level=2)
        1  . . MP (x1) (level=2)
        6  . a1620 (x3) (level=1)
        1  . . MN (x3) (level=2)
        1  . . MP (x3) (level=2)
        6  . a1720 (x1) (level=1)
        1  . . MN (x3) (level=2)
        1  . . MP (x3) (level=2)
       10  . a2311 (x10) (level=1)
        1  . . MN (x5) (level=2)
        1  . . MP (x5) (level=2)
        8  . ICV_1 (x6) (level=1)
        4  . . a1220 (x2) (level=2)
        1  . . . MN (x2) (level=3)
        1  . . . MP (x2) (level=3)

  OK.
```

```
netlist hcell a1220 s1220
```

```
  OK.
```

```
netlist report hierarchy layout
```

```
        =======================================
                 C A L I B R E   L V S
        HCELL ANALYSIS AND HIERARCHY TREE REPORT
        =======================================
```

Top Level Data

Netlist file: lay.net
Total Flat Device Count (TFDC)   =   280 (count of all devices represented flat)
Total Hierarchical Instance Count (THIC) =   138 (count of all devices expanded to hcells)

Potential Hcell Analysis

This report presents information useful for selecting LVS hcells for a netlist.
Cells are presented in order of potential memory savings if the cell is used as an hcell.

Column Definitions

Flat - The following columns present statistics concerning the flattened design.

 (1) Instances of this Cell
     The number of times the cell is instantiated throughout the entire flattened design.

 (2) Devices in this Cell (FDC)
     The number of devices in this cell when its entire contents are flattened (Flat
     Device Count).

 (3) Total Device Contrib. (1)x(2)
     The number of devices this cell contributes to the total flat device count.

 (4) % Total Device Contrib. ((3)/TFDC)*100

Column (3) represented as a percentage of total flat device count.

With Hcells - the following columns present statistics taking into account the current hcells and automatch setting.

 (5) Instances of this Cell
     The number of times the cell is instantiated within all existing hcells (always 1 for an hcell).

 (6) Instances in this Cell (HIC)
     The number of instances that would be in this cell if all non-hcells inside it were expanded
     (Hierarchical Instance Count).

 (7) Total Instance Contrib. (5)x(6)
     The number of instances this cell contributes to the total hierarchical instance count.

 (8) % Total Instance Contrib. ((7)/THIC)*100
     Column (7) represented as a percentage of total hierarchical instance count.

 (9) % Memory Savings
     Expected memory savings if this cell is used as an hcell.

(10) Cell Name
     Cell names.
     * designates leaf cells (all contents are devices).
     + designates current hcells.
     = designates cells with the same name in layout and source.
     # designates cells that would match via placementmatch.


```
<---------------- Flat ----------------->  <------------ With Hcells ------------->
    (1)        (2)        (3)       (4)        (5)        (6)       (7)       (8)       (9)        (10)
Instances    Devices    Total    % Total  Instances  Instances    Total   % Total       %       Cell Name
 of this    in this    Device    Device    of this    in this  Instance  Instance   Memory   * (leaf cell)
   Cell       Cell    Contrib.   Contrib.    Cell       Cell   Contrib.  Contrib.  Savings   + (hcell)
                       (FDC)     (1)x(2)    (3)/TFDC             (HIC)     (5)x(6)  (7)/THIC             = (same name)
                                                                                                 # (same #placements/pins)
=========  =========  ========  ========  =========  =========  ========  ========  =======  =================
        4          8        32        11          4          8        32        23       14   *  # a1240
        5          6        30        11          5          6        30        22       14   *  # a1230
        3          6        18       6.4          3          6        18        13      6.5   *  # a1620
        3          2         6       2.1          3          2         6       4.3      0.7   *  # a1310
        1        280       280     100.0          1        124       124        90      0.0   +=   lab7b
       10         10       100        36          1         10        10       7.2      0.0   *+   a2311
       22          4        88        31          1          4         4       2.9      0.0   *+   a1220
        1          6         6       2.1          1          6         6       4.3      0.0   *  # a1720
      140                                        53                                             MN
      140                                        53                                             MP
```


Hierarchy Tree

```
  Devices   Cell Name
  in this
    Cell
==========  =========
       280  lab7b (level=0)
         4  . a1220 (x10) (level=1)
         1  . . MN (x2) (level=2)
         1  . . MP (x2) (level=2)
         6  . a1230 (x5) (level=1)
         1  . . MN (x3) (level=2)
         1  . . MP (x3) (level=2)
         8  . a1240 (x4) (level=1)
         1  . . MN (x4) (level=2)
         1  . . MP (x4) (level=2)
         2  . a1310 (x3) (level=1)
         1  . . MN (x1) (level=2)
         1  . . MP (x1) (level=2)
         6  . a1620 (x3) (level=1)
         1  . . MN (x3) (level=2)
         1  . . MP (x3) (level=2)
         6  . a1720 (x1) (level=1)
         1  . . MN (x3) (level=2)
```

```
 1  . . MP (x3) (level=2)
10  . a2311 (x10) (level=1)
 1  . . MN (x5) (level=2)
 1  . . MP (x5) (level=2)
 8  . ICV_1 (x6) (level=1)
 4  . . a1220 (x2) (level=2)
 1  . . . MN (x2) (level=3)
 1  . . . MP (x2) (level=3)
```

OK.

```
response file interactive_hcells
```

OK.

```
netlist report hcells
```

OK.

```
response direct
```

OK.

```
netlist report hcells
```

```
a2311   s2311
a1220   s1220
```
OK.

The last command in this sequence is not required. It is simply a quick check of exactly what was contained in the Hcell list.

Transcript of Updating an Existing Hcell File Using a New Threshold

The example below starts where the previous example left off (querying what is in the current Hcell list). Therefore launching the Query Server is not required. (Although loading the rules and setting automatching and placementmatching on is duplicated for completeness.) You change the threshold to 8% memory savings and create the new Hcell file.

```
response direct
```

 OK.

```
netlist report hcells
```

```
a2311   s2311
a1220   s1220
```
 OK.

```
netlist automatch on
```

 OK.

```
netlist placementmatch on
```

 OK.

```
netlist read query_rules
```

```
Initializing LVS ...

READING layout ...
Layout READ.  CPU TIME = 0  REAL TIME = 0  LVHEAP = 0/0/1  MALLOC = 1/1/1

READING source ...
Source READ.  CPU TIME = 0  REAL TIME = 0  LVHEAP = 0/0/1  MALLOC = 1/1/1

Identifying CORRESPONDING cells ...
CORRESPONDING Cells Identified.  CPU TIME = 0  REAL TIME = 0

Adding GLOBAL elements ...
```

```
GLOBAL elements added.  CPU TIME = 0  REAL TIME = 0

Resolving DEEP SHORTS ...
DEEP SHORTS resolved.  CPU TIME = 0  REAL TIME = 0

Resolving HIGH SHORTS ...
HIGH SHORTS resolved.  CPU TIME = 0  REAL TIME = 0

Deleting TRIVIAL PINS ...
TRIVIAL PINS deleted.  CPU TIME = 0  REAL TIME = 0
   OK.
```

```
netlist evaluation threshold 8
```

```
   OK.
```

```
netlist evaluation current hcells no
```

```
   OK.
```

```
netlist select hcells
```

```
                  ========================
                   C A L I B R E   L V S
                  HCELL EVALUATION REPORT
                  ========================


     Total Hier.   Saved   Total  Potential Layout  Source
    Instance Count By This Savings Remaining  Cell    Cell
    Layout   Source  Cell   So Far  Savings   Name    Name
   ================ ======= ======= ========= ====== =======
       138      138   51%     51%       35%
       118      118   14%     58%       24%   a1240   s1240
        99       99   16%     65%      9.1%   a1230   s1230
        90       90  9.1%     68%      0.0%   a1620   s1620
   OK.
```

```
response file interactive_hcells
```

```
   OK.
```

```
netlist report hcells
```

```
   OK.
```

```
response direct
```

 OK.

```
netlist report hcells
```

```
a2311    s2311
a1220    s1220
a1240    s1240
a1230    s1230
a1620    s1620
```
 OK.

Again, the last line is not required. It just shows you that the new Hcells were
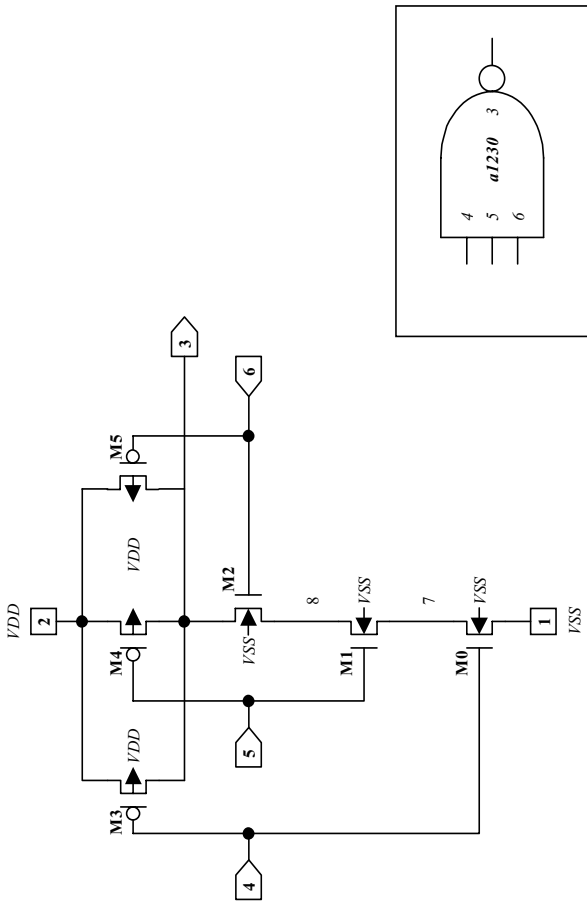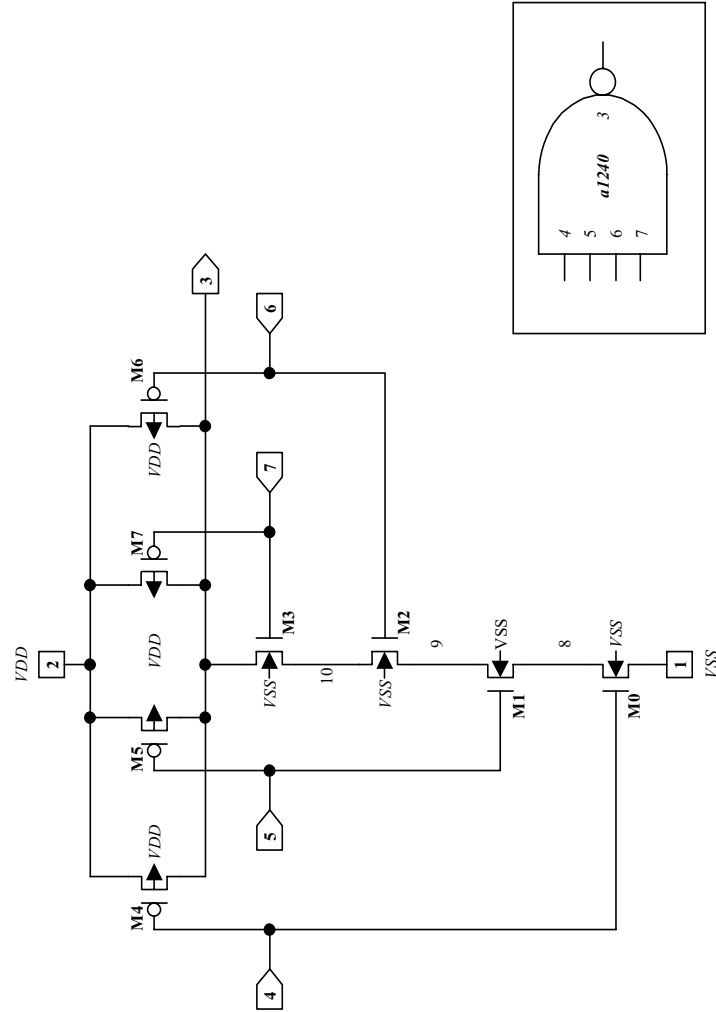indeed added to the Hcell list.

Appendix D
Schematics for Lab Circuit

This appendix contains simple hand-drawn schematics to aid in troubleshooting during lab work.
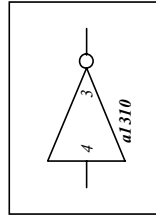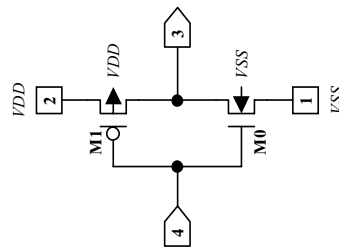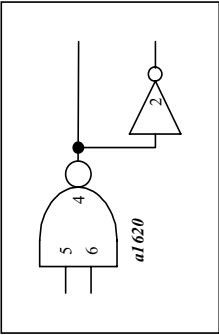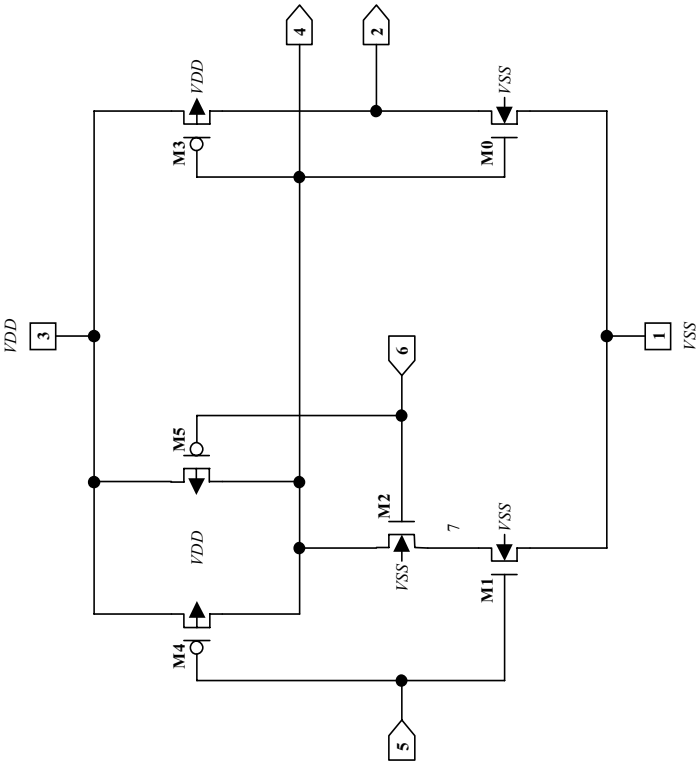
Cell a1230

Cell a1240

Cell a1310

Cell a1620

Cell a1720

Cell a2311

NOTES: