HW/SW-Codesign
Implementation Hints

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Abstract

This article provides some additional hints/explanations for implementing a HW/SW-system with the given SCARTS environment. It covers the implementation of an AMBA AHB master, provides some hints how the camera interface can be implemented and finally gives specific configuration settings, which we found most suitable for the camera operation. Please note, that the given descriptions and settings are only suggestions, which we consider reasonable. Use your best professional judgment to decide, whether you stick to them or whether you use own settings or other means for implemenation, if you deem them to be more suitable. For general information on the involved components, please read the respective manuals.

1 AMBA AHB Master

If you want to access the AMBA bus directly from a hardware module, it is necessary to add and implement an AHB master interface for your module. Fortunately, there is a ready to use AHB master helper component (*ahbmst*) in the *grlib* [1]. There is, however, no detailed documentation of the *ahbmst* module since it is only an internal module of the *grlib*. The most important I/O signals of this component are explained in Table 1.

Signal	Description
dmai.wdata	data word that should be written
dmai.burst	set it to high to enable burst mode
dmai.irq	set it to low
dmai.size	set it to "010" for a 32 bit transfer
dmai.write	low: read operation, high: write operation
dmai.busy	set it to low
dmai.start	set it high to start a new transfer, set it to low to stop a transfer
dmai.address	destination address
dmao.ready	signals when the master is ready to receive new data
dmao.rdata	data output of read request

Table 1: I/O Signals of *ahbmst* component.

To perform a write access (burst transfer) the following steps are required:

- set the data and destination address signals
- set *dmai.start* to high
- every cycle *dmao.ready* is high we can increase the address and apply a new data word
- to stop the transfer set *dmai.start* to low

Figure 1 shows a waveform of such a write acceess. Note, that there is one speciality when using the burst transfer mode: Since the AHB master component uses 10-bit addressing internally, we have to stop and restart a transfer when dmai.address reaches a 1k bound (that is if dmai.address(11 downto 10) changes). For implementation examples how to integrate the *ahbmst* component, you can look into other modules of the *grlib*, e.g., *atahost_ahbmst.vhd* or *svgactrl.vhd*.

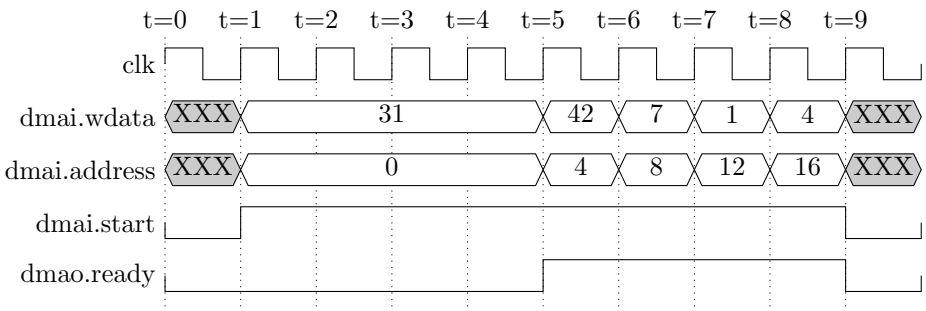

Figure 1: AHB Burst Mode.

2 Interface to the Camera

Here are some hints for the camera interface:

- Due to the unshielded ribbon cable, which connects the camera to the FPGA board, signal integritiy problems (e.g., crosstalk) can arise at higher clock rates. Use the PLL in the camera for generating the camera clock. This allows you to use a lower clock frequency (e.g., 10 MHz) from the FPGA to the camera, which reduces disturbances on the ribbon cable. The procedure to set up the PLL is desribed in the Terasic TRDB-D5M Hardware specification [2]. PLL register values to create a camera clock of 30 MHz are shown in Table 2.
- A further activity to reduce disturbances on the cable is to lower the slewrate of the camera output signals. Recommended settings can be found in Table 3.
- To avoid metastable upsets within the logic of your camera controller, use synchronizers on all data and control inputs.

Register	Value	Meaning
0x10	0x51	Power PLL
0x11	(30 << 8)|4	PLL m Factor = 8, PLL n Divider = 4
0x12	1	PLL p1 Divider
0x10	(1 << 1)|0x51	Use and Power PLL
0x0A	1 << 15	invert pixel clock

Table 2: PLL Register Settings.

Register	Value	Meaning
0x07	(1 << 10)|(7 << 7)|(1 << 1)	Data Slew Rate = 1, Clock Slew Rate = 7, Chip Enable

Table 3: Slew Rate Register Settings.

3 Camera Settings

Register settings to get an image of 800x480 pixels are listed in Table 4. To get a feasible image from the camera, it is necessary to setup the gain register for each color channel. There are two different gain settings: analog and digital. Appropriate values are listed in Table 5 (taken from the Terasic example application which can be downloaded from [2]). To change the brightness of the image it proved to be more effective to change the camera exposure time (Register 0x09, feasible values range from 500 to 2000) than to change the gain settings. However, take into account that this affects the frame rate.

Register	Value	Meaning
0x03	1441	row size
0x04	2401	column size
0x22	2	row skipping
0x23	3	column skipping
0x20	1 << 15	mirror rows
0x1e	0x4006|(1 << 8)	snapshot mode

Table 4: Resolution Register Settings.

Register	Value	Meaning
0x2b	(10 << 8)|(0 << 6)|29)	green1: analog gain = 29, digital gain = 10
0x2c	(10 << 8)|(0 << 6)|39)	blue: analog gain = 39, digital gain = 10
0x2d	(10 << 8)|(0 << 6)|42)	red: analog gain = 42, digital gain = 10
0x2e	(10 << 8)|(0 << 6)|29)	green2: analog gain = 29, digital gain = 10

Table 5: Gain Register Settings.

References

[1] Aeroflex Gaisler AB. Grlib ip library. http://www.gaisler.com/cms/index.php?option=com_content&task=section&id=13&Itemid=125, 2008. [online; last visit 10.10.2011].

[2] Terasic Technologies Inc. 5 mega pixel digital camera package. http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=68&No=281&PartNo=1, 2011. [online; last visit 10.10.2011].