EE 619 (ZELE)

Project-1 [15 Marks]

Submission Deadline: 29th March 11:55 PM

- Submission must be in the format *ROLLNO_EE619_Project1.pdf* only
- Submissions after deadline will not be accepted under any circumstances
- Report all values preferably in tabular format where ever it is appropriate
- The submission must contain appropriate plots labelled clearly
- Please go through the supporting material for noise and non-linearity simulations

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Consider the Common Source LNA shown below (Fig. 1). Design the LNA in UMC 65 nm technology to meet the following specifications.

- **Center frequency (f_0) = 2.49 GHz and Bandwidth > 100 MHz**
- **Gain (Vout/Vin) @f_0 > 20 dB**
- **S11 @f_0 < -13 dB**
- **IIP3 (Input referred to 50 Ω) > -2 dBm**
- **P1dB (Input referred to 50 Ω) > -12 dBm**
- **NF @f_0 < 2.5 dB**
- **Total Power (including bias circuitry) < 4 mW**

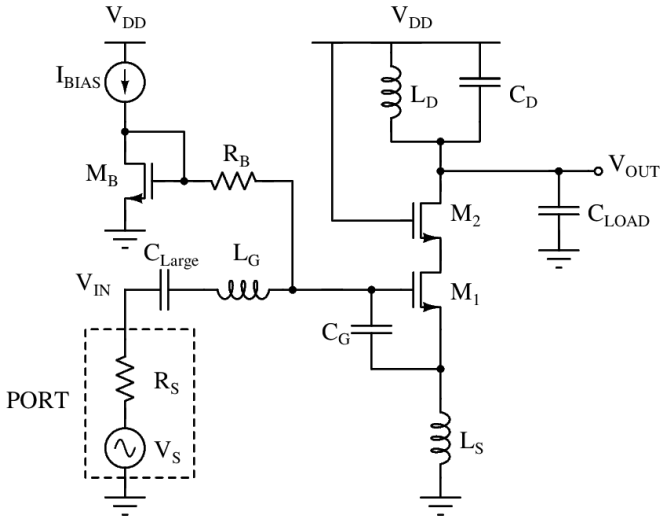

Fig.1 Common Source LNA

Component	Instance in UMC 65
MOSFET	N_12_LLLVTRF
Inductor	L_SY30K_RFVIL
Capacitor	MIMCAPS_20F_M1_RFKF
Resistor	RNHR_LLRF

Table.1 List of components from UMC 65 lib

Use V_{DD} = 1.2 V, C_{LOAD} = 250 fF.
Use components C_{Large}, C_{LOAD}, PORT (50 Ω), I_{BIAS} from analogLib and rest from UMC 65 library.

1. Bias the circuit appropriately and tabulate the values of I_{BIAS}, L_G, L_S, L_D, C_G, C_D, C_{Large}, R_B and W/L for all the transistors. Report power dissipation. Show the annotated DC operating points of the circuit.

2. Show the plots of Gain, S_{11}, IIP3, P1dB, NF and annotate the important points clearly.

3. Tabulate the noise contribution of the individual devices. Identify the major noise contributors.