Project 1

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1 Student Details

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2 Methedology

I used Lecture-12 and Thomas Lee to get an idea of how to start designing the circuit.

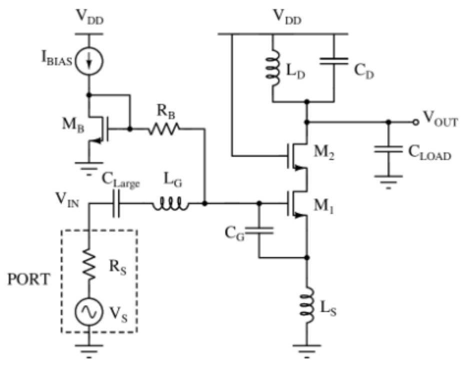


Figure 1: Inductive Degeneration CS LNA Circuit

I used the following steps to design the circuit:

- I chose RB first
- Selected Bias Current
- Set L = 60nm and selected a width of 1um for all Mosfets
- Using impedance matching, I calculated the value of L_S, The Transit Frequency of the given Mosfet came out to be more than 60GHz, But for Impedance Matching, no such L_S was realizable, therefore I set L_S approximately 1nH and started working from there

- Selected C_G such that a realizable LG can be set for resonance
- I chose L_D and C_D such that these and CLOAD resonate at 2.49GHz.
- Iteratively changed values of L_S, L_G, C_G, C_D, L_D, and C_{LOAD} to get the desired specs.
- L_D and C_D had a huge impact on P1dB and IIP3
- Set Multipliers of M1 and M2 to 10
- From simulations, understood higher width required for Lower NF, therefore increased width of all transisitors to 4.5um
- To match Power constraints I decreased Bias current to less than 300uA.

These are the equations which helped me get a rough idea of the values of the components:

- $R_S = \omega_T L_S$, where R_S is the port resistance = 50Ω
- Then used the modified equation which takes account of Parsasitic Capacitance, $R_S = \omega_T L_S \left(\frac{C_G}{C_G + C_{par}}\right)^2$
- $\omega_0^2 = \frac{1}{(L_G + L_S)(C_G + C_{par})}$, where ω_0 is the resonant frequency = 2.49GHzS
- $\omega_0^2 = \frac{1}{L_D(C_D + C_{LOAD})}$

Given, $V_{DD} = 1.2V$, Therefore to match the power constrain: $Power < 4mW$, We needed current drawn from V_{DD} to be less than 3.33 mA.

3 Final Values and Schematic

Power Dissipation = 2.98554 mA * 1.2 V = 3.58265 mW
The final values of the components are given in Table.

Table 1: Final Component Values

Component	**Value**
R_B	1 kΩ
I_{Bias}	215 μA
L_S	1.5 nH
C_G	616.56 fF
L_G	5.5 nH
C_D	581.944 fF
L_D	4 nH
C_{Large}	40 pF
W/L (same for all MOSFETS)	$\frac{4.5\mu M}{60nM}$

Schematic of the circuit with annotated DC operating points

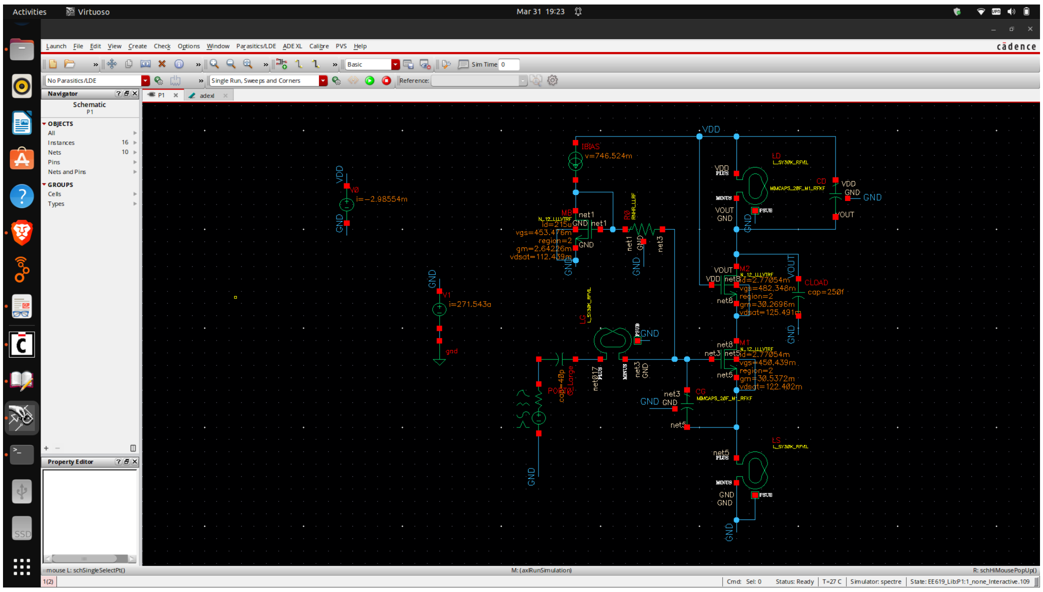


Figure 2: Annotated Schematic

4 Simulations Plots

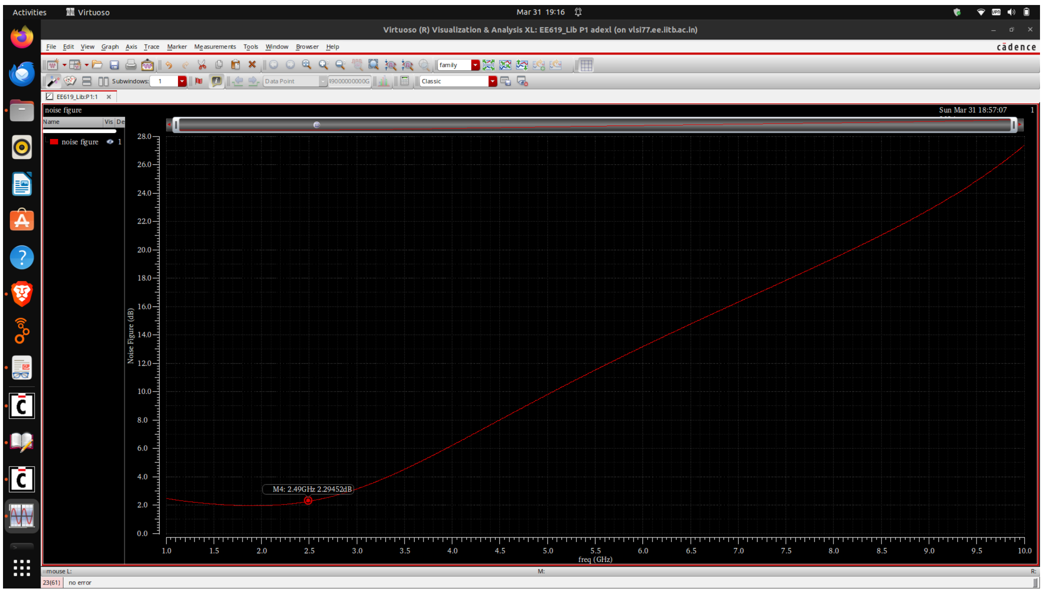


Figure 3: Noise Figure vs Frequency

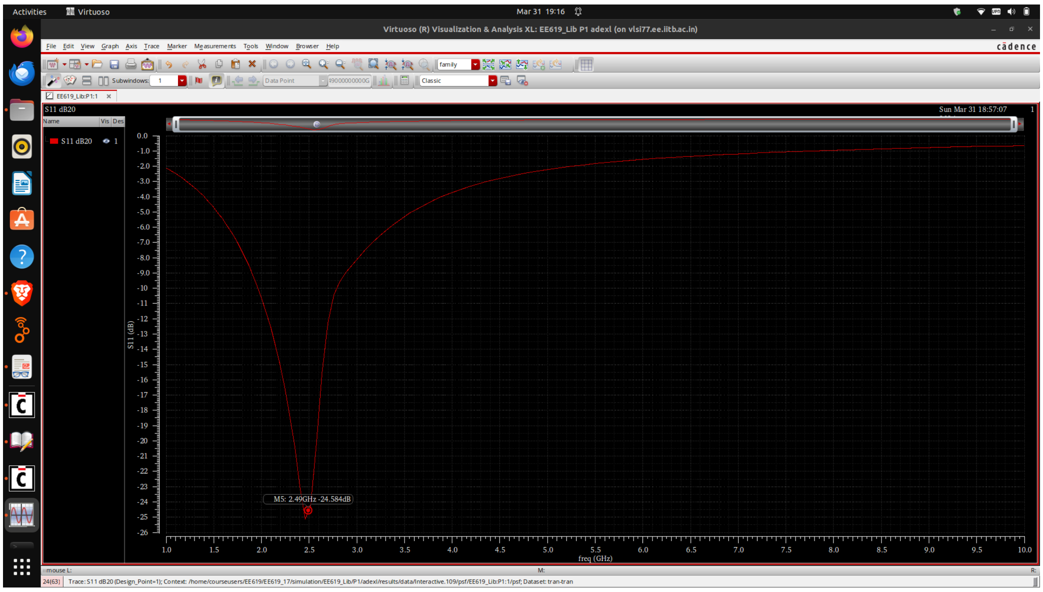


Figure 4: S11 vs Frequency

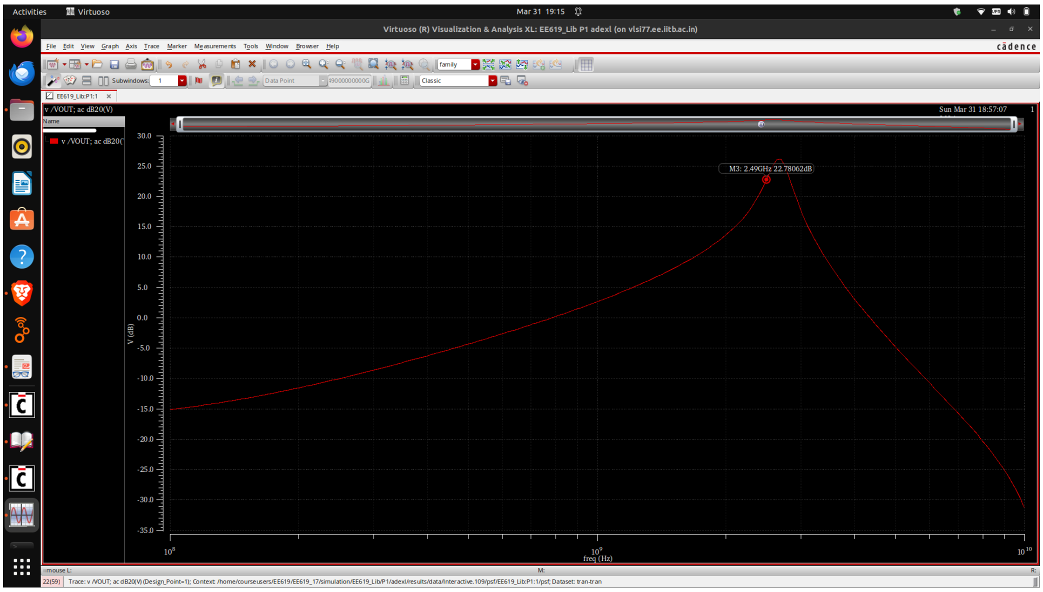


Figure 5: Gain(dB) vs Frequency

5 Noise Contributions

The noise contributions of the different components are given in Table ??.

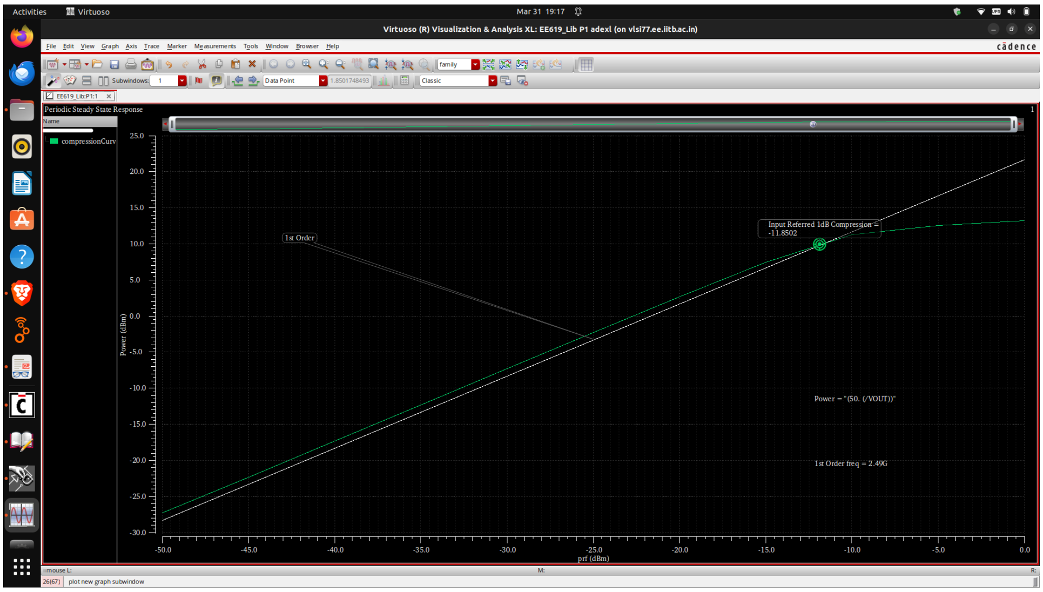


Figure 6: P1dB vs Frequency

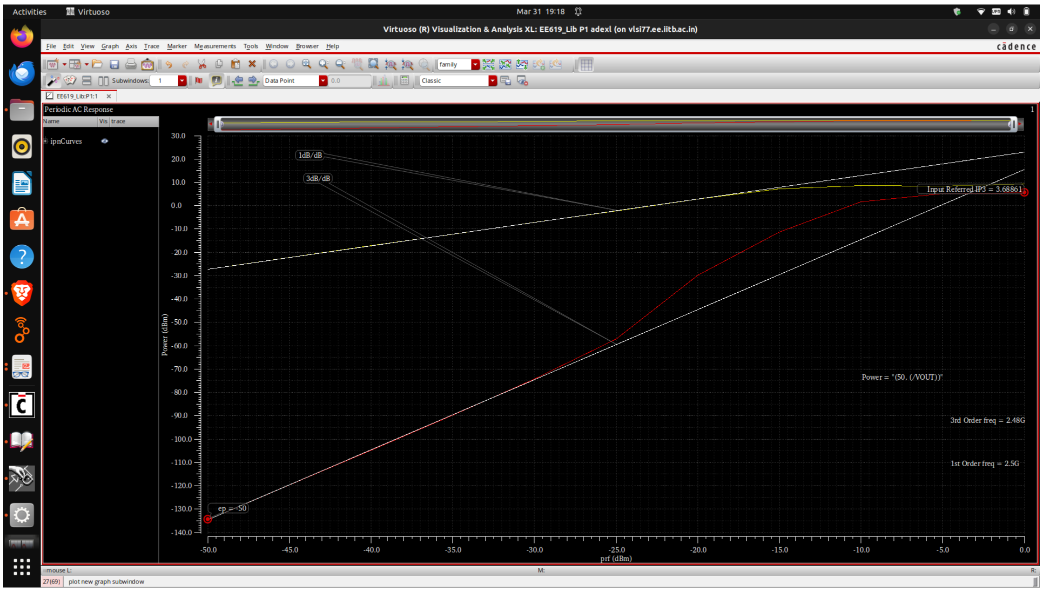
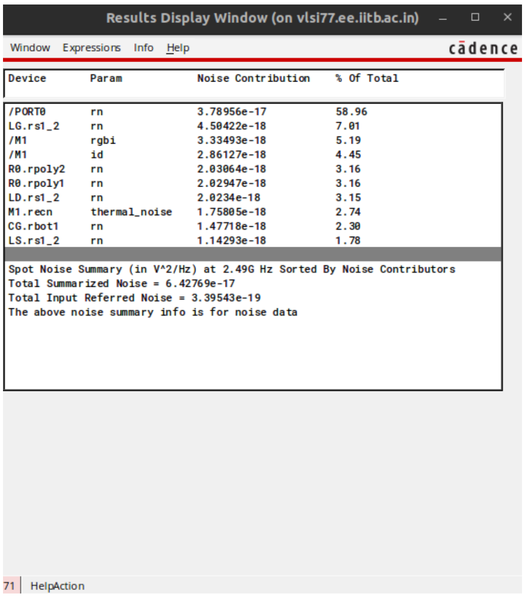


Figure 7: IIP3 vs Frequency



Results Display Window (on vlsi77.ee.iitb.ac.in)

Window Expressions Info Help cādence

Device	Param	Noise Contribution	% Of Total
/PORT0	rn	3.78956e-17	58.96
LG.rs1_2	rn	4.50422e-18	7.01
/M1	rgbi	3.33493e-18	5.19
/M1	id	2.86127e-18	4.45
R0.rpoly2	rn	2.03064e-18	3.16
R0.rpoly1	rn	2.02947e-18	3.16
LD.rs1_2	rn	2.0234e-18	3.15
M1.recn	thermal_noise	1.75805e-18	2.74
CG.rbot1	rn	1.47718e-18	2.30
LS.rs1_2	rn	1.14293e-18	1.78

Spot Noise Summary (in V^2/Hz) at 2.49G Hz Sorted By Noise Contributors
Total Summarized Noise = 6.42769e-17
Total Input Referred Noise = 3.39543e-19
The above noise summary info is for noise data

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Figure 8: Noise Contributions in descending order