EE 619 (ZELE)

Project-2 [35 Marks]

VCO Design and Layout

Submission Deadline: 19th April 2024, 11:55 PM

- Submission must be in the format *ROLLNO_EE619_Project2.pdf* only
- Submissions after deadline will not be accepted under any circumstances
- Report all values preferably in tabular format wherever appropriate
- The submission must contain appropriate plots labelled clearly
- Please go through the supporting material for PSS and PNOISE simulations

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In this project you will design and layout a Voltage Controlled Oscillator (VCO) that can be used to generate LO signals. All the results have to be from the post-layout PEX simulations in the C+CC extraction mode unless otherwise mentioned. The layouts should be symmetric and optimised for area. The VCO centre frequency (f_{OSC}) is assigned based on your roll no. and the allotment is uploaded on Moodle.

Components from UMC 65: NMOS-N_12_LLLVTRF, PMOS-P_12_LLLVTRF, Capacitor-MIMCAPS_20F_MM, Inductor- L_SY30K_RFVIL, Varactor-VARMIS_12_LLRF
Use transistor length = 60 nm.

Components from analogLib: I_{BIAS}, C_L

Use V_{DD} = 1.2 V and C_L = 100 fF.

VCO specifications (post-layout):

• Differential VCO with frequency f_{OSC} for V_{TUNE} = 0.6 V

• Phase noise at max. and min. frequency must be ≤ -100 dBc/Hz at an offset of 1 MHz

• Max. K_{VCO} = 200MHz/V

• Single ended peak-to-peak voltage swing > 0.8 V_{PP}

• DC power dissipation < 3mW

• Frequency tuning should be done with varactors for continuous tuning

A representative top level schematic (Fig. 1) is shown for your reference showing frequency tunability in the VCO using varactors. You can choose any architecture for the VCO. For further reference (design of VCO) please refer “Ch-8, RF Microelectronics by Razavi”.

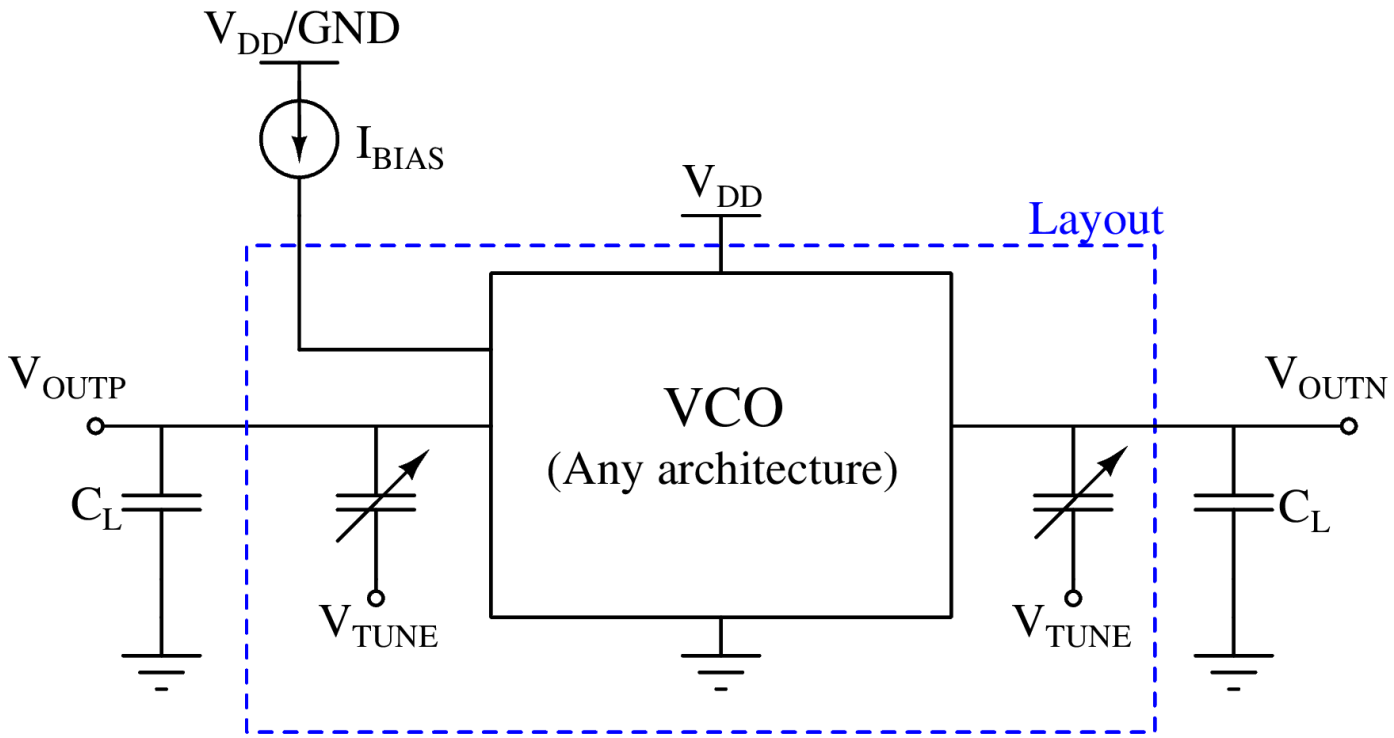

Fig. 1 Top level schematic of the VCO with frequency tuning

1. Provide the VCO architecture along with the component values. Explain your choice of architecture. Briefly describe the design procedure. [5 Marks]
2. Provide a high resolution image of your layout. Provide DRC and LVS summary screenshots. (Points will be awarded based on quality of the layout) [10 Marks]
3. Show the transient signals at output nodes for the f_{OSC} assigned to you. [2 Marks]
4. Plot the frequency vs V_{TUNE} for V_{TUNE} ranging from 0 to 1.2 V. Report frequency tuning range. [5 Marks]
5. Compare the results obtained in 4 with schematic simulation results. [2 Marks]
6. Plot the phase noise (100 KHz to 2 MHz offset) plot of the VCO at f_{OSC}. [4 Marks]
7. Superimpose the phase noise plot (100 KHz to 2 MHz offset) at f_{OSC} from the PEX simulations by running it in C+CC Mode and R+C+CC Mode. [4 Marks]
8. Observe the frequency variation of the VCO by varying the V_{DD} from 1-1.4V. (Keep V_{TUNE} = 0.6 V). Reason out your observations. [3 Marks]

Note: The VCO centre frequency (f_{OSC}) is assigned based on your roll no. and the allotment is uploaded on Moodle.

==========Happy Oscillations==========