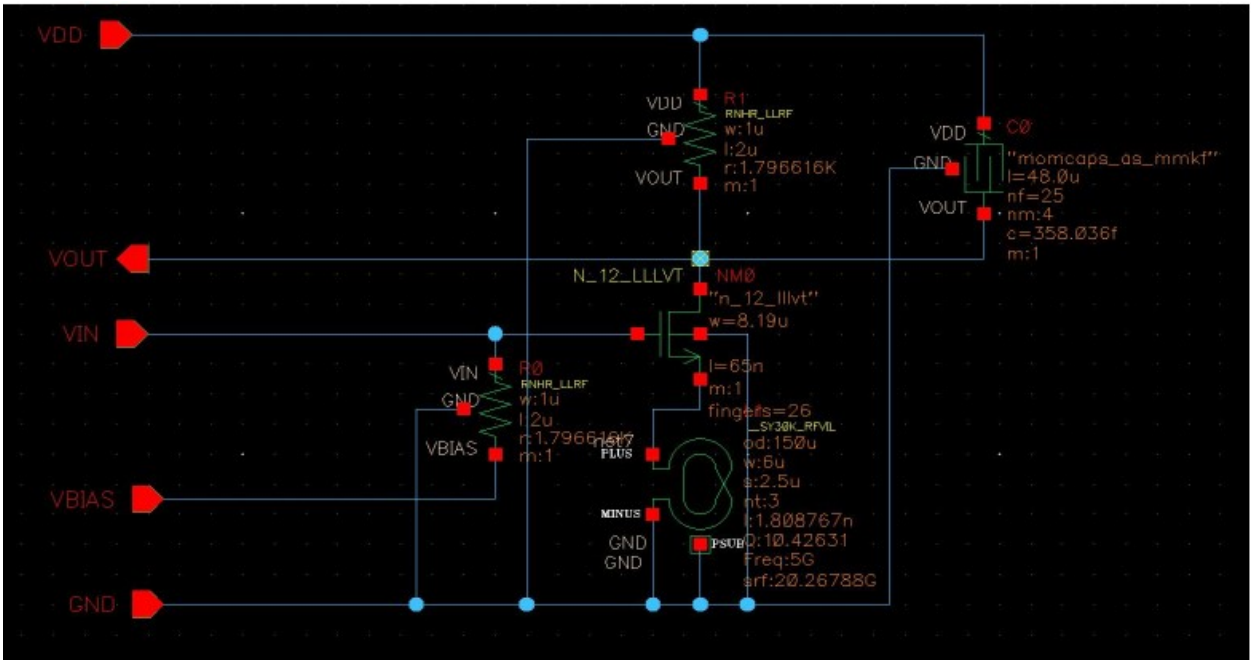
Layout with UMC65

Below is the example schematic used for layout.



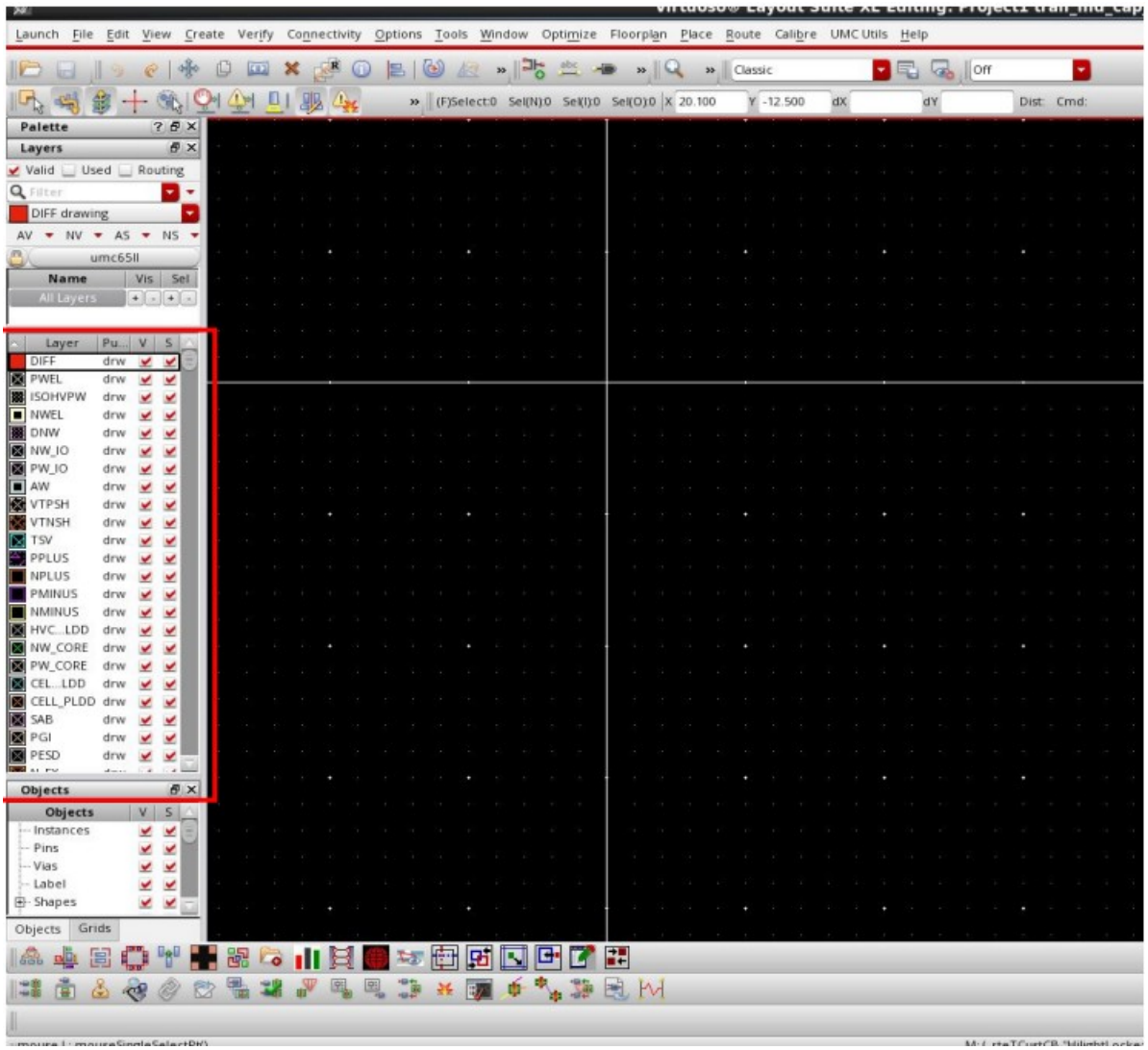
Once the design achieves the target specifications, create a symbol of the circuit as shown above (for detailed procedure of symbol creation - refer the video uploaded in the moodle.)

Once the symbol is ready as shown above,

1. Goto Launch → Layout XL - You will see the below window

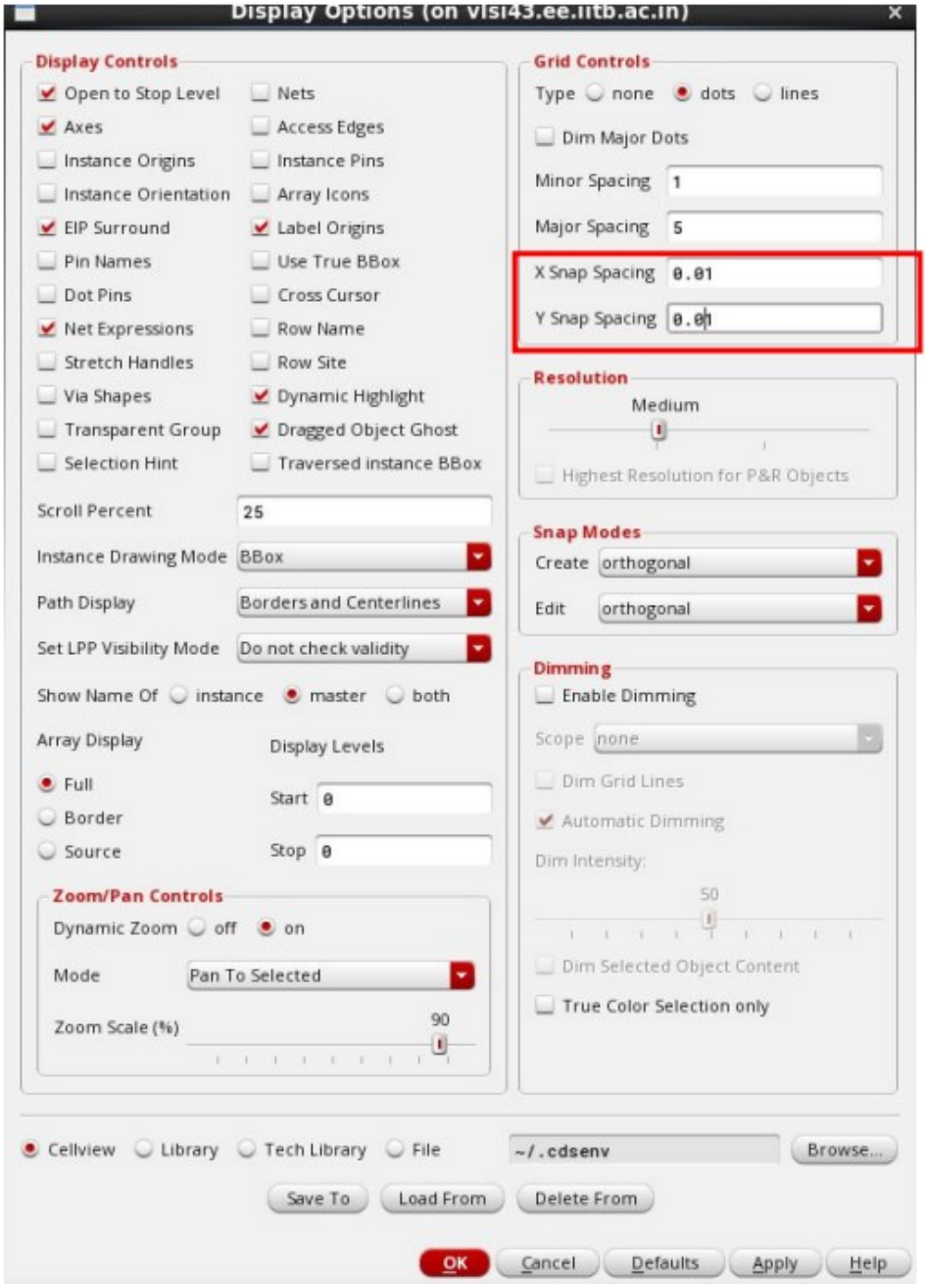
Select “Create New” if you are opening Layout for first time else “Open existing”.

You will see the below window, make sure you see the layers’ information on left side of window as shown below.



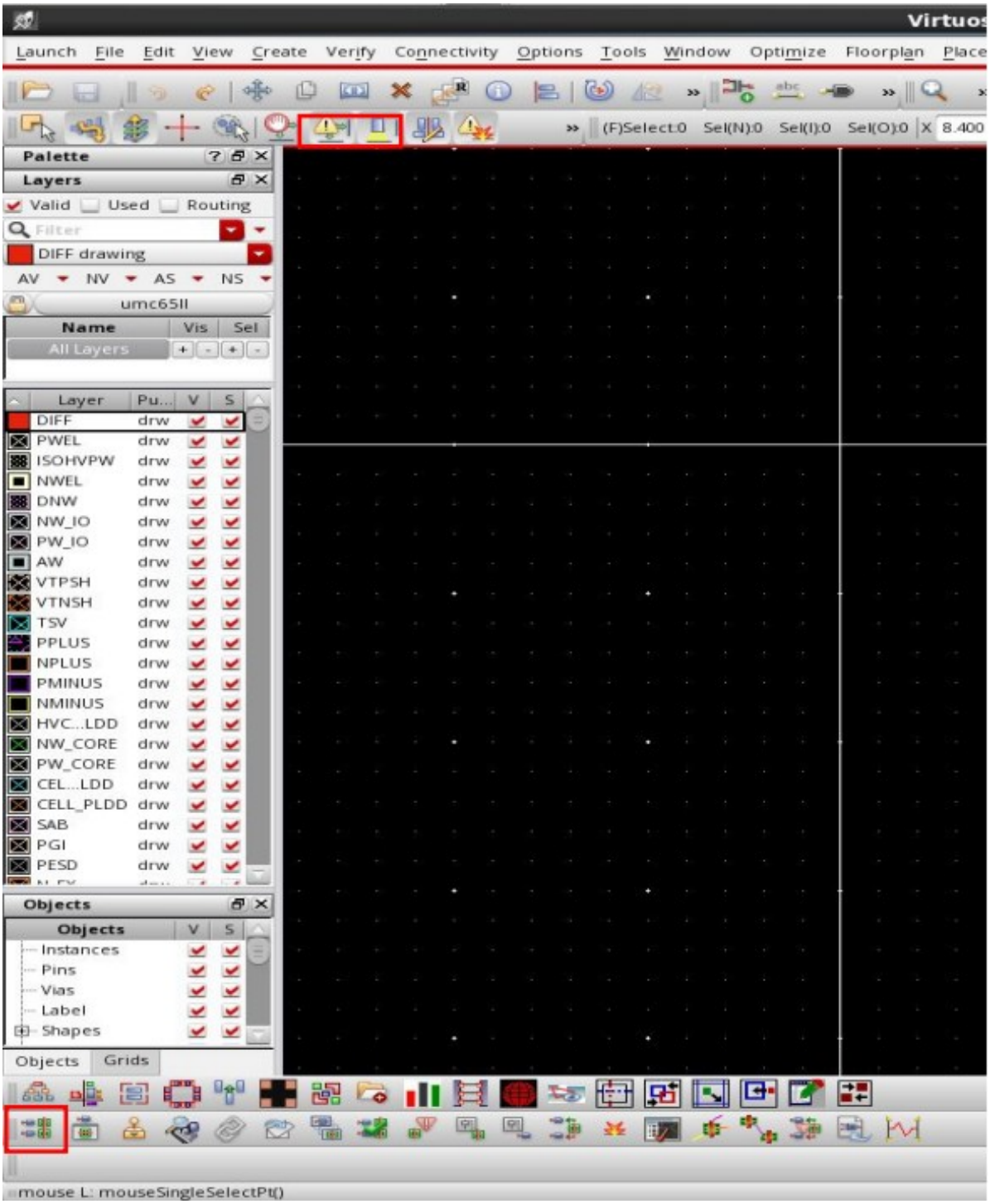
Press E to edit the Display Options.

Every time LayoutXL is opened, make sure grid settings (X & Y-snap spacings) are set properly as shown in below figure. Click apply and Ok after changes are made.

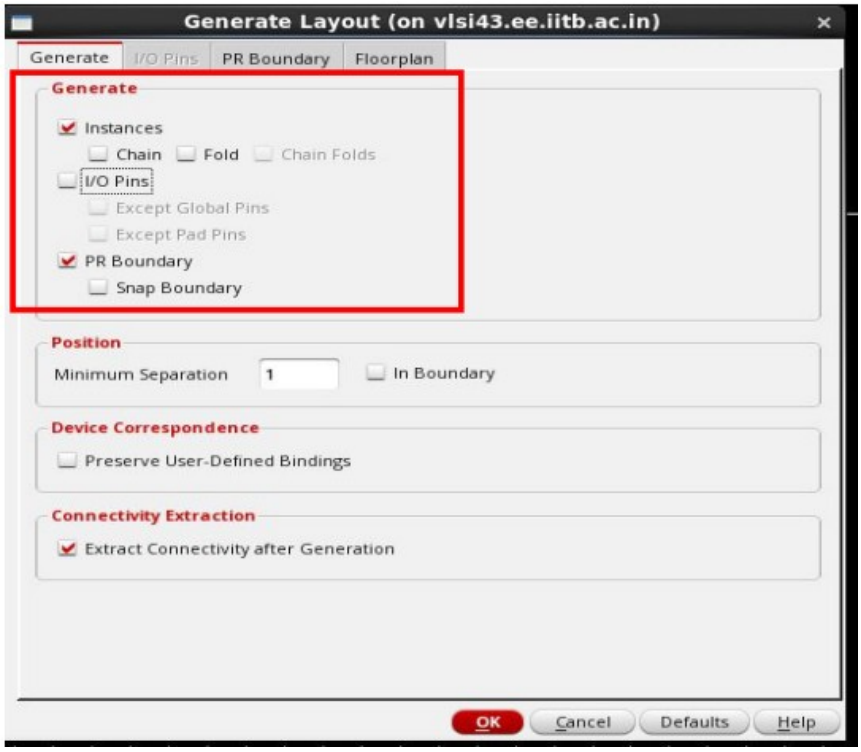


Set DRC post-edit and Notify ON so that minimum spacing issues will be recognized while routing (at top left in the below figure) .

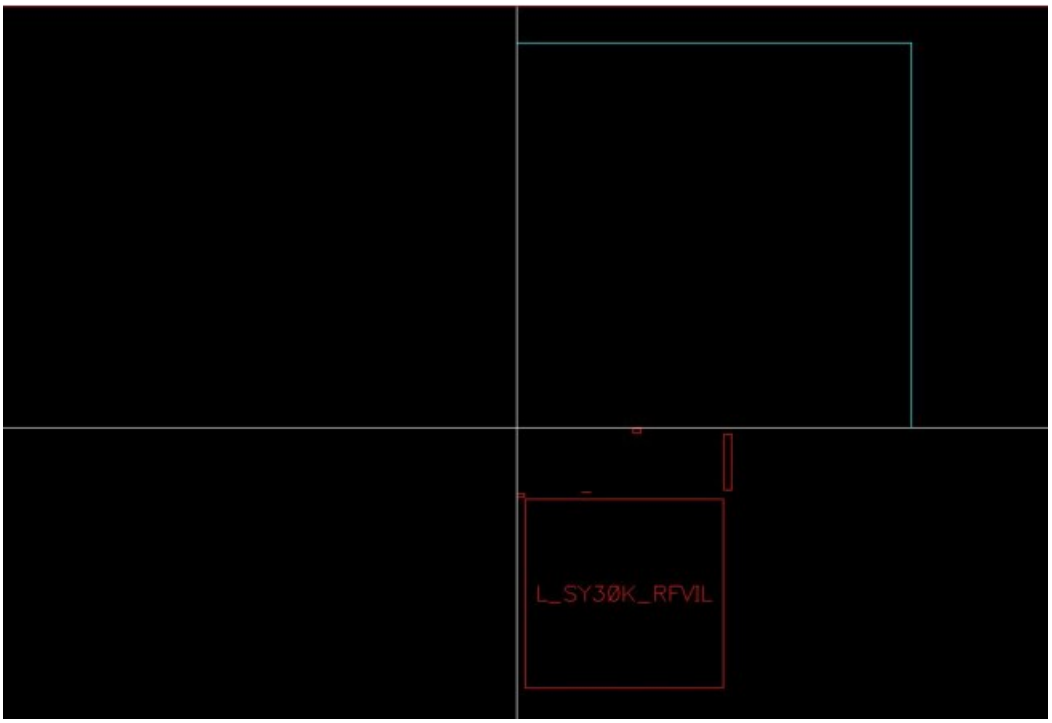
Generate layout of all instances from schematic using the button (at bottom left in below figure).



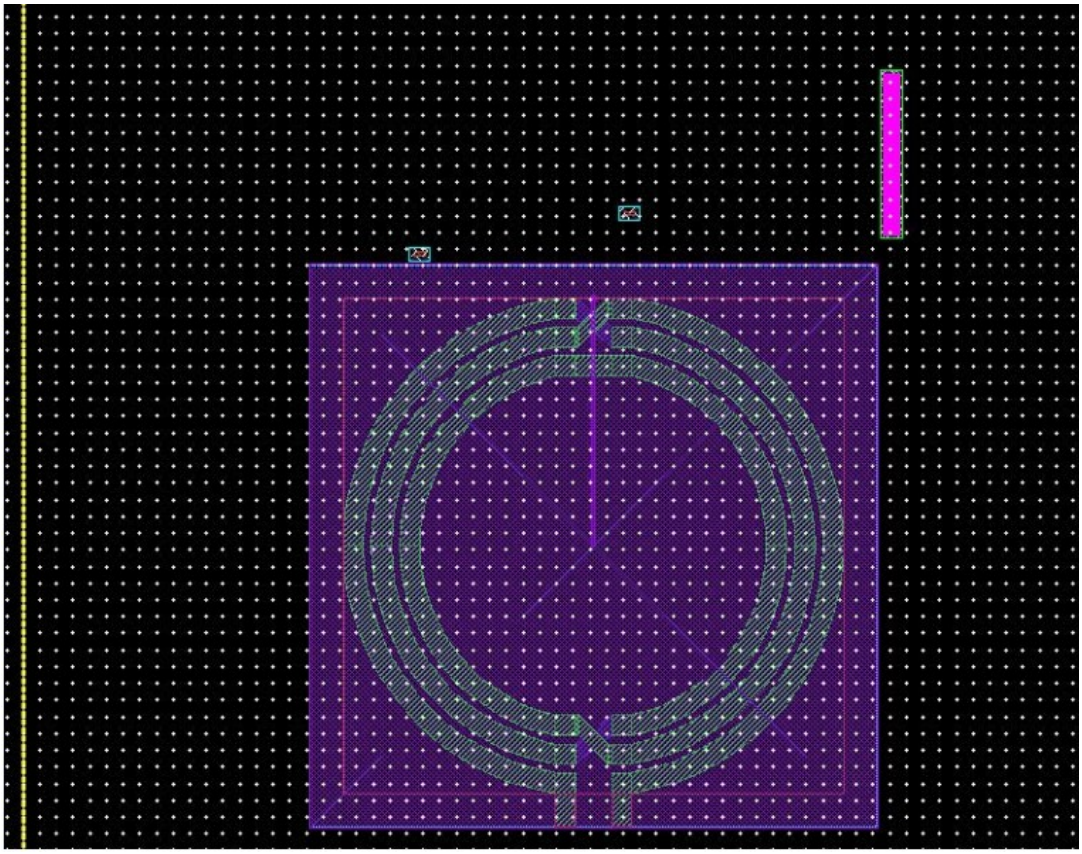
While generating Instances, select the options as shown below.



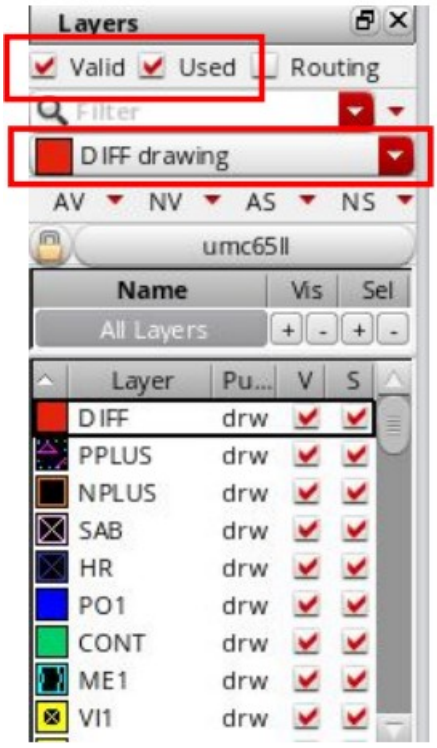
Below shows the layout of instances. The red color boxes are the layout outline of generated instances and the blue box is PR boundary (Place and Route).



Press Shift +F to view the layout of the instances, below figure shows the layout of the instances.



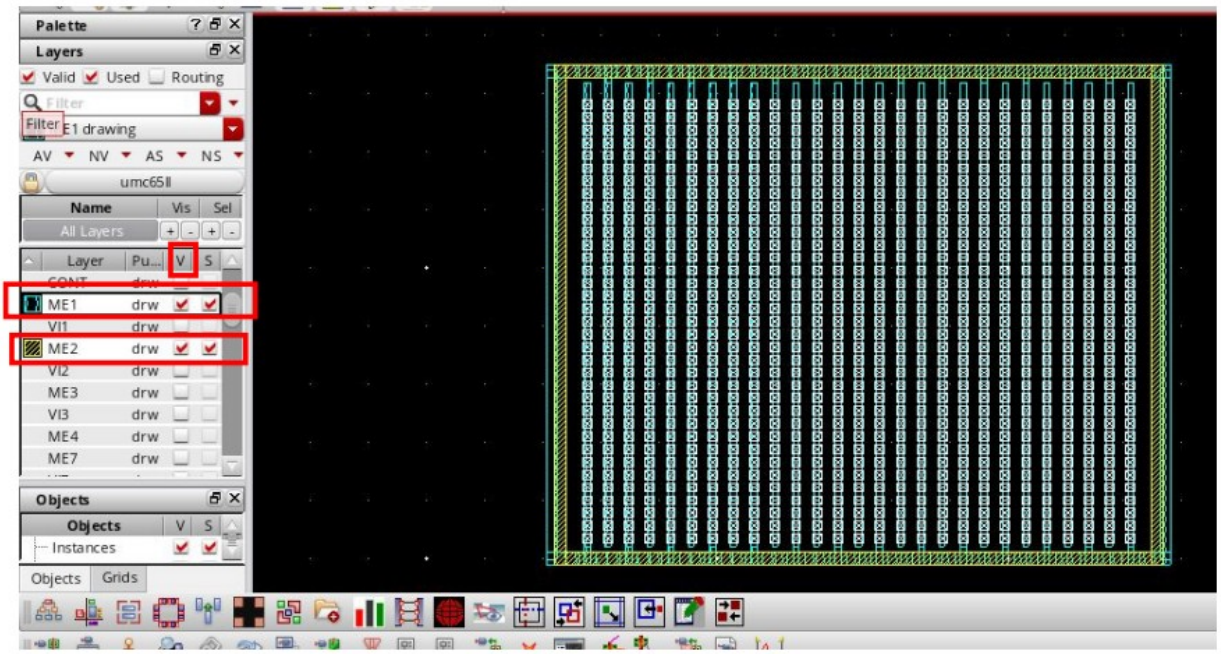
Select “Used” in options of layers as shown below.



You can select the layer you want to draw (to route) as highlighted in above figure. Use **R** or **Shift+ctrl+W** or any other related option to route. If more help is required here, you can refer the Video.

Observe the metal layers used at each terminal of the instance, so that the appropriate metal can be used for connectivity to the particular terminal. You can turn on or turn off metal view as follows. This may help in identifying the metal to be used for connectivity.

- Click on **V**, and select the layers to view. In below figure ME1 and ME2 are selected by selecting the checkbox against it.

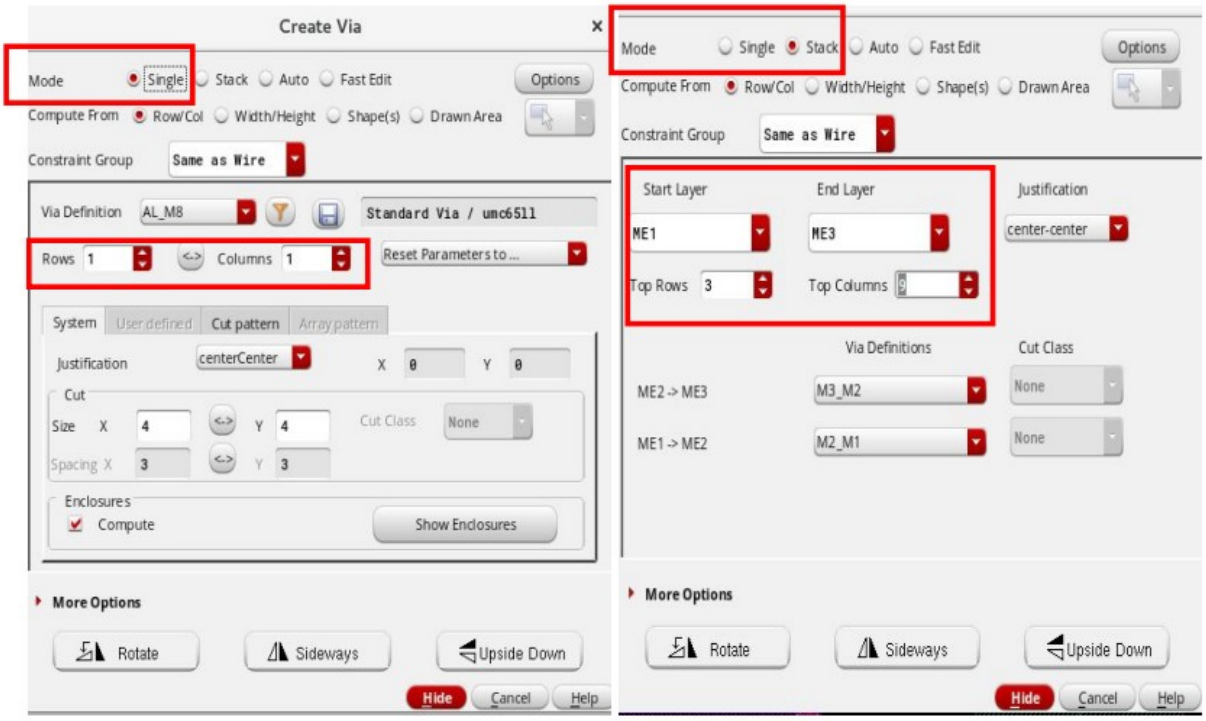


Creating Contacts: Press O for “create Via” window.

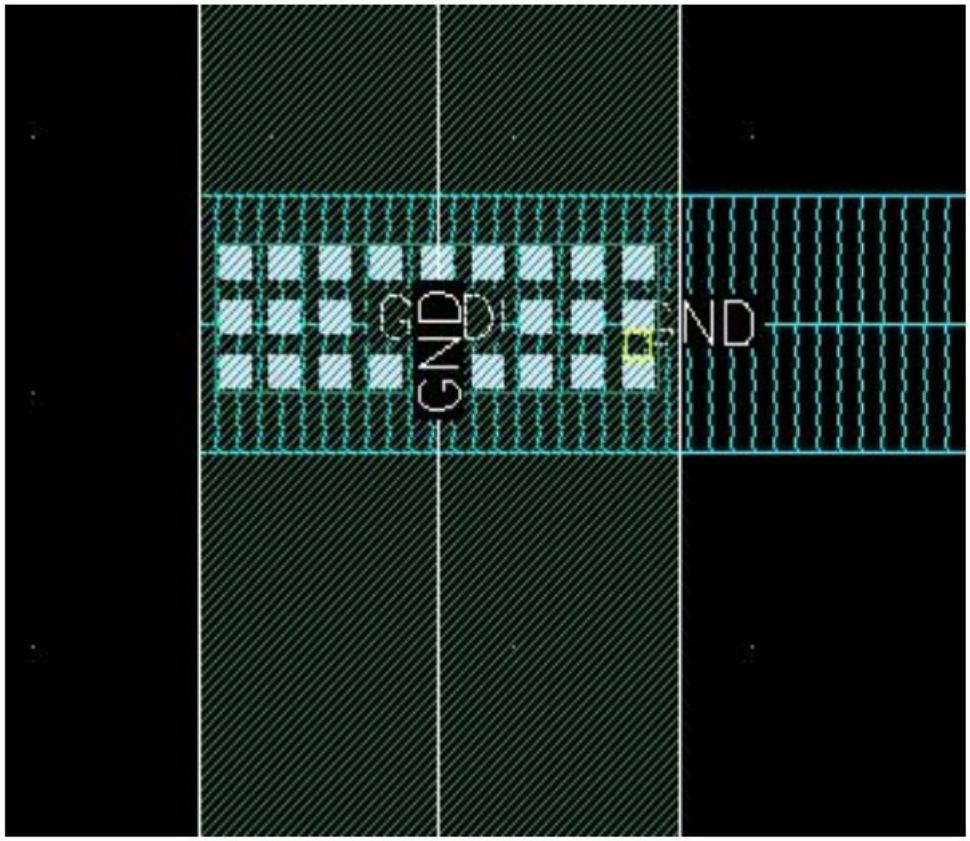
- If you need contact between Metal N and Metal N+1 or Metal N-1, select single contact and select the appropriate Via definition.

- If you need contact between Metal N and any higher (>N+1) or lower metals (< N-1), select the stack mode. Mention the choice of start metal and end metal. Below figures illustrates the above two points respectively.

- Here a stacked contact between M1 and M3 is selected. If multiple rows/ columns of contacts are required, it can be changed accordingly, here multiple stacked contacts of 3 X 9 are selected.



Above generated 3 X 9 ME1-ME3 contact looks as follows, make sure you have enough contacts placed according to metal width.



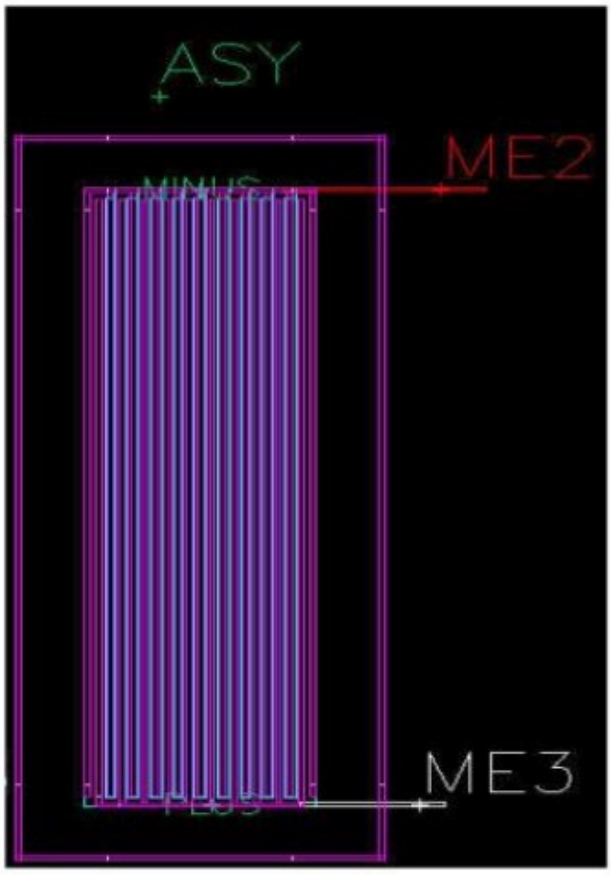
Connecting MOM caps:

Depending on the top and bottom metals of the capacitor (press Q on capacitor in schematic), PLUS terminal has to be connected with bottom metal +2 and MINUS terminal has to be connected with bottom metal+1. You may need to use Stacked contacts.

For Example refer below picture.

4-2. ASymmetrical MOMCAPS

- The example is as shown below (ME1 to ME6):
  - BM=1 (Button metal is ME1)
  - Metal Ring : ME1,ME4,ME5,ME6
    - User can be pin out
      - PLUS : ME2, ME3
      - MINUS : ME2, ME3

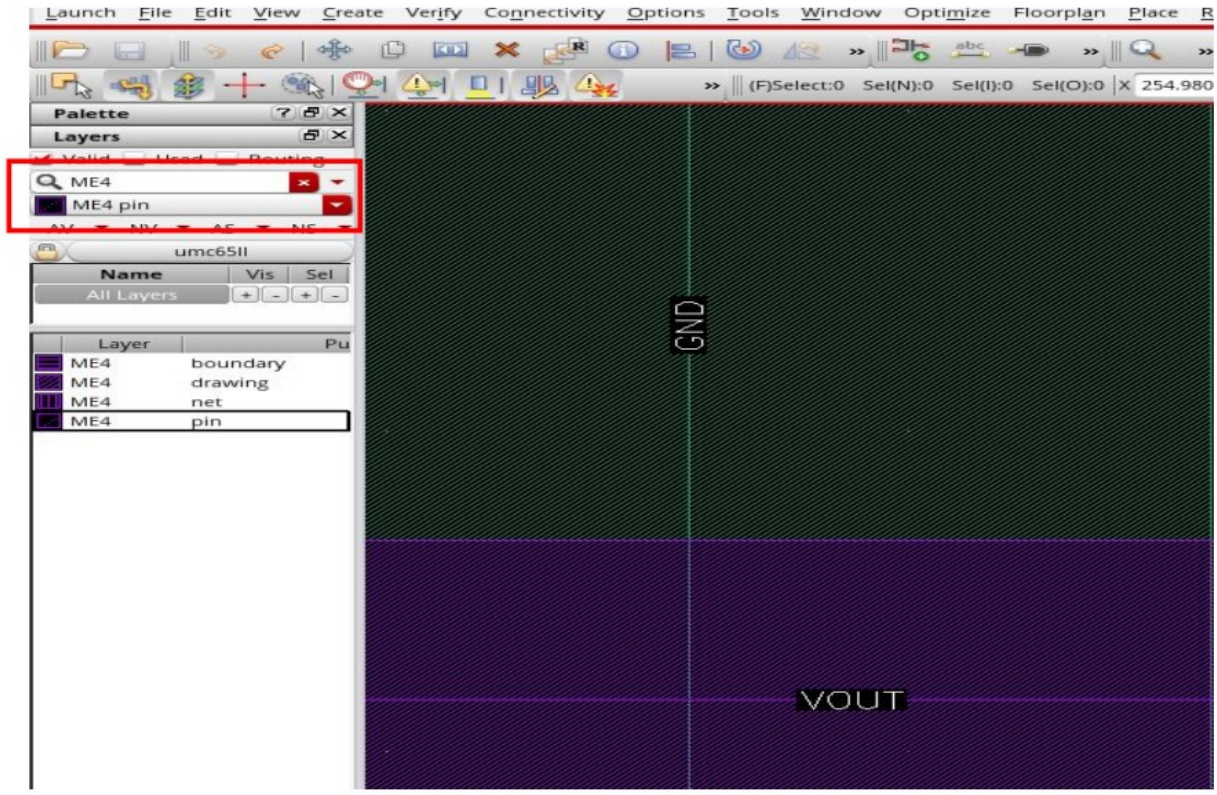


Resistor connections:

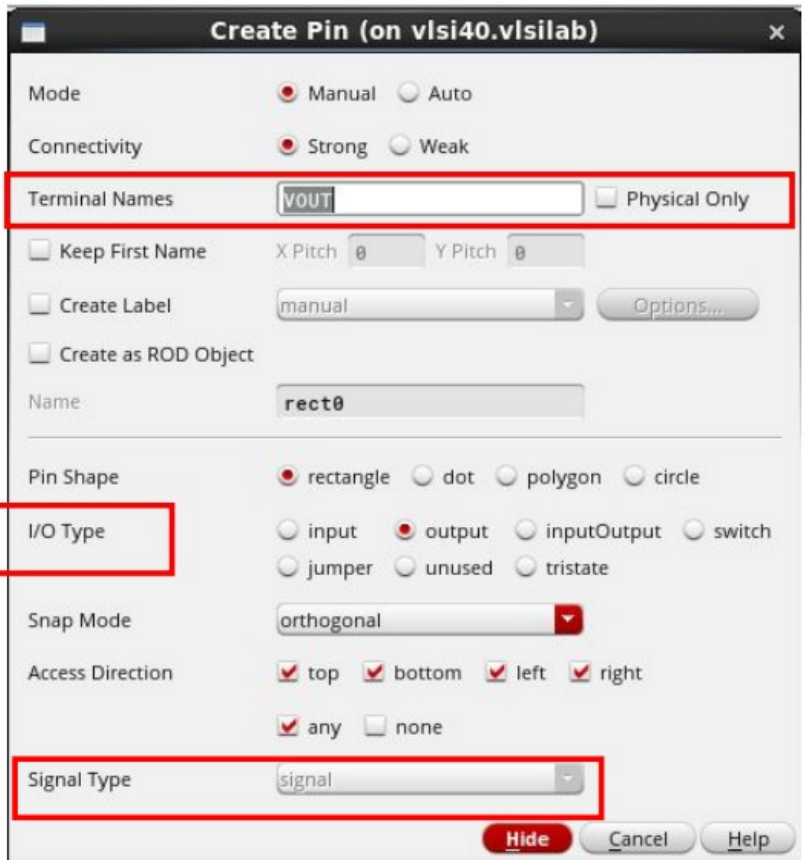
Find the metal used for resistor terminals (try enabling each metal individually as mentioned before), and extend the terminals with that metal to connect to the other metal tracks in the layout. You may need to use stacked contacts. Once all routing is done, create pins and labels.

Creating Labels/Pins:

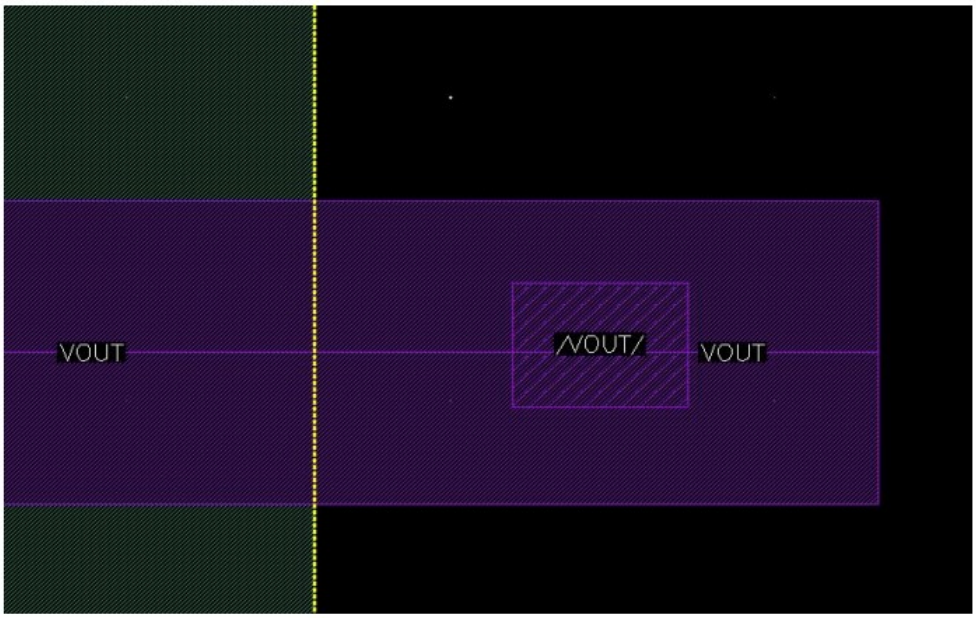
Select the required Metal pin layer, below VOUT is routed in M4, and for creating a pin, **ME4 pin** should be selected in layers.



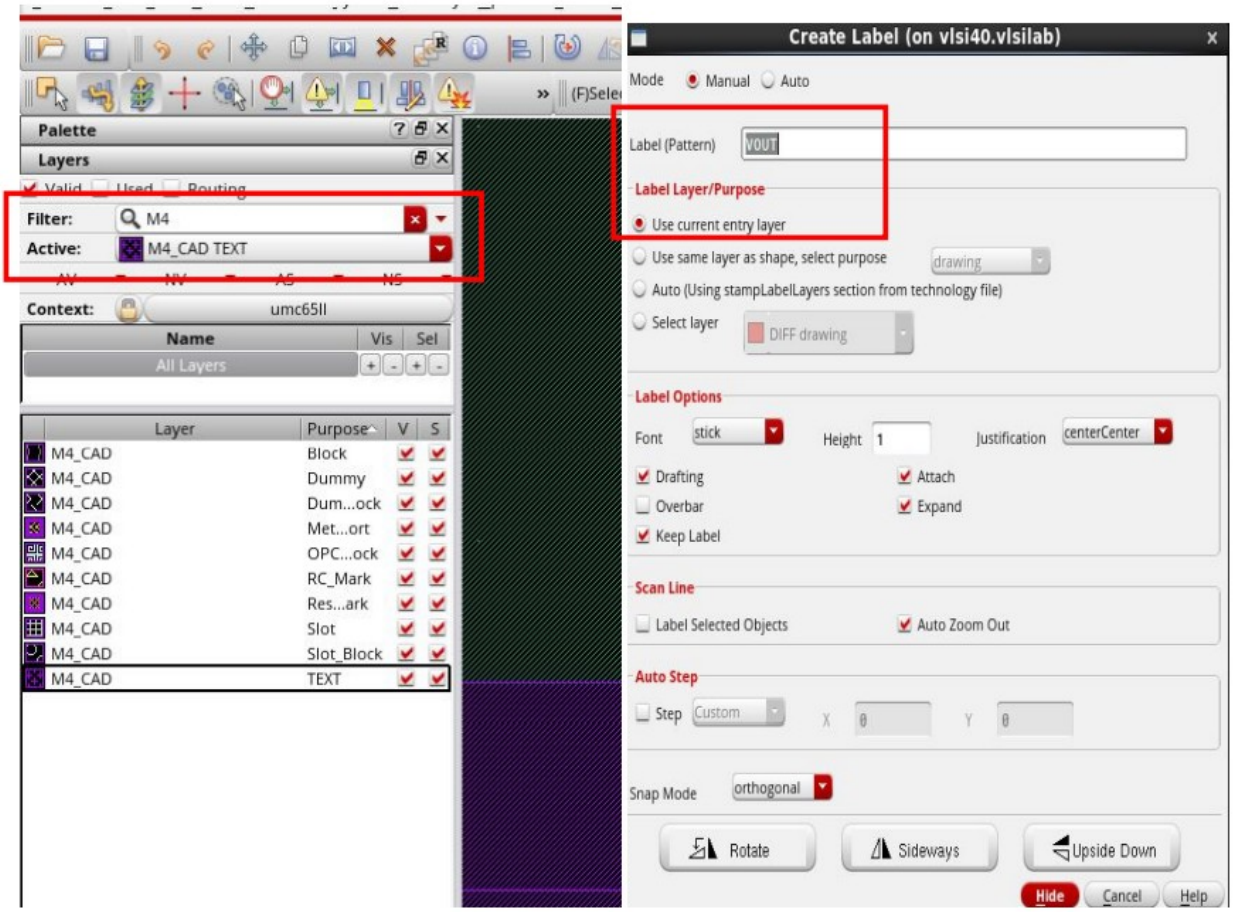
After selecting required metal pin in layers, press **Ctrl+P** to open Create pin window. Enter the appropriate terminal name, here it is chosen as **VOUT**, select the **I/O type** and **Signal type**. While creating pin for VDD or GND, select power and ground signal types respectively. Press hide after entering required settings. Below shows the create pin window.



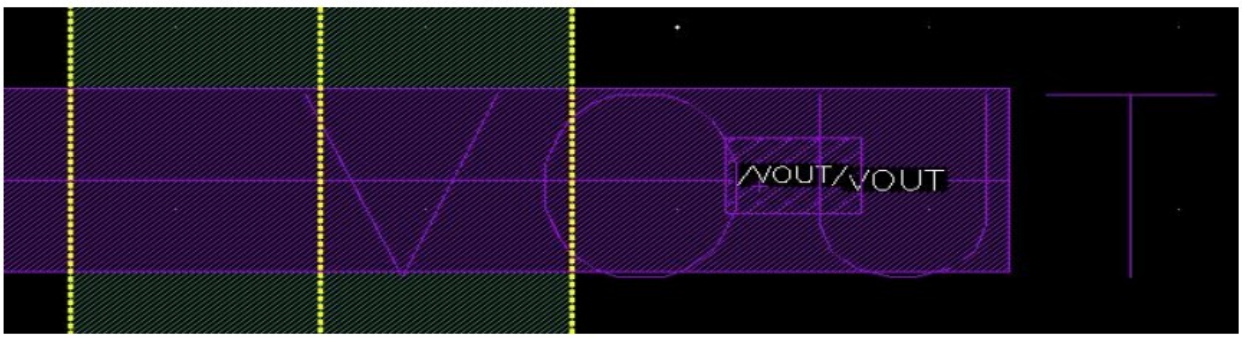
Click on the metal layer where pin needs to be created and draw the pin. Below is an example.



To create Label for the pin, press **'l'** on the pin to open create label window and select M**X**_CAD_TEXT in layers. Here, since ME4 is used to create pin, M4_CAD_TEXT is used to label it. Below shows the selection of M**X**_CAD_TEXT and create label window. Press hide after selecting the required options.



Make sure the pointer of text label is kept in pin area, below is pin and label of VOUT.



After all pins are created, Run DRC .

To run DRC:

- DRC rule file can be found at:

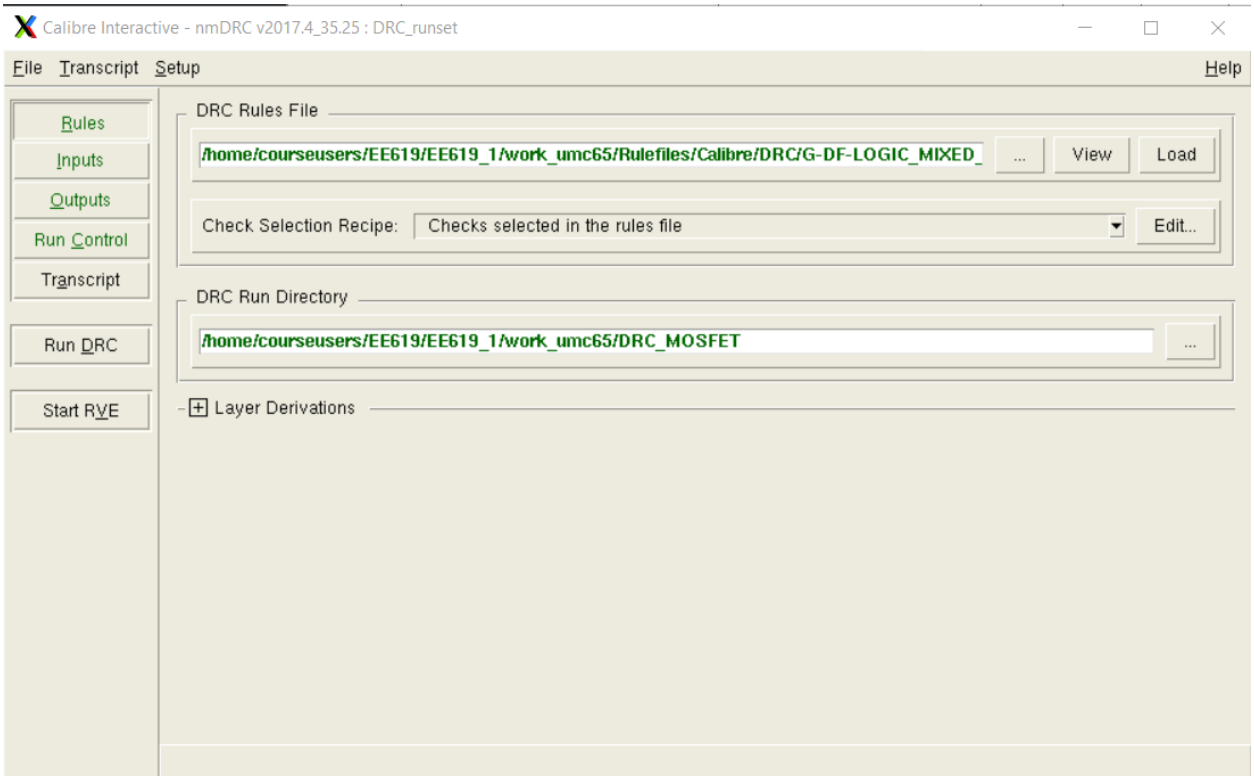
  /home/courseusers/EE619/EE619_XX/work_umc65/Rulefiles/Calibre/DRC/

  where XX represents your login ID number.

- Rule file : **G-DF-LOGIC_MIXED_MODE65N-1P8M1T0F1U-LL-Calibre-drc-1.19_P1**

- Now, to run DRC Menu→ Calibre → Run nmDRC

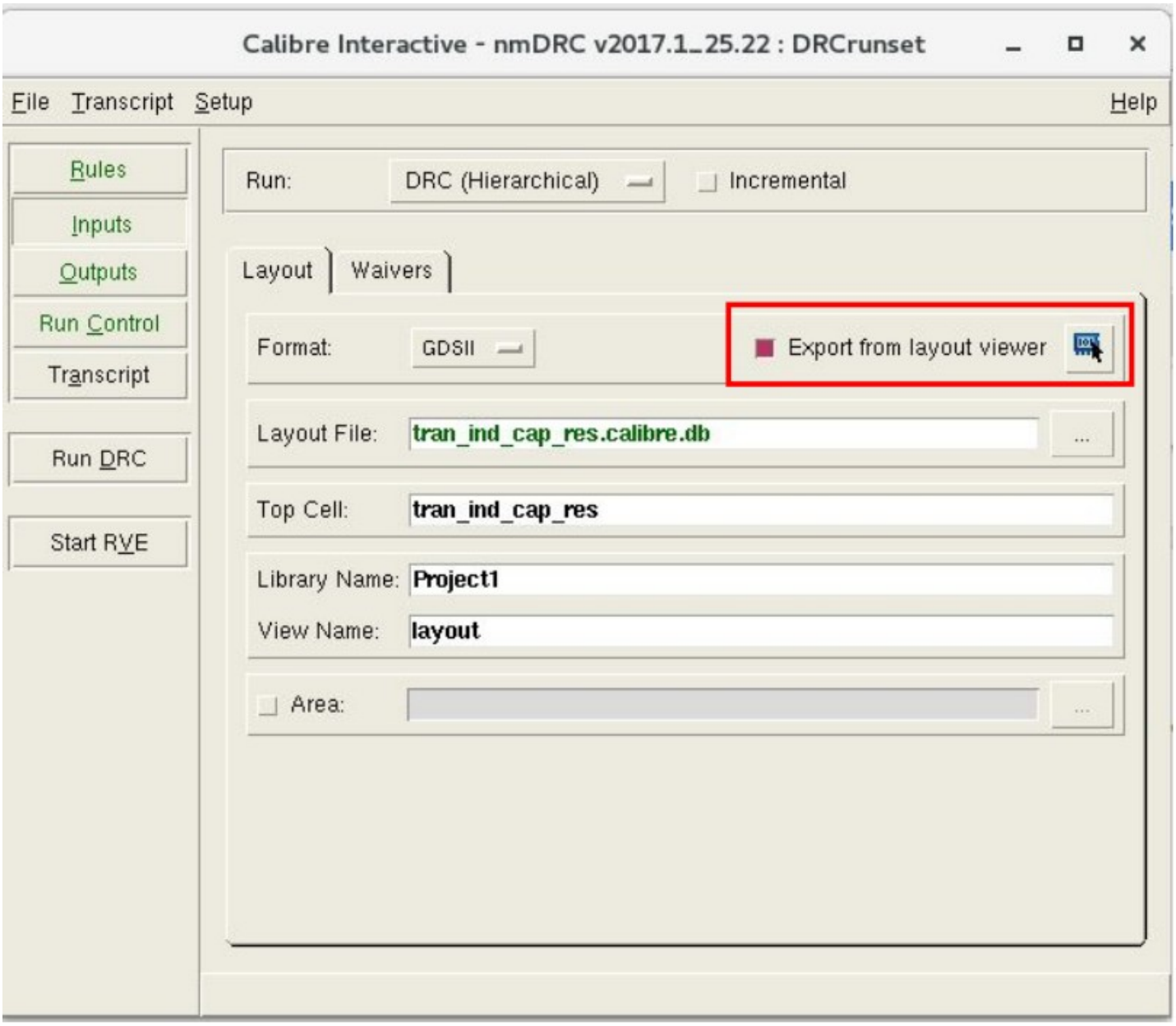
Calibre Interactive window will appear as shown below.



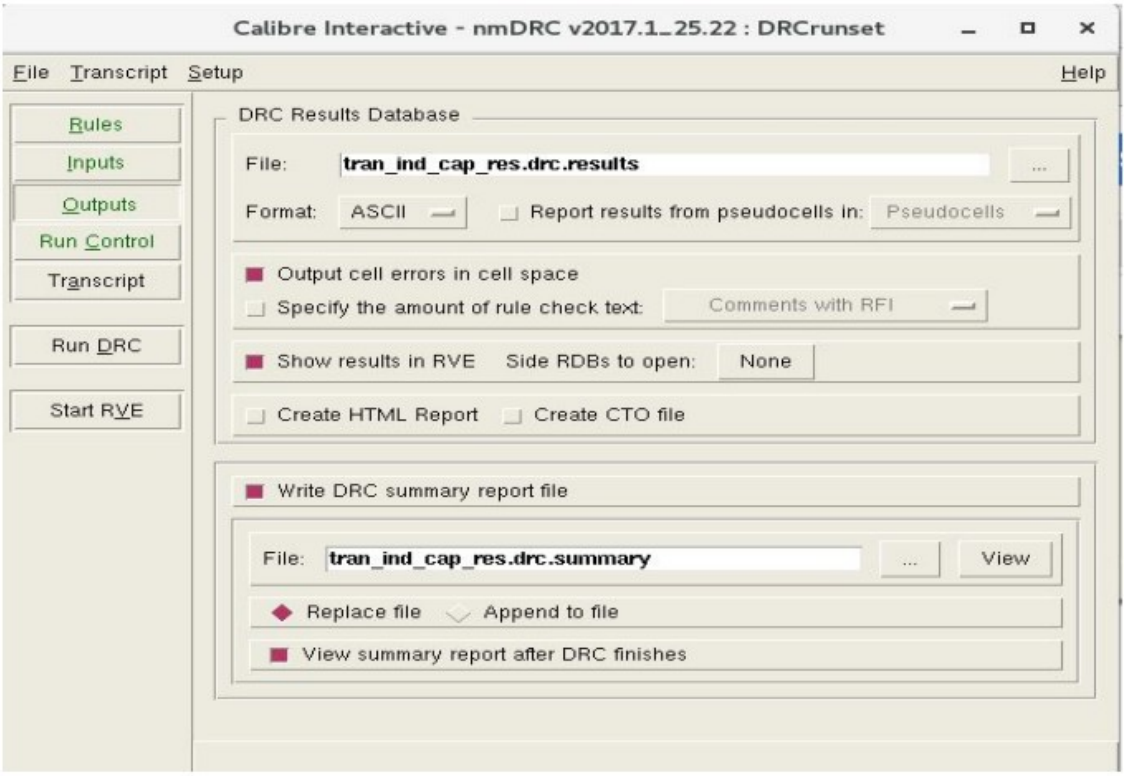
In the **DRC Rules file**, browse to the edited DRC file. - make sure you select the right one. (Hint: file name contains *1P8M1T0F1U-LL*)

Provide a **DRC run directory**, where tool can dump the log/summary files. It can be any directory as shown above (DRC_MOSFET), If required you can create a new one.

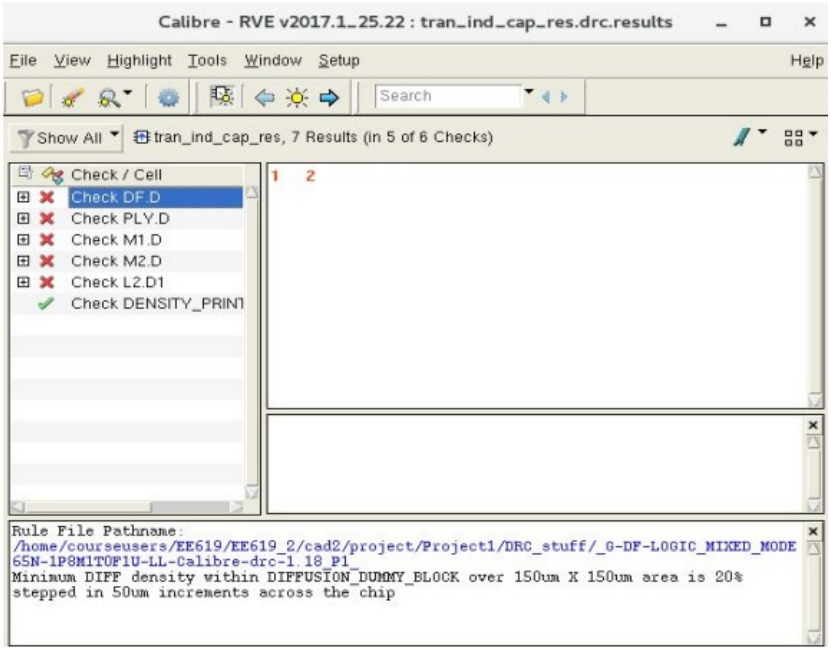
Settings in **DRC inputs**, - follow the below figure.



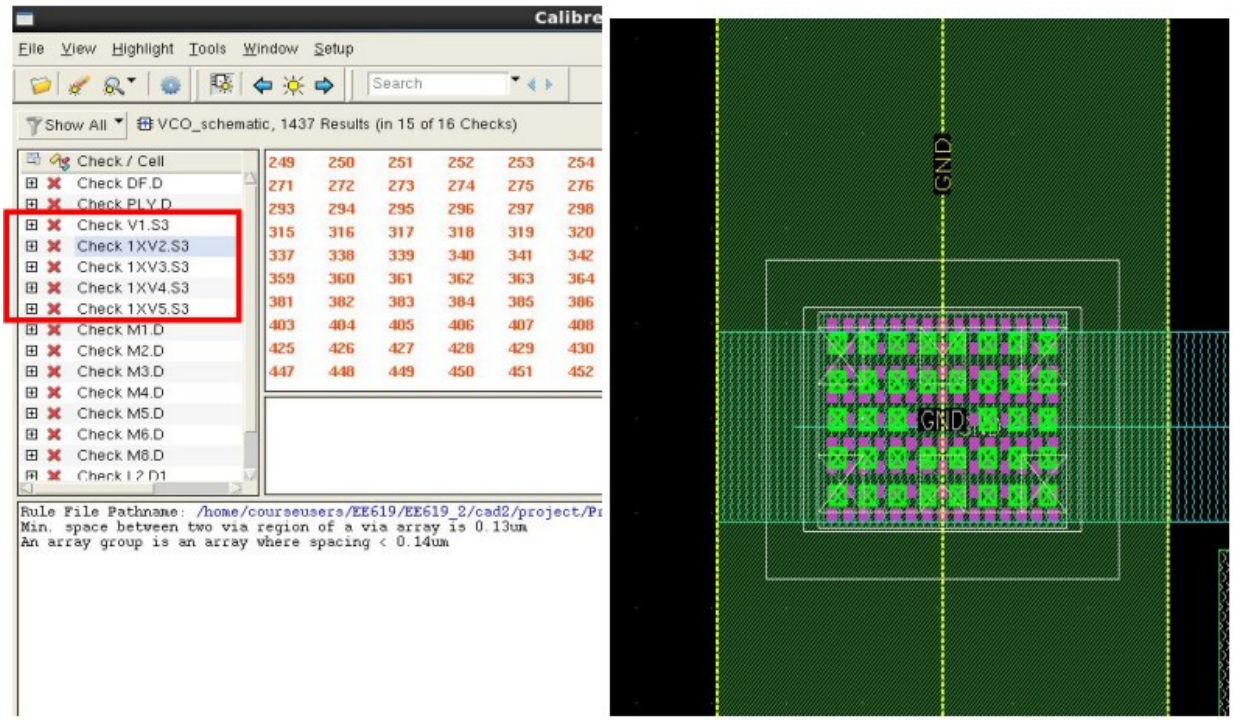
Outputs : should look like the following (here **tran_ind_cap_res** is the schematic name). Let the Run Control settings be the default ones, need not to change anything.



Click **Run DRC** to check the DRC errors. Calibre RVE window with DRC results will pop up at the end of DRC run. You can ignore drc errors about density (Check*.D) and you can also ignore if any DRC errors exist inside the stacked contacts. Below is the calibre RVE window that shows the DRC errors.



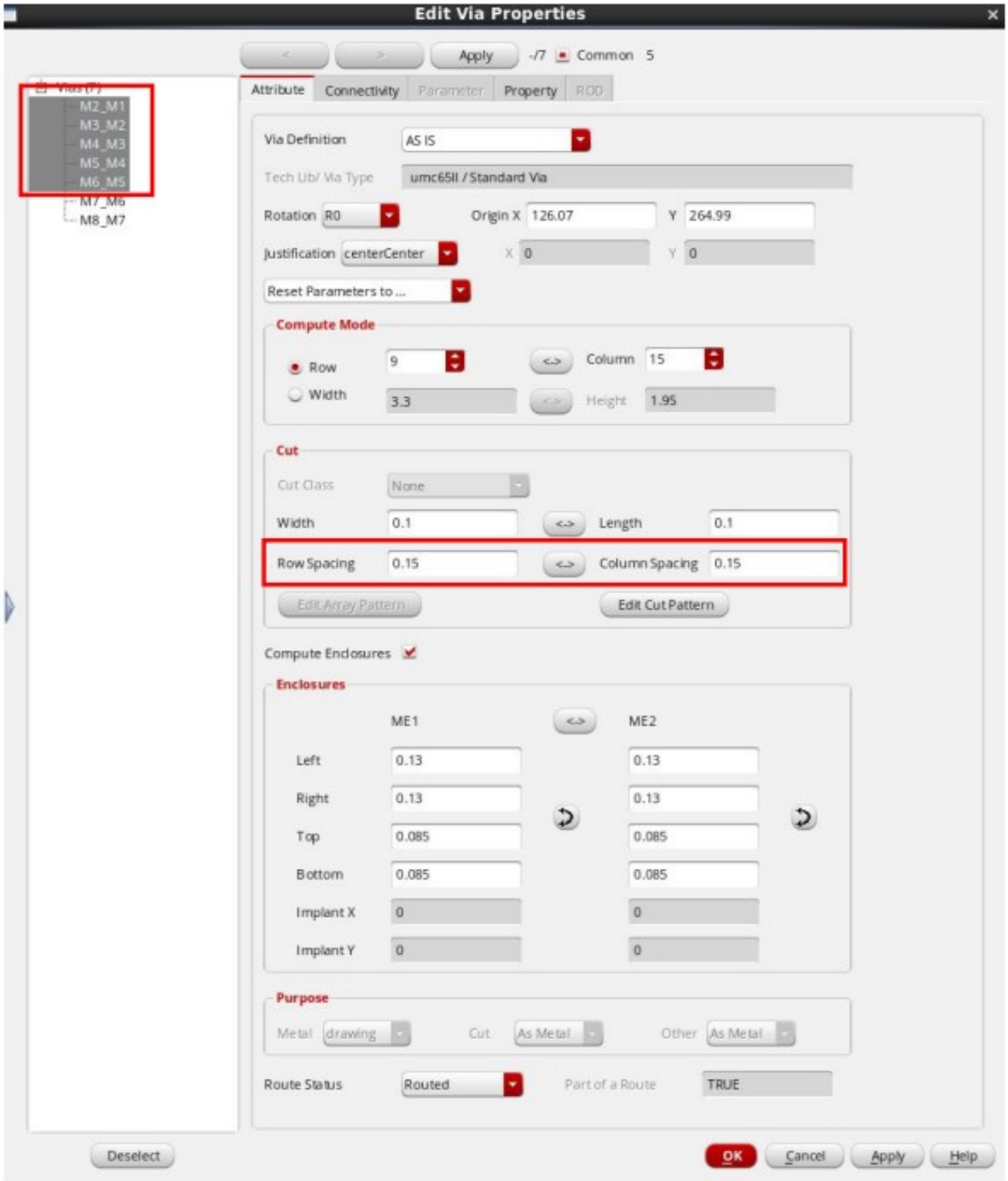
To resolve DRC errors related to minimum spacing between vias (in stacked contacts), you can follow the below procedure.



Above shows DRC error due to default spacing (0.11um) between vias (M1-M2, M2-M3, M3-M4, M4-M5, M5-M6) and the right side is the stacked contact. To clear this sort of errors, the spacing between the vias have to be increased.

Note that spacing rules from M1- M5 are similar whereas they vary in case of metals M6-M8. For M1-M5 (vias including any of these metals) the minimum spacing between the vias should be > 0.13um as indicated above. To change the via spacing select the via, press **'Q'** for properties window and change the spacing as shown below.

Note that all the contacts M1-M2, to M5-M6 should be selected to change spacing at once.


Edit Via Properties
Apply
-/7
Common 5
Vias (7)
M2_M1
M3_M2
M4_M3
M5_M4
M6_M5
M7_M6
M8_M7
Attribute
Connectivity
Parameter
Property
ROD
Via Definition
AS IS
Tech Lib/ Via Type
umc65ll / Standard Via
Rotation
R0
Origin X
126.07
Y
264.99
Justification
centerCenter
X
0
Y
0
Reset Parameters to ...
Compute Mode
Row
9
Column
15
Width
3.3
Height
1.95
Cut
Cut Class
None
Width
0.1
Length
0.1
Row Spacing
0.15
Column Spacing
0.15
Edit Array Pattern
Edit Cut Pattern
Compute Enclosures
Enclosures
ME1
ME2
Left
0.13
0.13
Right
0.13
0.13
Top
0.085
0.085
Bottom
0.085
0.085
Implant X
0
0
Implant Y
0
0
Purpose
Metal
drawing
Cut
As Metal
Other
As Metal
Route Status
Routed
Part of a Route
TRUE
Deselect
OK
Cancel
Apply
Help

Once DRC errors are resolved, You can run LVS.

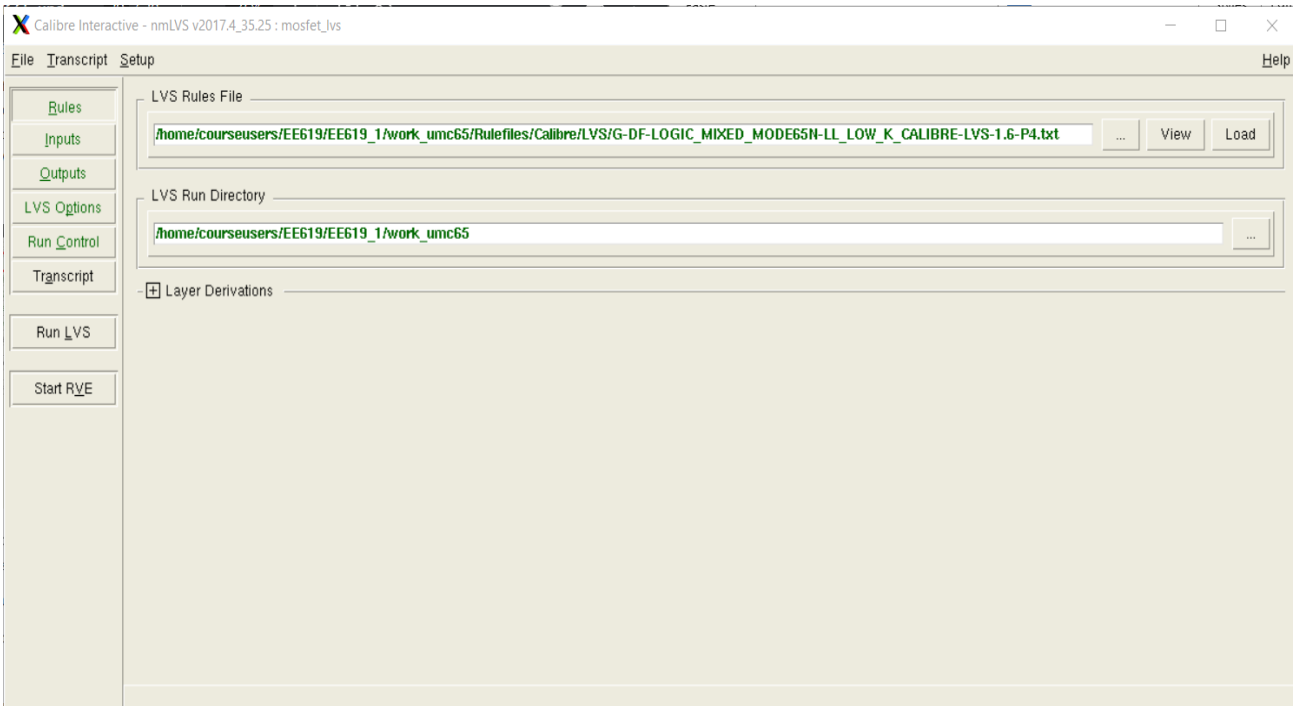
To run LVS :

LVS rule file is available at:

/home/courseusers/EE619/EE619_XX/work_umc65/Rulefiles/Calibre/LVS/G-DF-LOGIC_MIXED_MODE65N-LL_LOW_K_CALIBRE-LVS-1.6-P4.txt

where XX represents your login ID number.

- To invoke LVS, click on menu→ calibre → Run nmLVS. Below shows the LVS window.

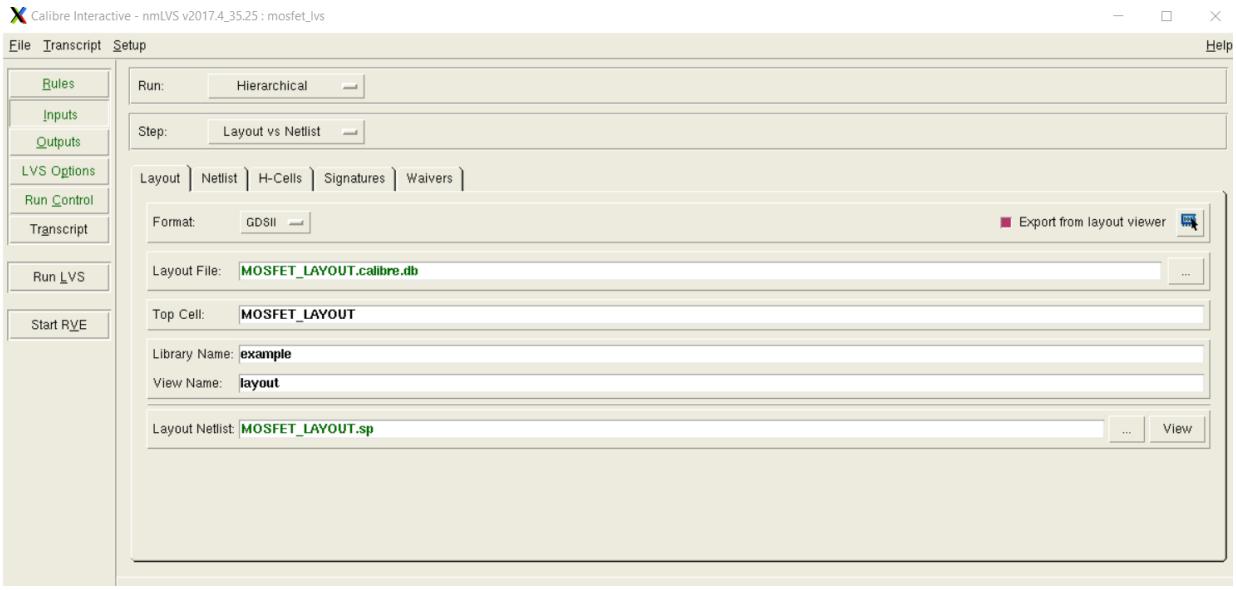


Browse the LVS Rules File to the modified rules file. If required, you can give different destination directory than the default one.

You need to add CDL_include_file.cir file to source netlist inputs. CDL_include_file.cir can be found at

/home/courseusers/EE619/EE619_XX/work_umc65/Rulefiles/Calibre/

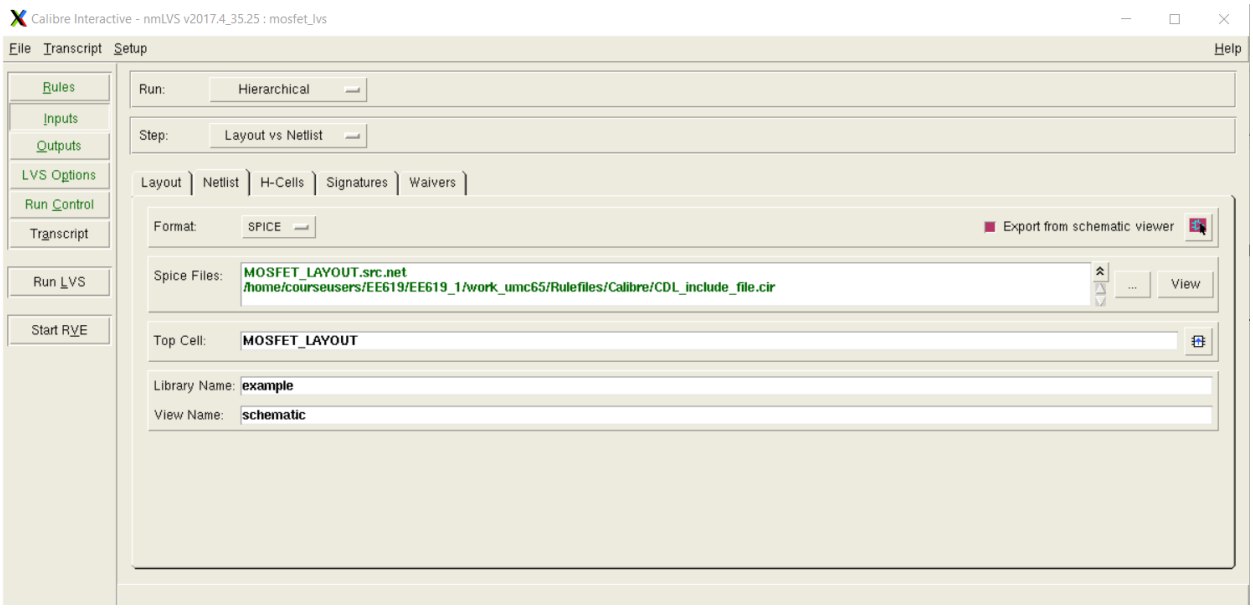
Below shows the inputs of LVS. **Inputs** from **layout** should look as follows, make sure Export from layout viewer is enabled.



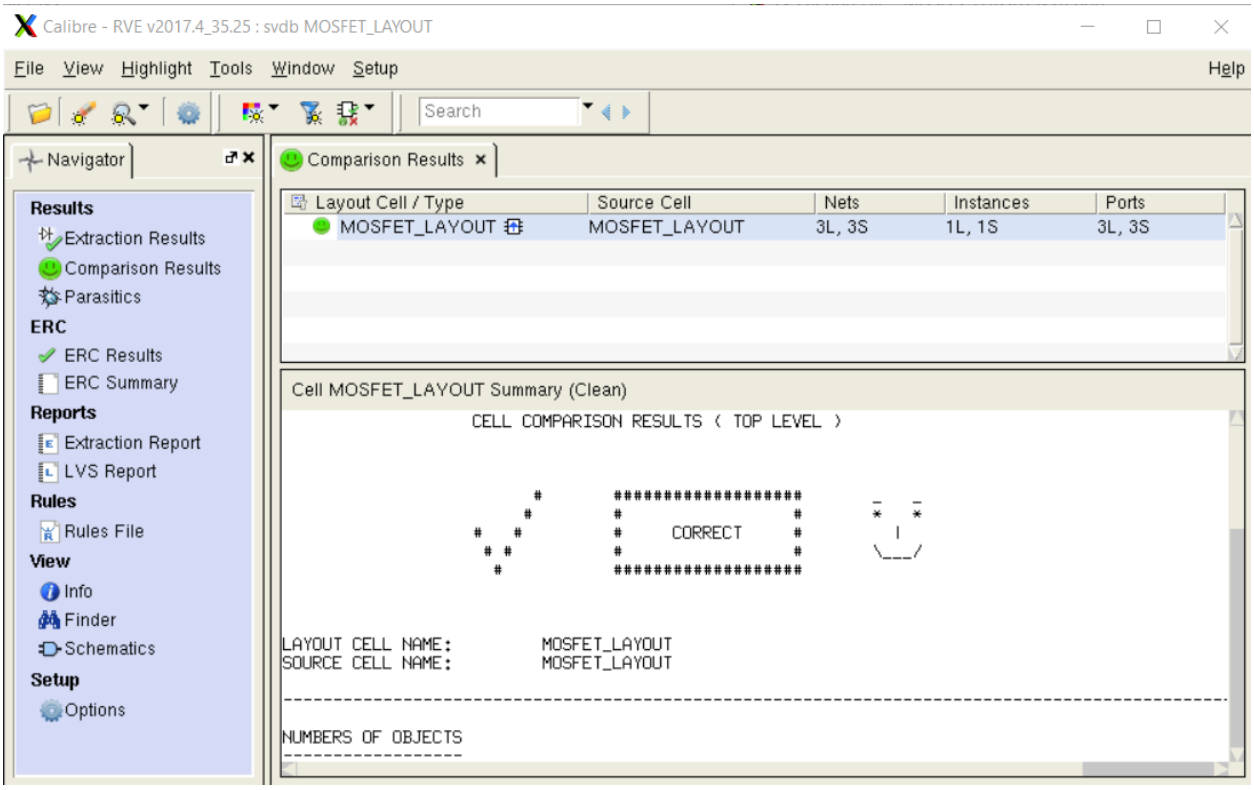
In Netlist tab, ensure Export from layout viewer option is enabled.

In the **Spice files** option, **CDL_include_file.cir** should be added along with *.src.net file. Press on ^ symbol and press **Enter** to get new line in Spice files, then browse to add

/home/courseusers/EE619/EE619_XX/work_umc65/Rulefiles/Calibre/CDL_include_file.cir. After adding the file it should look as follows.



After making above mentioned changes, Click on **Run LVS**. After completion of the run, calibre RVE window will pop-up where you can see the mismatches (if any) between Layout and schematic. Click on "**Comparison results**" to check mismatches. You should clear all mismatches and finally should ensure designs are matched [The Green Smiley :)].



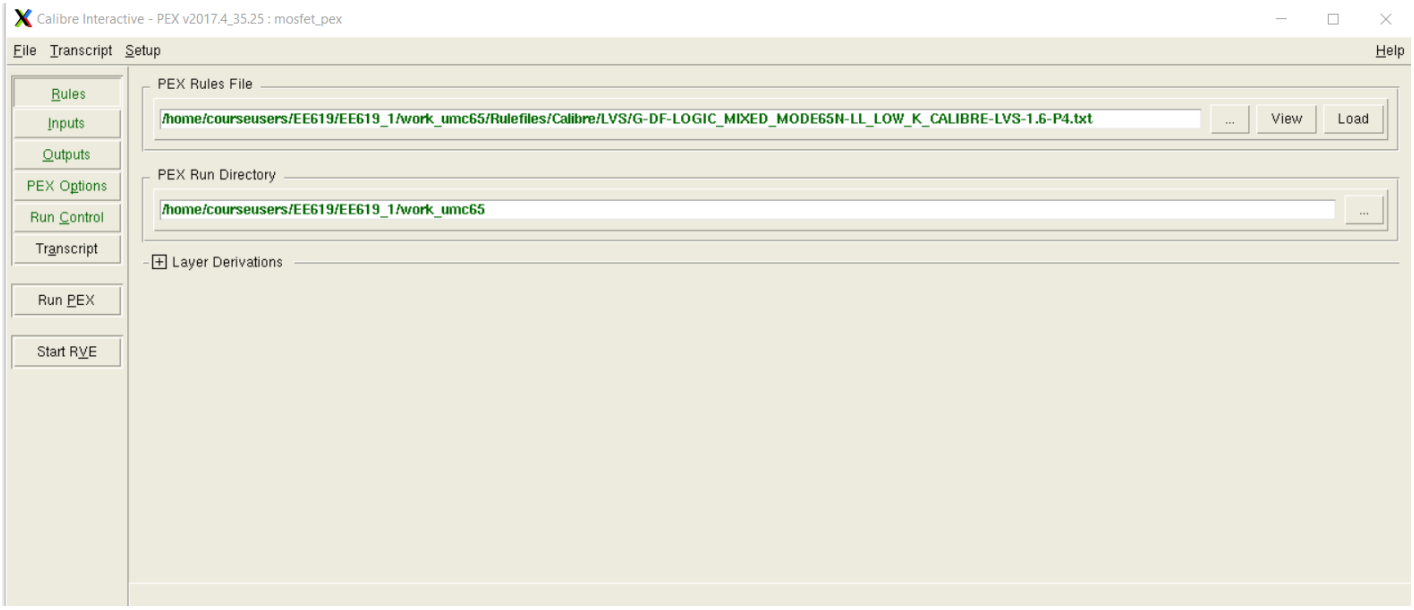
After successful completion of LVS, PEX can be run.

To Run PEX:

PEX rule file can be found at:

/home/courseusers/EE619/EE619_XX/work_umc65/Rulefiles/Calibre/LVS/G-DF-LOGIC_MIXED_MODE65N-LL_LOW_K_CALIBRE-LVS-1.6-P4.txt

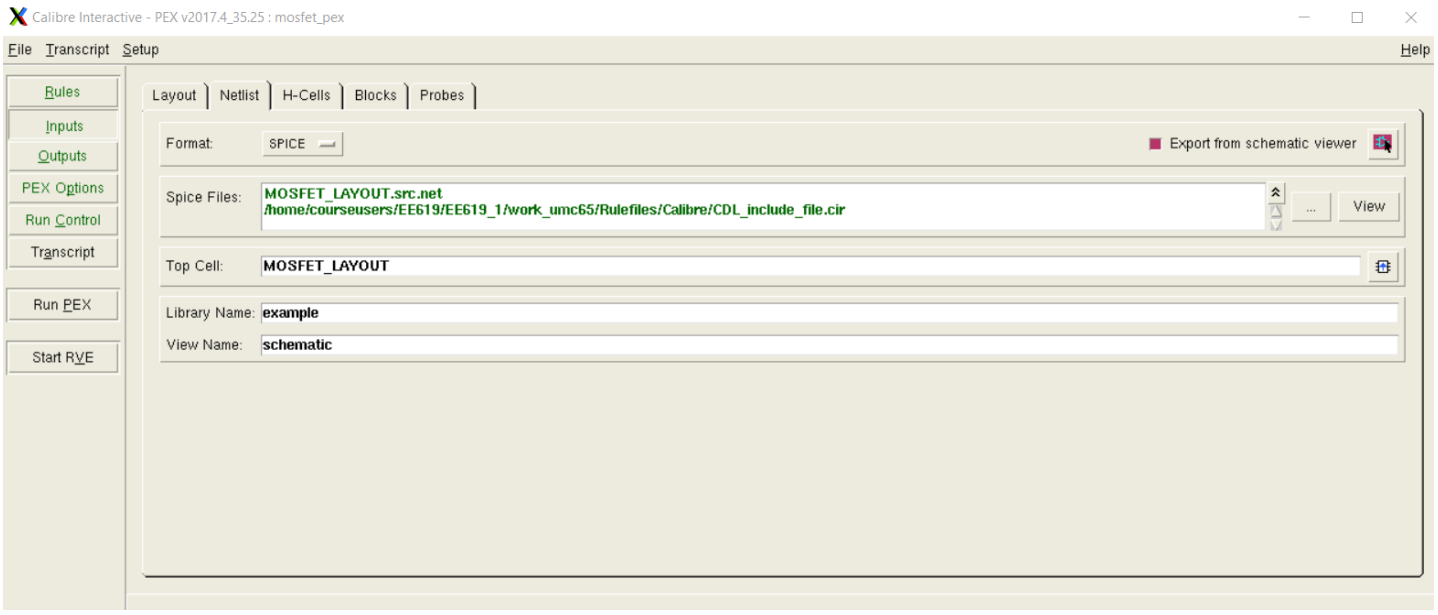
Click on menu → Calibre → Run PEX to open the Calibre PEX window.



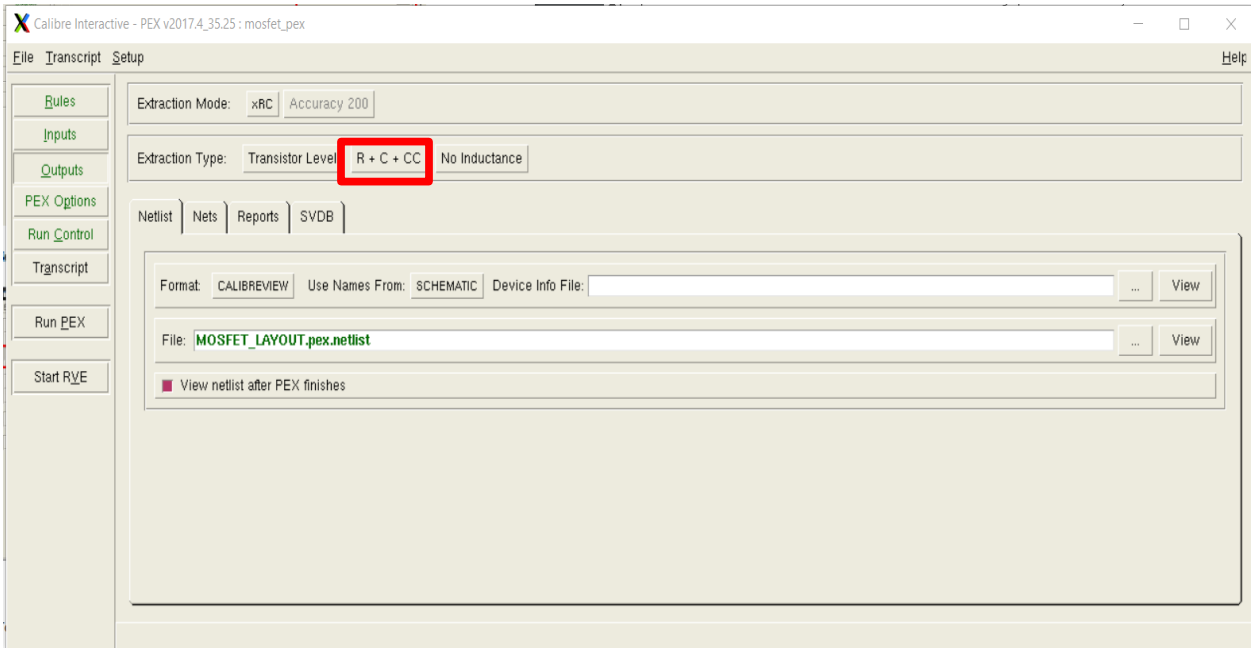
Browse the PEX rules file as shown above. File can be found at:

/home/courseusers/EE619/EE619_XX/work_umc65/Rulefiles/Calibre/LVS/G-DF-LOGIC_MIXED_MODE65N-LL_LOW_K_CALIBRE-LVS-1.6-P4.txt

- Do not change anything in default settings under Inputs→ layout.
- Add **CDL_include_file.cir** at Spice files under **Inputs → netlist** (this is similar to LVS) - shown below.



Settings on **Outputs** should be as below

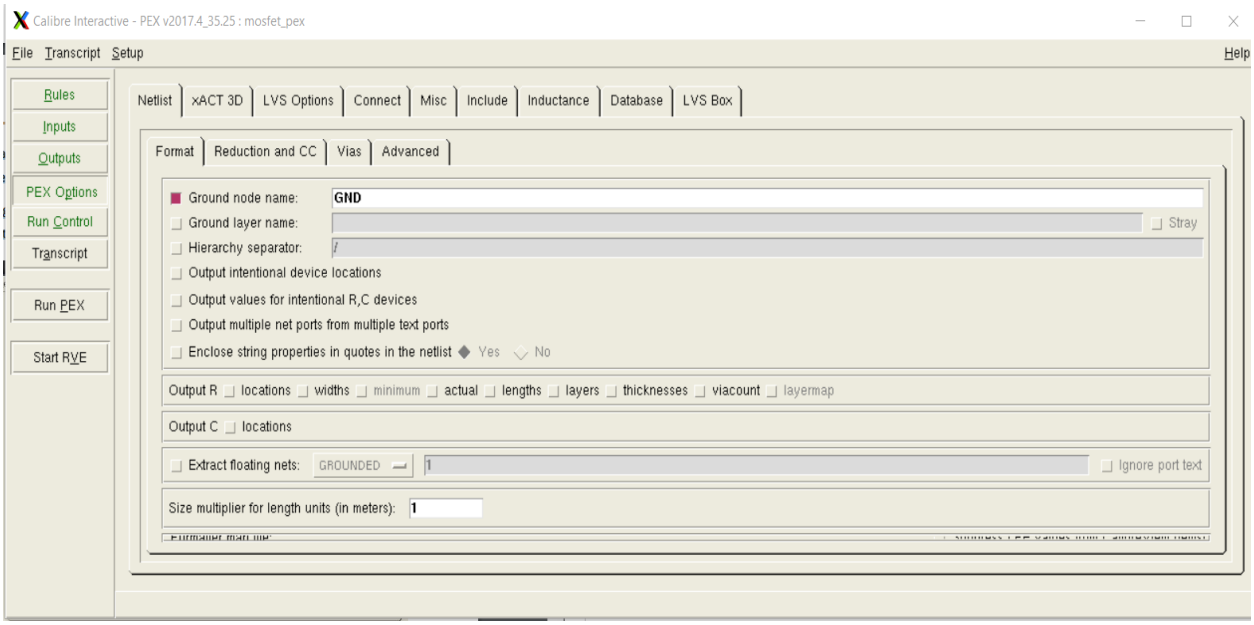


- To change the extraction type, click on the highlighted tab and select the extraction type (e.g. C+CC, R+C+CC)
- Enable “CALIBREVIEW” in Format.

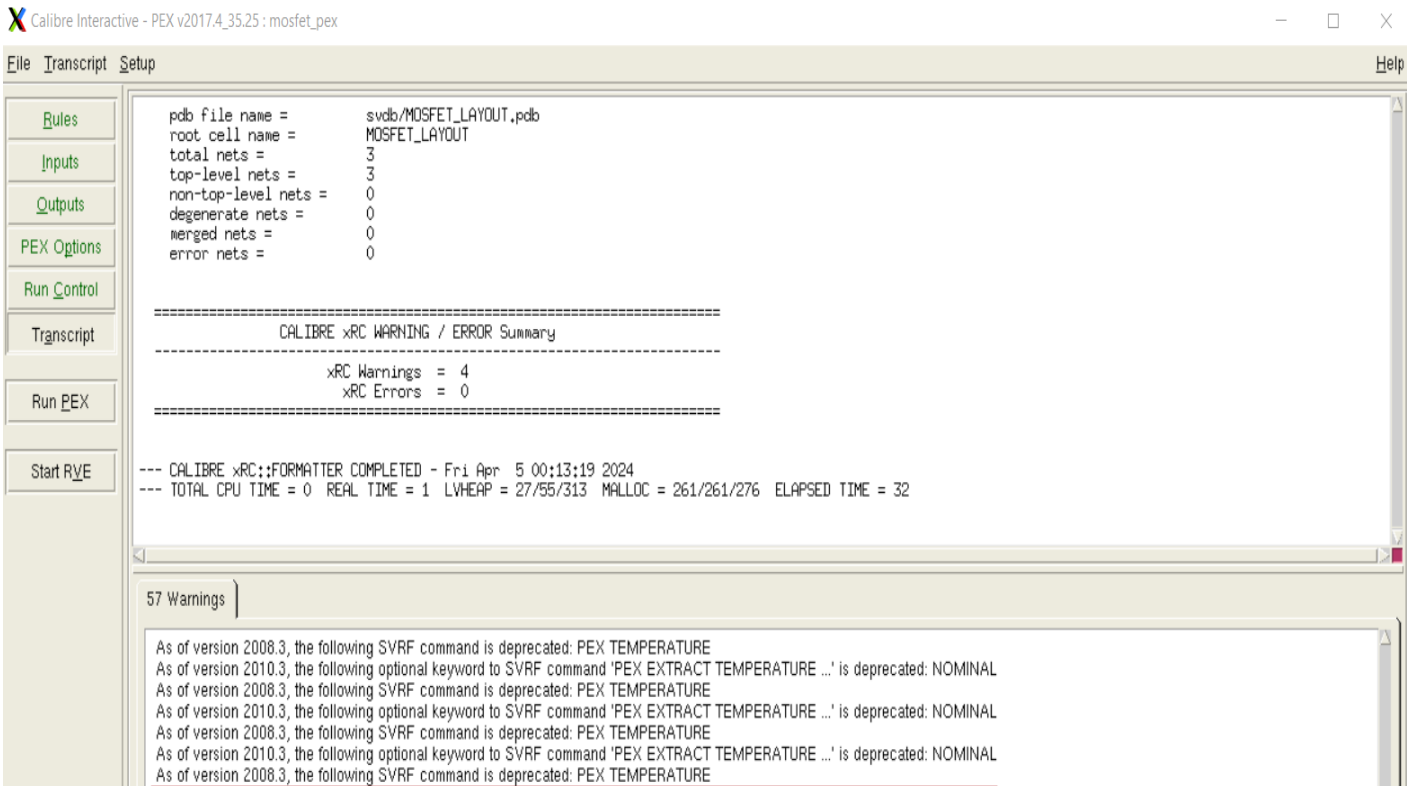
To run PEX click on **“Run PEX”**

Check for warnings/ ERRORS. If any ERRORS exists, you need to fix them. If any warnings related to design are present they need to be cleared.

Below settings is made in “PEX options” to avoid a warning related to GND net. If required, you may do the same.



On successful run, You should see something similar to the following and Calibre View window pops up.



Calibre View window

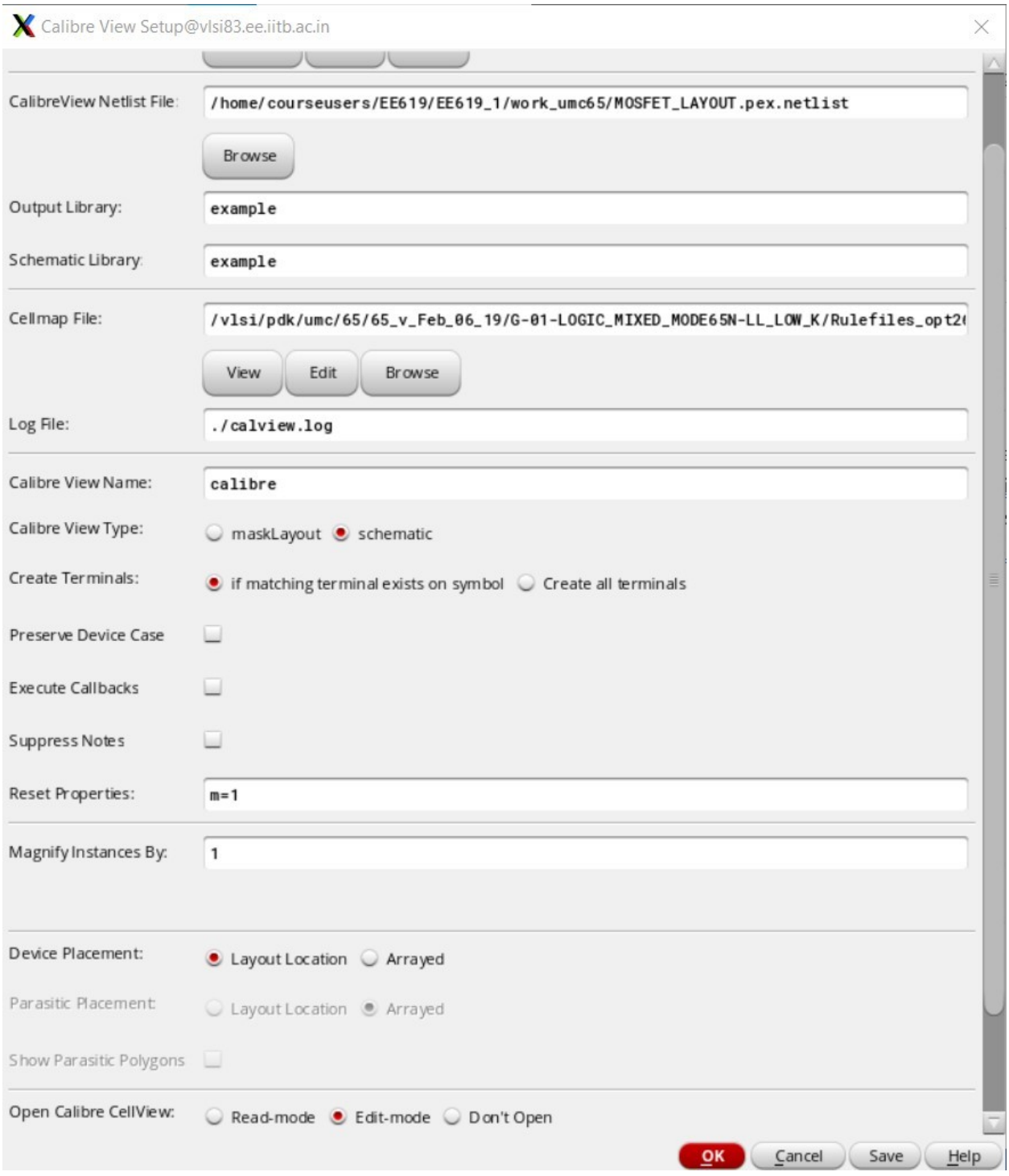
- Cellmap file can be found in the following location

/home/courseusers/EE619/EE619_XX/work_umc65/Rulefiles/Calibre/calview.cellmap

- Select calibre View type = Schematic

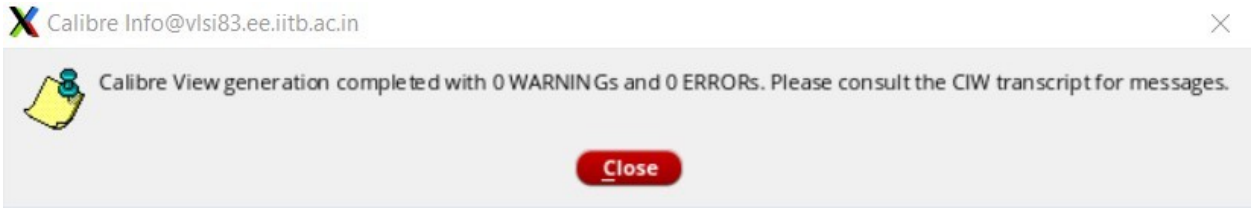
- Open calibre Cellview = Edit-mode

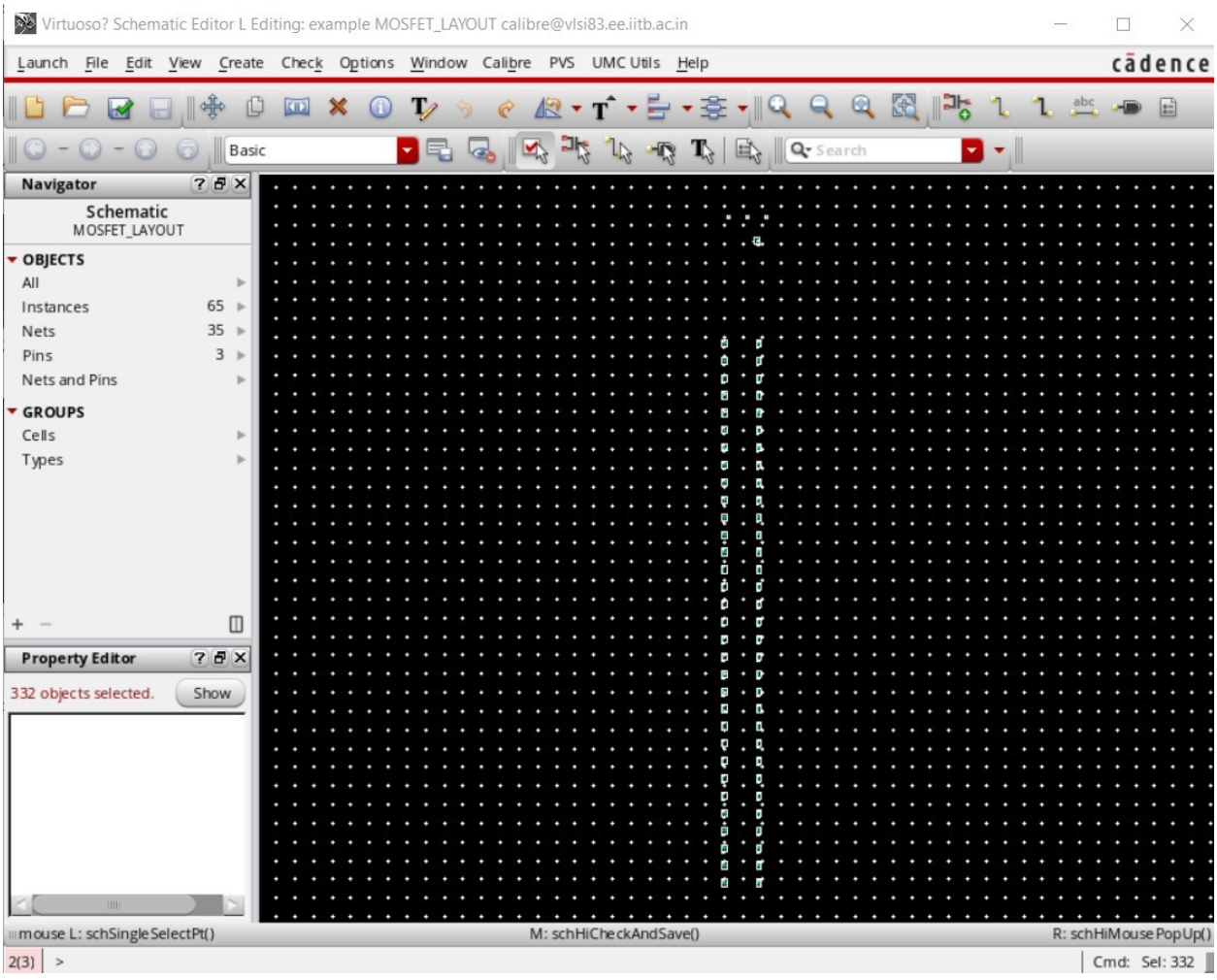
Below is the Calibre View window.



Press OK after settings are made as mentioned above.

You will see the extracted circuit components including parasitic resistor/capacitor/Inductor values. Ensure there are no warnings and errors.



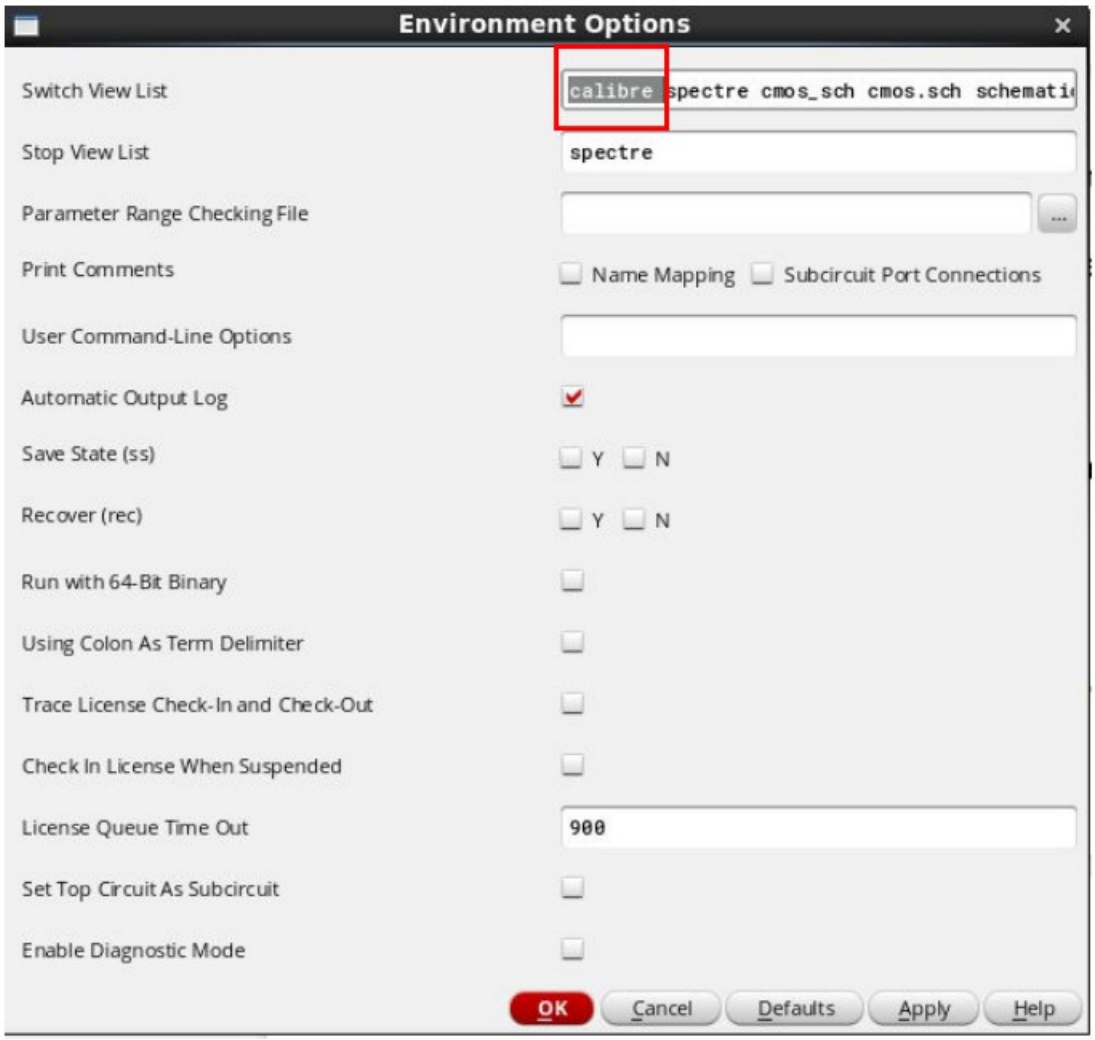


With this, extracted netlist is ready for post- layout simulations.

To run post-layout simulation, open the ADE-L of the test-bench where the schematic symbol is instantiated,

- Menu → Setup → Environment

- It opens the Environment view window.
- Add calibre at the beginning in the switch view list.
- Run the simulation to check the post-layout results.



Below shows the layout of the schematic on 1st page of this document.