

Project 1

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1 Student Details

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Frequency of Oscillation: 5.4 GHz

2 Q1: VCO architecture design

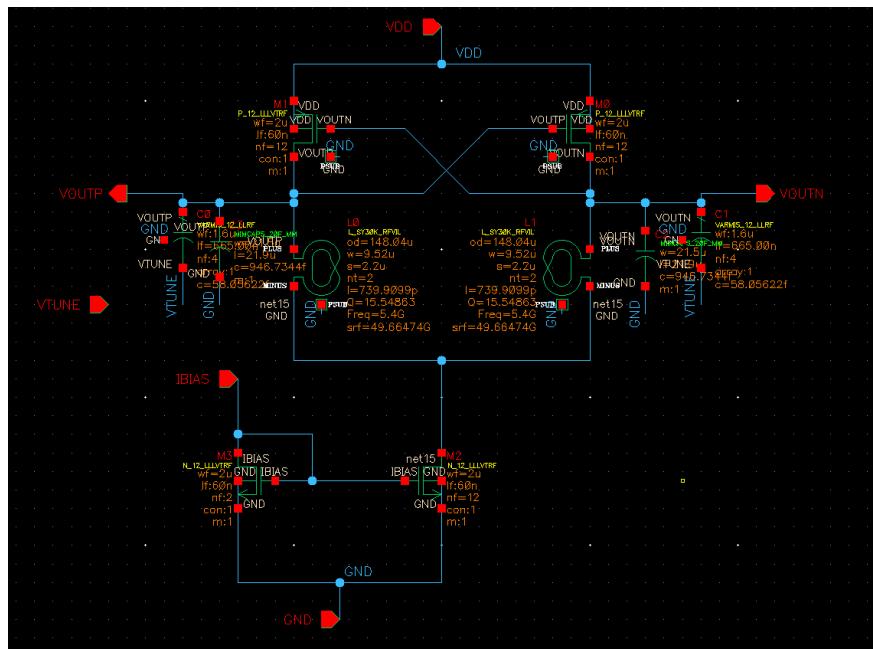


Figure 1: Schematic for the VCO architecture

I have designed the VCO using PMOS with tail current source as it has lower phase noise compared to its NMOS variant. These are the component values used in the design:

- L = 740pH
- Max varactor capacitance = 58.056fF
- Capacitor C2 and C3 = 946.73fF
- W/L (for all Mosfets) = $\frac{2um}{60nm}$

- Gate fingers M0, M1, M2 = 12
- Gate fingers M3 = 2
- $I_{bias} = 300\mu A$

Average DC current through VDD = 2.2mA. Therefore power dissipation in the VCO = $2.2 \times 1.2 = 2.64\text{mW}$

Design Procedure:

- First decided the I_{SS} current using the max power dissipation.
- Using this decided number of fingers in the MOSFET and therefore I_{bias} .
- Using the minimum voltage swing criteria decided on the inductor value
- From here using the given fosc, decided max value of varactor capacitance and the min capacitance (which is done using the capacitors in parallel to varactors as at $vtune = 0$ $C = C_{var} + C_{min} = C_{min}$ as $C_{var} = 0$ at $vtune = 0$) required so that KVCO does not exceed 200MHZ/V and at $vtune = 0.6V$, I get a oscillatory frequency of 5.4GHz
- Kept on fine tuning capacitance, inductance and also played with W/L of Mosfets to get the desired specs in schematic simulations
- In Layout, i tried placing the components as symmetric as possible and also as nicely as possible to ease routing and also to make the layout look good and reduce parasitics
- Once DRC and LVS was passed, extracted the layout and ran the post layout simulations, where the results were different from the schematic simulations, more specifically, oscillatory frequency reduced due to addition of parasitics
- Therefore changed the capacitance in parallel to varactor so as to compensate for the extra parasitics

3 Q2: Layout of the VCO architecture

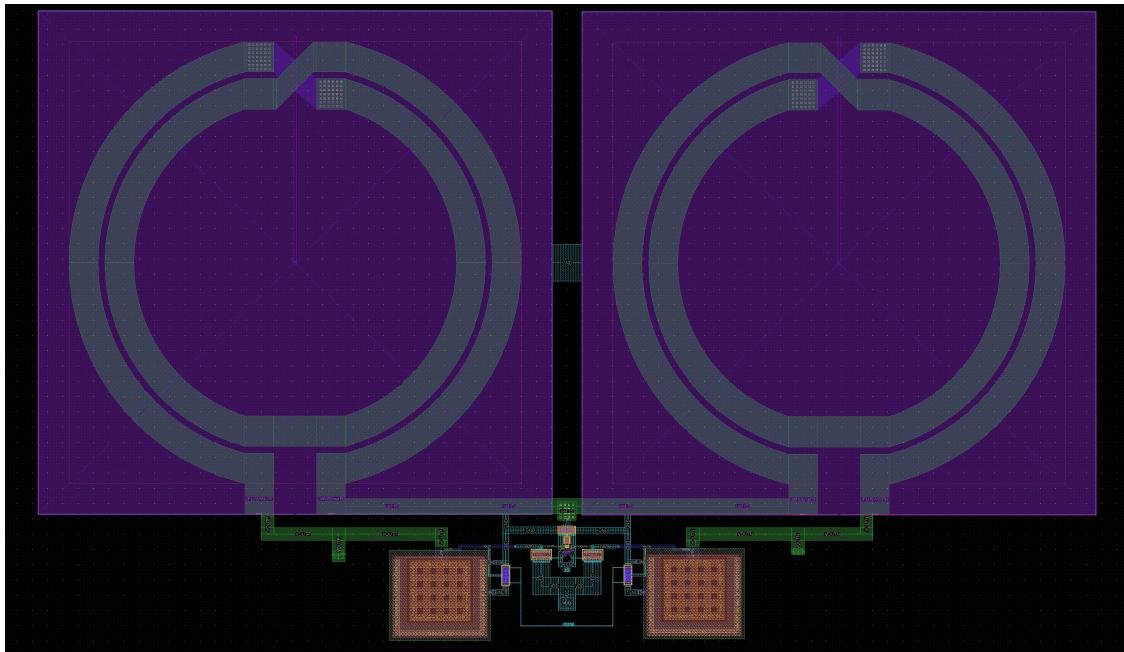


Figure 2: Layout for the VCO architecture

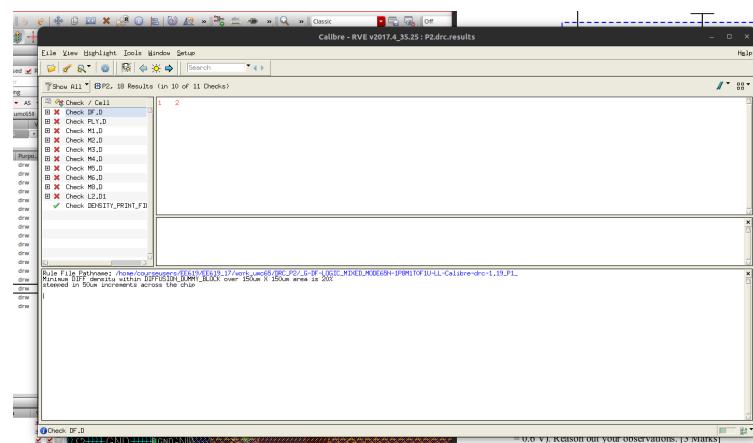


Figure 3: Summary of DRC

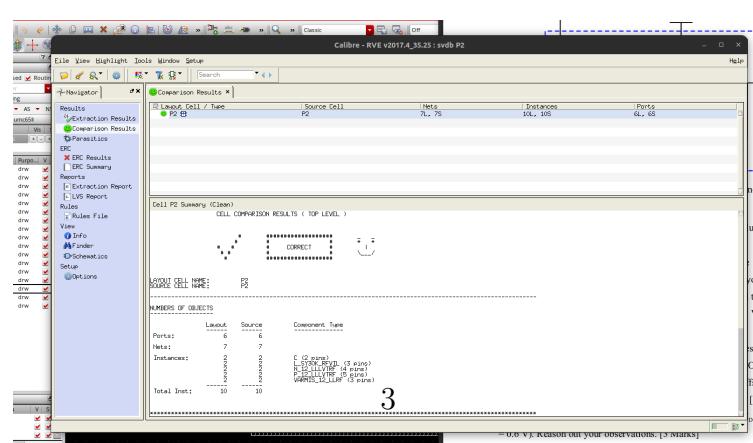


Figure 4: Summary of LVS

4 Q3: Transient signals of the VCO

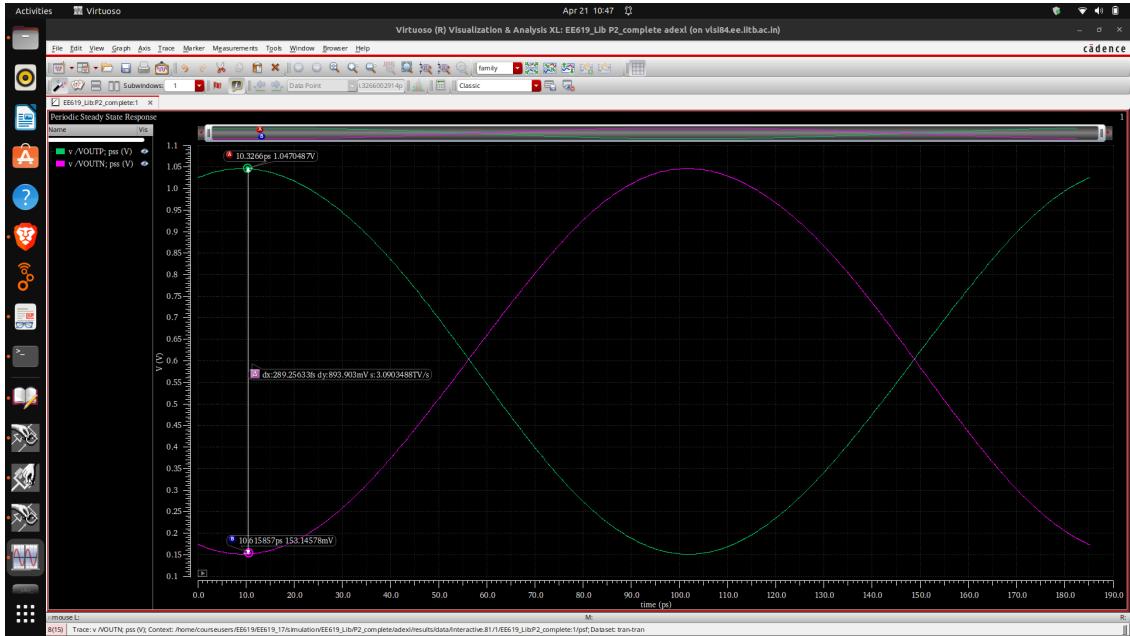


Figure 5: Transient signals for the VCO. We can see the voltage swing is

5 Q4: Frequency vs Vtune

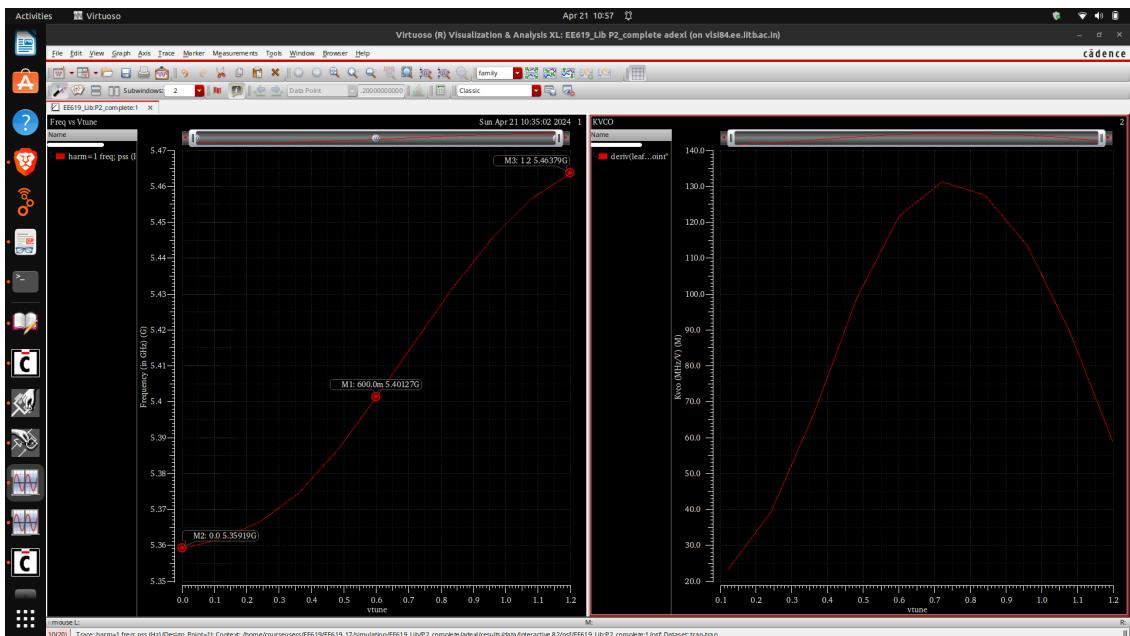


Figure 6: Frequency vs Vtune for the VCO in left side and KVCO in the right side

Here we can see that the frequency varies from 5.359GHz to 5.463 GHz and KVCO remains well below 200MHz/V as per the given specification. At $v_{tune} = 0.6V$, the frequency of oscillation is 5.40127GHz

6 Q5: Comparison of Q4 with schematic

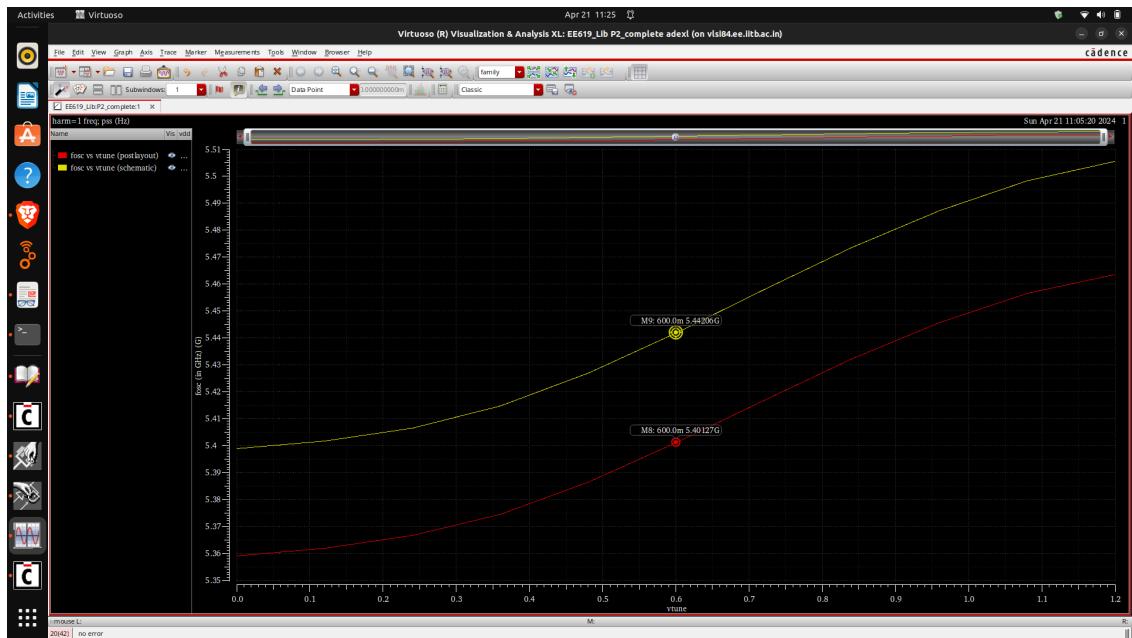


Figure 7: Comparison of fosc post layout (C+CC extraction) and schematic

From the above graphs we can conclude that post layout, the parasitic capacitance decreases the frequency of operation.

7 Q6: Phase Noise at fosc

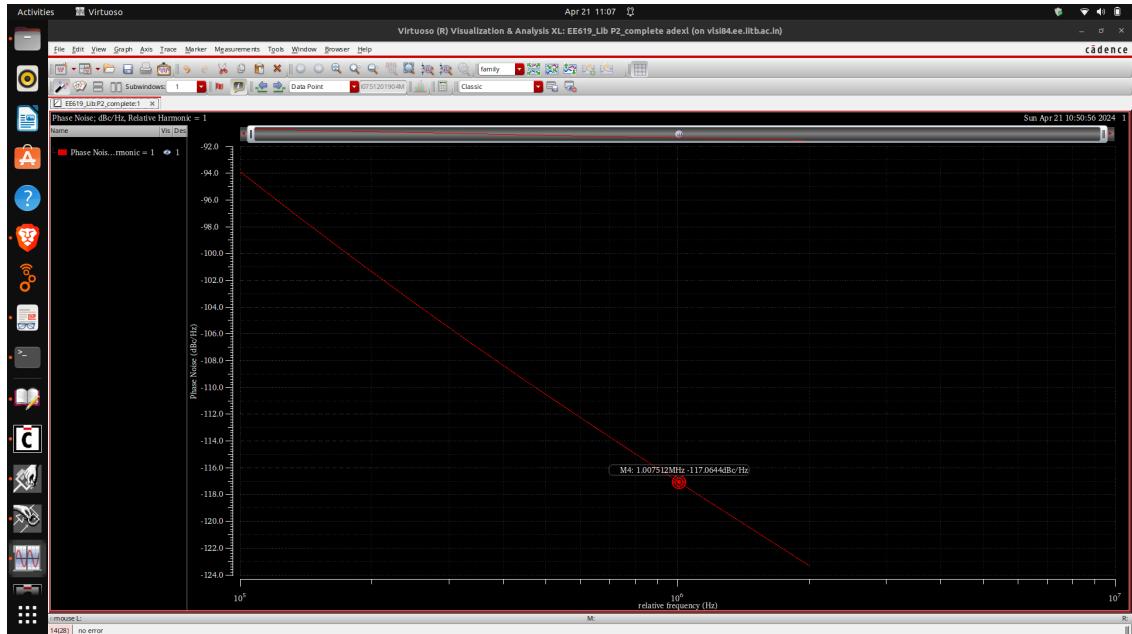


Figure 8: Phase Noise at fosc

Along with this, below are the plots for phase noise at max frequency and min frequency of operation:

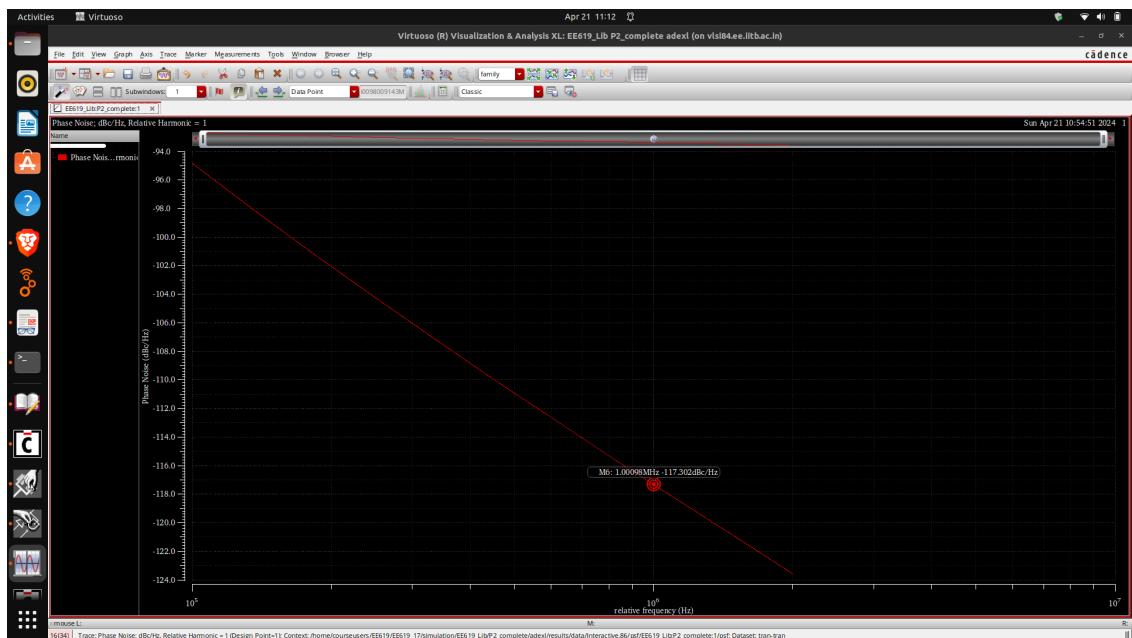


Figure 9: Phase Noise at max frequency

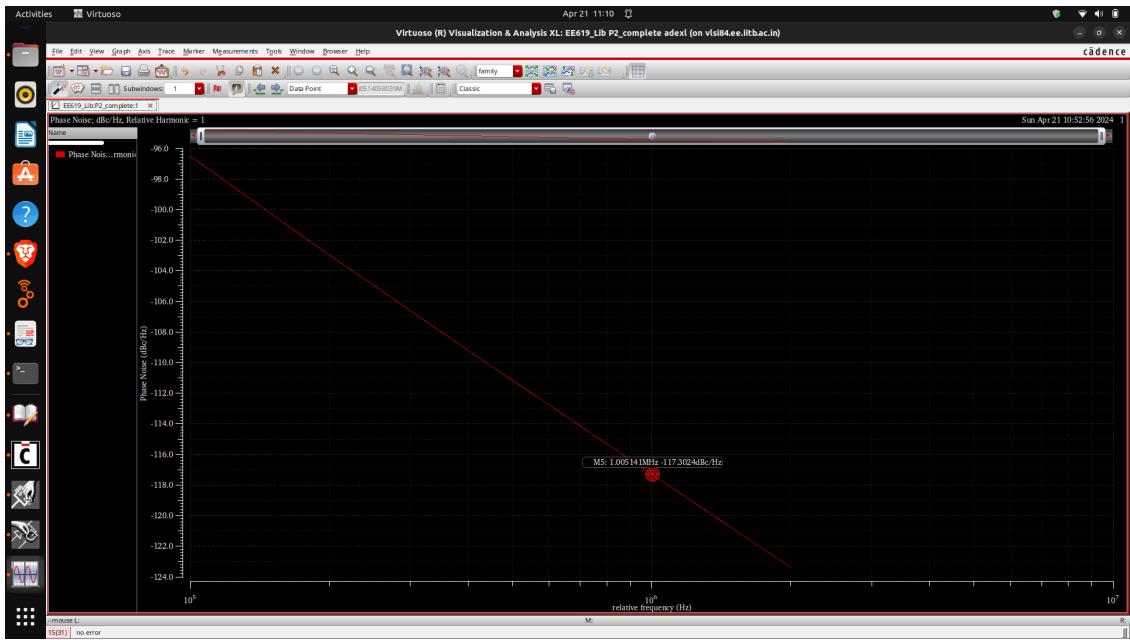


Figure 10: Phase Noise at min frequency

All these are post layout and they meet the specifications.

8 Q7: Superimposed Phase Noise plot for R+C+CC and C+CC extraction

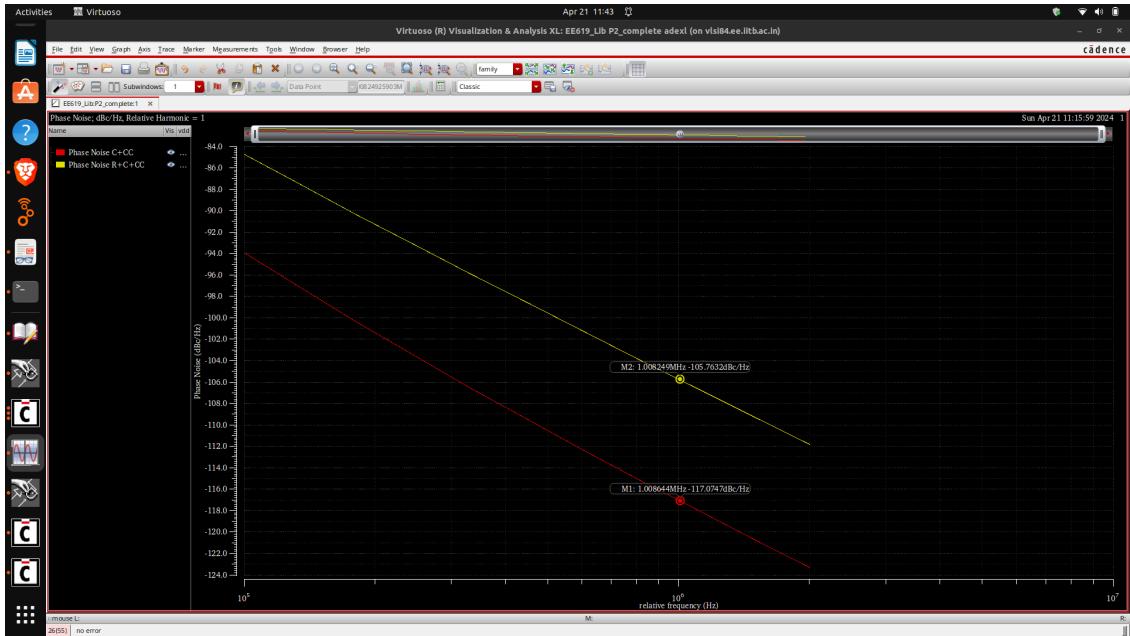


Figure 11: Phase Noise plot for R+C+CC and C+CC extraction

From the plot we can clearly see that in the R+C+CC extraction, resistance introduced during layout significantly increases phase noise but the still meet the criteria of being below

-100dBc/Hz at 1MHz offset.

9 Q8: Frequency Variation with VDD



Figure 12: Frequency variation with VDD keeping vtune = 0.6V

We observe that as VDD increases, the frequency of oscillation decreases because as VDD increases, vtune moves away from VDD thereby shifting towards lower regions. Approximately for all the VDD we can say that the highest achievable frequency would remain approximately same. As VDD increases, vtune moves away from the centre point therefore, the voltage across varactor increases, therefore capacitance increases and therefore frequency decreases.